



V852[™] 32-BIT RISC MICROCONTROLLER

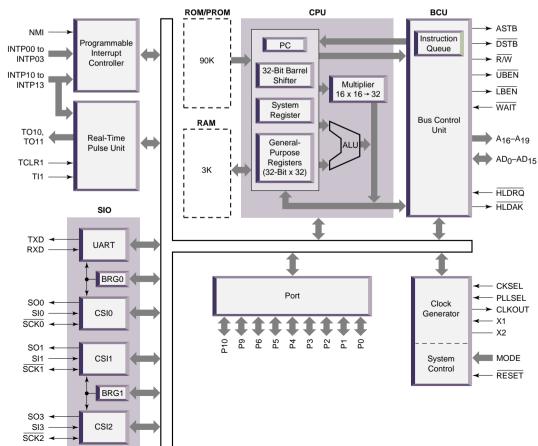
The high-speed V852 microcontroller features the high-performance 32-bit RISC engine of NEC's V850[™] family and targets low-power designs with large embedded code. The device has nearly three times the on-chip memory of the V851[™] (90K versus 32K of ROM and 3K versus 1K of RAM). Many versions of the V850 core are available as part of NEC's ASIC library. The architecture of the V852 device is highly optimized for fast DSP-like operation and very efficient implementation of C programmability.

SPECIFICATIONS

- Clock frequency: DC to 25 MHz
- Performance
 - 29 Dhrystone MIPS
 - 133 MIPS/W
- Two-cycle MAC instruction

- 5V operation

- Power consumption: 217 mW at 25 MHz
- 0.5-µm CMOS process technology
- 6.15 mm x 6.15 mm die size
- Package
 - 100-pin plastic QFP
 - 14 mm x 14 mm



BLOCK DIAGRAM

FEATURE DESCRIPTION

CPU

- Highly integrated microcontroller
 - 32-bit arithmetic logic unit (ALU)
 - Thirty-two general-purpose 32-bit registers
 - 32-bit barrel shifter
- Single-cycle 16 x 16 → 32-bit hardware multiplier
- Powerful RISC instruction set
 - 74 RISC instructions: 16- and 32-bit
 - Two-cycle MAC function for DSP applications
 - Saturated operation instructions (over/ underflow detection function)
 - Single-cycle 32-bit shift instructions
 - Bit manipulation instructions
 - Load and store instructions with 8-/16-/32-bit data
- Fast instruction execution: 40 ns at 25 MHz

MEMORY

- 90K single-cycle internal ROM or PROM
- 3K single-cycle internal RAM

EXTERNAL BUS INTERFACE

- 16-MB linear external memory expansion
- Multiplexed 24-bit address/16-bit data bus
- Programmable and external wait functions
- Idle state insertion for slow memory
- Multiple bus mastership

INTERRUPTS

- 16 maskable interrupts plus NMI
- Eight programmable priority levels on all interrupts and traps
- Specifiable rising and/or falling edge detection
- 32 software traps

PERIPHERALS

- 68 general-purpose, reassignable I/O pins
- Real-time pulse unit
 - 16-bit timer/event counter with four 16-bit capture/compare registers
 - 16-bit interval timer
- Serial interface
 - UART
 - Clocked serial interface: three channels
 - Dedicated baud rate generator: two channels
- Clock generator
 - Internal PLL (5x or 1x)
 - Direct clock input (1/2x)

OTHER

- Power saving features
 - Halt/idle/stop modes
 - Clock output stop function
 - Fully static operation

ORDERING INFORMATION

PART NUMBER	INTERNAL ROM	PACKAGE
µPD70P3002GC-25-7EA	90K OTP PROM	100-pin plastic QFP (fine pitch), 14 mm x 14 mm
µPD703002GC-25-xxx-7EA	90K masked ROM	100-pin plastic QFP (fine pitch), 14 mm x 14 mm

Note: xxx indicates ROM code suffix.



For literature, call **1-800-366-9782** 7 a.m. to 6 p.m. Pacific time or fax your request to **1-800-729-9288** or visit our Web site at www.nec.com

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