

54ACT112

Dual JK Negative Edge-Triggered Flip-Flop

General Description

The 'ACT112 contains two independent, high-speed JK flip-flops with Direct Set and Clear inputs. Synchronous state changes are initiated by the falling edge of the clock. Triggering occurs at a voltage level of the clock and is not directly related to the transition time. The J and K inputs can change when the clock is in either state without affecting the flip-flop, provided that they are in the desired state during the recommended setup and hold times relative to the falling edge of the clock. A LOW signal on $\overline{S}_D$ or $\overline{C}_D$ prevents clocking and forces Q or $\overline{Q}$ HIGH, respectively. Simultaneous LOW signals on $\overline{S}_D$ and $\overline{C}_D$ force both Q and $\overline{Q}$ HIGH.

Asynchronous Inputs:

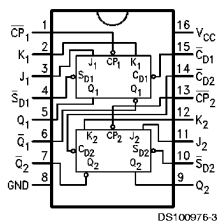
- LOW input to $\overline{S}_D$ sets Q to HIGH level
- LOW input to $\overline{C}_D$ sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

Features

- 'ACT112 has TTL-compatible inputs
- Outputs source/sink 24 mA
- Standard Microcircuit Drawing (SMD) 5962-8995001

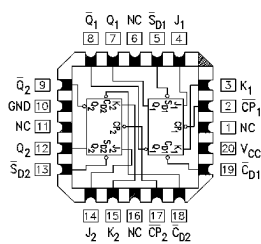
Connection Diagram

Pin Assignment for
DIP and Flatpack



DS100976-3

Pin Assignment
for LCC



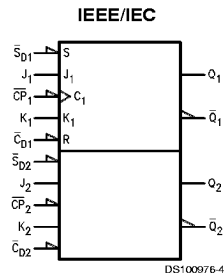
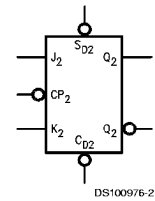
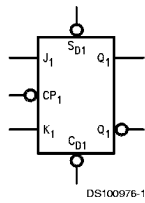
DS100976-5

Pin Descriptions

Pin Names	Description
J ₁ , J ₂ , K ₁ , K ₂	Data Inputs
CP ₁ , CP ₂	Clock Pulse Inputs (Active Falling Edge)
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs (Active LOW)
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs (Active LOW)
Q ₁ , Q ₂ , $\overline{Q}_1$, $\overline{Q}_2$	Outputs

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Logic Symbols



Truth Table

Inputs					Outputs	
$\overline{S}_D$	$\overline{C}_D$	$\overline{CP}$	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	M	h	h	$\overline{Q}_0$	Q_0
H	H	M	l	h	L	H
H	H	M	h	l	H	L
H	H	M	l	l	Q_0	$\overline{Q}_0$

H (h) = HIGH Voltage Level

L (l) = LOW Voltage Level

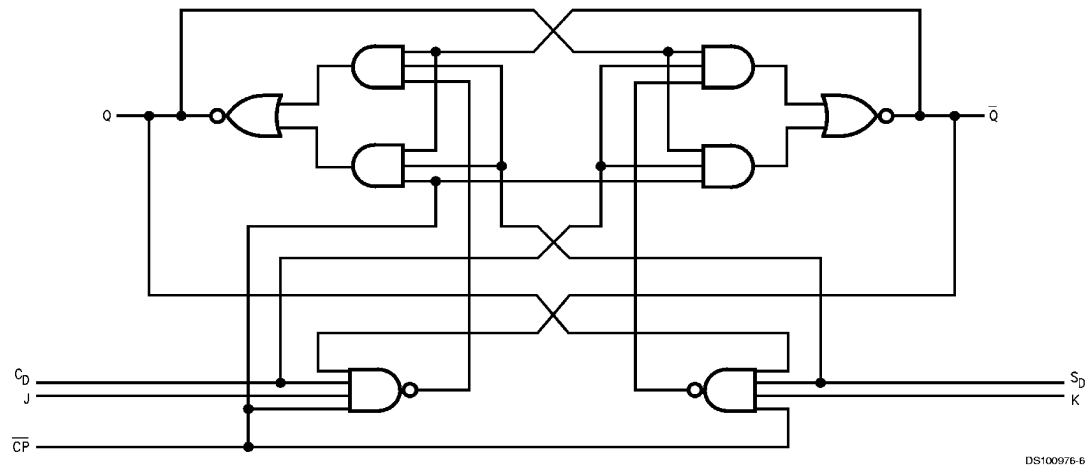
X = Immaterial

M = HIGH-to-LOW Clock Transition

Q_0 ($\overline{Q}_0$) = Before HIGH-to-LOW Transition of Clock

Lower case letters indicate the state of the referenced input or output one setup time prior to the HIGH-to-LOW clock transition.

Logic Diagram (One Half Shown)



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	–0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	–20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	–0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	–20 mA
$V_O = V_{CC} + 0.5$	+20 mA
DC Output Voltage (V_O)	–0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	–65°C to +150°C

Junction Temperature (T_J)

CDIP

175°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	–55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	125 mV/ns
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	$T_A = -55^\circ\text{C to } +125^\circ\text{C}$	Units	Conditions
			Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage	4.5	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	2.0		
V_{IL}	Maximum Low Level Input Voltage	4.5	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	0.8		
V_{OH}	Minimum High Level Output Voltage	4.5	4.4	V	$I_{OUT} = -50 \mu A$
		5.5	5.4		
		4.5	3.70	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -24 \text{ mA}$ $I_{OH} = -24 \text{ mA}$ (Note 2)
		5.5	4.70		
V_{OL}	Maximum Low Level Output Voltage	4.5	0.1	V	$I_{OUT} = 50 \mu A$
		5.5	0.1		
		4.5	0.5	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 24 \text{ MA}$ $I_{OL} = 24 \text{ mA}$ (Note 2)
		5.5	0.5		
I_{IN}	Maximum Input Leakage Current	5.5	± 1.0	μA	$V_I = V_{CC}, \text{ GND}$
I_{CCT}	Maximum I_{CC} /Input	5.5	1.6	mA	$V_I = V_{CC} - 2.1V$
I_{OLD}	Minimum Dynamic	5.5	50	mA	$V_{OLD} = 1.65V \text{ Max}$
I_{OHD}	Output Current(Note 3)	5.5	–50	mA	$V_{OHD} = 3.85V \text{ Min}$
I_{CC}	Maximum Quiescent Supply Current	5.5	80.0	μA	$V_{IN} = V_{CC}$ or GND

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics for 'ACT Family Devices

Symbol	Parameter	V _{CC} (V) (Note 4)	T _A = -55° C to +125° C C _L = 50 pF		Units
			Min	Max	
f _{max}	Maximum Clock Frequency	5.0	80		MHz
t _{PLH}	Propagation Delay CP _n to Q _n or $\overline{Q}_n$	5.0	1.0	14.0	ns
t _{PHL}	Propagation Delay CP _n to Q _n or $\overline{Q}_n$	5.0	1.0	14.0	ns
t _{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q _n or $\overline{Q}_n$	5.0	1.0	13.5	ns
t _{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q _n or $\overline{Q}_n$	5.0	1.0	13.5	ns

Note 4: Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements:

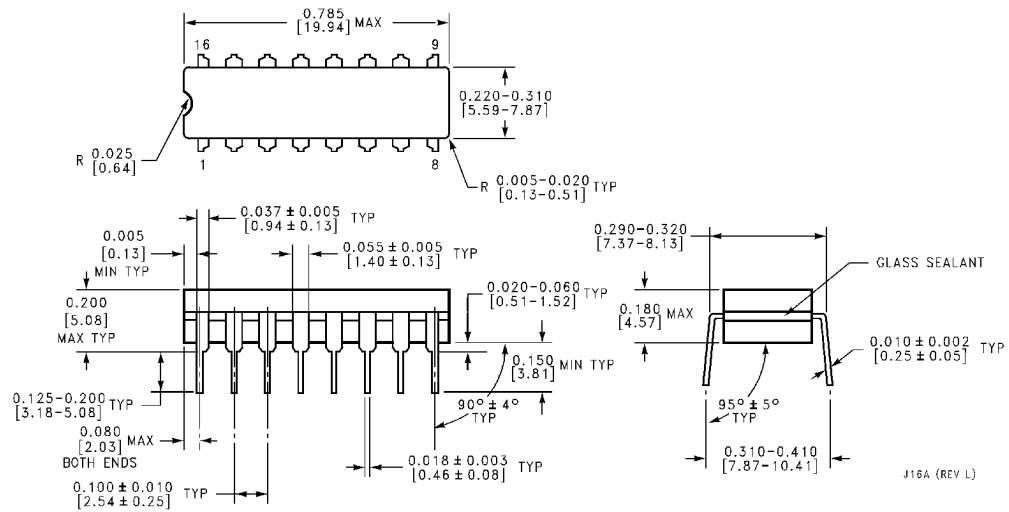
Symbol	Parameter	V _{CC} (V) (Note 5)	T _A = −55° C to +125° C C _L = 50 pF	Units
			Guaranteed Minimum	
t _S	Setup Time, HIGH or LOW J _n or $\overline{K}_n$ to CP _n	5.0	8.0	ns
t _H	Hold Time, HIGH or LOW J _n or $\overline{K}_n$ to CP _n	5.0	1.5	ns
t _W	Pulse Width CP _n or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$	5.0	5.0	ns
t _{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP _n	5.0	3.0	ns

Note 5: Voltage Range 5.0 is 5.0V ±0.5V

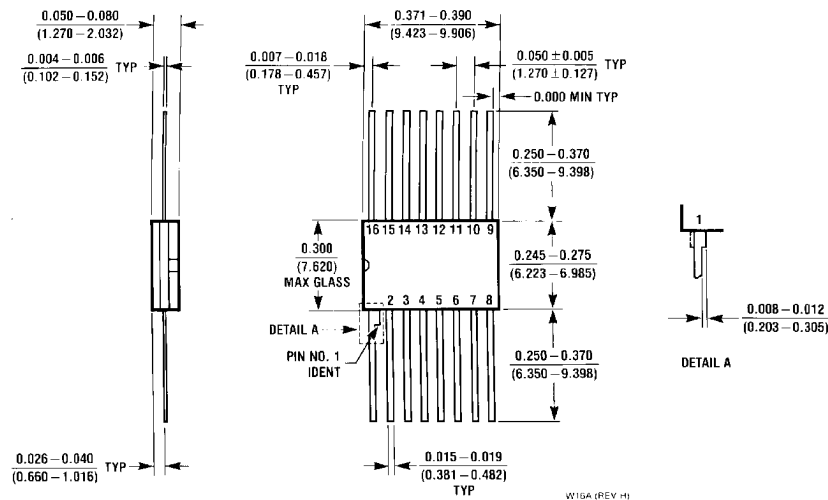
Capacitance

Symbol	Parameter	Max	Units	Conditions
C _{IN}	Input Capacitance	10.0	pF	V _{CC} = OPEN
C _{PD}	Power Dissipation Capacitance	60	pF	V _{CC} = 5.0V

Physical Dimensions inches (millimeters) unless otherwise noted

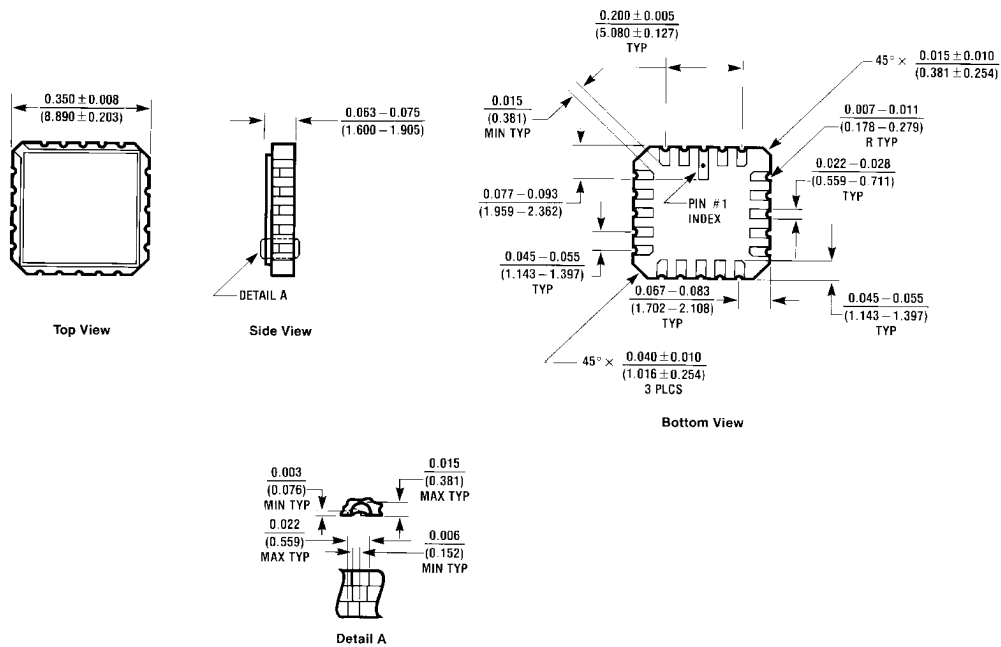


**16-Lead Ceramic Dual-in-line
Package Number J16A**



**16-Lead Cerpack
Package Number W16A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Ceramic Leadless Chip Carrier
Package Number E20A

E20A (REV D)

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