

HDMI Switch ICs

1 for input 1 output buffer with Termination sense correspondence (Sync with HPD_SINK)



BU16024KV

No.09063EDT03

●Description

BU16024KV is 1 for input 1 output HDMI/DVI buffer LSI. Each port supports 2.25Gbps. (HDMI 1.3a).

This device control is simple. It requires only 3.3V and a few GPIO controls.

Terminated resistors(50Ω) are integrated at each input port. When HPD_SINK is L, termination resistors are turned off. TMDS inputs are high impedance.

This device is integrated equalization function and DDC buffer function, so It can adapt long cable.

●Features

- 1) Supports 2.25 Gbps signaling rate for 480i/p, 720i/p, and 1080i/p resolution to 12-bit color depth
- 2) Compatible with HDMI 1.3a
- 3) 5V tolerance to all DDC and HPD_SINK inputs
- 4) Integrated DDC buffer
- 5) Integrated switchable 50Ω receiver termination
- 6) Integrated equalizer circuit to adapt long cable
- 7) Selectable output De-Emphasis Supports
- 8) High Impedance outputs when disabled
- 9) HBM ESD protection exceed 10kV
- 10) 3.3-V supply operation
- 11) 48-Pin VQFP package
- 12) ROHS compatible

●Applications

Digital TV, DVD Player, Set-Top-Box, Audio Video Receiver, Digital Projector, DVI or HDMI Switch Box, PC

●Line up matrix

Part No.	Power Supply (V)	ESD (KV)	Input (ch)	Output (ch)	Data rate (Gbps)	Hot Plug Control	Termination Sense Correspondence	Switching Method	DDC Buffer	Equalizer	De emphasis	Package	RoHS
BU16020KV	3 to 3.6	10	HDMI 4ch	HDMI 1ch	2.7	Yes	Yes	GPIO/I ² C	Yes	Yes (adaptive)	Yes	VQFP100	Yes
BU16018KV	3 to 3.6	10	HDMI 3ch	HDMI 1ch	2.25	Yes	Yes	GPIO	Yes	Yes	Yes	VQFP80	Yes
BU16027KV	3 to 3.6	10	HDMI 3ch	HDMI 1ch	2.25	Yes	Yes	GPIO	Yes	Yes	Yes (Always ON)	VQFP64	Yes
BU16006KV	3 to 3.6	10	HDMI 2ch	HDMI 1ch	2.25	Yes	Yes	GPIO	Yes	Yes	Yes (Always ON)	VQFP64	Yes
BU16024KV	3 to 3.6	10	HDMI 1ch	HDMI 1ch	2.25	Yes	Yes	-	Yes	Yes	Yes	VQFP48C	Yes

●OUTSIDE DIMENSION CHART

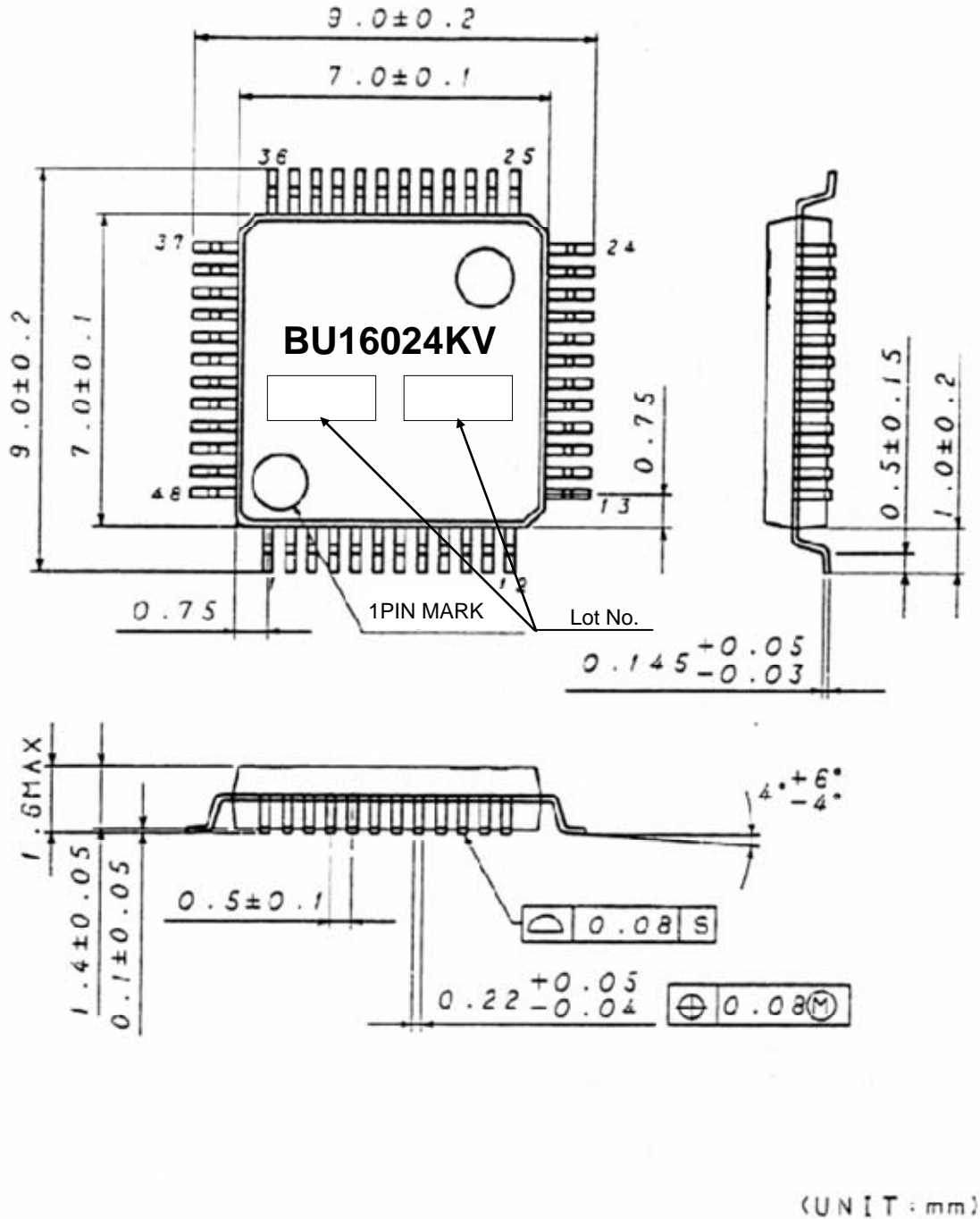
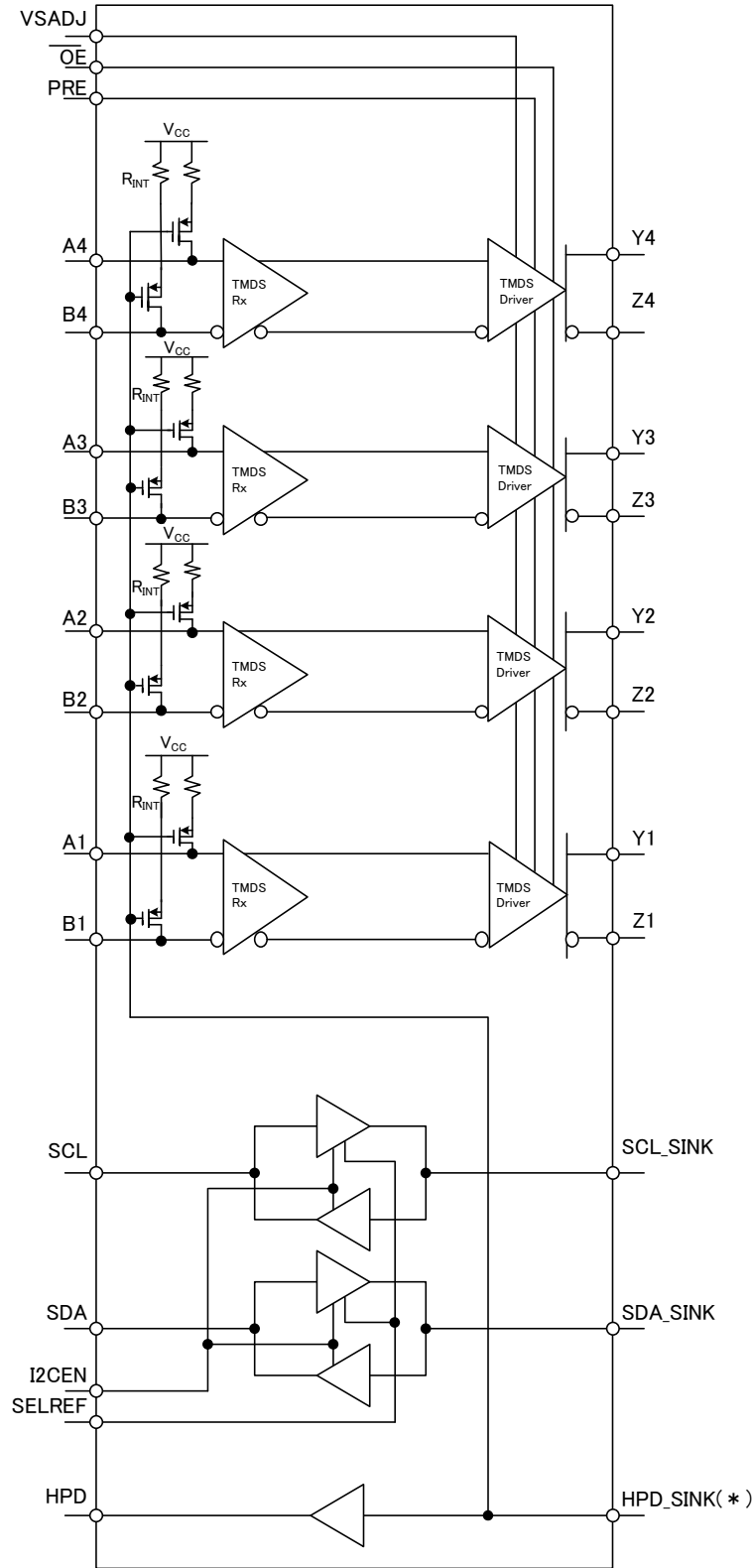


Figure 1-1 Outside dimension chart

●BLOCK DIAGRAM



(*) when HPD_SINK = "L". Termination resistor is turned off.

Figure 2-1 Block Diagram

●PIN EXPLANATION

1). PIN ASSIGNMENT

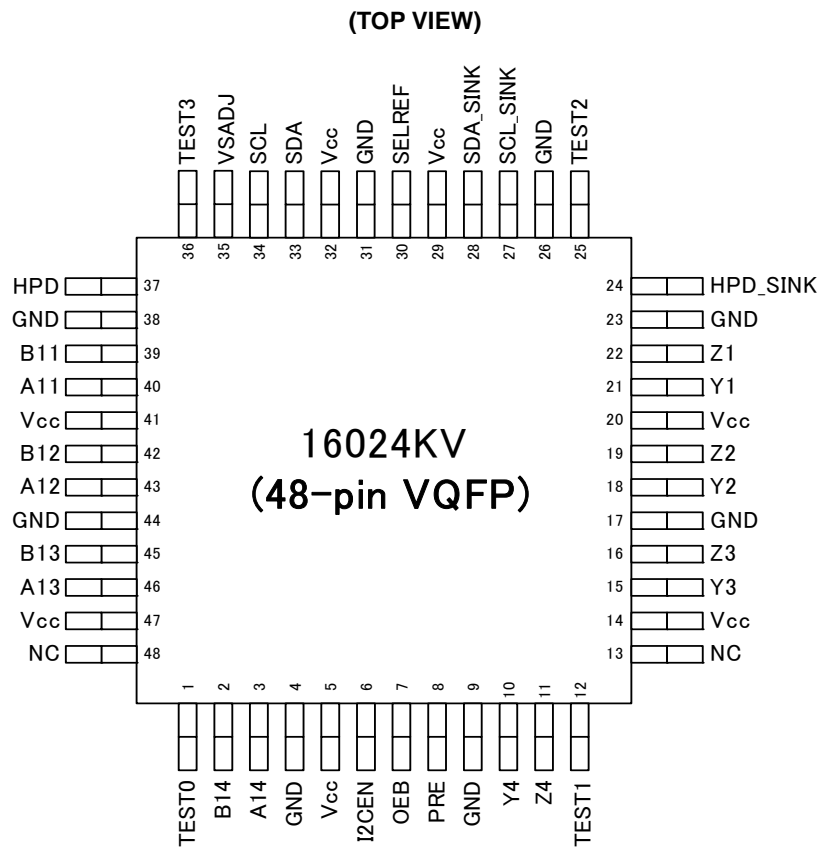


Figure 3-1 Pin Location

2). PIN LIST

TERMINAL		I/O	DESCRIPTION
NAME	No.		
B1, B2, B3, B4	39, 42, 45, 2	I	TMDS Negative inputs
A1, A2, A3, A4	40, 43, 46, 3	I	TMDS Positive inputs
Z1, Z2, Z3, Z4	22, 19, 16, 11	O	TMDS Negative outputs
Y1, Y2, Y3, Y4	21, 18, 15, 10	O	TMDS Positive outputs
HPD	37	O	Hot plug detector output
HPD_SINK	24	I	Hot plug detector input
SCL	34	I/O	DDC Bus clock line to source
SDA	33	I/O	DDC Bus data line to source
SCL_SINK	27	I/O	DDC Bus clock line to sink
SDA_SINK	28	I/O	DDC Bus data line to sink
VSADJ	35	I	TMDS Compliant voltage swing control(via 4.64k Ω to GND)
I ² CEN	6	I	I ² C Repeater enable Low : High-Z High : Active
SELREF	30	I	SCL_SINK/SDA_SINK Output voltage select
TEST0, 1, 2, 3	1, 12, 25, 36	I	Open or GND connect (recommend)
N.C	13, 48		Open or GND connect (recommend)
OEB	7	I	TMDS Output enable Low : Active High : High-Z
PRE	8	I	TMDS Output de-emphasis adjustment Low : OFF High : ON
V _{CC}	5, 14, 20, 29, 32, 41, 47	-	Power supply
GND	4, 9, 17, 23, 26, 31, 38, 44	-	Ground

● EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

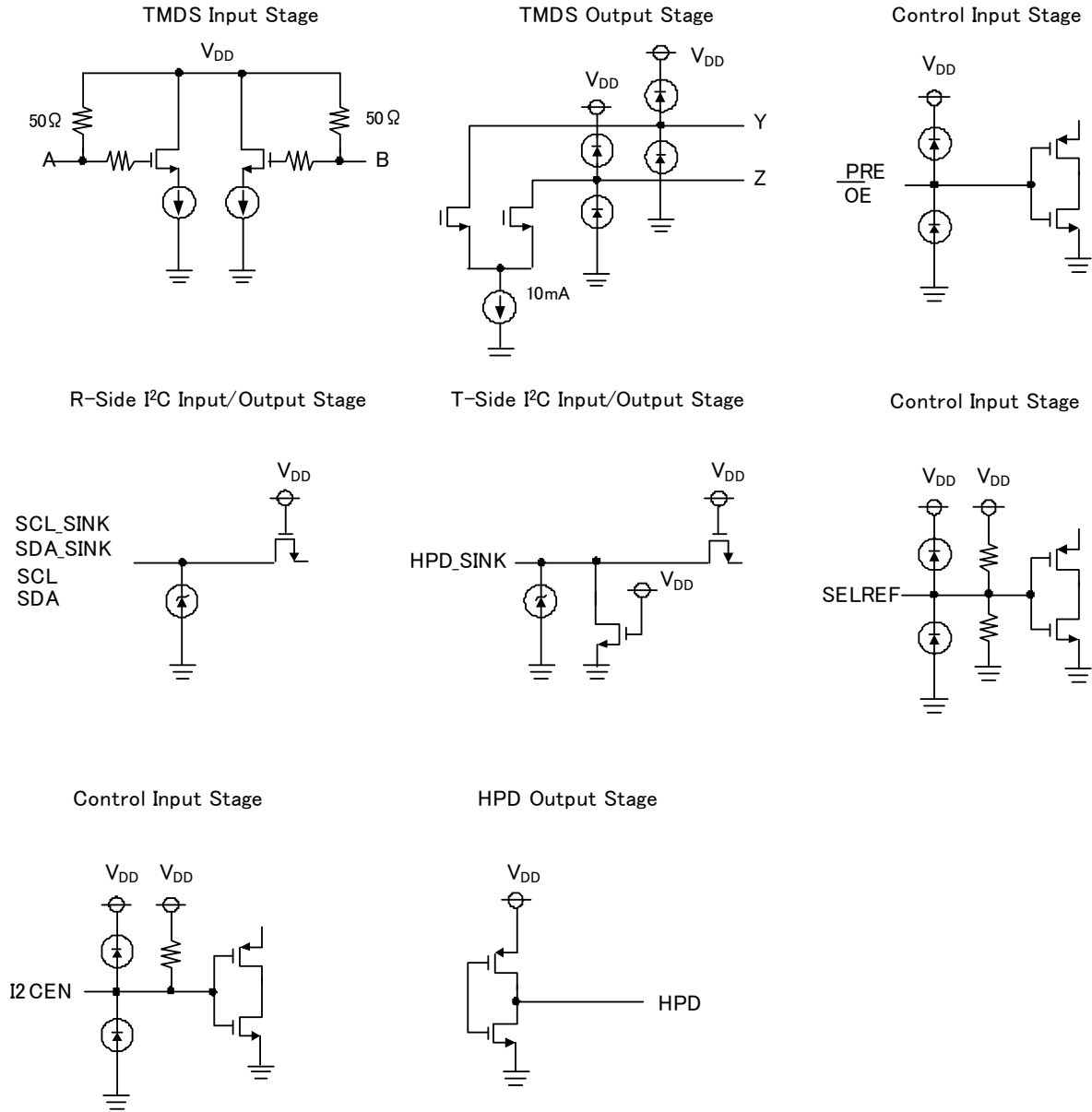


Figure 4-1 I/O pin schematic diagram

● ELECTRICAL SPECIFICATIONS

1.) ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)⁽¹⁾

ITEM	MIN.	TYP.	MAX.	UNIT
Supply voltage (V _{CC})	-0.3	-	4.0	V
SCL, SCL_SINK, SDA, SDA_SINK, HPD_SINK input voltage	-0.3	-	6.0	V
Differential input voltage	2.5	-	4	V
PRE, I ² CEN, SELREF, OEB input voltage	-0.3	-	4	V
Power dissipation	-	-	1200 ※1	mW
Storage temperature range	-55	-	125	°C

※70mm×70mm×1.6mm glass epoxy board mount. (Reverse Cu occupation rate: 15mm×15mm)

When it's used by than Ta=25°C, it's reduced by 12mW/°C.

2.) RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{CC}	Supply voltage	3.0	3.3	3.6	V
T _A	Operating free-air temperature	0	-	70	°C
TMDS DIFFERENTIAL PINS (A/B)					
V _{ID}	Receiver peak-to-peak differential input voltage	150	-	1560	mVp-p
V _{IC}	Input common mode voltage	V _{CC} -0.6	-	V _{CC} +0.01	V
R _{VSADJ}	Resistor for TMDS compliant voltage swing range	4.6	4.64	4.68	kΩ
AV _{CC}	TMDS output termination voltage, see Figure 5-1	3	3.3	3.6	V
R _T	Termination resistance, see Figure 5-1	45	50	55	Ω
Signaling rate		0	-	2.25	Gbps
STATUS(HPD_SINK)					
V _{IH}	LVTTTL High-level input voltage	2.4	-	5.5	V
V _{IL}	LVTTTL Low-level input voltage	GND	-	0.8	V
DDC PINS (SCL_SINK, SDA_SINK, SDA, SCL)					
V _{I(DDC)}	Input voltage	GND	-	5.5	V

3.) ELECTRICAL CHARACTERISTICS

Over recommended operating conditions (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP. ⁽¹⁾	MAX.	
I _{CC}	Supply current	V _{IH} = V _{CC} , V _{IL} = V _{CC} -0.4V, R _{VSADJ} = 4.64kΩ R _T = 50Ω, AV _{CC} = 3.3V Am/Bm = 2.25 Gbps HDMI data pattern, m = 2,3,4 A1/B1 = 225 MHz clock	-	140	170	mA
P _D	Power dissipation	V _{IH} = V _{CC} , V _{IL} = V _{CC} -0.4V, R _{VSADJ} = 4.64kΩ R _T = 50Ω, AV _{CC} = 3.3V Am/Bm = 2.25Gbps HDMI data pattern, m = 2,3,4 A1/B1 = 225 MHz clock	-	480	700	mW
TMDS DIFFERENTIAL PINS (A/B; Y/Z)						
V _{OH}	Single-ended high-level output voltage	AV _{CC} = 3.3V, R _T = 50Ω, PRE = 0V	AV _{CC} - 10	-	AV _{CC} + 10	mV
V _{OL}	Single-ended low-level output voltage		AV _{CC} - 600	-	AV _{CC} - 400	mV
V _{SWING}	Single-ended low-level swing voltage		400	-	600	mV
V _{OD(O)}	Overshoot of output differential voltage		-	6%	15%	2xV _{swing}
V _{OD(U)}	Undershoot of output differential voltage		-	12%	25%	2xV _{swing}
V _{OD(pp)}	Steady state output differential voltage with de-emphasis	PRE = V _{CC} Am/Bm = 225 Mbps HDMI data pattern, m = 2,3,4 A1/B1 = 225 MHz clock	600	-	920	mVp-p
R _{INT}	Input termination resistance	V _{IN} = 2.9V	45	50	55	Ω
ΔV _{OC(SS)}	Change in steady-state common-mode output voltage between logic states		-	5	-	mV

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT	
			MIN.	TYP. ⁽¹⁾	MAX		
DDC Input and output							
Tx (SDA_SINK , SCL_SINK)							
$I_{IKR①}$	Input leak current,	$V_I = 5.5V$	-10	-	10	uA	
$I_{IKT②}$	Input leak current,	$V_I = V_{CC}$	-10	-	10	uA	
I_{OHT}	High-level output current	$V_O = 3.6V$	-10	-	10	uA	
I_{ILT}	Low-level input current	$V_{IL} = GND$	-10	-	10	uA	
V_{OLT}	Low-level output voltage	$RL = 4.7k\Omega$	SELREF = NC	0.43	-	0.57	V
			SELREF= GND	0.58	-	0.72	
			SELREF = Vcc	0.73	-	0.87	
$V_{OLT} - V_{IL}$	Low-level input voltage below output low-level voltage		SELREF = NC	-	100	-	mV
			SELREF= GND	-	250	-	
			SELREF = Vcc	-	400	-	
Rx (SDA, SCL)							
$I_{IKR①}$	Input leak current	$V_I = 5.5V$	-10	-	10	uA	
$I_{IKR②}$	Input leak current	$V_I = V_{CC}$	-10	-	10	uA	
I_{OHR}	High-level output current	$V_O = 3.6V$	-10	-	10	uA	
I_{ILR}	Low-level input current	$V_{IL} = GND$	-10	-	10	uA	
V_{OLR}	Low-level output voltage	$I_{OUT} = 4mA$	-	-	0.2	V	
STATUS PINS (HPD)							
$V_{OH(TTL)}$	TTL High-level output voltage	$I_{OH} = -8mA$	2.4	-	V_{CC}	V	
$V_{OL(TTL)}$	TTL Low-level output voltage	$I_{OL} = 8mA$	0	-	0.4	V	
CONTROL PINS (PRE, OEB)							
I_{IH}	High-level digital input current	$V_{IH} = V_{CC}$	-10	-	10	uA	
I_{IL}	Low-level digital input current	$V_{IL} = GND$	-10	-	10	uA	
CONTROL PINS (I²CEN, SELREF,)							
I_{IH}	High-level digital input current	$V_{IH} = V_{CC}$	-45	-	45	uA	
I_{IL}	Low-level digital input current	$V_{IL} = GND$	-45	-	45	uA	
STATUS PINS (HPD_SINK)							
I_{IH}	High-level digital input current	$V_{IH} = 5.5V$	10	50	100	uA	
		$V_{IH} = V_{CC}$	5	30	80	uA	
I_{IL}	Low-level digital input current	$V_{IL} = GND$	-10	-	10	uA	

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP. ⁽¹⁾	MAX.	
TMDS DIFFERENTIAL PINS (Y/Z)						
t_{PLH}	Propagation delay time low-high-level output	See Figure5-2, $AV_{CC} = 3.3V$, $R_T = 50\Omega$, PRE = "H"	-	320	-	ps
t_{PHL}	Propagation delay time high-low-level output		-	335	-	ps
t_r	Differential output signal rise time (20%-80%)		-	120	-	ps
t_f	Differential output signal fall time (20%-80%)		-	120	-	ps
$t_{sk(p)}$	Pulse skew ($t_{PHL} - t_{PLH}$)		-	15	-	ps
$t_{sk(D)}$	Intra-pair differential skew, see Figure5-3		-	25	-	ps
DDC I/O PINS (SCL, SCL_SINK, SDA, SDA_SINK)						
t_{pdLHTR} (DDC)	Propagation delay time, low-to-high-level output Tx to Rx	$R_L = 4.7K\Omega$ $C_L = 100pF$	-	650	-	ns
t_{pdHLTR} (DDC)	Propagation delay time, high-to-low-level output Tx to Rx		-	200	-	ns
t_{pdLHRT} (DDC)	Propagation delay time, low-to-high-level output Rx to Tx	$R_L = 1.67K\Omega$ $C_L = 400pF$	-	500	-	ns
t_{pdHLRT} (DDC)	Propagation delay time, high-to-low-level output Rx to Tx		-	350	-	ns
t_r TX(DDC)	Tx output Rise time	$R_L = 4.7K\Omega$ $C_L = 100pF$	-	800	-	ns
t_f TX(DDC)	Tx output Fall time		-	150	-	ns
t_r RX(DDC)	Rx output Rise time	$C_L = 10pF$	-	950	-	ns
t_f RX(DDC)	Rx output Fall time		-	50	-	ns
C_{IO}	Input/output capacitance	$V_I = 0V$	-	15	-	pF
STATUS PINS(HPD)						
$t_{pdLH(HPD)}$	Propagation delay time, low-to-high-level output from HPD_SINK to HPD	$C_L = 10pF$	-	5	-	ns
$t_{pdHL(HPD)}$	Propagation delay time, high-to-low-level output from HPD_SINK to HPD	$C_L = 10pF$	-	5	-	ns
$t_{sx(HPD)}$	Switch time from port select to the latest valid status of HPD	$C_L = 10pF$	-	8	-	ns

Note:

All typical values are at 25°C and with a 3.3V supply.

● MEASUREMENT SYMBOL AND CIRCUIT

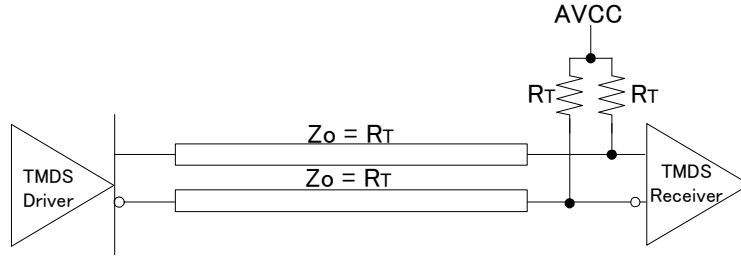


Figure 5-1 Termination for TMS Output Driver

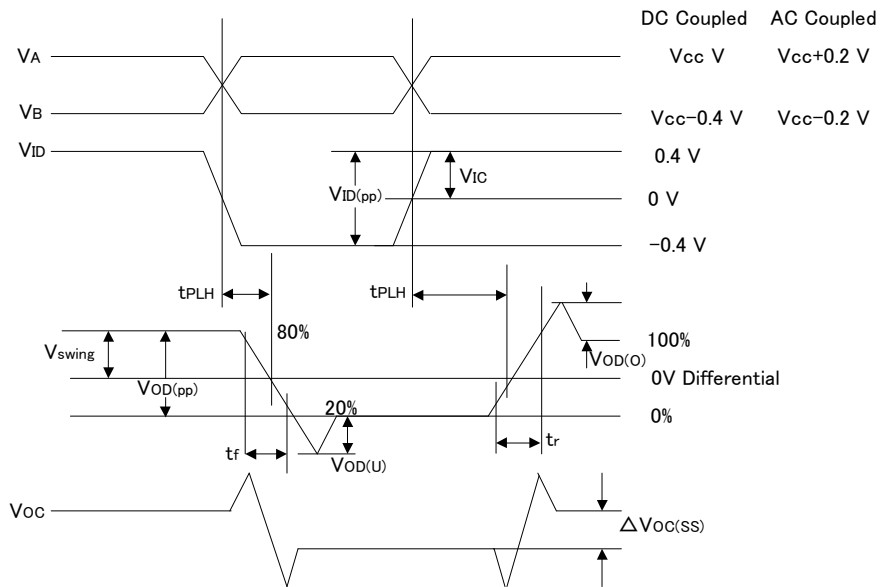
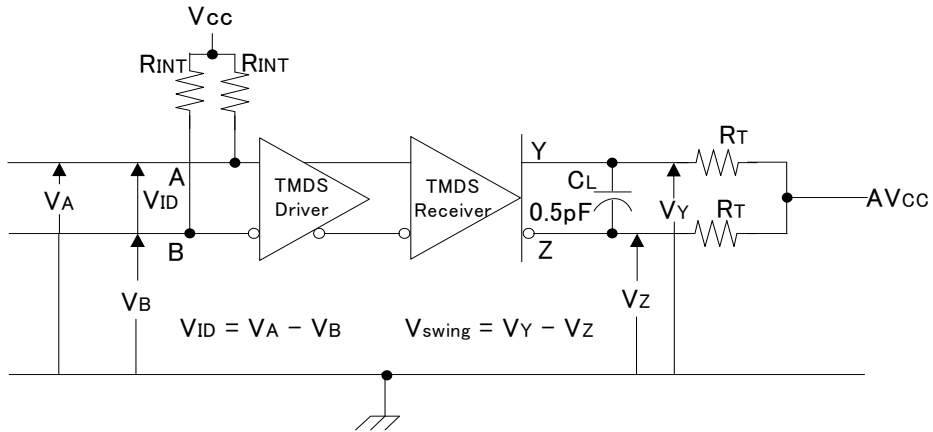


Figure 5-2 Timing Test Circuit and Definitions

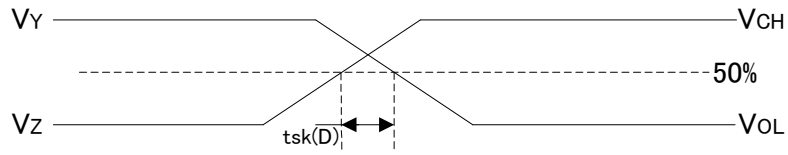


Figure 5-3 Definition of Intra-Pair Differential Skew

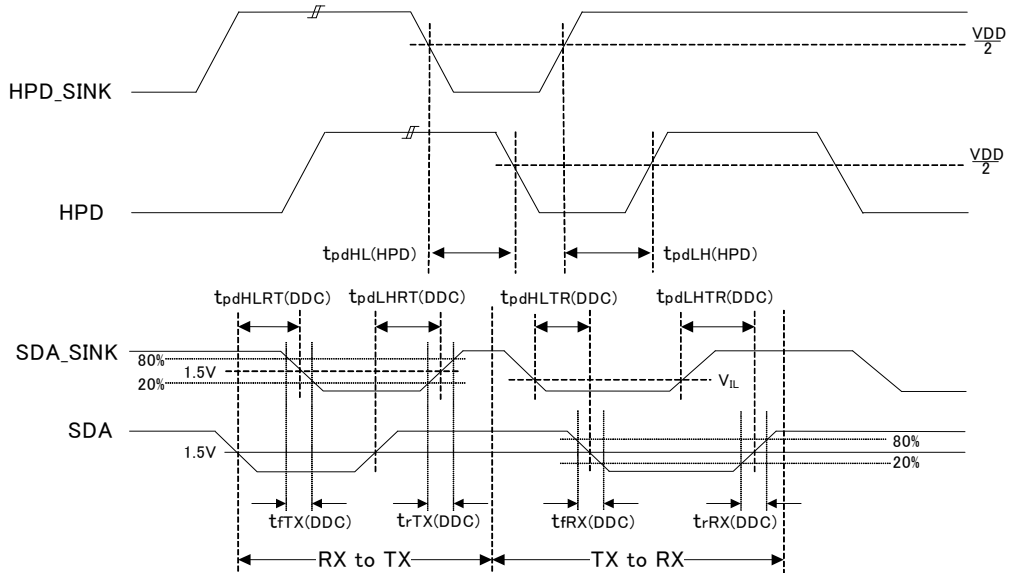


Figure 5-4 DDC and HPD Timing Definitions

1). Y and Z terminal ESD Diode notice.

Y and Z terminals are connected ESD diode.

When $VCC + 0.4 < AVCC$.

BU16024KV flow leak current from AVCC to VCC.

In order to pass the compliance test.

You must use mandatory application, refer Figure 6-1 for "Repeater" or "output Buffer" application.

If you use "Repeater" or "output Buffer"

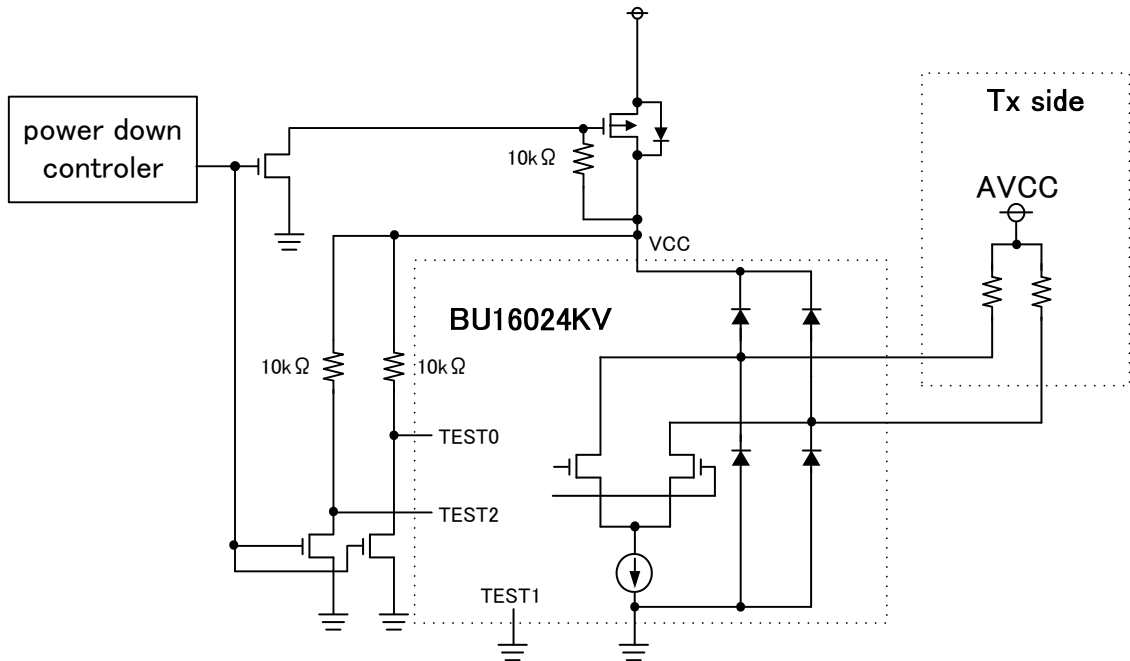


Figure 6-1 Leak current control

2). HPD_SINK Pull down resistance.

HPD_SINK is a 5V tolerant structure shown in Figure 6-2.

It needs some drive current to pull down HPD_SINK "H" to "L"(max10uA@HPD_SINK=2V).

So to pull down HPD_SINK, please use 10kΩ (or under 10kΩ) resistor.

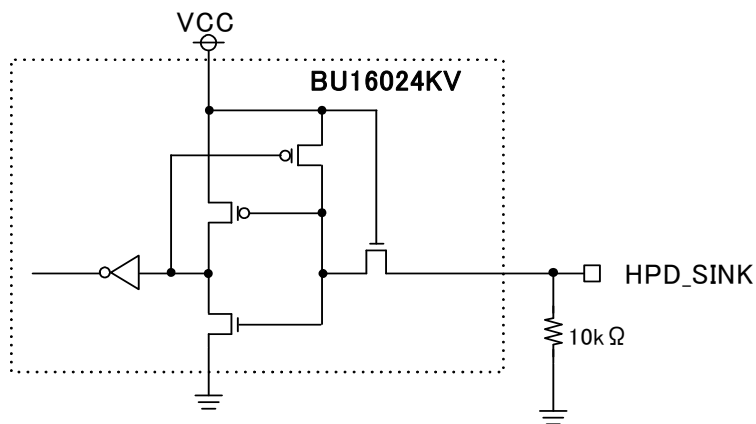


Figure 6-2 HPD_SINK I/O schematic

3). About don't use terminal.
 Unused TMDS input channel can be opened.

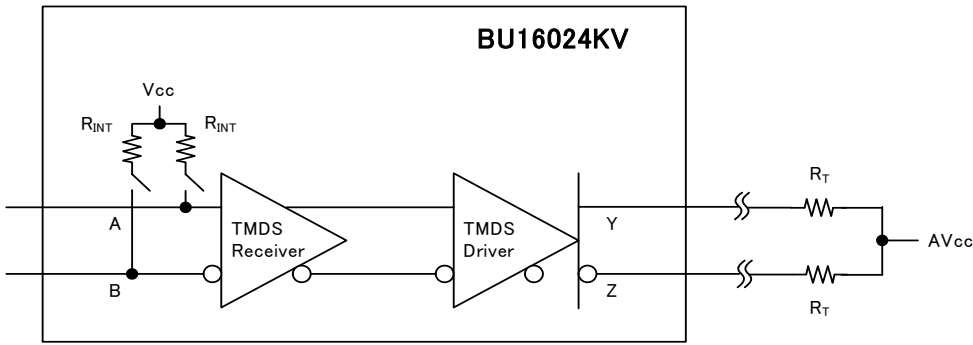


Figure 6-3 TMDS Input Fail-Safe Recommendation

Unused DDC Buffers of R side pulled up to Vdd .

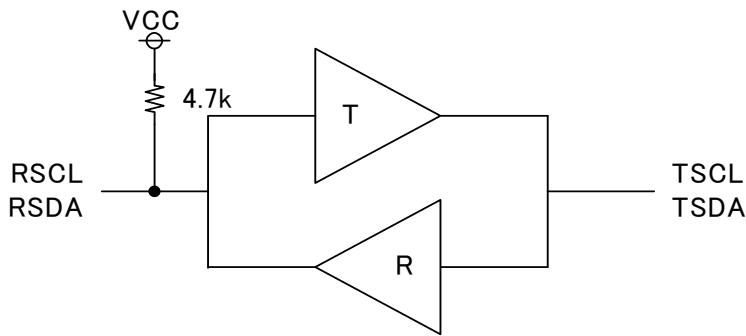


Figure 6-4 DDC Buffers in BU16024KV

Open unused HPDn.

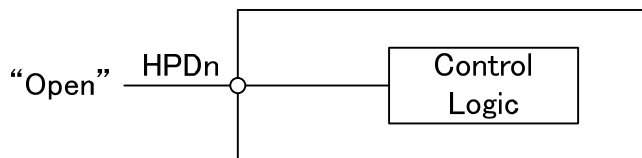


Figure 6-5 Open unused HPDn

4). About serial connect notice.

When HDMI sw output connect to other HDMI sw input like following application.
 There is possibility that. 1080p(12bit) image isn't displayed. It's depend on receiver IC characteristic.
 When system is required 1080p (12bit), Rohm doesn't recommend serial connect application.

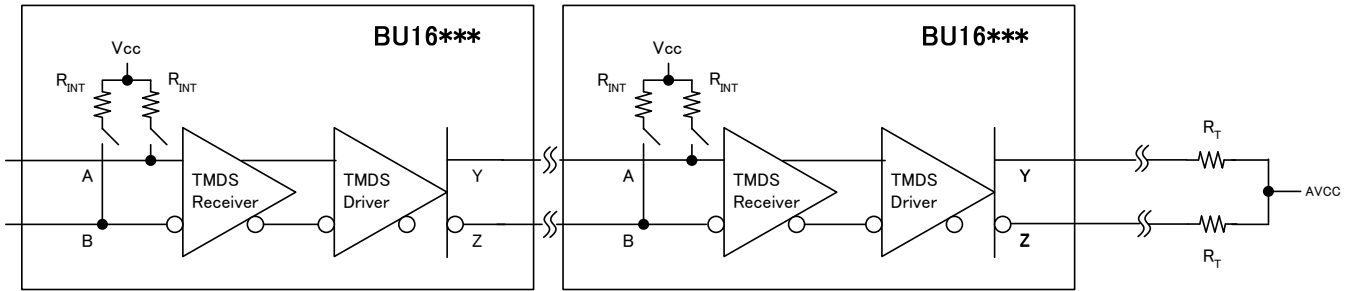


Figure 6-6 serial connect notice

5). AC Coupling capable.

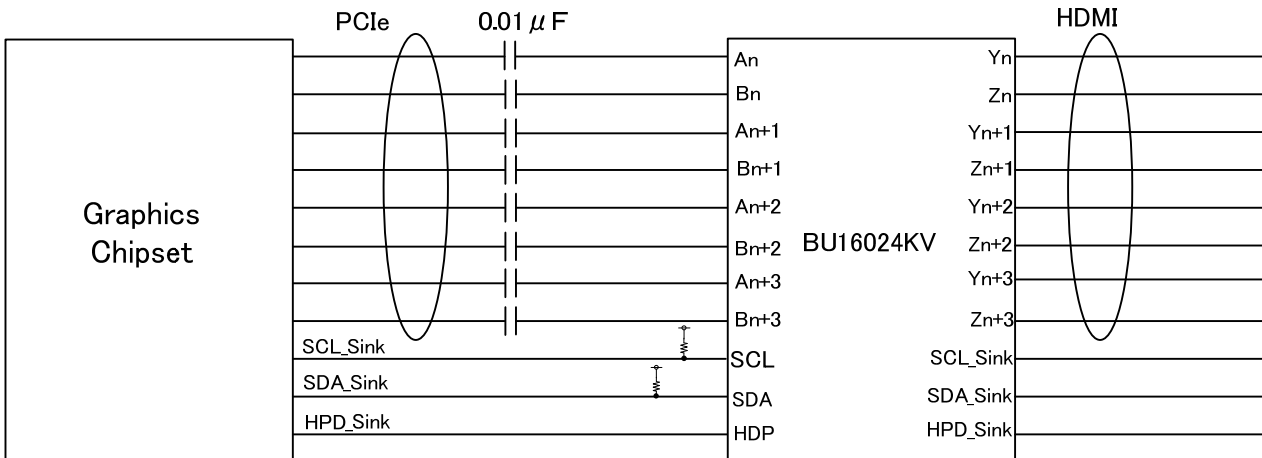


Figure 6-7 AC Coupling capable

6). Offset voltage appearance.

If differential input is opened, offset voltage appear at differential output OE is set to low to avoid it.

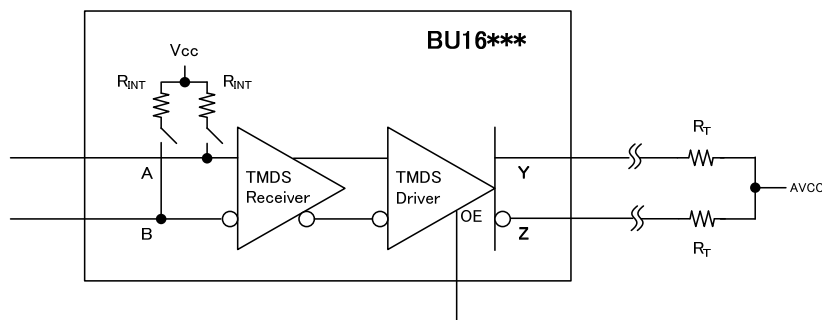


Figure 6-8 Offset voltage avoid

7). Limitation of Master and slave direction.

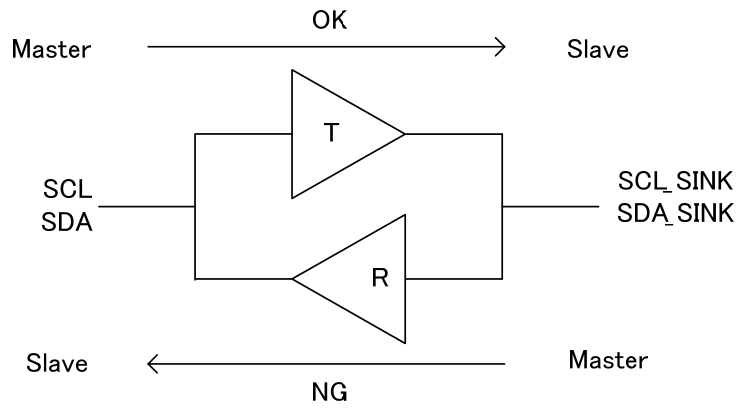


Figure 6-9 Limitation of Master and slave direction

●Ordering part number

B	U	1	6	0	2	4
---	---	---	---	---	---	---

ROHM model name

K	V
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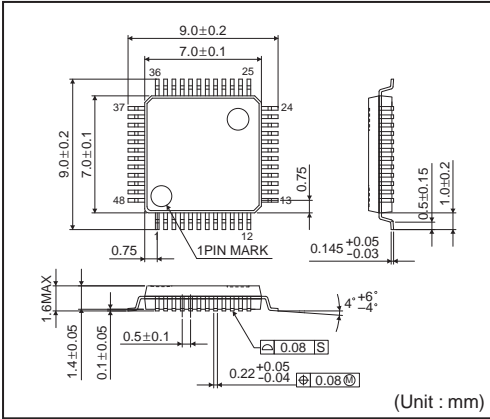
Package type
VQFP48C

E	2
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Packaging and forming specification
E2 =Reel-shaped emboss tapping

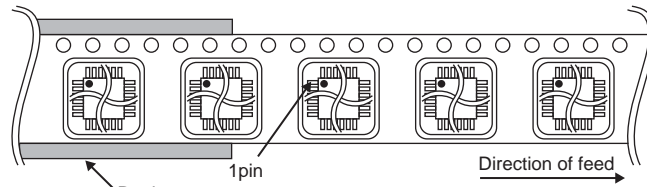
●Package specification

VQFP48C



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	1500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

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