HDMI Switch ICs

3 for input 1 output switch with Termination sense non correspondence (Unsync with HPD_SINK)

BU16027KV

No.09063EDT04

●Description

BU16027KV is 3 for input 1 output HDMI/DVI switch LSI. Each port supports 2.25Gbps. (HDMI 1.3a)
This device control is simple. It requires only 3.3V source and a few GPIO controls.
Terminated resistors(50Ω) are integrated at input port. When channel is not selected, termination resistors are turned off. TMDS inputs are high impedance.
This device is integrated equalization function and DDC buffer function, so It can adapt long cable.

●Features

1) Supports 2.25 Gbps signaling rate for 480i/p, 720i/p, and 1080i/p resolution to 12-bit color depth
2) Compatible with HDMI 1.3a
3) 5V tolerance to all DDC and HPD_SINK inputs
4) Integrated DDC buffer
5) Integrated switchable 50Ωreceiver termination
6) Integrated equalizer circuit to adapt long cable
7) HBM ESD protection exceeds 10kV
8) 3.3V fixed supply to TMDS I/Os
9) 64Pin VQFP package
10) ROHS compatible

●Applications

Digital TV, DVD Player, Set-Top-Box, Audio Video Receiver, Digital Projector, DVI or HDMI Switch Box

●Line up matrix

Part No.	Power Supply (V)	ESD (KV)	Input (ch)	Output (ch)	Data rate (Gbps)	Hot Plug Control	Termination Sense Correspondence	Switching Method	DDC Buffer	Equalizer	De emphasis	Package	RoHS
BU16020KV	3 to 3.6	10	HDMI 4ch	HDMI 1ch	2.7	Yes	Yes	GPIO/I^2C	Yes	Yes (adaptive)	Yes	VQFP100	Yes
BU16018KV	3 to 3.6	10	HDMI 3ch	HDMI 1ch	2.25	Yes	Yes	GPIO	Yes	Yes	Yes	VQFP80	Yes
BU16027KV	3 to 3.6	10	HDMI 3ch	HDMI 1ch	2.25	Yes	Yes	GPIO	Yes	Yes	Yes (Always ON)	VQFP64	Yes
BU16006KV	3 to 3.6	10	HDMI 2ch	HDMI 1ch	2.25	Yes	Yes	GPIO	Yes	Yes	Yes (Always ON)	VQFP64	Yes
BU16024KV	3 to 3.6	10	HDMI 1ch	HDMI 1ch	2.25	Yes	Yes	-	Yes	Yes	Yes	VQFP48C	Yes

© 2009 ROHM Co., Ltd. All rights reserved.

●OUTSIDE DIMENSION CHART

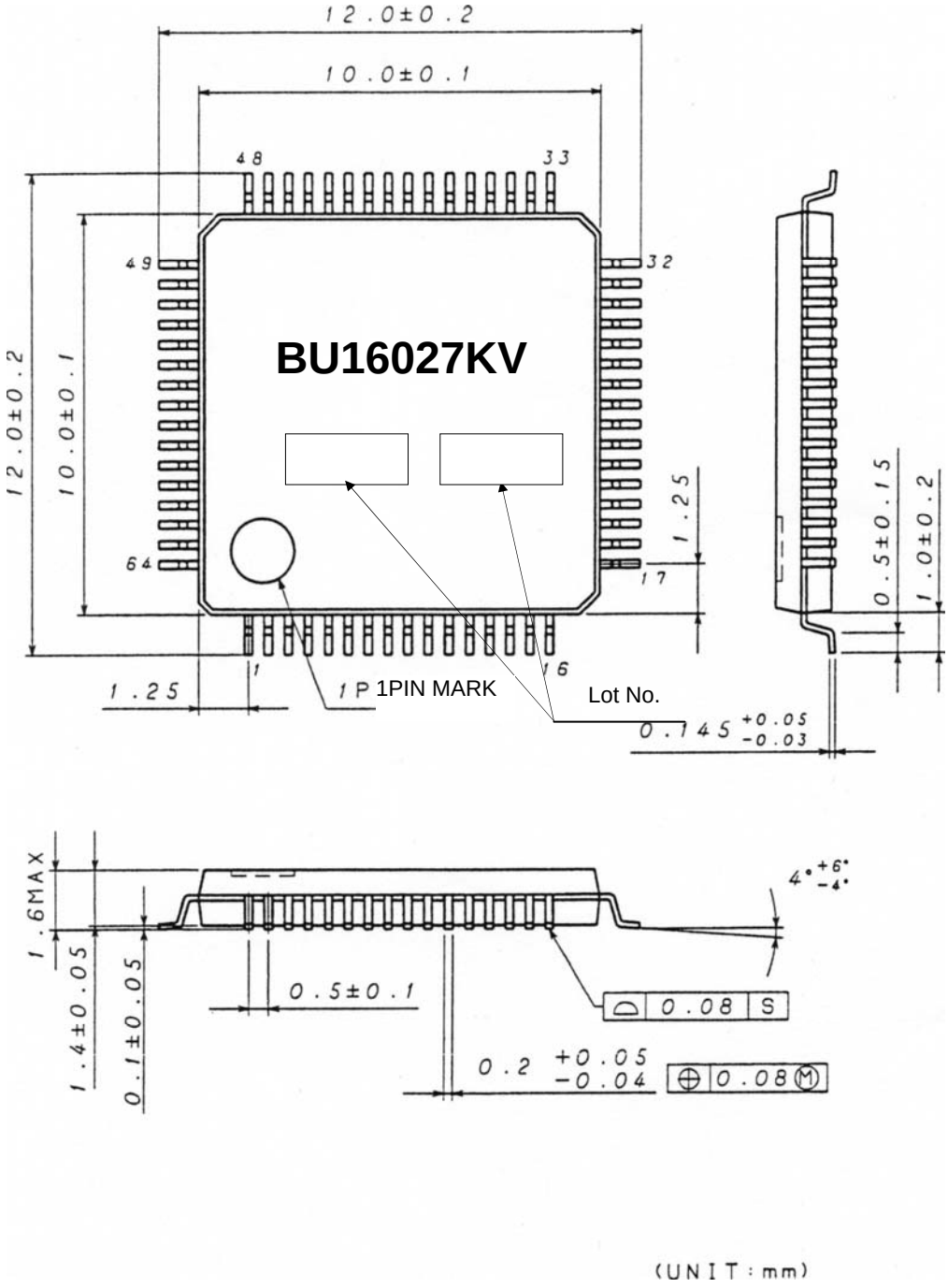


Figure 1-1 Outside dimension chart

© 2009 ROHM Co., Ltd. All rights reserved.

●BLOCK DIAGRAM

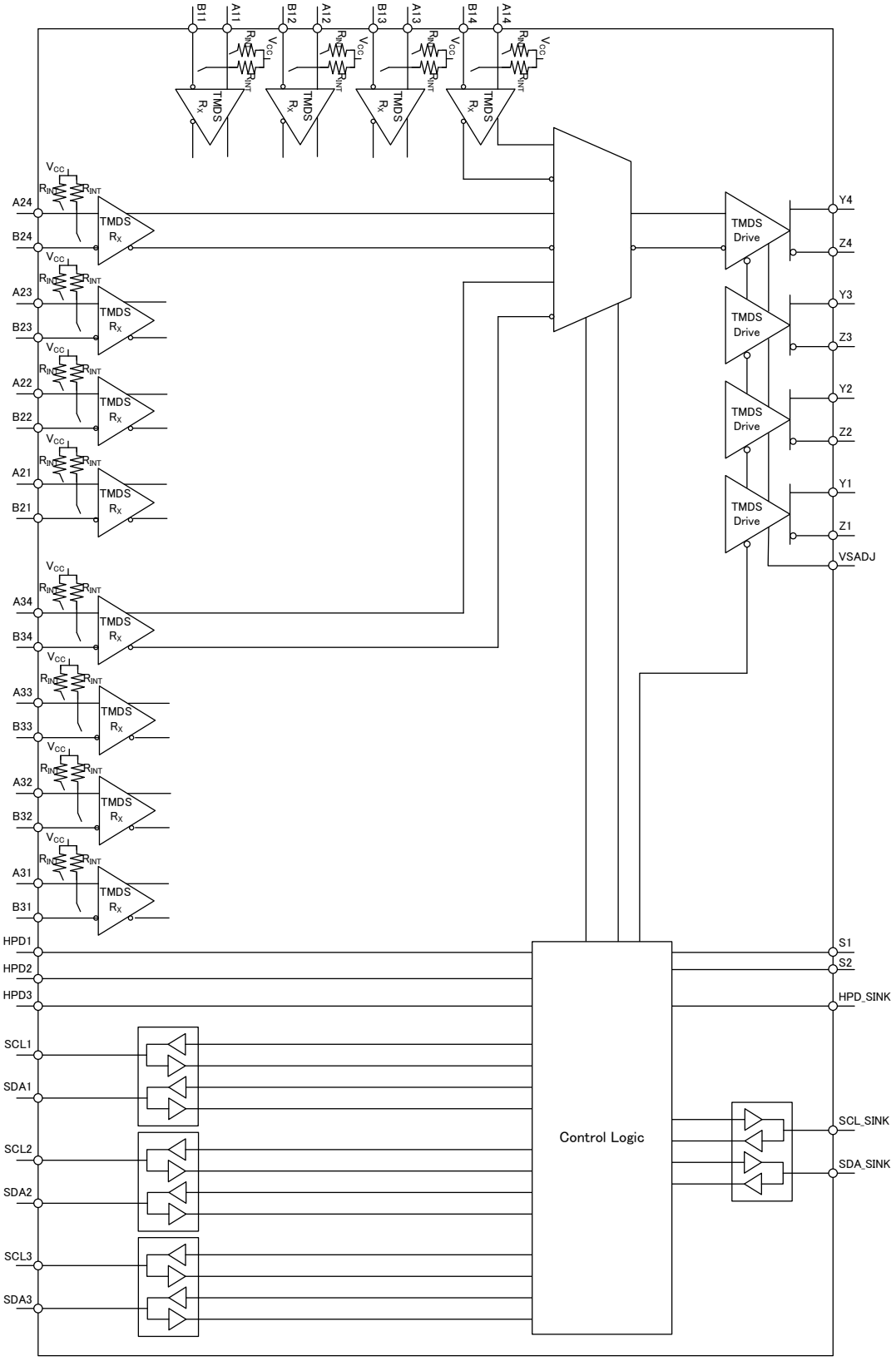


Figure 2-1 Block Diagram

© 2009 ROHM Co., Ltd. All rights reserved.

●PIN EXPLANATION

1). PIN ASSIGNMENT

(TOP VIEW)

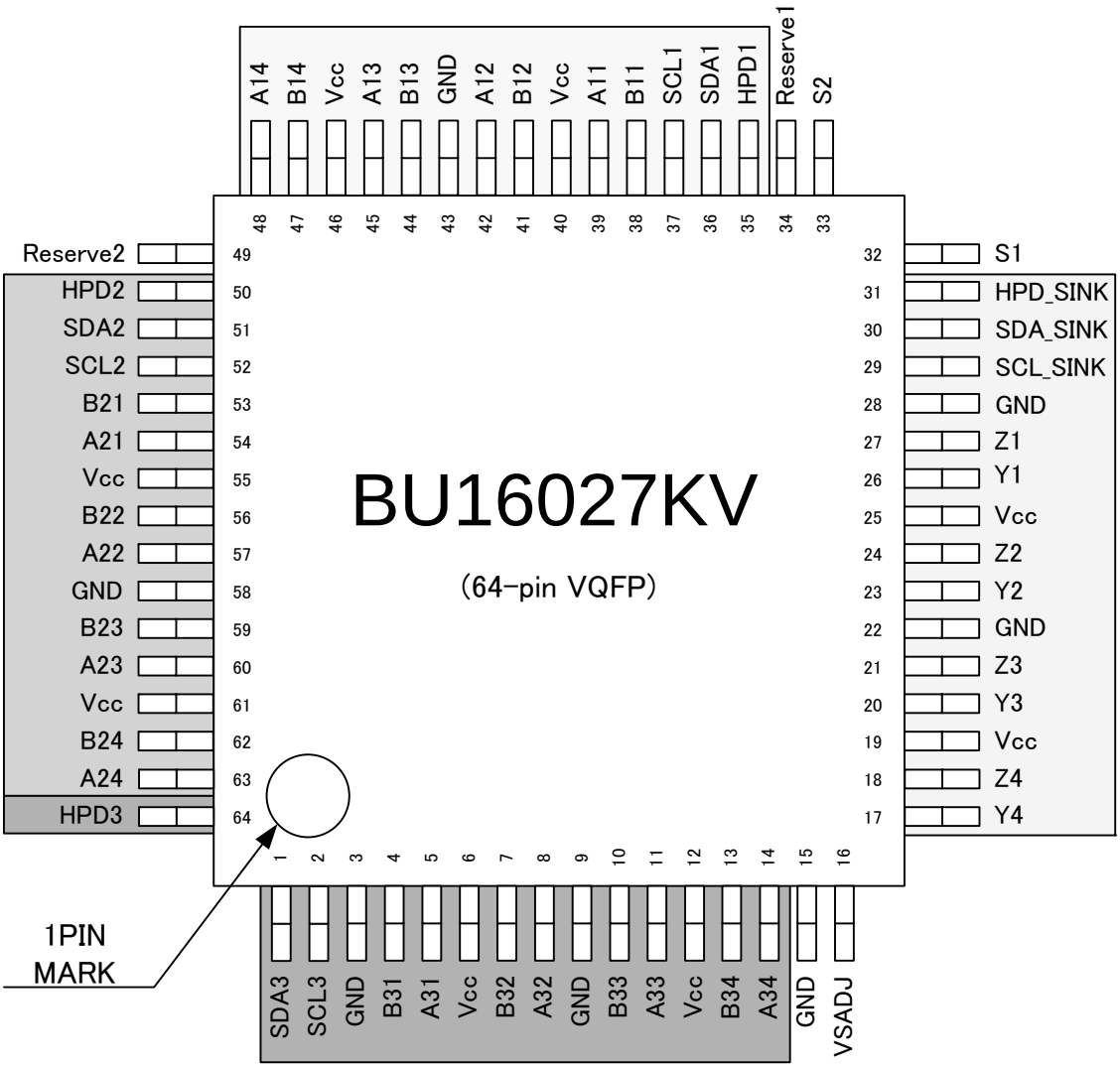


Figure 3-1 Pin Location

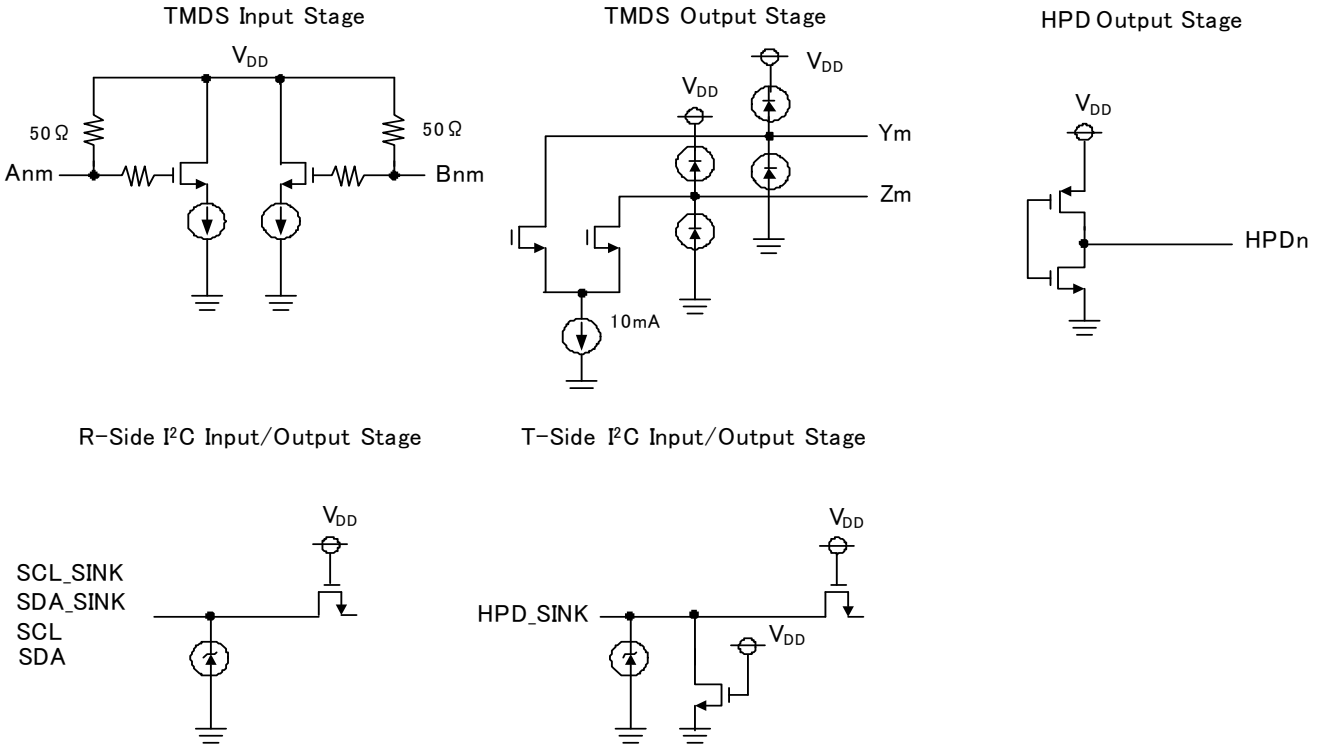
© 2009 ROHM Co., Ltd. All rights reserved.

2). PIN LIST

TERMINAL		I/O	DESCRIPTION
NAME	**No.**		
A11, A12, A13, A14	39, 42, 45, 48	I	Source port 1 TMDS positive inputs
A21, A22, A23, A24	54, 57, 60, 63	I	Source port 2 TMDS positive inputs
A31, A32, A33, A34	5, 8, 11, 14	I	Source port 3 TMDS positive inputs
B11, B12, B13, B14	38, 41, 44, 47	I	Source port 1 TMDS negative inputs
B21, B22, B23, B24	53, 56, 59, 62	I	Source port 2 TMDS negative inputs
B31, B32, B33, B34	4, 7, 10, 13	I	Source port 3 TMDS negative inputs
GND	3, 9, 15, 22, 28, 43, 58	-	Ground
HPD1	35	O	Source port 1 hot plug detector output (status pin)
HPD2	50	O	Source port 2 hot plug detector output (status pin)
HPD3	64	O	Source port 3 hot plug detector output (status pin)
HPD_SINK	31	I	Sink port hot plug detector input (status pin)
Reserve1	34	I/O	In High, Low, and Open, any setting is OK.
Reserve2	49	I/O	Non Connect Pin
SCL1	37	I/O	Source port 1 DDC I^2C clock line
SCL2	52	I/O	Source port 2 DDC I^2C clock line
SCL3	2	I/O	Source port 3 DDC I^2C clock line
SCL_SINK	29	I/O	Sink port DDC I^2C clock line
SDA1	36	I/O	Source port 1 DDC I^2C data line
SDA2	51	I/O	Source port 2 DDC I^2C data line
SDA3	1	I/O	Source port 3 DDC I^2C data line
SDA_SINK	30	I/O	Sink port DDC I^2C data line
S1, S2	32, 33	I	Source selector
VCC	6, 12, 19, 25, 40, 46, 55, 61	-	Power supply
VSADJ	16	I	TMDS compliant voltage swing control (via 4.64kΩ to GND)
Y1, Y2, Y3, Y4	26, 23, 20, 17	O	Sink port TMDS positive outputs
Z1, Z2, Z3, Z4	27, 24, 21, 18	O	Sink port TMDS negative outputs

© 2009 ROHM Co., Ltd. All rights reserved.

●EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



※n=1,2,3 m=1,2,3,4

Figure 4-1 I/O pin schematic diagram

© 2009 ROHM Co., Ltd. All rights reserved.

●SOURCE SELECTION LOOKUP TABLE

CONTROL PINS			I/O SELECTED	HOT PLUG DETECT STATUS			
HPD_SINK	**S1**	**S2**	**Y/Z**	**SCL_SINK SDA_SINK**	**HPD1**	**HPD2**	**HPD3**
H/L	H	H	A1/B1 Terminations of A2/B2 and A3/B3 are disconnected	SCL1 SDA1	HPD _SINK	L	L
H/L	L	H	A2/B2 Terminations of A1/B1 and A3/B3 are disconnected	SCL2 SDA2	L	HPD _SINK	L
H/L	L	L	A3/B3 Terminations of A1/B1 and A2/B2 are disconnected	SCL3 SDA3	L	L	HPD _SINK
H/L	H	L	None (Z) All terminations are disconnected	None (Z) Are pulled HIGH by external pull-up termination	HPD _SINK	HPD _SINK	HPD _SINK

(1)H: Logic high; L: Logic low; X: Don't care; Z: High impedance

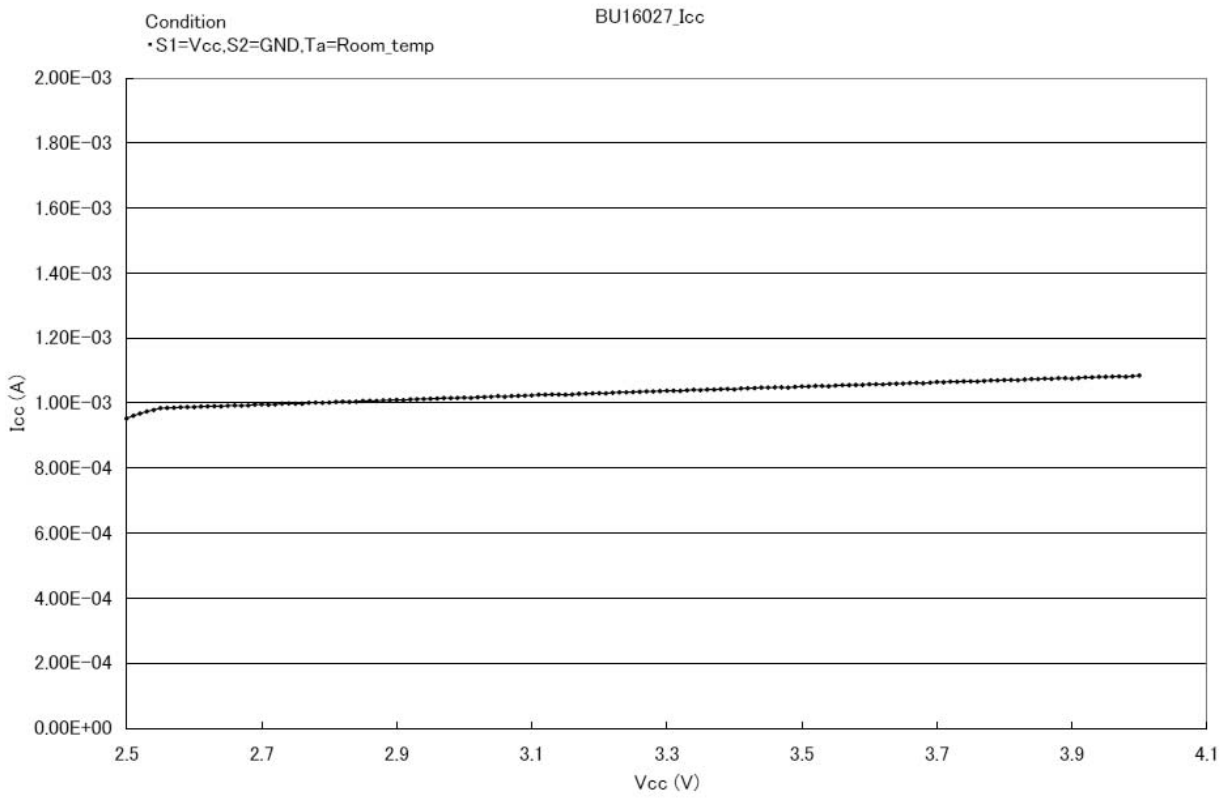


Figure 4-2 Supply voltage(Vcc) vs. Supply current(Icc) [S1=H,S2=L]

© 2009 ROHM Co., Ltd. All rights reserved.

●ERECTRICAL SPECIFICATIONS

1.）ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)(1)

ITEM	MIN.	TYP.	MAX.	UNIT
Power supply voltage(Vcc)	-0.3	-	4.0	V
DDC, HPD_SINK input voltage	-0.3	-	6.0	V
Differential input voltage	2.5	-	4.0	V
S1, S2 input voltage	-0.3	-	4.0	V
Power dissipation	-	-	1250	mW
Strage temperture range	-55	-	125	℃

※70mm×70mm×1.6mm glass epoxy board mount.（Reverse Cu occupation rate：15mm×15mm）
When it's used by than Ta=25℃, it's reduced by 12.5mW/℃.

2.）RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
T_A	Operating free-air temperature	0	-	70	℃
TMDS DIFFERENTIAL PINS					
V_{IC}	Input common mode voltage	V_{CC}–0.6	-	V_{CC}+0.01	V
V_{ID}	Receiver peak-to-peak differential input voltage	150	-	1560	mVp-p
R_{VSADJ}	Resistor for TMDS compliant voltage swing range	4.60	4.64	4.68	kΩ
AV_{CC}	TMDS Output termination voltage, see Figure 5-1.	3	3.3	3.6	V
R_T	Termination resistance, see Figure 5-1.	45	50	55	Ω
Signaling rate		0	-	2.25	Gbps
CONTROL PINS (S1,S2)					
VIH	LVTTL High-level input voltage	2	-	V_{CC}	V
VIL	LVTTL Low-level input voltage	GND	-	0.8	V
STATUS(HPD_SINK)					
V_{IH}	LVTTL High-level input voltage	2.4	-	5.5	V
V_{IL}	LVTTL Low-level input voltage	GND	-	0.8	V
DDC PINS (SCL_SINK, SDA_SINK,SDA[2:1],SCL[2:1])					
$V_{I(DDC)}$	Input voltage	GND	-	5.5	V

© 2009 ROHM Co., Ltd. All rights reserved.

3.）ELECTRICAL CHARACTERISTICS

Over recommended operating conditions (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.(1)	MAX.	
Icc	Supply current	V_{IH}- = Vcc,V_{IL} = Vcc-0.4V,R_{VSADJ} = 4.64kΩ R_T = 50Ω,AVcc = 3.3V Am/Bm = 2.25 Gbps HDMI data pattern, m = 2,3,4 A1,/B1 = 225 MHz clock	-	120	150	mA
P_D	Power dissipation	V_{IH} = V_{cc},V_{IL} = Vcc-0.4V,R_{VSADJ} = 4.64kΩ R_T = 50Ω,AVcc = 3.3V Am/Bm = 2.25Gbps HDMI data pattern, m = 2,3,4 A1/B1 =255 MH_Z clock	-	450	600	mW
TMDS DIFFERENTIAL PINS (A/B;Y/Z)						
V_{OH}	Single-ended high-level output voltage	See Figure 5-2, AVcc = 3.3V, R_T = 50Ω	AVcc-200	-	Avcc-50	mV
V_{OL}	Single-ended low-level output voltage		AVcc-600	-	Avcc-400	mV
V_{SWING}	Single-ended low-level swing voltage		300	-	460	mV
$Vod_{(O)}$	Overshoot of output differential voltage		-	6%	15%	$2xV_{swing}$
$Vod_{(U)}$	Undershoot of output differential voltage		-	12%	25%	$2xV_{swing}$
$V_{OD(pp)}$	Steady state output differential voltage	See Figure 5-2, Am/Bm = 250 Mbps HDMI data pattern , m = 2,3,4 A1/B1 = 25 MHz clock	600	-	920	mVp-p
R_{INT}	Input termination resistance	V_{IN} = 2.9V	45	50	55	Ω
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states		-	5	-	mV

© 2009 ROHM Co., Ltd. All rights reserved.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.(1)	MAX.	
DDC Input and output						
Tx						
V_{IH}	High-level input voltage		2.1	-	5.5	V
V_{IL}	Low-level input voltage		-0.3	-	0.35	V
I_{IKT}	Input leak current,	VI=5.5V	-10	-	10	uA
I_{IKT}	Input leak current,	VI=Vcc	-10	-	10	uA
I_{OHT}	High-level output current	VO=3.6V	-10	-	10	uA
I_{ILT}	Low-level input current	VIL=GND	-10	-	10	uA
V_{OLT}	Low-level output voltage	RL=4.7kΩ	0.43	0.5	0.57	V
V_{OLT}-V_{IL}	Low-level input voltage below output low-level voltage		20	100	190	mV
Rx						
V_{IH}	High-level input voltage		2.4	-	5.5	V
V_{IL}	Low-level input voltage		-0.3	-	0.8	V
I_{IKR}	Input leak current	VI=5.5V	-10	-	10	uA
I_{IKR}	Input leak current	VI=Vcc	-10	-	10	uA
I_{OHR}	High-level output current	VO=3.6V	-10	-	10	uA
I_{ILR}	Low-level input current	VIL=GND	-10	-	10	uA
V_{OLR}	Low-level output voltage	Iout = 4mA	-	-	0.2	V
DDC Input and output						
STATUS PINS (HPD 1, HPD 2, HPD 3)						
$V_{OH(TTL)}$	TTL High –level output voltage	I_{OH} = -8mA	2.4	-	Vcc	V
$V_{OL(TTL)}$	TTL Low –level output voltage	I_{OL} = 8mA	0	-	0.4	V
CONTROL PINS (S1, S2)						
I_{IH}	High –level digital input current	V_{IH} = Vcc	-10	-	10	uA
I_{IL}	Low –level digital input current	V_{IL} = GND	-10	-	10	uA
STATUS PINS (HPD_SINK)						
I_{IH}	High –level digital input current	V_{IH} = 5.5V	10	50	100	uA
		V_{IH} = Vcc	5	30	80	uA
I_{IL}	Low –level digital input current	V_{IL} = GND	-10	-	10	uA

© 2009 ROHM Co., Ltd. All rights reserved.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.(1)	MAX.	
DDC Input and output						
Tx						
V_{IH}	High-level input voltage		2.1	-	5.5	V
V_{IL}	Low-level input voltage		-0.3	-	0.35	V
I_{IKT}	Input leak current,	VI=5.5V	-10	-	10	uA
I_{IKT}	Input leak current,	VI=Vcc	-10	-	10	uA
I_{OHT}	High-level output current	VO=3.6V	-10	-	10	uA
I_{ILT}	Low-level input current	VIL=GND	-10	-	10	uA
V_{OLT}	Low-level output voltage	RL=4.7kΩ	0.43	0.5	0.57	V
V_{OLT}-V_{IL}	Low-level input voltage below output low-level voltage		20	100	190	mV
Rx						
V_{IH}	High-level input voltage		2.4	-	5.5	V
V_{IL}	Low-level input voltage		-0.3	-	0.8	V
I_{IKR}	Input leak current	VI=5.5V	-10	-	10	uA
I_{IKR}	Input leak current	VI=Vcc	-10	-	10	uA
I_{OHR}	High-level output current	VO=3.6V	-10	-	10	uA
I_{ILR}	Low-level input current	VIL=GND	-10	-	10	uA
V_{OLR}	Low-level output voltage	Iout = 4mA	-	-	0.2	V
DDC Input and output						
STATUS PINS (HPD 1, HPD 2, HPD 3)						
$V_{OH(TTL)}$	TTL High –level output voltage	I_{OH} = -8mA	2.4	-	Vcc	V
$V_{OL(TTL)}$	TTL Low –level output voltage	I_{OL} = 8mA	0	-	0.4	V
CONTROL PINS (S1, S2)						
I_{IH}	High –level digital input current	V_{IH} = Vcc	-10	-	10	uA
I_{IL}	Low –level digital input current	V_{IL} = GND	-10	-	10	uA
STATUS PINS (HPD_SINK)						
I_{IH}	High –level digital input current	V_{IH} = 5.5V	10	50	100	uA
		V_{IH} = Vcc	5	30	80	uA
I_{IL}	Low –level digital input current	V_{IL} = GND	-10	-	10	uA

© 2009 ROHM Co., Ltd. All rights reserved.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.(1)	MAX.	
TMDS DIFFERENTIAL PINS (Y/Z)						
t_{PLH}	Propagation delay time low-high-level output	See Figure 5-2, AV_{CC} = 3.3V, R_T = 50Ω	-	480	-	ps
t_{PHL}	Propagation delay time low-high-level output		-	500	-	ps
t_r	Differential output signal rise time (20%-80%)		-	150	-	ps
t_f	Differential output signal fall time (20%-80%)		-	150	-	ps
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)		-	20	-	ps
$t_{sk(D)}$	Intra-pair differential skew, see Figure 5-3.		-	50	-	ps
$t_{sk(o)}$	Inter-pair channel-to-channel output skew(2)		-	50	-	ps
$t_{sk(pp)}$	Part to part skew(3)		-	400	-	ps
DDC I/O PINS (SCL, SCL_SINK, SDA, SDA_SINK)						
t_{pdLHTR} (DDC)	Propagation delay time, low-to-high-level output Tx to Rx	R_L = 4.7kΩ C_L = 100pF	-	650	-	ns
t_{pdHLTR} (DDC)	Propagation delay time, high-to-low-level output Tx to Rx		-	200	-	ns
t_{pdLHRT} (DDC)	Propagation delay time, low-to-high-level output Rx to Tx	R_L = 1.67kΩ C_L = 400pF	-	500	-	ns
t_{pdHLRT} (DDC)	Propagation delay time, high-to-low-level output Rx to Tx		-	350	-	ns
tr $Tx_{(DDC)}$	Tx output Rise time	R_L = 4.7kΩ C_L = 100pF	-	800	-	ns
tf $Tx_{(DDC)}$	Tx output Fall time		-	150	-	ns
tr $Rx_{(DDC)}$	Rx output Rise time	R_L = 1.67kΩ C_L = 400pF	-	950	-	ns
tf $Rx_{(DDC)}$	Rx output Fall time		-	50	-	ns
t_{sx}	Select to switch output		-	8	-	ns
t_{dis}	Disable time		-	5	-	ns
t_{en}	Enable time		-	7	-	ns
$t_{sx(DDC)}$	Switch time from SCLn to SCL_SINK	C_L=10pF	-	800	-	ns
C_{IO}	Input/output capacitance	V_I=0V		15		pF
STATUS PINS (HPD1,HPD2,HPD3)						
$t_{pdLH(HPD)}$	Propagation delay time, low-to-high-level output from HPD_SINK to HPDn(n=1,2,3)	C_L=10pF	-	5	-	ns
$t_{pdHL(HPD)}$	Propagation delay time, high-to-low-level output from HPD_SINK to HPDn(n=1,2,3)	C_L=10pF	-	5	-	ns
$t_{sx(HPD)}$	Switch time from port select to the latest valid status of HPD	C_L=10pF	-	8	-	ns

Note:
1. All typical values are at 25℃ and with a 3.3V supply.
2. $t_{sk(o)}$ is the magnitude of the difference in propagation delay times between any specified terminals of channel 2 to 4 of a devices when inputs are tied together.
3. $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of channel 2 to 4 of two devices, or between channel 1 of two devices, when both devices operate with the same source, the same supply voltages, at the same temperature, and have identical packages and test circuits.

© 2009 ROHM Co., Ltd. All rights reserved.

● MEASUREMENT SYMBOL AND CIRCUIT

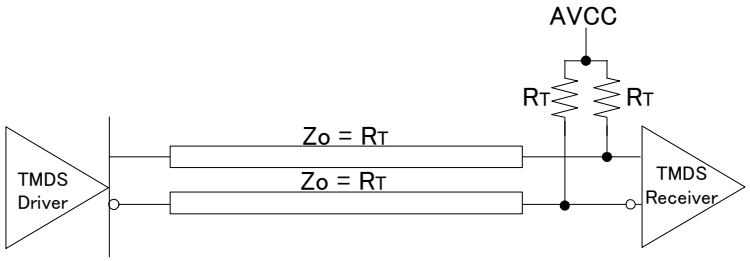
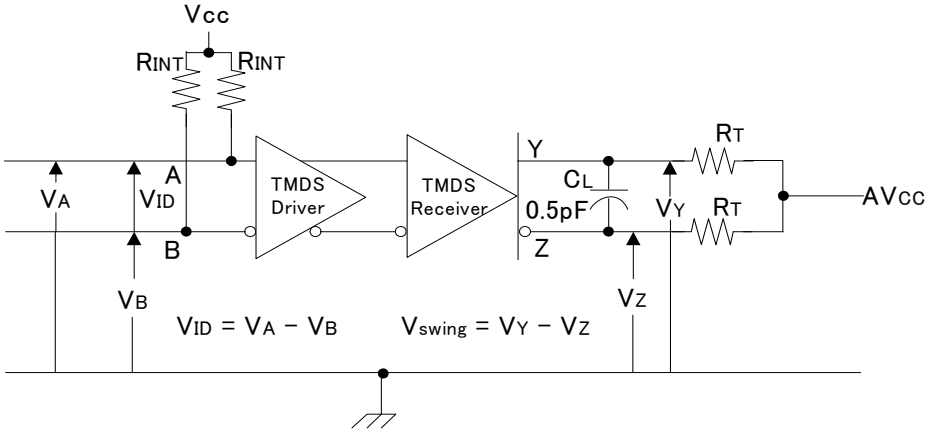


Figure 5-1 Termination for TMDS Output Driver



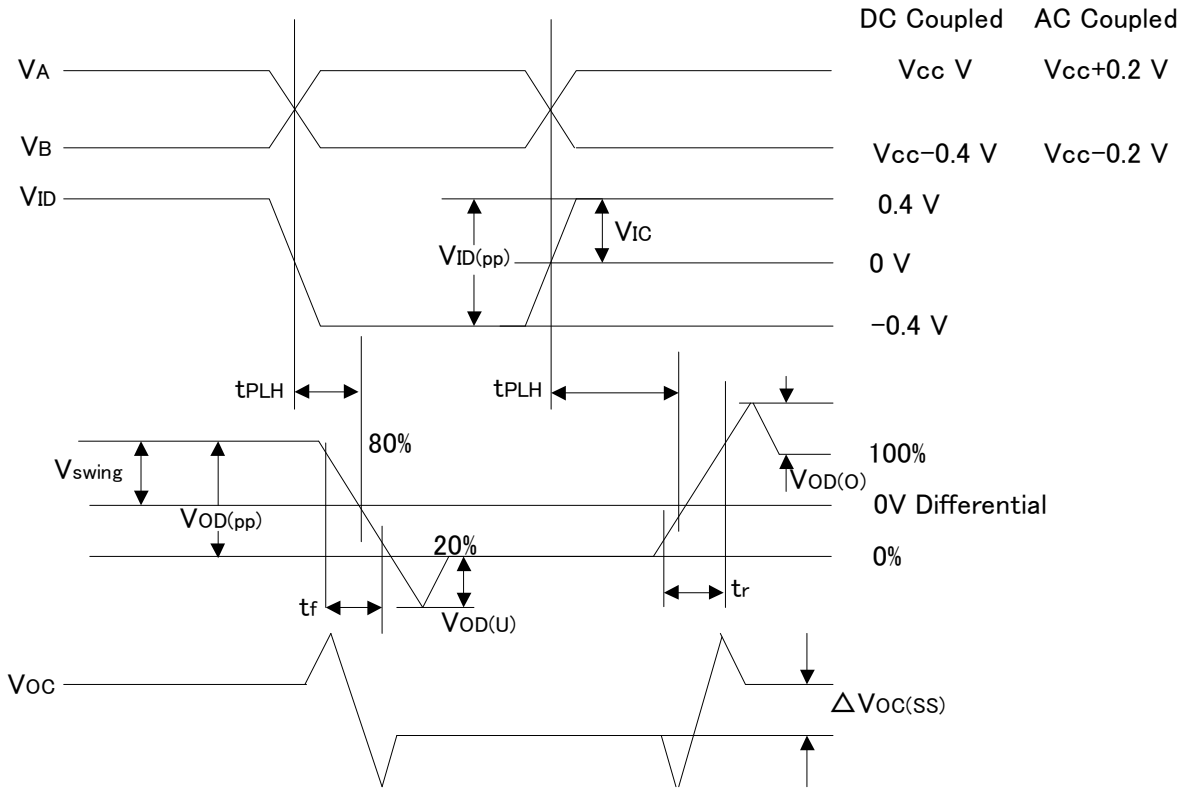


Figure 5-2 Timing Test Circuit and Definitions

© 2009 ROHM Co., Ltd. All rights reserved.

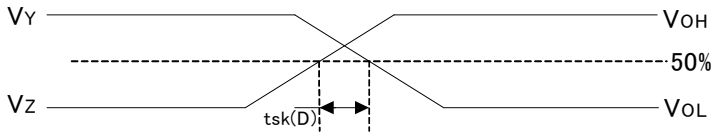


Figure 5-3 Definition of Intra-Pair Differential Skew

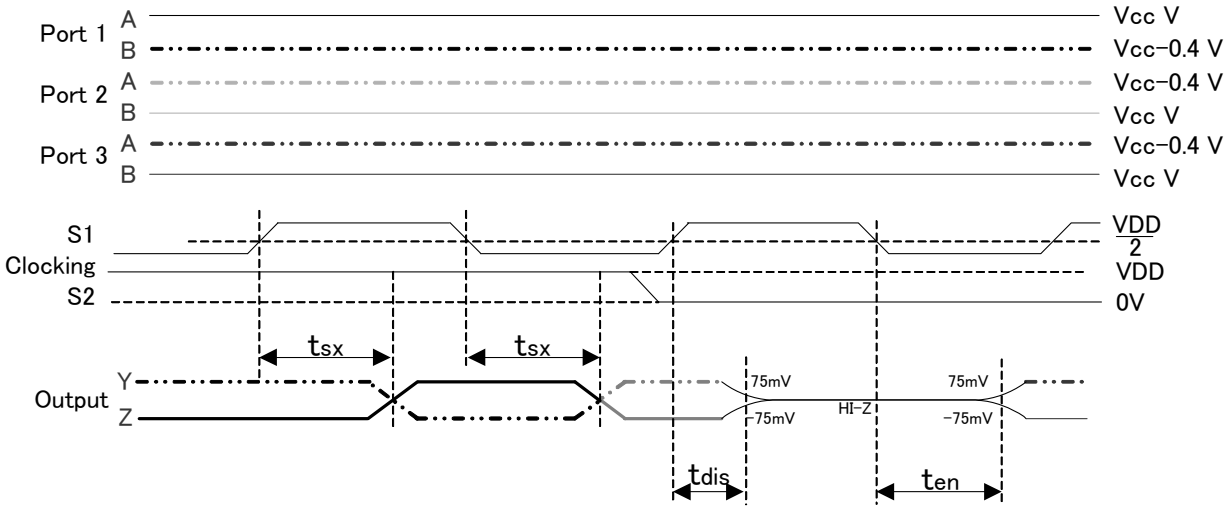


Figure 5-4 TMDS Outputs Control Timing Definitions

© 2009 ROHM Co., Ltd. All rights reserved.

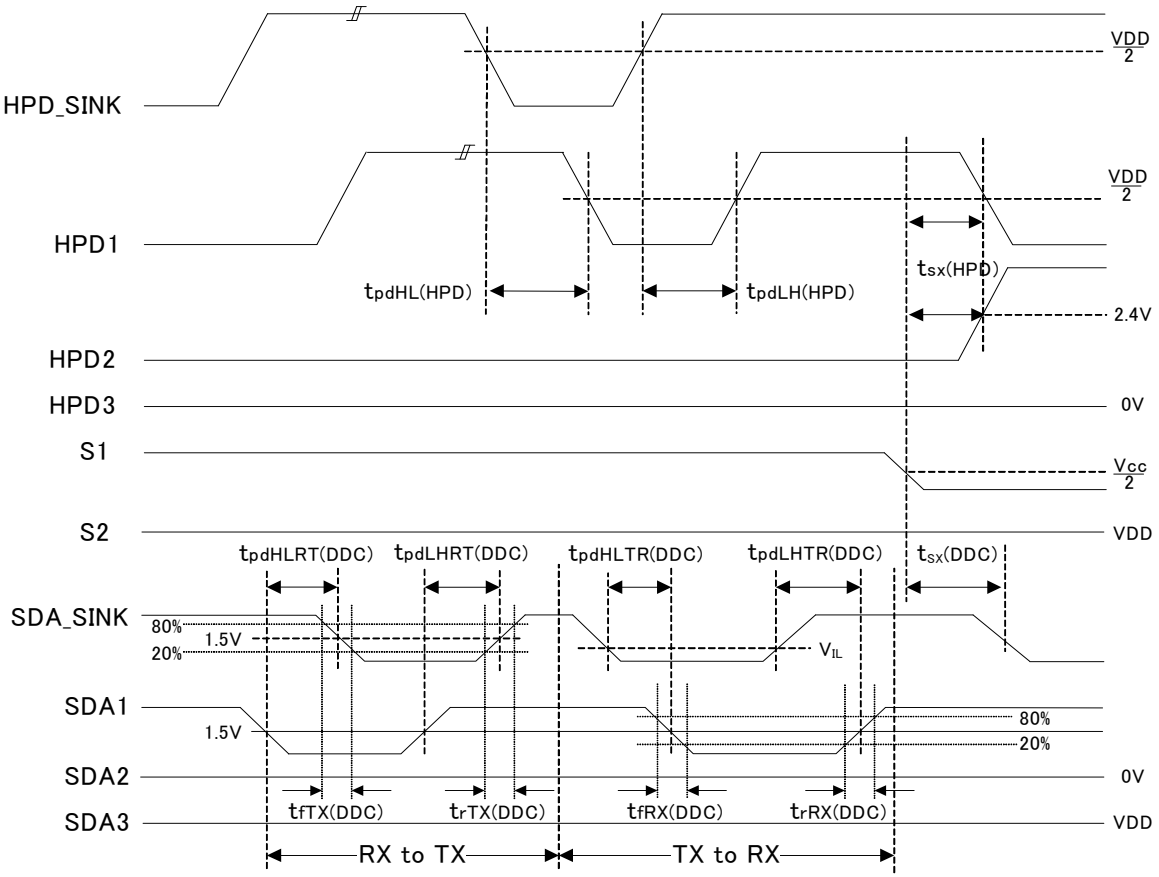


Figure 5-5 DDC and HPD Timing Definitions

© 2009 ROHM Co., Ltd. All rights reserved.

1). HPD_SINK Pull down resistance.

HPD_SINK is a 5V tolerant structure shown in Figure 6-1.
It needs some drive current to pull down HPD_SINK "H" to "L"(max10uA@HPD_SINK=2V).
So to pull down HPD_SINK, please use 10kΩ(or under 10kΩ) resistor.

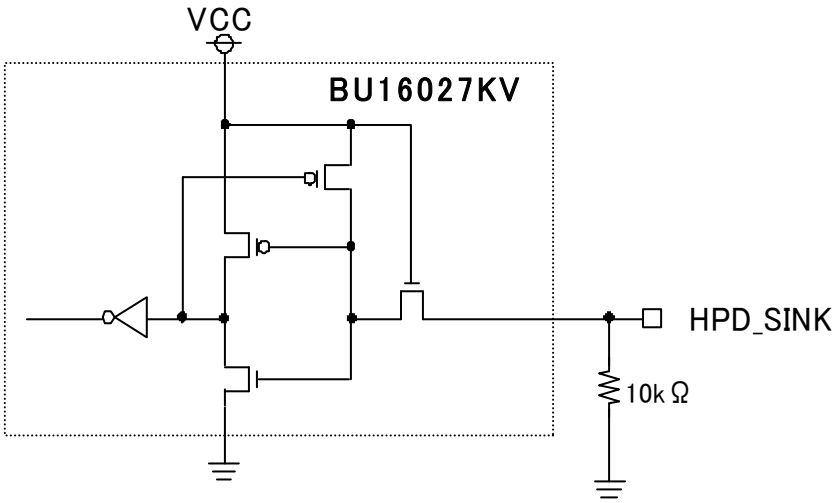


Figure 6-1 HPD_SINK I/O schematic

2). About don't use terminal.
Unused TMDS input channel can be opened.

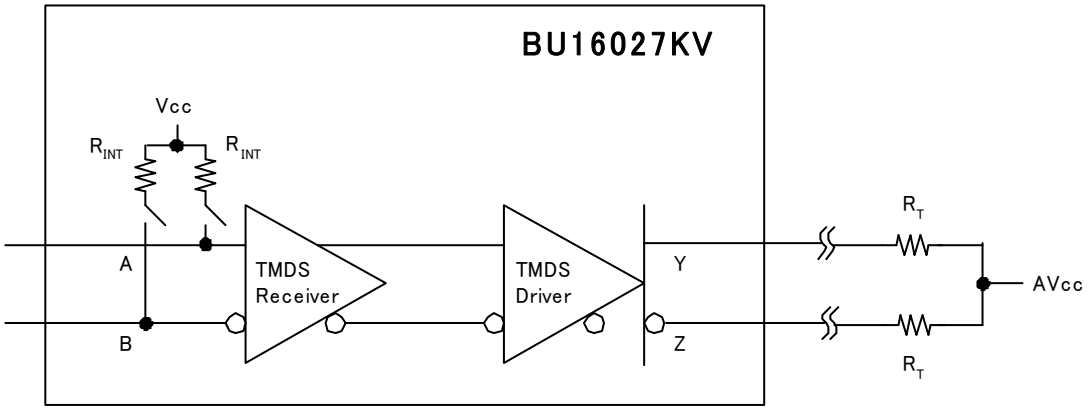


Figure 6-2 TMDS Input Fail-Safe Recommendation

Unused DDC Buffers of R side polled up to Vdd.

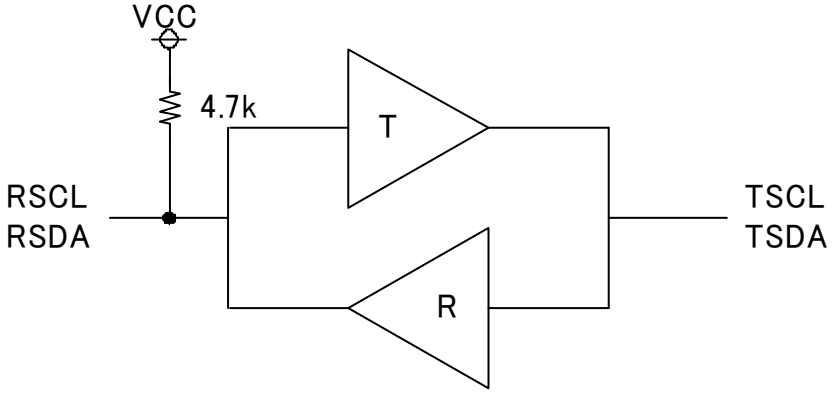


Figure 6-3 DDC Buffers in BU16027KV

© 2009 ROHM Co., Ltd. All rights reserved.

Open unused HPDn.

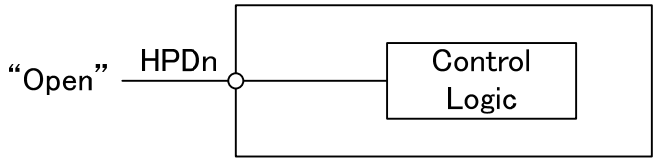


Figure 6-4 Open unused HPDn

3）. About serial connect notice.
When HDMI sw output connect to other HDMI sw input like following application.
There is possibility that. 1080p(12bit) image isn’t displayed. It’s depend on receiver IC characteristic.
When system is required 1080p (12bit) Rohm doesn’t recommend serial connect application. .

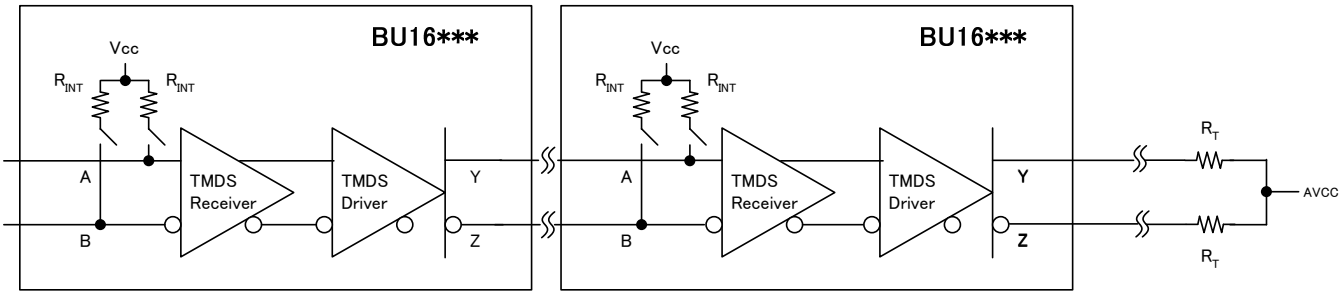


Figure 6-5 serial connect notice

4). Offset voltage appearance.
If differential input is opened, offset voltage appear at differential output OE is set to low to avoid it.

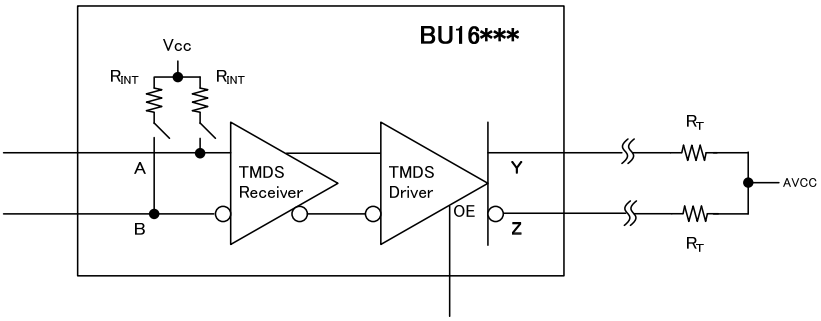


Figure 6-6 Offset voltage avoid

© 2009 ROHM Co., Ltd. All rights reserved.

5). Limitation of Master and slave direction.

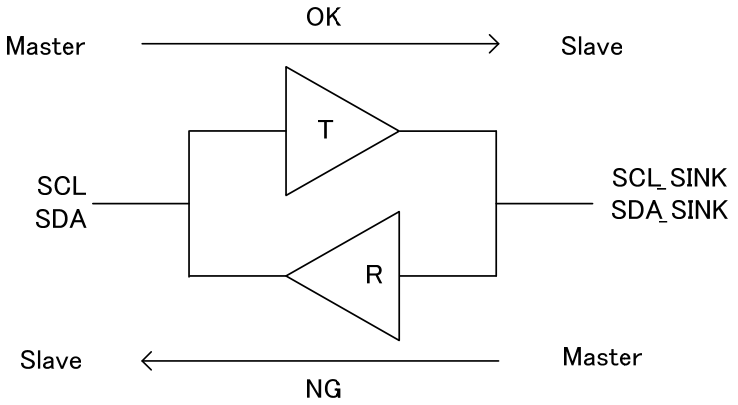


Figure 6-7 Limitation of Master and slave direction

6). Attention in use as repeater.

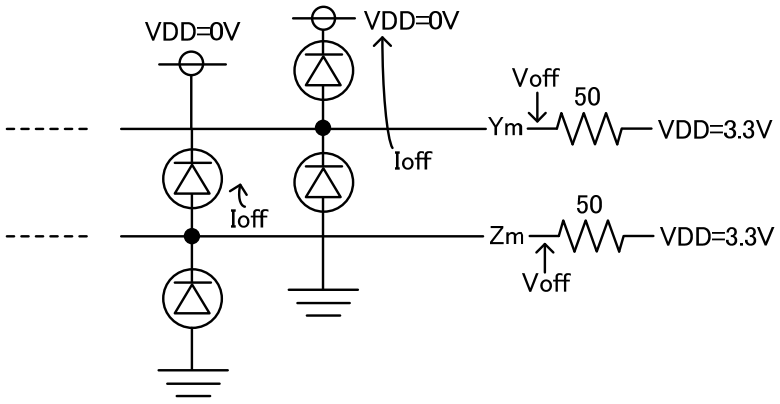


Figure 6-8 Ioff specification not meet to HDMI CTS

Depend on HDMI CTS, Voff must be less than VDD-10mV, but this IC not meet to CTS cause of Ioff.

© 2009 ROHM Co., Ltd. All rights reserved.

●Ordering part number

B	U	1	6	0	2	7

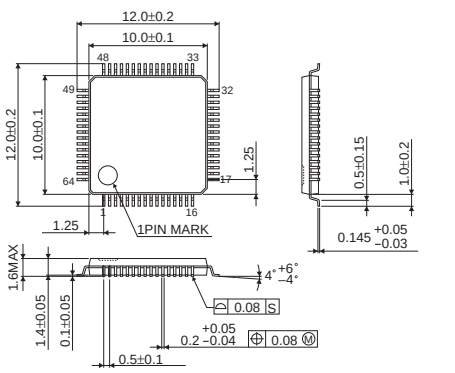
ROHM model name

K	V

Package type
VQFP64

●Package specification

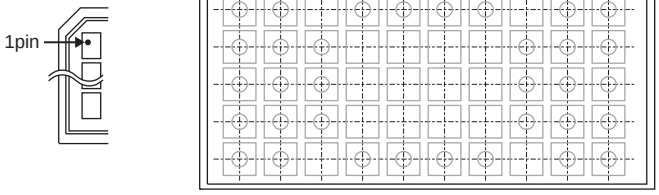
VQFP64



(Unit : mm)

<Tape and Reel information>

Container	Tray (with dry pack)
Quantity	1000pcs
Direction of feed	Direction of product is fixed in a tray



∗Order quantity needs to be multiple of the minimum quantity.

© 2009 ROHM Co., Ltd. All rights reserved.

Notes

No copying or reproduction of this document, in part or in whole, is permitted without the consent of ROHM Co.,Ltd.

The content specified herein is subject to change for improvement without notice.

The content specified herein is for the purpose of introducing ROHM's products (hereinafter "Products"). If you wish to use any such Product, please be sure to refer to the specifications, which can be obtained from ROHM upon request.

Examples of application circuits, circuit constants and any other information contained herein illustrate the standard usage and operations of the Products. The peripheral conditions must be taken into account when designing circuits for mass production.

Great care was taken in ensuring the accuracy of the information specified in this document. However, should you incur any damage arising from any inaccuracy or misprint of such information, ROHM shall bear no responsibility for such damage.

The technical information specified herein is intended only to show the typical functions of and examples of application circuits for the Products. ROHM does not grant you, explicitly or implicitly, any license to use or exercise intellectual property or other rights held by ROHM and other parties. ROHM shall bear no responsibility whatsoever for any dispute arising from the use of such technical information.

The Products specified in this document are intended to be used with general-use electronic equipment or devices (such as audio visual equipment, office-automation equipment, communication devices, electronic appliances and amusement devices).

The Products specified in this document are not designed to be radiation tolerant.

While ROHM always makes efforts to enhance the quality and reliability of its Products, a Product may fail or malfunction for a variety of reasons.

Please be sure to implement in your equipment using the Products safety measures to guard against the possibility of physical injury, fire or any other damage caused in the event of the failure of any Product, such as derating, redundancy, fire control and fail-safe designs. ROHM shall bear no responsibility whatsoever for your use of any Product outside of the prescribed scope or not in accordance with the instruction manual.

The Products are not designed or manufactured to be used with any equipment, device or system which requires an extremely high level of reliability the failure or malfunction of which may result in a direct threat to human life or create a risk of human injury (such as a medical instrument, transportation equipment, aerospace machinery, nuclear-reactor controller, fuel-controller or other safety device). ROHM shall bear no responsibility in any way for use of any of the Products for the above special purposes. If a Product is intended to be used for any such special purpose, please contact a ROHM sales representative before purchasing.

If you intend to export or ship overseas any Product or technology specified herein that may be controlled under the Foreign Exchange and the Foreign Trade Law, you will be required to obtain a license or permit under the Law.

ROHM SEMICONDUCTOR

Thank you for your accessing to ROHM product informations.
More detail product informations and catalogs are available, please contact us.

ROHM Customer Support System

http://www.rohm.com/contact/

© 2009 ROHM Co., Ltd. All rights reserved.