National Semiconductor

February 1988

CD4043BM/CD4043BC Quad TRI-STATE® NOR R/S Latches
CD4044BM/CD4044BC Quad TRI-STATE NAND R/S Latches

General Description

CD4043BM/CD4043BC are quad cross-couple TRI-STATE CMOS NOR latches, and CD4044BM/CD4044BC are quad cross-couple TRI-STATE CMOS NAND latches. Each latch has a separate Q output and individual SET and RESET inputs. There is a common TRI-STATE ENABLE input for all four latches. A logic "1" on the ENABLE input connects the latch states to the Q outputs. A logic "0" on the ENABLE input disconnects the latch states from the Q outputs resulting in an open circuit condition on the Q output. The TRI-STATE feature allows common bussing of the outputs.

Features

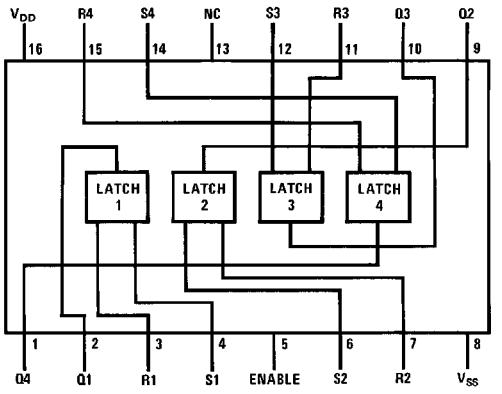
- Wide supply voltage range — 3V to 15V
- Low power — 100 nW (typ.)
- High noise immunity — 0.45 V_{DD} (typ.)
- Separate SET and RESET inputs for each latch
- NOR and NAND configuration
- TRI-STATE output with common output enable

Applications

- Multiple bus storage
- Strobed register
- Four bits of independent storage with output enable
- General digital logic

Connection Diagrams

CD4043BM/CD4043BC
Dual-In-Line and Flat Packages



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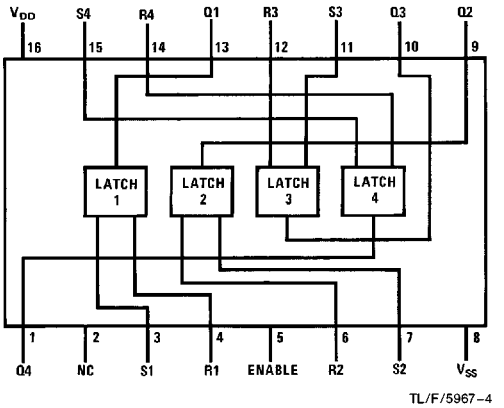
Top View

CD4044BM/CD4044BC
Dual-In-Line and Flat Packages



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Top View

Order Number CD4043B or CD4044B

Truth Table

CD4043BM/CD4043BC

S	R	E	Q
X	X	0	OC
0	0	1	NC
1	0	1	1
0	1	1	0
1	1	1	Δ

CD4044BM/CD4044BC

S	R	E	Q
X	X	0	OC
1	1	1	NC
0	1	1	1
1	0	1	0
0	0	1	ΔΔ

OC — TRI-STATE
NC — No change
X — Don't care
Δ — Dominated by S = 1 input
ΔΔ — Dominated by R = 0 input

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{DD})	−0.5V to +18V
Input Voltage (V_{IN})	−0.5V to V_{DD} +0.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{DD})	3.0V to 15V
Input Voltage (V_{IN})	0 to V_{DD} V
Operating Temperature Range (T_A)	
CD4043BM, CD4044BM	−55°C to +125°C
CD4043BC, CD4044BC	−40°C to +85°C

DC Electrical Characteristics CD4043BM/CD4044BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		5.0		0.01	5.0		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		10		0.01	10		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		20		0.02	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| \leq 1$ μA, V_{IL} = 0V, V_{IH} = V_{DD}								
		V_{DD} = 5.0V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| \leq 1$ μA, V_{IL} = 0V, V_{IH} = V_{DD}								
		V_{DD} = 5.0V	4.95		4.95	5.0		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| \leq 1$ μA								
		V_{DD} = 5.0V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| \leq 1$ μA								
		V_{DD} = 5.0V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 5.0V, V_O = 1.0V or 9.0V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11		11	8.25		11		V
I_{OL}	Low Level Output Current	V_{IL} = 0V, V_{IH} = V_{DD}								
		V_{DD} = 5.0V, V_O = 0.4V	0.64		0.51	1.0		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.6		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	6.8		2.4		mA
I_{OH}	High Level Output Current	V_{IL} = 0V, V_{IH} = V_{DD}								
		V_{DD} = 5.0V, V_O = 4.6V	−0.64		−0.51	−0.4		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−1.0		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−3.0		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4043BC/CD4044BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		20		0.01	20		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		40		0.01	40		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		80		0.02	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| \leq 1$ μA, V_{IL} = 0V, V_{IH} = V_{DD}								
		V_{DD} = 5.0V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| \leq 1$ μA, V_{IL} = 0V, V_{IH} = V_{DD}								
		V_{DD} = 5.0V	4.95		4.95	5.0		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V

DC Electrical Characteristics CD4043BC/CD4044BC (Continued)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
V_{IL}	Low Level Input Voltage	$\|I_O\| \leq 1\ \mu A$								
		$V_{DD} = 5.0V$, $V_O = 0.5V$ or $4.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1.0V$ or $9.0V$		3.0		4.5	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| \leq 1\ \mu A$								
		$V_{DD} = 5.0V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5			3.5		V
		$V_{DD} = 5.0V$, $V_O = 1.0V$ or $9.0V$	7.0		7.0			7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11		11			11		V
I_{OL}	Low Level Output Current (Note 3)	$V_{IL} = 0V$, $V_{IH} = V_{DD}$								
		$V_{DD} = 5.0V$, $V_O = 0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.3		1.1	2.2		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	3.6		3.0	6.0		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{IL} = 0V$, $V_{IH} = V_{DD}$								
		$V_{DD} = 5.0V$, $V_O = 4.6V$	−0.52		−0.44	−0.32		−0.36		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−1.3		−1.1	−0.8		−0.9		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−3.6		−3.0	−2.4		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$	−0.3			−0.3			−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$	0.3			0.3			1.0	μA

AC Electrical Characteristics*

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, input $t_r = t_f = 20$ ns, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}, t_{PHL}	Propagation Delay S or R to Q	$V_{DD} = 5.0V$		175	350	ns
		$V_{DD} = 10V$		75	175	ns
		$V_{DD} = 15V$		60	120	ns
t_{PZH}, t_{PHZ}	Propagation Delay Enable to Q (High)	$V_{DD} = 5.0V$		115	230	ns
		$V_{DD} = 10V$		55	110	ns
		$V_{DD} = 15V$		40	80	ns
t_{PZL}, t_{PLZ}	Propagation Delay Enable to Q (Low)	$V_{DD} = 5.0V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5.0V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{WO}	Minimum SET or RESET Pulse Width	$V_{DD} = 5.0V$		80	160	ns
		$V_{DD} = 10V$		40	80	ns
		$V_{DD} = 15V$		20	40	ns
C_{IN}	Input Capacitance			5.0	7.5	pF

*AC Parameters are guaranteed by DC correlated testing.

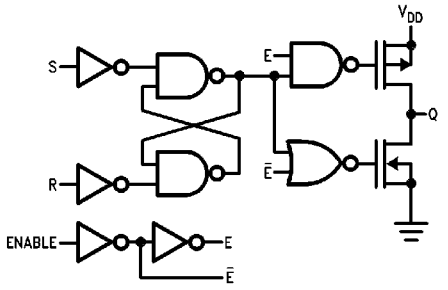
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Schematic Diagrams

CD4043BM/CD4043BC



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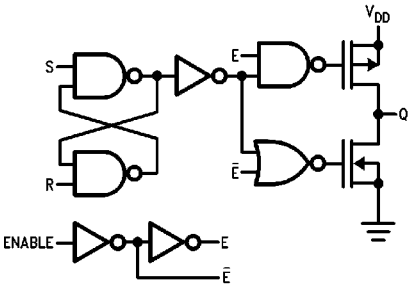
CD4044BM/CD4044BC



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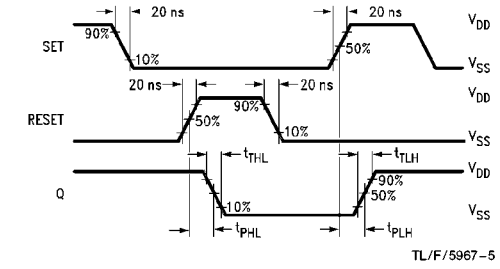
Timing Waveforms

CD4043B



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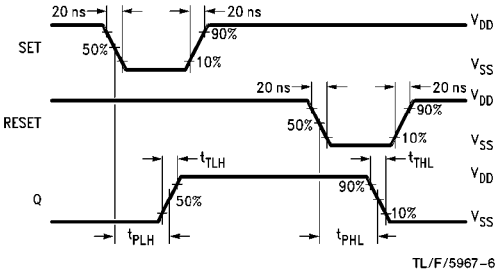
CD4044B



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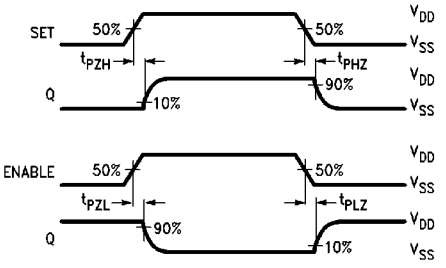
Enable Timing



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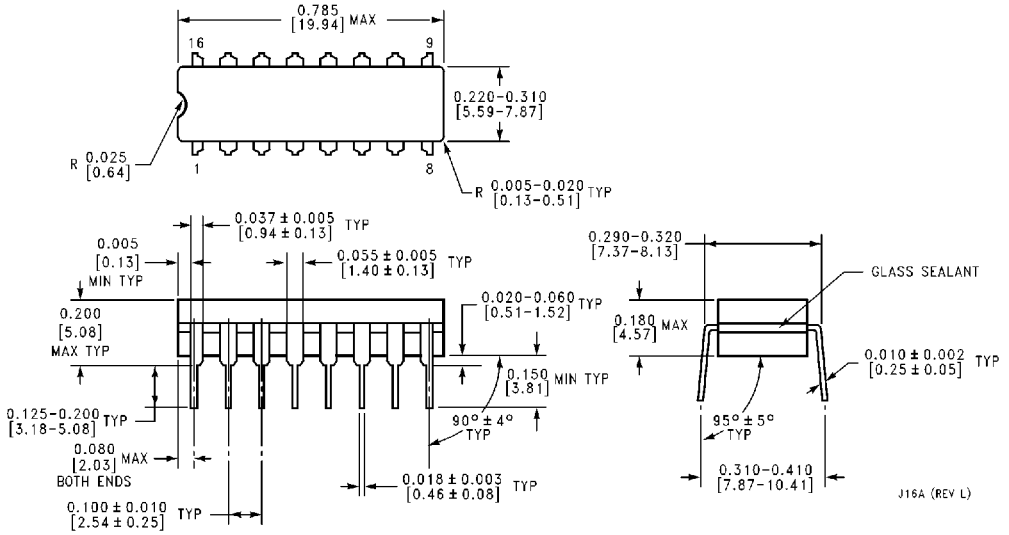
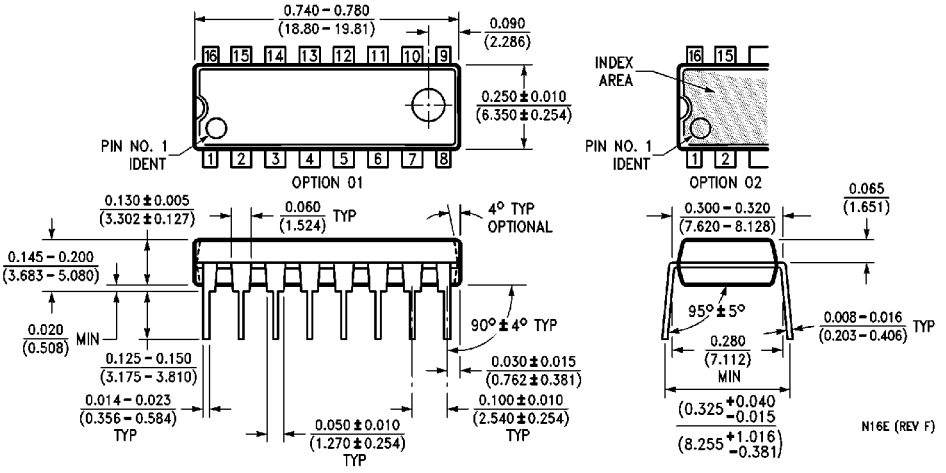
Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number CD4043BMJ, CD4043BCJ, CD4044BMJ or CD4044BCJ
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number CD4043BMN, CD4043BCN, CD4044BMN or CD4044BCN
NS Package Number N16E

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