# GMM2649228CNTG

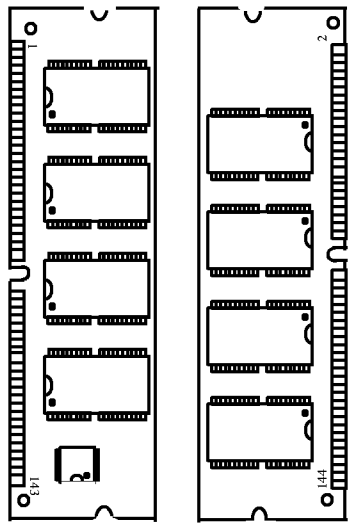
8,388,608 WORDS x 64 BIT
SYNCHRONOUS DYNAMIC RAM SO-DIMM

## Description

The GMM2649228CNTG is a 8M x 64 bits Synchronous Dynamic RAM SO-DIMM which is assembled 8pieces of 4M x 16bits Synchronous DRAMs in 54 pin TSOP II package and one 2048 bit EEPROM in 8 pin TSSOP package mounted on a 144 pin printed circuit board with decoupling capacitors. The GMM2649228CNTG is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

The GMM2649228CNTG provides common data inputs and outputs.

**GMM2649228CNTG** (Both Side)




## Features

* PC100,PC66 Compatible
  7K(2-2-2),7J(3-2-2),10K(PC66)
* 3.3V +/- 0.3V Power supply
* Maximum Clock frequency
  100 / 125 MHz
* LVTTL Interface
* Burst read/write operation and burst read/ single write operation capability
* Programmable burst length ;
  1, 2, 4, 8, Full page
* Programmable burst sequence
  Sequential / Interleave
* Full Page burst length capability
  Sequential burst
  Burst stop capability
* Programmable $\overline{CAS}$ Latency ; 2, 3
* CKE power down mode
* Input / Output data masking
* 4096 Refresh Cycles / 64ms
* Auto refresh / Self refresh Capability
* Serial Presence Detect with EEPROM

## Pin Name

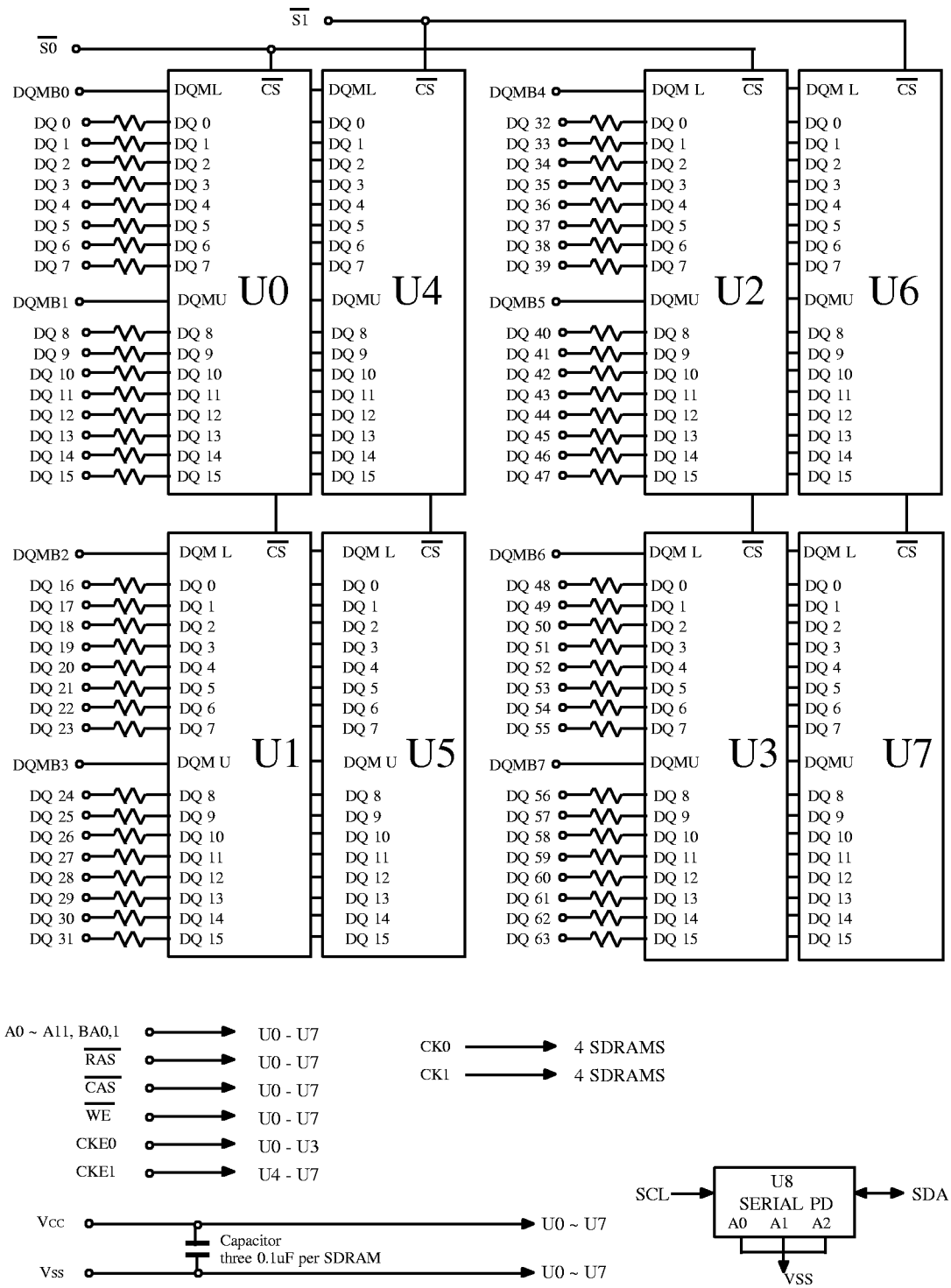
| | |
|---|---|
| CK0,1 | Clock inputs |
| CKE0,1 | Clock Enable |
| $\overline{S0,1}$ | Chip Select |
| $\overline{RAS}$ | Row Address Strobe |
| $\overline{CAS}$ | Column Address Strobe |
| $\overline{WE}$ | Write Enable |
| A0~A11 | Address input |
| BA0,1 | Bank Address input |
| DQ0~63 | Data input / output |
| DQMB0~7 | Data input / output Mask |
| Vcc | Power for internal circuit |
| Vss | Ground for internal circuit |
| NC | No Connect |
| SDA | Serial Data input / output |
| SCL | Serial Clock |
| DU | Don't Use |

## Pin Configuration

| Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | Vss | 25 | DQMB1 | 49 | DQ13 | 73 | DU | 97 | DQ22 | 121 | DQ24 |
| 2 | Vss | 26 | DQMB5 | 50 | DQ45 | 74 | CK1 | 98 | DQ54 | 122 | DQ56 |
| 3 | DQ0 | 27 | Vcc | 51 | DQ14 | 75 | Vss | 99 | DQ23 | 123 | DQ25 |
| 4 | DQ32 | 28 | Vcc | 52 | DQ46 | 76 | Vss | 100 | DQ55 | 124 | DQ57 |
| 5 | DQ1 | 29 | A0 | 53 | DQ15 | 77 | NC | 101 | Vcc | 125 | DQ26 |
| 6 | DQ33 | 30 | A3 | 54 | DQ47 | 78 | NC | 102 | Vcc | 126 | DQ58 |
| 7 | DQ2 | 31 | A1 | 55 | Vss | 79 | NC | 103 | A6 | 127 | DQ27 |
| 8 | DQ34 | 32 | A4 | 56 | Vss | 80 | NC | 104 | A7 | 128 | DQ59 |
| 9 | DQ3 | 33 | A2 | 57 | NC | 81 | Vcc | 105 | A8 | 129 | Vcc |
| 10 | DQ35 | 34 | A5 | 58 | NC | 82 | Vcc | 106 | BA0 | 130 | Vcc |
| 11 | VDD | 35 | Vss | 59 | NC | 83 | DQ16 | 107 | Vss | 131 | DQ28 |
| 12 | VDD | 36 | Vss | 60 | NC | 84 | DQ48 | 108 | Vss | 132 | DQ60 |
| 13 | DQ4 | 37 | DQ8 | 61 | CK0 | 85 | DQ17 | 109 | A9 | 133 | DQ29 |
| 14 | DQ36 | 38 | DQ40 | 62 | CKE0 | 86 | DQ49 | 110 | BA1 | 134 | DQ61 |
| 15 | DQ5 | 39 | DQ9 | 63 | Vcc | 87 | DQ18 | 111 | A10/AP | 135 | DQ30 |
| 16 | DQ37 | 40 | DQ41 | 64 | Vcc | 88 | DQ50 | 112 | A11 | 136 | DQ62 |
| 17 | DQ6 | 41 | DQ10 | 65 | $\overline{RAS}$ | 89 | DQ19 | 113 | Vcc | 137 | DQ31 |
| 18 | DQ38 | 42 | DQ42 | 66 | $\overline{CAS}$ | 90 | DQ51 | 114 | Vcc | 138 | DQ63 |
| 19 | DQ7 | 43 | DQ11 | 67 | $\overline{WE}$ | 91 | Vss | 115 | DQMB2 | 139 | Vss |
| 20 | DQ39 | 44 | DQ43 | 68 | CKE1 | 92 | Vss | 116 | DQMB6 | 140 | Vss |
| 21 | Vss | 45 | Vcc | 69 | $\overline{S0}$ | 93 | DQ20 | 117 | DQMB3 | 141 | SDA |
| 22 | Vss | 46 | Vcc | 70 | A12* | 94 | DQ52 | 118 | DQMB7 | 142 | SCL |
| 23 | DQMB0 | 47 | DQ12 | 71 | $\overline{S1}$ | 95 | DQ21 | 119 | Vss | 143 | Vcc |
| 24 | DQMB4 | 48 | DQ44 | 72 | A13* | 96 | DQ53 | 120 | Vss | 144 | Vcc |

* These pins are not used in this module

## Block Diagram



## Pin Description

| Pin Name | DESCRIPTION |
|---|---|
| CK0,1 (input pins) | CK is the master clock input to this pin. The other input signals are referred at CK rising edge. |
| CKE0,1 (input pins) | This pin determines whether or not the next CK is valid. If CKE is High, the next CK rising edge is valid. If CKE is Low, the next CK rising edge is invalid. This pin is used for power-down and clock suspend modes. |
| $\overline{S}$0,1 (input pins) | When $\overline{S}$ is Low, the command input cycle becomes valid. When $\overline{S}$ is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held. |
| $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (input pins) | Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section. |
| A0 ~ A11 (input pins) | Row address (AX0 to AX11) is determined by A0 to A11 level at the bank active command cycle CK rising edge. Column address is determined by A0 to A7 level at the read or write command cycle CK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, both banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by BA0 is precharged. |
| BA0,1 (input pin) | BA0,1 are bank select signal. If BA0 is Low and BA1 is High, bank 0 is selected. If BA0 is High and BA1 is Low, bank 1 is selected. If BA0 is Low and BA1 is High, bank 2 is selected. If BA0 is High and BA1 is High, bank 3 is selected. |
| DQ0 ~ DQ63 (I/O pins) | Data is input and output from these pins. These pins are the same as those of a conventional DRAMs. |
| DQMB0 ~ DQMB7 (input pins) | DQMB controls input/output buffers.<br>• Read operation: If DQMB is High, The output buffer becomes High-Z. If the DQMB is Low, the output buffer becomes Low-Z.<br>• Write operation: If DQMB is High, the previous data is held (the new data is not written). If DQMB is Low, the data is written. |
| $V_{CC}$ (power supply pins) | 3.3 V is applied. ($V_{CC}$ is for the internal circuit) |
| $V_{SS}$ (power supply pins) | Ground is connected. ($V_{SS}$ is for the internal circuit) |
| NC | No Connection pins. |

## Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit | Note |
|---|---|---|---|---|
| Voltage on any pin relative to Vss | $V_T$ | -0.5 to Vcc+0.5 (<= 4.6 (max)) | V | 1 |
| Supply voltage relative to Vss | $V_{CC}$ | -0.5 to +4.6 | V | 1 |
| Short circuit output current | $I_{OUT}$ | 50 | mA | |
| Power dissipation | $P_T$ | 8.0 | W | |
| Operating temperature | Topr | 0 to +70 | C | |
| Storage temperature | Tstg | -55 to +125 | C | |

Notes : 1. Respect to Vss

## Recommended DC Operating Conditions (Ta = 0 to + 70C)

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$, $V_{CCQ}$ | 3.0 | 3.6 | V | 1 |
| | $V_{SS}$, $V_{SSQ}$ | 0 | 0 | V | |
| Input high voltage | $V_{IH}$ | 2.0 | Vcc + 0.3 | V | 1, 2 |
| Input low voltage | $V_{IL}$ | -0.3 | 0.8 | V | 1, 3 |

Notes : 1. All voltage referred to Vss.

2. $V_{IH}$ (max) = 5.6V for pulse width <= 3ns

3. $V_{IL}$ (min) = -2.0V for pulse width <= 3ns

**DC Characteristics** (Ta = 0 to 70C, $V_{CC}$, $V_{CCQ}$ = 3.3 V +/- 0.3 V, $V_{SS}$, $V_{SSQ}$= 0 V)

| Parameter | | Symbol | -8 | -7K | -7J | -10K | Unit | Test conditions | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | | Max | Max | Max | Max | | | |
| Operating current | | $I_{CC1}$ | 560 | 560 | 560 | 520 | mA | Burst length= 1<br>$t_{RC}$ = min | 1, 2, 3 |
| Standby current in power down | | $I_{CC2P}$ | 12 | 12 | 12 | 12 | mA | CKE = $V_{IL}$,<br>$t_{CK}$ = 12 ns | 5 |
| Standby current in power down (input signal stable) | | $I_{CC2PS}$ | 3.2 | 3.2 | 3.2 | 3.2 | mA | CKE=$V_{IL}$,<br>$t_{CK}$= infinity | 6 |
| Standby current in non power down ($\overline{CAS}$ latency=2) | | $I_{CC2N}$ | 80 | 80 | 80 | 80 | mA | CKE,CS = $V_{IL}$,<br>$t_{CK}$ = 12ns | 4 |
| Standby current in non power down (input signal stable) | | $I_{CC2NS}$ | 32 | 32 | 32 | 32 | mA | CKE,CS = $V_{IL}$,<br>$t_{CK}$ = infinity | 8 |
| Active standby current in power down | | $I_{CC3P}$ | 40 | 40 | 40 | 40 | mA | CKE = $V_{IL}$,<br>$t_{CK}$ = 12 ns,<br>DQ = High-Z | 1,2,5 |
| Active standby current in power down (input signal stable) | | $I_{CC3PS}$ | 32 | 32 | 32 | 32 | mA | CKE = $V_{IL}$,<br>$t_{CK}$ = infinity | 2,6 |
| Active standby current in non power down | | $I_{CC3N}$ | 200 | 200 | 200 | 200 | mA | CKE,CS = $V_{IH}$,<br>$t_{CK}$ = 12 ns,<br>DQ = High-Z | 1,2,4 |
| Active standby current in non power down (input signal stable) | | $I_{CC3NS}$ | 100 | 100 | 100 | 100 | mA | CKE,CS = $V_{IH}$,<br>$t_{CK}$ = infinity | 2,8 |
| Burst operating current | ( CL= 2 ) | $I_{CC4}$ | 800 | 900 | 600 | 600 | mA | $t_{CK}$ = min<br>BL = 4 | 1,2,3 |
| | ( CL= 3 ) | $I_{CC4}$ | 1100 | 900 | 900 | 900 | mA | | |
| Refresh current | | $I_{CC5}$ | 850 | 850 | 850 | 750 | mA | $t_{RC}$ = min | 3 |
| Self refresh current | | $I_{CC6}$ | 3.2 | 3.2 | 3.2 | 3.2 | mA | $V_{IH}$ >= $V_{CC}$ - 0.2<br>$V_{IL}$ <=0.2V | 7 |

## DC Characteristics (Ta = 0 to 70C, $V_{CC}$, $V_{CCQ}$ = 3.3 V +/- 0.3 V, $V_{SS}$, $V_{SSQ}$= 0 V)

| Parameter | Symbol | - 8 , - 7K, - 7J, - 10K | | Unit | Test conditions | Notes |
|---|---|---|---|---|---|---|
| | | Min | Max | | | |
| Input leakage current | $I_{LI}$ | -1 | 1 | uA | 0<,= Vin <,= VCC | |
| Output leakage current | $I_{LO}$ | -1.5 | 1.5 | uA | 0 <,= Vout <,=VCC DQ = disable | |
| Output high voltage | $V_{OH}$ | 2.4 | - | V | $I_{OH}$ = -2 mA | |
| Output low voltage | $V_{OL}$ | - | 0.4 | V | $I_{OL}$ =2 mA | |

Notes : 1. $I_{CC}$ depends on output load condition when the device is selected. $I_{CC}$ (max) is specified at the output open condition.
2. One bank operation.
3. Addresses are changed once per one cycle.
4. Addresses are changed once per two cycles.
5. After power down mode, CLK operating current.
6. After power down mode, no CLK operating current.
7. After self refresh mode set, self refresh current.
8. Input signals are $V_{IH}$ or $V_{IL}$ fixed.

## Capacitance (Ta = 25C, $V_{CC}$, $V_{CCQ}$ = 3.3V +/- 0.3V)

| Symbol | Parameter | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| $C_{I1}$ | Input capacitance (A0 ~ A11, BA0,1) | - | 55 | pF | 1, 3 |
| $C_{I2}$ | Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$) | - | 48 | pF | 1, 3 |
| $C_{I3}$ | Input capacitance (CK0, CK1) | - | 35 | pF | 1, 3 |
| $C_{I4}$ | Input capacitance ($\overline{S0,S1}$, CKE0,1) | - | 55 | pF | 1, 3 |
| $C_{I5}$ | Input capacitance (DQMB0 ~ DQMB7) | - | 12 | pF | 1, 3 |
| $C_{I/O}$ | Input / output capacitance (DQ0 ~ DQ63) | - | 14 | pF | 1, 2, 3 |

Note : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. DQMB = $V_{IH}$ to disable Dout.
3. This parameter is sampled and not 100% tested.

**AC Characteristics** (Ta = 0 to 70C, $V_{CC}$, $V_{CCQ}$ = 3.3 V +/- 0.3 V, $V_{SS}$, $V_{SSQ}$ = 0 V)

| Parameter | | Symbol | -8 | | -7K | | -7J | | -10K | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| System clock cycle time | (CL=2) | $t_{CK}$ | 12 | - | 10 | - | 15 | - | 15 | - | ns | 1 |
| | (CL=3) | $t_{CK}$ | 8 | - | 10 | - | 10 | - | 10 | - | | |
| CLK high pulse width | | $t_{CKH}$ | 3 | - | 3 | - | 3 | - | 3 | - | ns | 1 |
| CLK low pulse width | | $t_{CKL}$ | 3 | - | 3 | - | 3 | - | 3 | - | ns | 1 |
| Access time from CLK | (CL=2) | $t_{AC}$ | - | 8 | - | 6 | - | 8 | - | 9 | ns | 1, 2 |
| | (CL=3) | $t_{AC}$ | - | 6 | - | 6 | - | 6 | - | 8 | | |
| Data-out hold time | | $t_{OH}$ | 3 | - | 3 | - | 3 | - | 3 | - | ns | 1, 2 |
| CLK to Data-out low impedence | | $t_{LZ}$ | 2 | - | 2 | - | 2 | - | 2 | - | ns | 1, 2, 3 |
| CLK to Data-out high impedence ( CL = 2,3 ) | | $t_{HZ}$ | - | 6 | - | 6 | - | 6 | - | 7 | ns | 1, 4 |
| Data-in setup time | | $t_{DS}$ | 2 | - | 2 | - | 2 | - | 2 | - | ns | 1 |
| Data-in hold time | | $t_{DH}$ | 1 | - | 1 | - | 1 | - | 1 | - | ns | 1 |
| Address setup time | | $t_{AS}$ | 2 | - | 2 | - | 2 | - | 2 | - | ns | 1 |
| Address hold time | | $t_{AH}$ | 1 | - | 1 | - | 1 | - | 1 | - | ns | 1 |
| CKE setup time | | $t_{CES}$ | 2 | - | 2 | - | 2 | - | 2 | - | ns | 1, 5 |
| CKE setup time for power down exit | | $t_{CESP}$ | 2 | - | 2 | - | 2 | - | 2 | - | ns | 1 |
| CKE hold time | | $t_{CEH}$ | 1 | - | 1 | - | 1 | - | 1 | - | ns | 1 |
| Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) setup time | | $t_{CS}$ | 2 | - | 2 | - | 2 | - | 2 | - | ns | 1 |
| Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) hold time | | $t_{CH}$ | 1 | - | 1 | - | 1 | - | 1 | - | ns | 1 |
| Ref/Active to Ref/Active command period | | $t_{RC}$ | 72 | - | 70 | - | 70 | - | 90 | - | ns | 1 |
| Active to Precharge command period | | $t_{RAS}$ | 48 | 120000 | 50 | 120000 | 50 | 120000 | 60 | 120000 | ns | 1 |
| Active command to column command (same bank) | | $t_{RCD}$ | 24 | - | 20 | - | 20 | - | 30 | - | ns | 1 |
| Precharge to active command period | | $t_{RP}$ | 24 | - | 20 | - | 20 | - | 30 | - | ns | 1 |

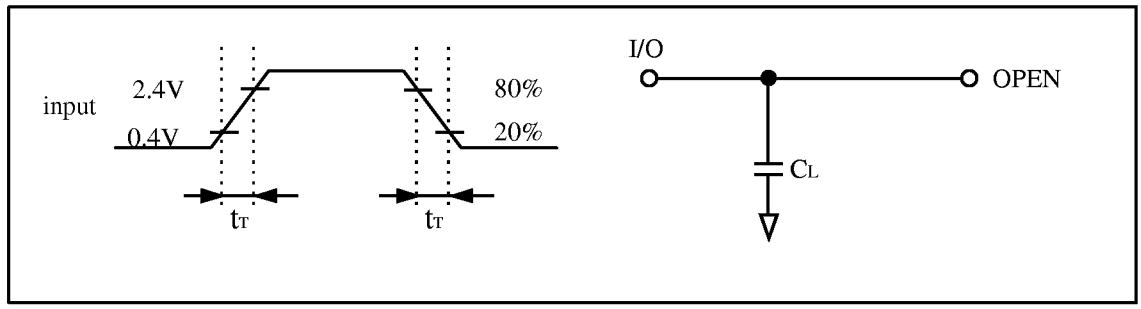
**AC Characteristics** (Ta = 0 to 70C, $V_{CC}$, $V_{CCQ}$ = 3.3 V +/- 0.3 V, $V_{SS}$, $V_{SSQ}$ = 0 V) (Continued)

| Parameter | Symbol | - 8 | | - 7K | | - 7J | | - 10K | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| Write recovery or data-in to precharge lead time | $t_{RWL}$ | 8 | - | 10 | - | 10 | - | 15 | - | ns | 1 |
| Active (a) to Active (b) command period | $t_{RRD}$ | 16 | - | 20 | - | 20 | - | 20 | - | ns | 1 |
| Refresh period | $t_{REF}$ | - | 64 | - | 64 | - | 64 | - | 64 | ms | |

Notes : 1. AC measurement assumes $t_T$ = 1ns. Reference level for timing of input signals is 1.40V. If $t_T$ is longer than 1ns,transition time compensation should be considered.
2. Access time is measured at 1.40V. Load condition is $C_L$ = 50pF without termination.
3. $t_{LZ}$ (min)defines the time at which the outputs achieves the low impedence state.
4. $t_{HZ}$ (max)defines the time at which the outputs achieves the high impedence state.
5. $t_{CES}$ define CKE setup time to CKE rising edge except power down exit command.

## Test Condition

* Input and output-timing reference levels: 1.4V
* Input waveform and output load: See following figures



## Relationship Between Frequency and Minimum Latency

| Parameter | | Symbol | -8 | | -7K | -7J | | -10K | | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| Frequncy(MHz) | | | 125 | 83 | 100 | 100 | 66 | 100 | 66 | |
| $t_{CK}$ (ns) | | | 8 | 12 | 10 | 10 | 15 | 10 | 15 | |
| Active command to column command (same bank) | | $l_{RCD}$ | 3 | 2 | 2 | 2 | 2 | 3 | 2 | 1 |
| Active command to active command period (same bank) | | $l_{RC}$ | 9 | 6 | 7 | 7 | 6 | 9 | 6 | = [$l_{RAS}$ +$l_{RP}$], 1 |
| Active command to precharge command (same bank) | | $l_{RAS}$ | 6 | 4 | 5 | 5 | 4 | 6 | 4 | 1 |
| Precharge command to active command (same bank) | | $l_{RP}$ | 3 | 2 | 2 | 2 | 2 | 3 | 2 | 1 |
| Write recovery or data-in to precharge command (same bank) | | $l_{RWL}$ | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Active command to active command (different bank) | | $l_{RRD}$ | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 1 |
| Self refresh exit time | | $l_{SREX}$ | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |
| Last data in to active command (Auto precharge, same bank) | | $l_{APW}$ | 4 | 3 | 3 | 3 | 3 | 4 | 3 | = [$l_{RWL}$ +$l_{RP}$], 1 |
| Self refresh exit to command input | | $l_{SEC}$ | 9 | 6 | 7 | 7 | 6 | 9 | 6 | = [$l_{RC}$] |
| Precharge command to high impedence | (CL=2) | $l_{HZP}$ | - | 2 | 2 | - | 2 | - | 2 | |
| | (CL=3) | $l_{HZP}$ | 3 | 3 | 3 | 3 | 3 | 3 | 3 | |
| Last data out to active command (auto precharge) (same bank) | | $l_{APR}$ | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |
| Last data out to precharge (early precharge) | (CL=2) | $l_{EP}$ | - | - 1 | -1 | - | - 1 | - | - 1 | |
| | (CL=3) | $l_{EP}$ | -2 | - 2 | -2 | -2 | - 2 | -2 | - 2 | |
| Column command to column command | | $l_{CCD}$ | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |
| Write command to data in latency | | $l_{WCD}$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| DQM to data in | | $l_{DID}$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| DQM to data out | | $l_{DOD}$ | 2 | 2 | 2 | 2 | 2 | 2 | 2 | |
| CKE to CLK disable | | $l_{CLE}$ | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |
| Register set to active command | | $l_{RSA}$ | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |
| $\overline{CS}$ to command disable | | $l_{CDD}$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| Power down exit to command input | | $l_{PEC}$ | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |

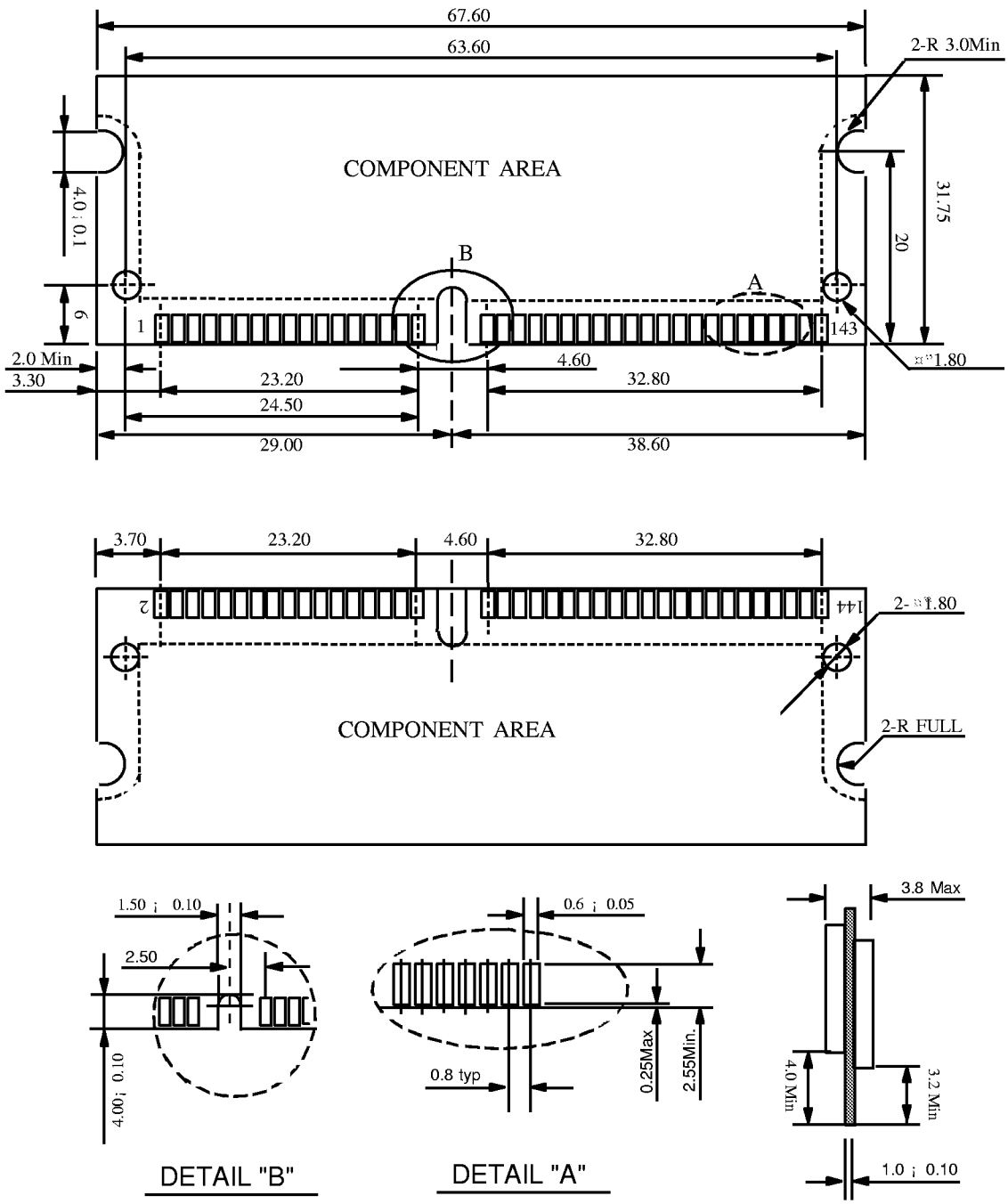
## Relationship Between Frequency and Minimum Latency

| Parameter | | Symbol | -8 | | -7K | -7J | | -10K | | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| Frequncy(MHz) | | | 125 | 83 | 100 | 100 | 66 | 100 | 66 | |
| $t_{CK}$ (ns) | | | 8 | 12 | 10 | 10 | 15 | 10 | 15 | |
| Burst stop to output valid data hold | (CL=2) | $l_{BSR}$ | - | 1 | 1 | - | 1 | - | 1 | |
| | (CL=3) | $l_{BSR}$ | 2 | 2 | 2 | 2 | 2 | 2 | 2 | |
| Burst stop to output high impedence | (CL=2) | $l_{BSH}$ | - | 2 | 2 | - | 2 | - | 2 | |
| | (CL=3) | $l_{BSH}$ | 3 | 3 | 3 | 3 | 3 | 3 | 3 | |
| Burst stop to write data ignore | | $l_{BSW}$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

Notes : 1. $l_{RCD}$ to $l_{RRD}$ are recommended value.

## Package Dimension

Unit: mm




NOTE : 1. Tolerances on all dimensions ¡ 0.15 unless otherwise specified.
2. Thickness(* Mark) includes Plating and / or Metallization.