P54/74FCT3821C/D–P54/74FCT3823C/D
P54/74FCT3825C/D
3.3 VOLT BUS INTERFACE REGISTERS

FEATURES

- Function and Drive Compatible with the Fastest TTL Logic

- Inputs and Outputs Interface with TTL Logic Levels

- 3.3V ± 0.2V Power Supply and CMOS for Lowest Power Dissipation

- FCT3-D speed at 5.1ns max. (Com'l)
  FCT3-C speed at 6.0ns max. (Com'l)

- Edge-rate Control Circuitry for Significantly Improved Noise Characteristics

- ESD protection exceeds 2000V

- 48 mA Sink Current (Com'l), 32 mA (Mil) 15mA Source Current (Com'l), 12 mA (Mil)

- Multiple Center Power and Ground Pins

- Clamp Diodes on all Inputs for Ringing Supressions

- High Speed PArallel Registers with Positive Edge-triggered D-type Flip-Flops

- Buffered Common Clock Enable ($\overline{EN}$) and Asynchronous Clear Input ($\overline{CLR}$)

- Manufactured in 0.4 micron PACE Technology™

DESCRIPTION

The 'FCT3820 series bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/ data paths or buses carrying parity. The 'FCT3821 is a buffered, 10 bit wide version of the popular 'FCT374 function. The 'FCT3823 is a 9-bit wide buffered register with Clock Enable ($\overline{EN}$) and Clear ($\overline{CLR}$) — ideal for parity bus interfacing in high-performance microprogrammed systems. The 'FCT3825 is a 8-bit buffered register with all the 'FCT3823 controls plus multiple enables ($\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA and RD/$\overline{WR}$. They are ideal for use as an output port requiring high I_{OL}/I_{OH}.

The 'FCT3800 family of devices are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in the high impedance state.

The 'FCT3820 interface family is manufactured using PACE Technology™ which is Performance Advanced CMOS Engineered to use 0.4 micron effective channel lengths giving 250 picoseconds loaded* internal gate delays. The nominal supply voltage is reduced from the conventional 5.0V to 3.3V, thus reducing the output swings dramatically. This, together with the (lower inductance) center power and ground pins, significantly reduces noise and ground bounce that would otherwise occur for very high speed circuitry.

FUNCTIONAL BLOCK DIAGRAM

1804 01
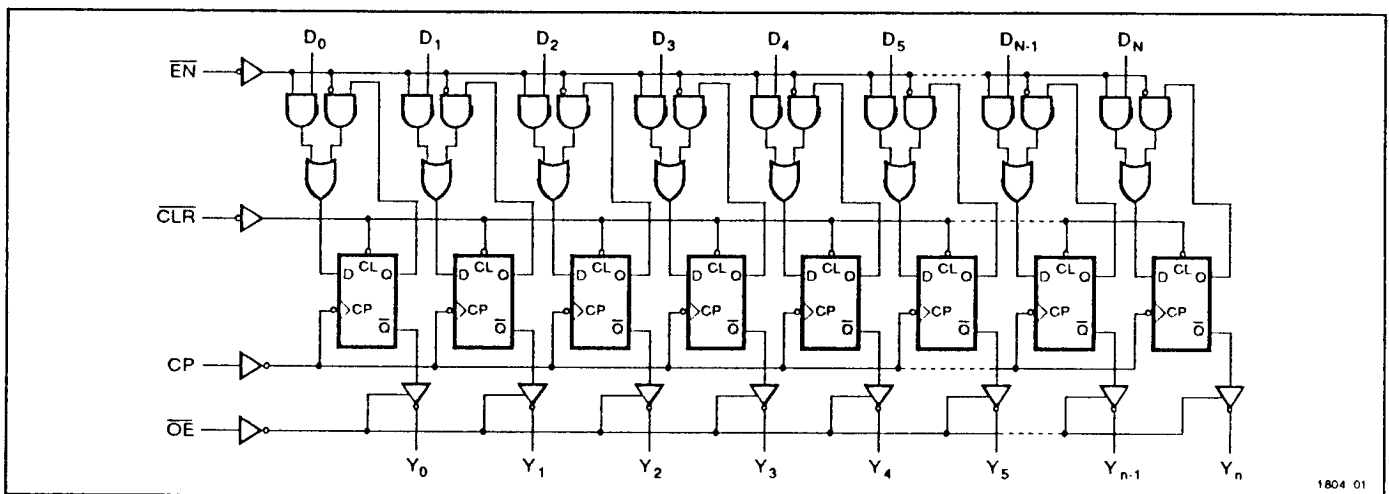
PERFORMANCE
SEMICONDUCTOR CORPORATION

Means Quality, Service and Speed

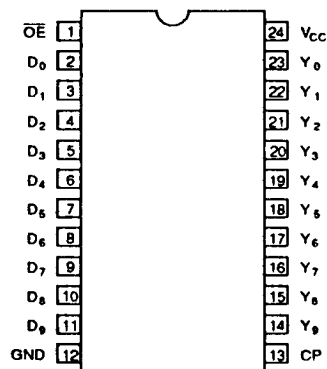©1992 Performance Semiconductor Corporation
4/1/92 - 4

1

PRODUCT SELECTOR GUIDE

Non-inverting	Device		
	10-Bit	9-Bit	8-Bit
	'FCT3821	'FCT3823	'FCT3825

1804 Tbl 01
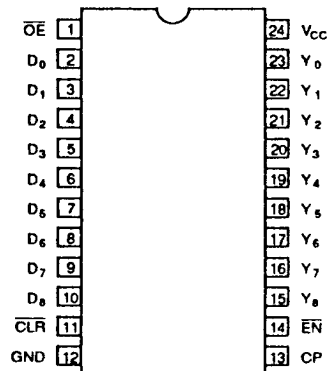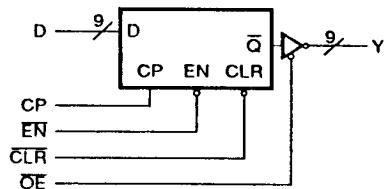
LOGIC SYMBOLS

PIN CONFIGURATONS

'FCT3821 (10-Bit Register)
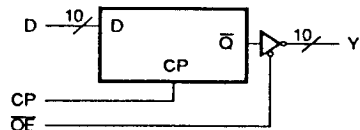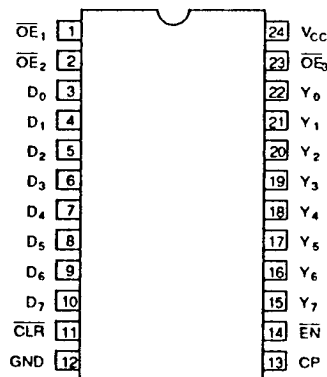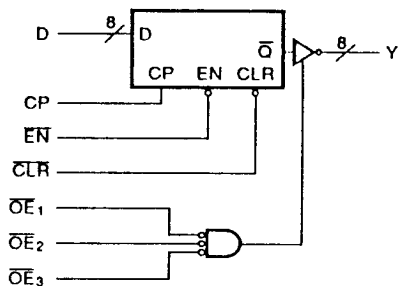
DIP (D4,P4) SOIC (S4)

1804 02

'FCT3823 (9-Bit Register)

DIP (D4,P4) SOIC (S4)

1804 03

'FCT3825 (8-Bit Register)

DIP (D4,P4) SOIC (S4)

1804 04

4/1/92 - 4

2

ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	−65 to +150	°C
T_A	Ambient Temperature Under Bias	−65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	−0.5 to +5.0	V
I_{IN}	Input Current	−30 to +5.0	mA

Notes: 1804 Tbl 02
1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	−0.5 to V_{CC} + 0.5	V
V_{OUT}	Voltage Applied to Output	−0.5 to V_{CC} + 0.5	V

1804 Tbl 03
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	−55°C	+125°C
Commercial	0°C	+70°C

1804 Tbl 04

Supply Voltage (V_{CC})	Min	Max
Military	+3.1V	+3.5V
Commercial		

1804 Tbl 05

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0		V_{CC} + 0.5	V		
V_{IL}	Input LOW Voltage		−0.5		0.8	V		
V_H	Hysteresis			0.35		V		All inputs
V_{IK}	Input Clamp Diode Voltage			−0.7	−1.2	V	MIN	I_{IN} = −18mA
V_{OH}	Output HIGH Voltage	Military/Commercial (CMOS)	V_{CC} − 0.2	V_{CC}		V	MIN	I_{OH} = −300μA
		Military (TTL)	2.4			V	MIN	I_{OH} = −12mA
		Commercial (TTL)	2.4			V	MIN	I_{OH} = −15mA
V_{OL}	Output LOW Voltage	Military/Commercial (CMOS)		GND	0.2	V	MIN	I_{OL} = 300μA
		Military (TTL)		0.3	0.5	V	MIN	I_{OL} = 32mA
		Commercial (TTL)		0.3	0.5	V	MIN	I_{OL} = 48mA
I_{IH}	Input HIGH Current				5	μA	MAX	V_{IN} = V_{CC}
I_{IL}	Input LOW Current				−5	μA	MAX	V_{IN} = GND
I_{IH}	Input HIGH Current				5	μA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current				−5	μA	MAX	V_{IN} = 0.5V
I_{OS}	Output Short Circuit Current[2]		−60	−120	−225	mA	MAX	V_{OUT} = 0.0V
C_{IN}	Input Capacitance[3]			5	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance[3]			9	12	pF	MAX	All outputs

1804 Tbl 06

Notes:
1. Typical limits are at V_{CC} = 3.3V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{os} tests should be performed last.
3. This parameter is guaranteed but not tested.

4/1/92 · 4

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
I_{CC}	Quiescent Power Supply Current (CMOS inputs)	0.003	0.5	mA	V_{CC} = MAX, f_1 = 0, Outputs Open, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	0.5	2.0	mA	V_{CC} = MAX, $V_{IN} = V_{CC} - 0.6V$[2], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]	1.5	0.25	mA/mHz	V_{CC} = MAX, One Bit Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE} = \overline{EN}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
I_C	Total Power Supply Current[5]	1.7	4.0	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{OE} = \overline{EN}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.2	6.0	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{OE} = \overline{EN}$ = GND, $V_{IN} = V_{CC} - 0.6V$ or V_{IN} = GND
		4.0	7.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE} = \overline{EN}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		6.2	16.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE} = \overline{EN}$ = GND, $V_{IN} = V_{CC} - 0.6V$ or V_{IN} = GND

1804 Tbl 07

Notes:
1. Typical values are at V_{CC} = 3.3V, +25°C ambient and maximum loading.
2. Per TTL driven input ($V_{IN} = V_{CC} - 0.6V$); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels

ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = V_{CC} - 0.6V$)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_1 = Input Frequency
N_1 = Number of Inputs at f_1
All currents are in milliamps and all frequencies are in megahertz.

AC CHARACTERISTICS

Sym.	Parameter	Test Conditions	'FCT3821C–3825C				'FCT3821D–3825D				Units	Fig. No.
			MIL		COM'L		MIL		COM'L			
			Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Clock to Y_1 ($\overline{OE}$ = LOW)	$C_L = 50pF$ $R_L = 500\Omega$	–	7.0	–	6.0	–	6.0	–	5.1	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay Clock to Y_1 ($\overline{OE}$ = LOW)	$C_L = 300pF^2$ $R_L = 500\Omega$	–	13.5	–	12.5	–	12.5	–	11.0	ns	1, 5
t_{PLH}	Propagation Delay Clear to Y_1	$C_L = 50pF$ $R_L = 500\Omega$	–	8.5	–	8.0	–	8.0	–	6.8	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y_1	$C_L = 50pF$ $R_L = 500\Omega$		8.0		7.0		7.0		6.2	ns	1, 7, 8
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y_1	$C_L = 300pF^2$ $R_L = 500\Omega$		13.5		12.5		12.5		11.0	ns	1, 7, 8
t_{PHZ} t_{PHL}	Output Disable Time $\overline{OE}$ to Y_1	$C_L = 5pF^2$ $R_L = 500\Omega$		6.2		6.2		4.6		5.7	ns	1, 7, 8
t_{PHZ} t_{PHL}	Output Disable Time $\overline{OE}$ to Y_1	$C_L = 50pF$ $R_L = 500\Omega$		6.5		6.5		4.9		5.9	ns	1, 7, 8

1804 Tbl 08

AC OPERATING REQUIREMENTS

Sym.	Parameter	Test Conditions	'FCT3821C–3825C				'FCT3821D–3825D				Units	Fig. No.
			MIL		COM'L		MIL		COM'L			
			Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.		
t_{SU}	Data to CP Set-up Time		3.0	–	3.0	–	1.5	–	1.5	–	ns	4
t_h	Data CP Hold Time		1.5	–	1.5	–	1.0	–	1.0	–	ns	4
t_{su}	Enable $\overline{EN}$ to CP Set-up Time		3.0	–	3.0	–	1.5	–	1.5	–	ns	9
t_h	Enable $\overline{EN}$ to CP Hold Time	$C_L = 50pF$ $R_L = 500\Omega$	0.0	–	0.0	–	0.0	–	0.0	–	ns	9
t_{rec}	Clear Recovery $\overline{CLR}$ to CP		6.0	–	6.0	–	4.5	–	4.5	–	ns	6
$t_w(H)$ $t_w(L)$	Clock Pulse Width		6.0	–	6.0	–	6.0	–	5.5	–	ns	5
$t_w(L)$	$\overline{CLR}$ Pulse Width		6.0	–	6.0	–	6.0	–	5.5	–	ns	5

1804 Tbl 09

Notes:
1. Minimum limits are guaranteed but not tested on Propagation Delays.
2. These parameters are guaranteed but not tested.

4/1/92 - 4

PIN DESCRIPTION

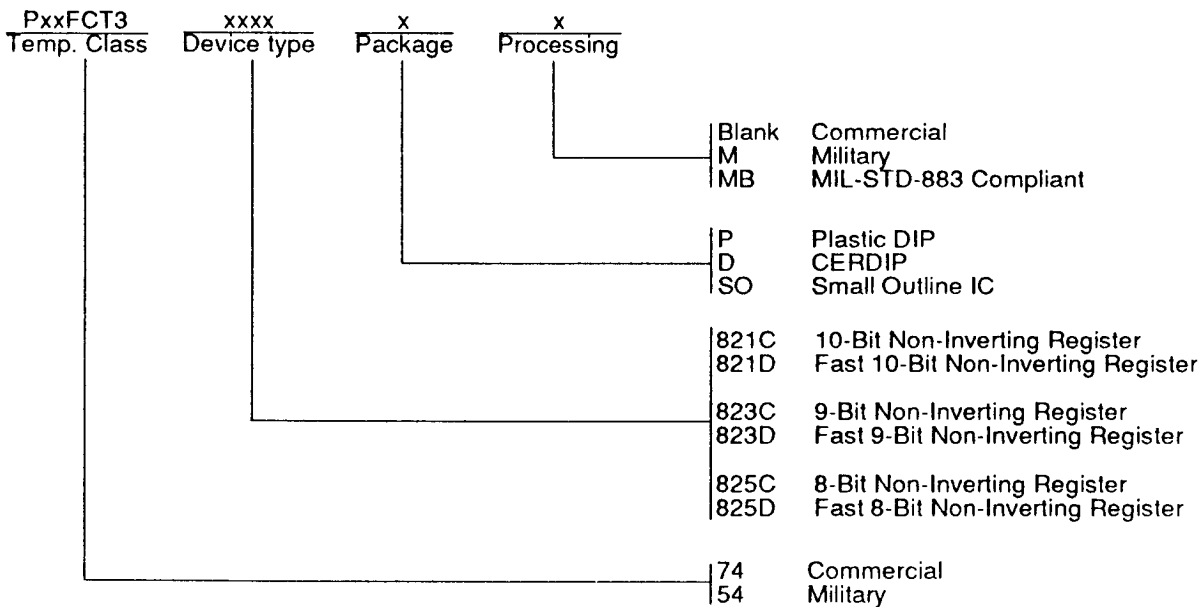| Name	I/O	Description
D_1	I	The D flip-flop data inputs.
$\overline{CLR}$	I	For both inverting and non-inverting registers, when the clear input is LOW and $\overline{OE}$ is LOW, the Q_1 outputs are LOW. When the clear input is HIGH, data can be entered into the register.
CP	O	Clock Pulse for the register; enters data into the register on the LOW-to-HIGH transition.
$Y_1, \overline{Y}_1$	O	The register three-state outputs.
$\overline{EN}$	I	Clock Enable. When the clock enable is LOW, data on the D_1 input is transferred to the Q_1 output on the LOW-to HIGH clock transition. When the clock enable is HIGH, the Q_1 outputs do not change state, regardless of the data or clock input transitions.
$\overline{OE}$	I	Output Control. When the $\overline{OE}$ input is HIGH, the Y_1 outputs are in the high impedence state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_1 outputs.

1804 Tbl 10

FUNCTION TABLES

Inputs					Internal Outputs		Function
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	D_1	CP	Q_1	Y_1	
H	H	L	L	⌐	L	Z	High Z
H	H	L	H	⌐	H	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	⌐	L	Z	Load
H	H	L	H	⌐	H	Z	
L	H	L	L	⌐	L	L	
L	H	L	H	⌐	H	H	

1804 Tbl 11

H = HIGH, L = LOW, X = Don't Care, NC = No Change,
⌐ = LOW-to-HIGH Transition, Z = HIGH Impedance

ORDERING INFORMATION

PxxFCT3 — Temp. Class
xxxx — Device type
x — Package
x — Processing

Blank	Commercial
M	Military
MB	MIL-STD-883 Compliant

P	Plastic DIP
D	CERDIP
SO	Small Outline IC

821C	10-Bit Non-Inverting Register
821D	Fast 10-Bit Non-Inverting Register
823C	9-Bit Non-Inverting Register
823D	Fast 9-Bit Non-Inverting Register
825C	8-Bit Non-Inverting Register
825D	Fast 8-Bit Non-Inverting Register

| 74 | Commercial |
| 54 | Military |

1804 05