# Introduction

## Description

The PMD Module implements the complete ATM 25Mbps Physical Media Dependent (PMD) sublayer. The module is designed to interface to the ATM 25Mbps Controller Module series of devices which have the embedded Transmission Convergence (TC) layer function. The chip is a mixed signal design fabricated in an IBM BiCMOS process and in a 64-pin TQFP module.

The Media Interface Module (MIM) provides the connection between the PMD Module and the media interface connector (typically RJ-45). The MIM includes the transformer isolation, the waveshape filtering, and a 4-wire choke for both the Transmit and Receive paths. This component is available from Pulse Engineering, Inc. as part number PE-67583.

## Key Features

- Provides the complete ATM-25 Mbps PMD sublayer function
- PLL Clock and data recovery, based on proven IBM Token Ring technology
- Line equalization on-chip
- 5-V to 3.3-V regulator on-chip
- Supports 32-MHz oscillator or 4-MHz crystal for master clock generation
- Packaged in a 64-pin TQFP
- Uses a single +5-V supply, and dissipates 480 mW
- With MIM, the PMD chip supports UTP 3, 4, 5, or STP cabling

## Module Part Numbers

The module P/N is as follows:

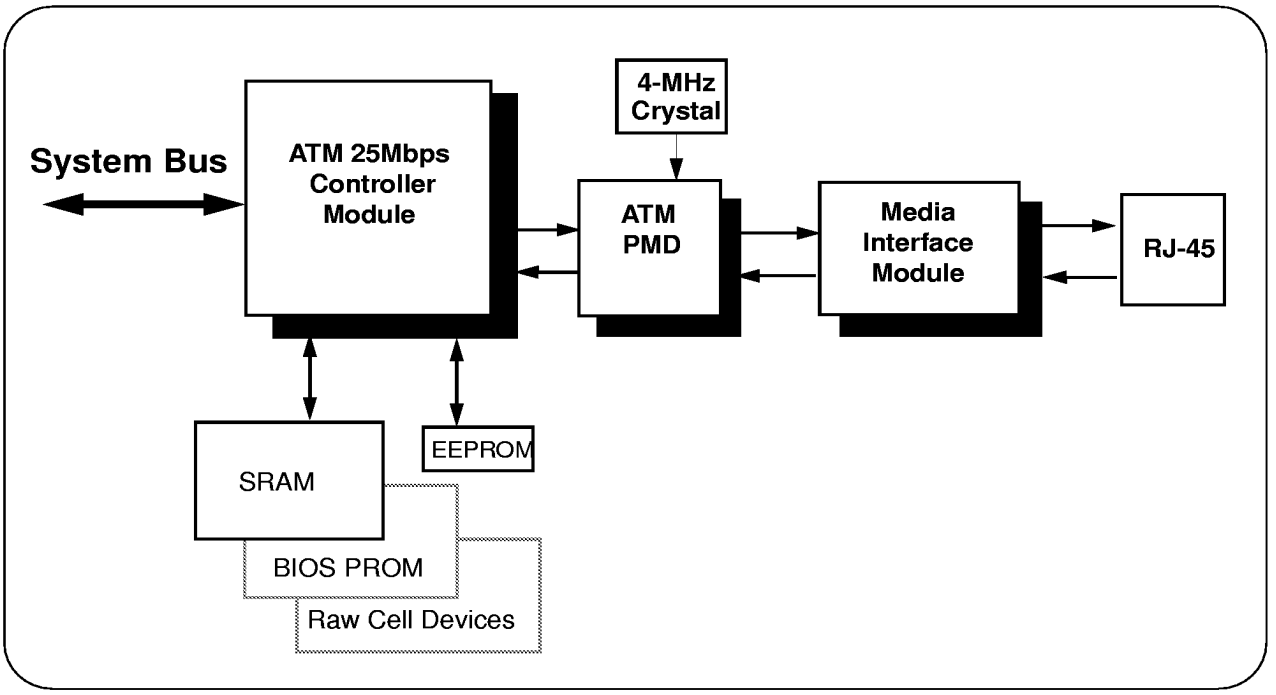
- 64-pin TQFP — P/N IBM30CMTA5PRLQAAAT

## Compliance

The PMD Module is compliant with the ATM Forum *Physical Interface Specification for 25.6Mb/s Over Twisted Pair Cable.*

## Typical ATM 25Mbps System Application

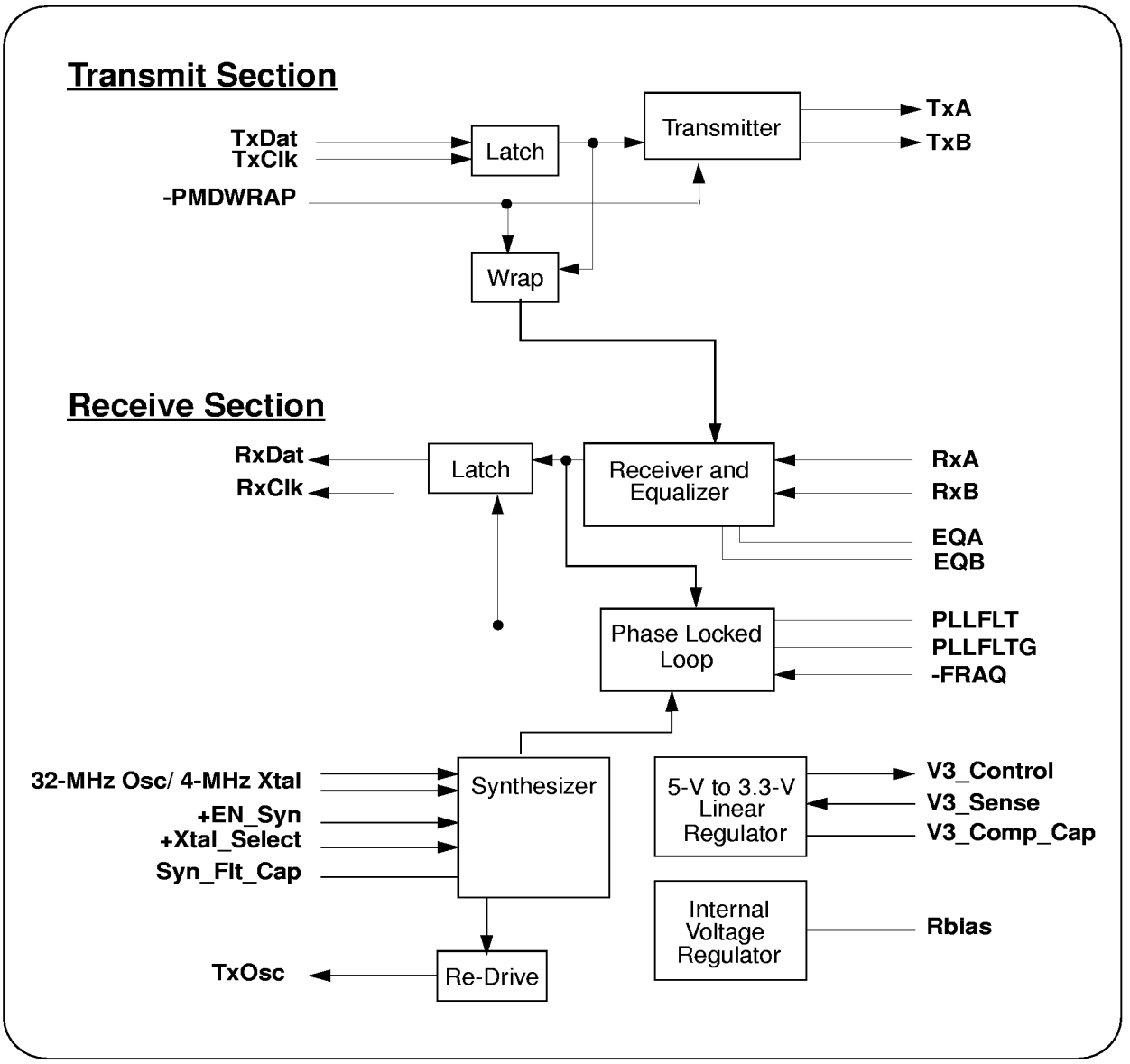
**Figure 1. Typical ATM 25Mbps Design**



## PMD Block Diagram

The PMD chip consists of nine main functional blocks, divided into the Transmit section, the Receive section and the miscellaneous section. The Block Diagram is shown below, and each functional block is subsequently described in detail.

**Figure 2. PMD Functional Block Diagram**



## Transmit Section

### *Transmitter*

The Transmit section of the chip takes the clock (TxCLK) and data (TxDAT) signals from the ATM Controller Chip, latches the data signal with the rising edge of the clock signal, and transmits the signal from the PMD chip through the MIM and onto the media. The transmitter is a switched current source through differential open drain circuit and requires external pull-up resistors. The power and levels of the transmitter are set by the combination of an on-chip voltage reference and an external bias resistor.

### *Wrap Function*

The Wrap function in the PMD chip allows the normally transmitted data to be wrapped back to the Receive section to support self-test. Using the WRAP function, the PMD and the ATM Controller Chip operation can be functionally tested by sending and receiving ATM cells to and from the Controller Chip.

During the Wrap test, the front-end Transmit and Receive pins of the PMD chip are degated, isolating the PMD chip from the network.

## Receiver Section

### *Receiver and Equalizer*

This section of the PMD chip takes the transformer-coupled signal from the MIM, receives it, equalizes it, pre-amplifies it, and converts it to digital levels.

The receiver also detects the signal amplitude and disables the receiver if the signal amplitude is too low.

### *Phase Locked Loop*

This section of the PMD chip derives the data clock from the input data stream. The Phase Locked Looped (PLL) has two modes of operation: Normal Phase Locked mode and Frequency Acquisition mode. The Frequency Acquisition mode sets the center frequency of the Voltage Controlled Oscillator (VCO) by locking the VCO to a 32-MHz signal from the local crystal oscillator. Under Normal mode, the PLL extracts the clock and data signals from the received data stream, re-times them with a latch, and transmits them to the ATM Controller Chip.

## Miscellaneous

### *Synthesizer Circuit*

The synthesizer circuit allows either a 32-MHz crystal oscillator or a 4-MHz crystal to be used as the master clock source. The 4-MHz crystal option has both cost and EMC benefits. When a 32-MHz oscillator is used, the synthesizer function is optional; however, the synthesizer can be used to improve the duty cycle of the 32-MHz clock (TxOsc).

### *5-V to 3.3-V Linear Regulator Circuit*

The 5-V to 3.3-V control circuit, when combined with external components, provides a regulated 3.3-V (+/-10%) supply voltage from the 5-V (+/- 10%) power supply. The maximum output current which can be supplied with this circuit is 300 mA.

# PMD Usage

This section covers all aspects of PMD usage, including configuration, and initialization for each of the various modes of operation. The module has three modes of operation: normal Transmit/Receive mode, PMD Front-End Wrap mode and Power-Down Stand-by mode. The three modes of operation are controlled by the ATM Controller Chip.

For all modes of operation, the PMD chip, the MIM, and all of the peripheral components must be wired according to the connection diagram shown in Figure 6 on page 15.

## Normal Transmit and Receive Mode

This is the normal mode of operation. Transmit clock and data are received from the ATM Controller Chip and transmitted onto the media. Data are received from the media, the clock is recovered from the data, and both the clock and data are provided to the ATM Controller Chip.

### Configuration

To configure for Normal Transmit and Receive mode, the input signal, +STANDBY, must be held high (for ATM ISA, this must be done with a resistor). The levels on input signals +XTAL_SELECT and +EN_SYN depend on the user selection. This is described further in "Oscillator/Crystal Configuration" on page 6.

All other control signals (such as -PMD_Wrap and -FRAQ) are controlled by the ATM Controller Chip.

### Initialization

The initialization of the PMD chip is completely handled by the ATM Controller Chip. During initialization, the PLL on the PMD chip is placed in Frequency Acquisition (FRAQ) mode and the PLL is locked to the local 32-MHz signal. After initialization, the ATM Controller Chip will place the PLL in Phase mode and the PLL will lock on to the incoming data stream.

**Note:** During normal operation, the ATM Controller Chip continually monitors the recovered clock; and if the recovered clock drifts from 32 MHz due to input signal loss (temporary or permanent), the ATM Controller Chip automatically puts the PLL into FRAQ mode for a period of 64 uS. After the 64 uS, the ATM Controller Chip can place the PLL back into Phase mode and attempt to recover the clock and data. The user is referred to the ATM Controller Chip documentation to determine how the Controller Chip can respond to these types of front-end error conditions.

## PMD Wrap Mode

The PMD Wrap mode is available as a diagnostic or Self-Test mode.The Transmit data from the ATM Controller Chip is wrapped back through the receiver and PLL circuits; and the recovered clock and data are sent back to the ATM Controller Chip.

### Configuration

To configure for Wrap mode, the input signal +STANDBY must be held high (this must be done with a resistor). The PMD Wrap mode is entirely controlled by the ATM Controller Chip. For more information, refer to the ATM Controller Chip documentation.

### Initialization

All initialization is handled by the ATM Controller Chip. Typically, the same initialization sequence is required in PMD Wrap mode as is required in the Normal mode.

## Power-Down Mode

Power-Down mode (or Stand-by mode) places the PMD module in a power-down stand-by state to reduce power consumption. In this mode "all" outputs are tri-stated (see below for further details). The power dissipation in Reset mode is significantly lower than Normal operation.

### Configuration

Power-Down mode does not affect the 3.3-V regulator circuit or the synthesizer/oscillator circuit and the TxOSc output. In Power-Down mode, the output signal +TxOsc will remain active in order to provide the 32-MHz clock signal to the ATM Controller Chip. The +32-MHz signal can be optionally tri-stated while the PMD Module is in Power-Down mode by

tying the input signal +EN_Syn low. This technique may be required to support in-circuit test, where all output driver circuits must be tri-stated.

The PMD Module is put into Power-Down mode by asserting the +STANDBY input. When using this module with the ATM Controller Chip, it is recommended that the +STANDBY input be tied to ground (through a resistor).

Because the PLL circuits are turned off during Power-Down mode, the PMD RxClk will not become active until 10 ms after the +STANDBY input signal is de-asserted. The time is required to allow the PLL filter capacitor time to charge up.

## Oscillator/Crystal Configuration

As its local reference clock, the PMD Module supports the use of either a 32-MHz oscillator or a 4-MHz crystal. The crystal option provides for a lower cost solution and reduces the board EMC.

To use the 4-MHz crystal option, inputs +XTAL_SEL and +EN_SYN must be asserted (**Important Note**: Both of these inputs have on-chip pull-down resistors which make the default selection the 32-MHz oscillator with the synthesizer disabled). The crystal circuit is placed across inputs X1 and X2. The exact circuit and crystal P/N must be used as shown in Figure 6 on page 15.

To use the 32-MHz Oscillator option, the input +XTAL_SEL must be de-asserted (held low). The signal, +XTAL_SEL, has an integrated pull-down resistor so floating this I/O is equivalent to selecting the 32-MHz Oscillator option. The 32-MHz oscillator output is connected to PMD input X1. The +EN_Syn input is optional for Oscillator mode and its purpose is to improve the signal characteristics (duty cycle) of the +32-MHz output from the PMD Module.

When +EN_SYN is asserted, the +32-MHz signal provides a re-timed 32-MHz clock which has multiple uses. A typical use is in a concentrator/hub application, where a single crystal/oscillator is used and each of the subsequent PMD modules connects the +32-MHz output and X1 input in daisy-chain fashion. The primary PMD module could use either an oscillator or a crystal as the timing source. Each of the subsequent modules uses the Oscillator mode; and **all** modules have +EN_SYN asserted.

The specifications for the re-timed 32-MHz clock are as follows:

- Worst case output duty cycle at the module I/O: 48–52%
- Worst case input duty cycle at the chip I/O: 30–70%
- Start-up time: 100 ms from module power up (1-uF external capacitor)
- Output rise/fall times: 4 ns
- Maximum jitter on the output clock edge: TBD
- Filtering of jitter from the input clock: 100 KHz (-70 dB at 32 MHz)

**Note:** In applications where the 32-MHz clock is daisy chained, the start-up time delay can be cumulative for the number of times it is repeated.

# I/O Specifications

## PMD Module Pin Descriptions

The following table lists the PMD I/O pins and their definitions, which are grouped by function. The pin number is provided for the 64-pin TQFP package.

**Table 1: PMD 64-Pin TQFP Module Pin Descriptions**

| Pin | Pin Name | Type | Description |
|---|---|---|---|
| | | | **CLOCK AND DATA INTERFACE PINS** |
| 47 | +RxClk | O, Z | **Received Clock:** The clock signal recovered from the data received from the network. |
| 53 | +RxDat | O, Z | **Received Data:** The re-timed NRZI data received from the network. |
| 3 | +TxClk | IPU | **Transmit Clock:** The input signal from the ATM Controller Chip that is used to sample the TxDat signal. |
| 4 | +TxDat | IPU | **Transmit Data:** The NRZI encoded data from the ATM Controller Chip to be transmitted to the network. |
| | | | **CONFIGURATION AND CONTROL PINS**<br>(See "PMD Usage" on page 5 for details.) |
| 13 | -FRAQ | IPU | **Frequency Acquisition:** Puts the PLL in Frequency Acquisition (FRAQ) mode. This mode sets the center frequency of the VCO by locking the VCO to the local crystal oscillator.<br>Lo = FRAQ mode<br>Hi = Normal operation |
| 50 | +STANDBY | I | **Standby:** Puts PMD in a Reduced Power Stand-by mode.<br>Lo = Normal operation<br>Hi = Power-Down Stand-by mode<br>This pin does not perform a POR function; and it does not have an on-chip pull-up or pull-down resistor. It must be externally biased. |
| 23 | -PMD_WRAP | IPU | **PMD Wrap Mode:** Puts the chip in Wrapback mode, which connects the Transmit signal to the on-chip receiver. During this mode, the Transmit outputs (TxA/B) and Receive inputs (RxA/B) are isolated from the media.<br>Lo = Wrap<br>Hi = Normal |
| | | | **OSCILLATOR/CRYSTAL INPUT AND REDRIVE PINS** |
| 12 | X1 | A, I | **Crystal or Oscillator Input**: First input of the 4-MHz Crystal Circuit Analog input or 32-MHz Oscillator TTL input. |
| 16 | X2 | A | **Crystal:** Second input of 4-MHz Crystal Analog input circuit. |
| 37 | SYN_FLT_CAP | A | **Synthesizer Filter Capacitor:** Connection for external capacitor component for synthesizer circuit. Component is only required when synthesizer is used (+EN_SYN asserted). |
| 64 | +XTAL_SEL | IPD | **Crystal Select:** Selects 32-MHz oscillator or 4-MHz crystal as the clock source.<br>Lo= Selects 32-MHz Oscillator Operation<br>Hi= Selects 4-MHz Crystal Operation |
| I/O Type Definitions:<br>O = TTL Output<br>Z = Tri-state<br>A = Analog | | | IPD = TTL Input with 15-kΩ Pull-Down Resistor<br>IPU = TTL Input with 15-kΩ Pull-Up Resistor<br>I = TTL Input |

## Table 1: PMD 64-Pin TQFP Module Pin Descriptions

| Pin | Pin Name | Type | Description |
|---|---|---|---|
| 38 | +EN_SYN | IPD | **Enable Synthesizer:** Enables Synthesizer operation. Required when 4-MHz crystal is used. It is optional when the 32-MHz oscillator is used. |
| 11 | +TxOsc | O, Z | **TxOSc:** A 32-MHz Clock signal derived from the 4-MHz Crystal or the 32-MHz Oscillator signal. |
| **FRONT END TRANSMITTER AND RECEIVER** | | | |
| 18, 19 | TxA, TxB | A | **Transmit Outputs:** These differential, high-current drive outputs drive the Media Interface Module |
| 30, 31 | RxA, RxB | A | **Receiver Inputs:** These are differential inputs from the isolation transformer. They feed a differential equalizer/amplifier to provide valid data to the PLL. These pins have a DC bias level of Vdd/2 and should not be loaded with a DC path to ground. Normal connection of these pins is to the Media Interface Module. |
| **TR FRONT END DISCRETE COMPONENT CONNECTION PINS** | | | |
| 25 | RBIAS | A | **Current Bias Resistor:** Used in conjunction with an internal bandgap reference voltage to generate an accurate current reference. |
| 35, 36 | EQA, EQB | A | **Equalizer:** Connection points for components for the on-chip equalizer. |
| 42 | PLLFLT | A | **PLL Filter:** This is where the component for the PLL filter are connected. *THIS PIN IS EXTREMELY SENSITIVE TO NOISE.* |
| 43 | PLLFLTG | A | **PLL Filter Current Return:** This is dedicated current return for the PLL. *THIS PIN IS EXTREMELY SENSITIVE TO NOISE AND SHOULD NOT BE CONNECTED TO GROUND.* |
| **5-V TO 3.3-V CONVERSION PINS** | | | |
| 49 | V3_SENSE | A | **3.3-V Sense Signal:** Sense input from 3.3-V supply to the PMD regulator circuit. |
| 48 | V3_CONTROL | A | **3.3-V Control Signal:** Output from the PMD regulator circuit to external PNP transistor circuit. |
| 45 | V3_COMP_CAP | A | **Compensation Capacitor**: Connects to off-chip compensation capacitor for 3.3-V conversion circuit. |
| **POWER AND GROUND** | | | |
| – | VDD | | Positive (+5 V) Supply Pins: Digital.<br>Pins 2, 9, 21, 58 |
| – | GND | | Negative (Ground) Supply Pins: Digital.<br>Pins 7, 10, 17, 20, 22, 54, 57, 59 |
| 39 | AVDD | | Positive (+5 V) Supply Pins: Analog. |
| 32, 40 | AGND | | Negative (Ground) Supply Pins: Analog. |
| **NO CONNECTS** | | | |
| – | NC | | **Reserved:** Do not make board-level connections to the following signals:<br>• 1, 5, 6, 8, 14, 15, 24, 26, 27, 28, 29, 33, 34, 41, 44, 46, 51, 52, 55, 56, 60, 61, 62, 63 |
| I/O Type Definitions:<br>O = TTL Output<br>Z = Tri-state<br>A = Analog | | | IPD = TTL Input with 15-kΩ Pull-Down Resistor<br>IPU = TTL Input with 15-kΩ Pull-Up Resistor<br>I = TTL Input |

## PMD Module DC Specifications

The following table gives the electrical specifications for the PMD Digital I/O.

**Table 2. DC Specifications for PMD I/O**

| Symbol | Parameter | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| VOH | Minimum High-Level Output Voltage | IOH =-1 mA | 3.0 | | V |
| VOL | Minimum Low-Level Output Voltage | IOL = 1 mA | | 0.4 | V |
| VIH | Minimum High-Level Input Voltage | | 2.0 | | V |
| VIL | Maximum Low-Level Input Voltage | | | 0.8 | V |
| IOZ | Maximum Output Leakage Current in TRI_STATE | VOUT=Vdd or GND | -10 | +10 | uA |
| IN1 | Input Current w/o Integrated Resistor | VI=Vdd or GND | -1 | +1 | uA |
| IN1 | Input Current w/ Integrated Resistor | VI=Vdd or GND | -500 | +500 | uA |

The analog I/O have unique properties and characteristics, and must be wired with the components exactly as shown in Figure 5 on page 14.

The transmitter (TxA, TxB) output signal levels are not standard logic levels. The levels are designed to meet the ATM 25Mbps Transmit templates. The typical values are 3.7 V peak to peak for STP cable and 3 V peak to peak for UTP cables when measured at the Media Interface Connector.

The receiver input pins (RxA, RxB) have a DC bias level of Vdd/2 and should not be loaded with a DC path to Ground. Normal connection of these pins is to the MIIM

## PMD Module AC Specifications

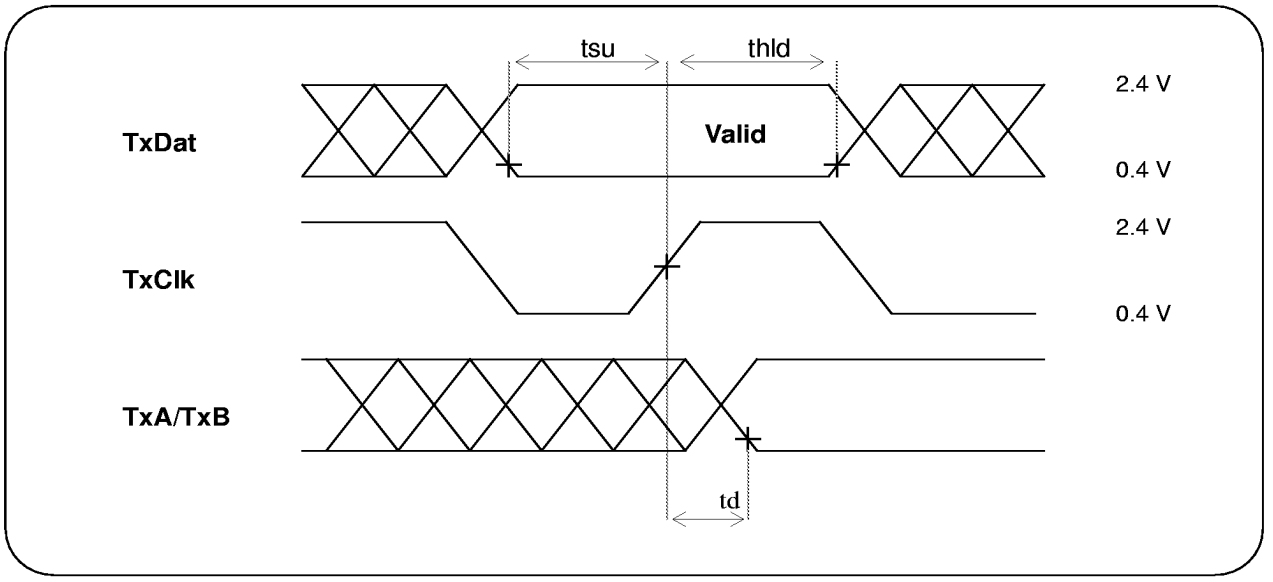
The PMD AC timings are provided for reference only. The ATM Controller Chip is designed to connect directly to the PMD chip and meet all of the interface timings.

### Transmit Timing Information

**Table 3. Transmit Timings — AC Specifications**

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| tsu | Set-up time | 4 | | | ns |
| thld | Hold time | 4 | | | ns |
| td | Delay from TxClk transition to the TxA/TxB transition | | 10 | | ns |

**Figure 3. Transmit Timing Diagrams**

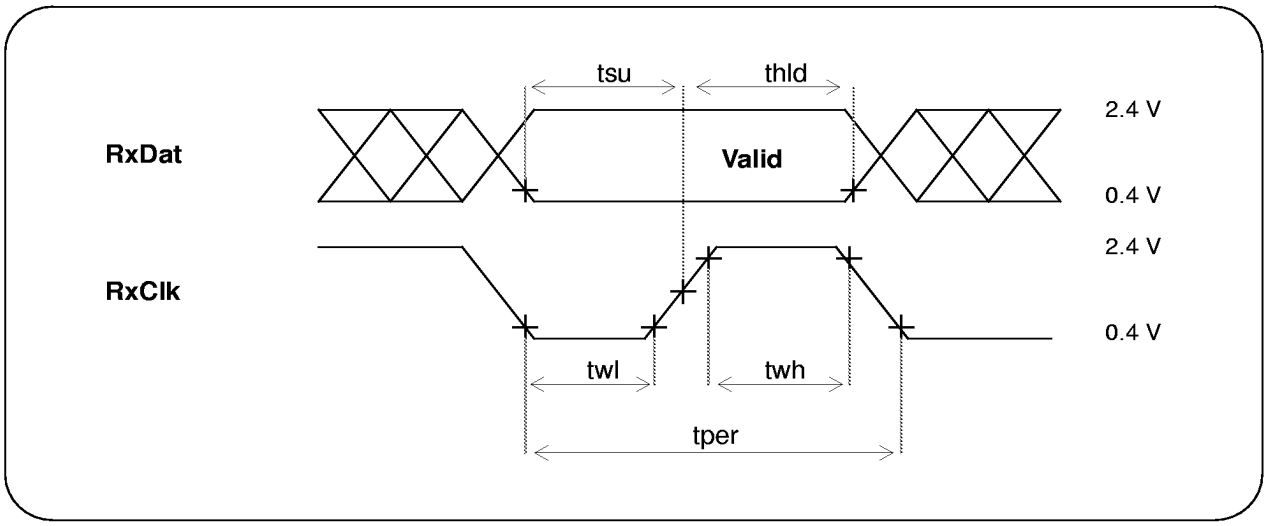


## PMD Module Receive Timing Information

### Table 4. Receive Timings—AC Specifications

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| tsu | Set-up time | 8 | | | ns |
| thld | Hold time | 8 | | | ns |
| twh | Pulse duration, RxClk high | 12 | | | ns |
| twl | Pulse duration, RxClk low | 12 | | | ns |
| tper | Period of RxClk | | 31.25 | | ns |

**Figure 4. Receive Timing Diagram**



# PMD Module Physical Specifications

## Power Dissipation

Table 5 provides the power supply dissipation for the PMD Module.

**Table 5. PMD Power Dissipation**

| | IEVdd Nominal | Card Power | Chip Power |
|---|---|---|---|
| Total (nom) | 123 mA | 625 mW | 480 mW |
| Total (max) | 147 mA | 750 mW | 600 mW |
| Total (reset) | 19 mA | 103 mW | 103 mW |

## Electrical Characteristics — Absolute Ratings

Table 6 gives the absolute ratings for various electrical characteristics.

**Table 6. Absolute Electrical Ratings for the PMD Module**

| | |
|---|---|
| Supply Voltage (Vdd) | +4.5 V to +5.5 V |
| DC Input Voltage (VIN) | -0.5 V to (Vdd + 0.5 V) |
| DC Output Voltage (VOUT) | -0.5 V to (Vdd + 0.5 V) |
| Storage Temperature Range (Tstg) | -56°C to +150°C |
| Operating Temperature Range | 0°C-70°C (typical) |
| Power Dissipation (PD) | 750 mW |
| ESD Rating | -2000 V to +2000 V |

## Thermal Characteristics

**Table 7. Thermal Characteristics**

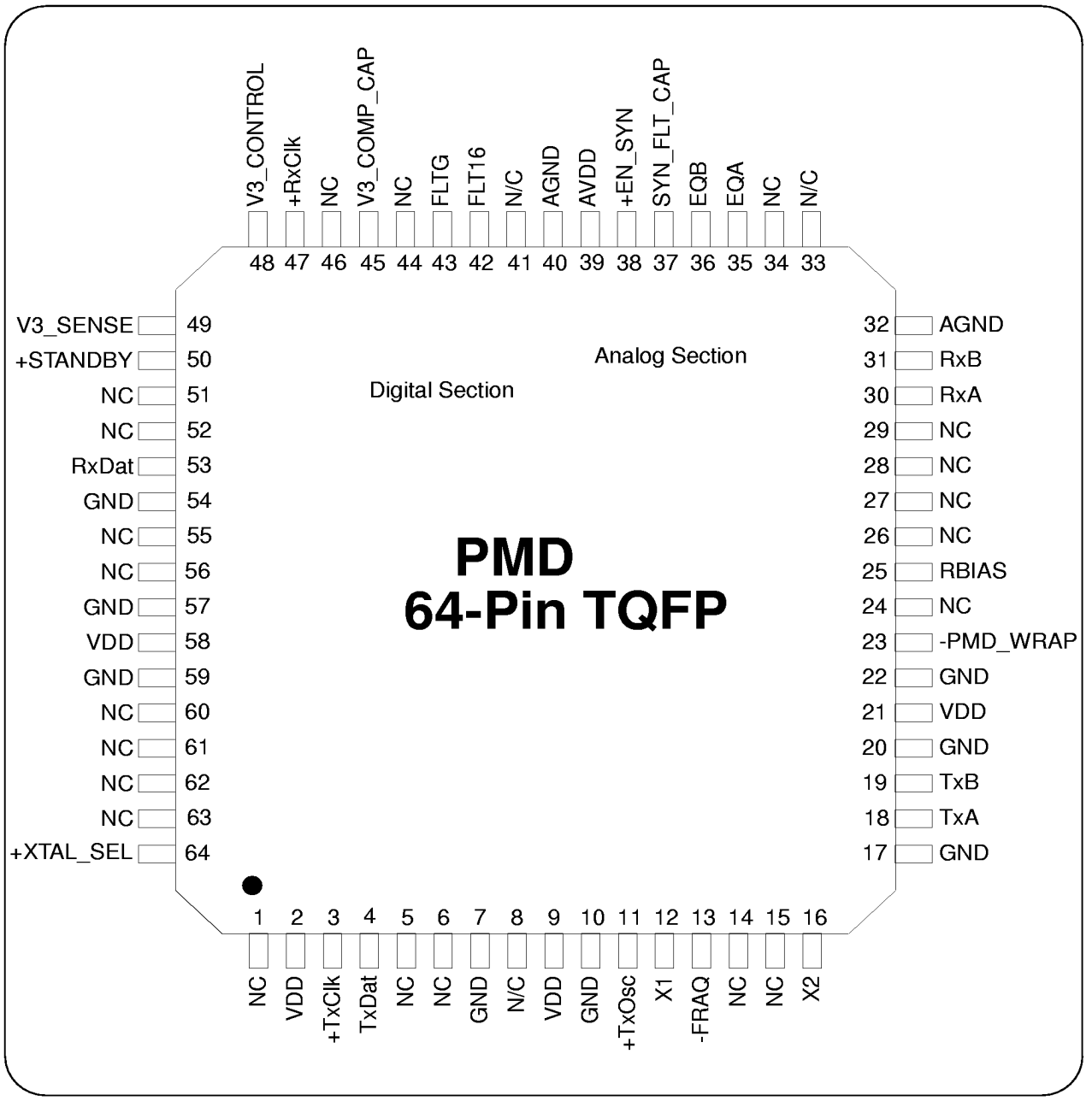
| Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| Thermal Resistance: Junction to Ambient | | 45 | | C/W | 0 ft./min. airflow |

## Mechanical Drawing

A complete mechanical drawing of the PMD module is available upon request.

## PMD Module Pin Diagram (64-Pin TQFP Package)

**Figure 5. PMD 64-pin TQFP Pin Diagram as Viewed from the Top of the Module.**



## Interface Circuit for ATM25 Application

**Figure 6. Interface Circuit for ATM25 Application**

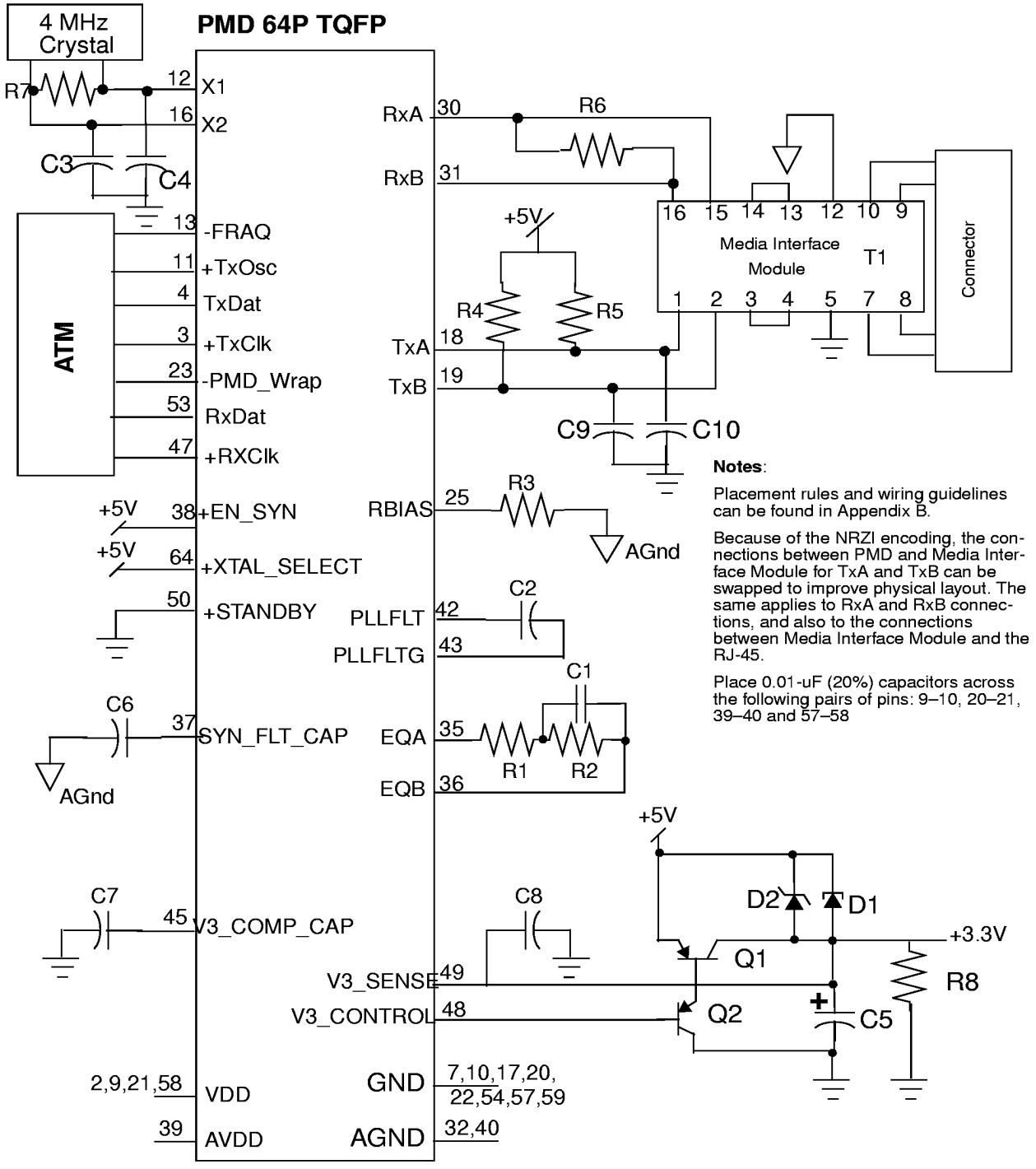
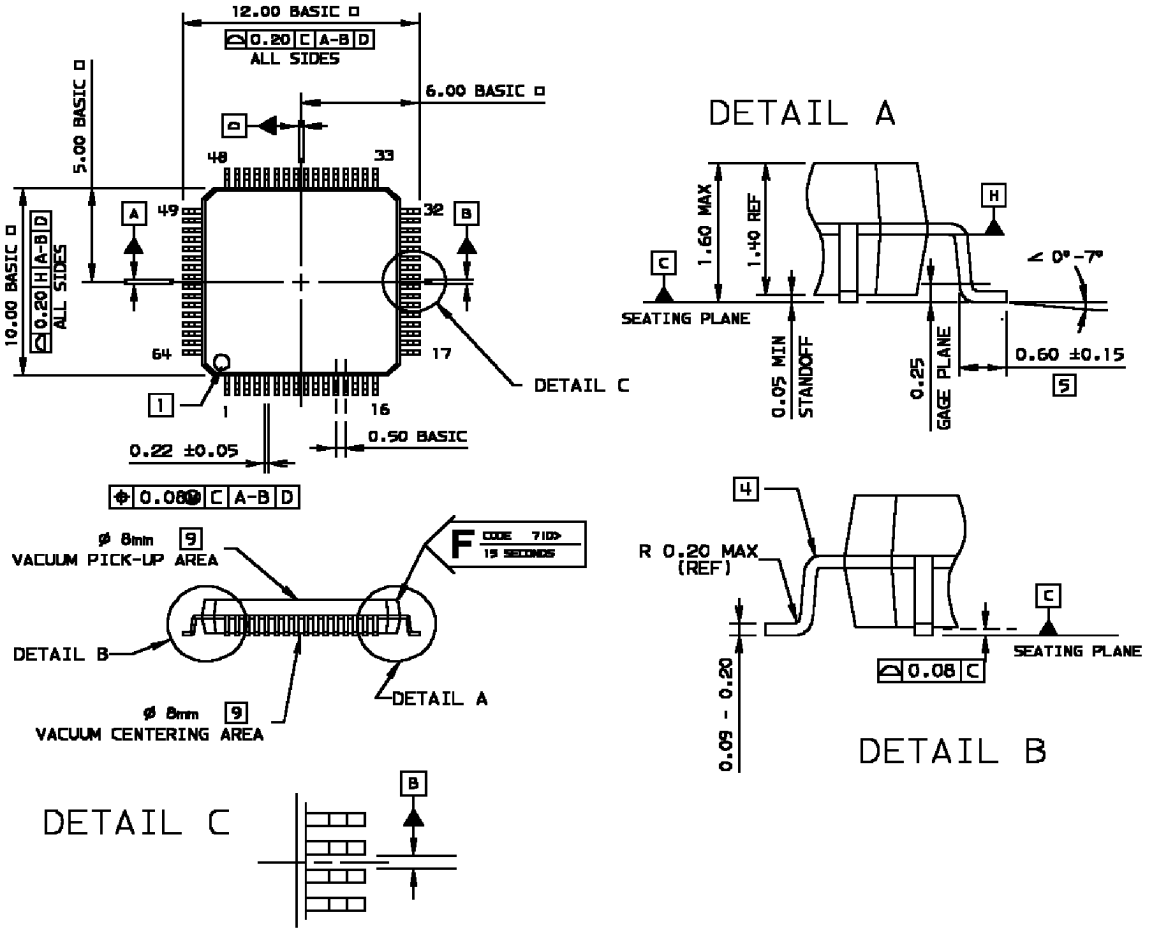


Figure 7. Package Diagrams

# 64 Lead Thin PQFP




1. PIN 1 VISUAL INDICATOR MUST BE EASILY DISTINGUISHABLE FROM ANY MOLD EJECTOR PIN MARKS.
2. LEAD FINISH TO BE Sn/Pb ALLOY. MAXIMUM Sn TO BE 90%. THICKNESS TO BE 5.0 - 20.0 MICROMETERS.
3. MARKING: IBM OR SUPPLIER P/N. DATE CODE, AND MFG'S LOGO.
4. FLASH MAY EXTEND TO INNER VERTICAL SECTION OF LEAD.
5. FOOT LENGTH IS DETERMINED USING GAGE PLANE METHOD PER JEDEC 5PP-008
6. DATUMS A, B, AND D ARE LOCATED AT THE CENTER OF THE SPACE BETWEEN THE CENTER LEADS AND IS MEASURED AT DATUM PLANE H. DATUM D IS ⊥ TO DATUM A-B.
7. APPLICABLE SPECIFICATIONS FOR FINISHED COMPONENTS:
   - A- 68X5655 - MOISTURE SENSITIVE
   - B- 6231587 - GENERAL MECHANICAL
   - C- 23F0325 - PACKAGE FOR SHIPMENT
   - D 2413138 - FLAME APPLICATION PT. FOR FLAMMABILITY SPEC
8. DIMENSIONALLY, THIS PHYSICAL OUTLINE IS EQUIVALENT TO JEDEC REGISTRATION MO-136, VARIATION "BJ".
9. NO MOLD PROTRUSIONS OR INDENTATIONS ALLOWED. LASER MARKING IN THE VACUUM PICK-UP AREA IS ALLOWED