

## 1. Overview

The M32C/84 group (M32C/84, M32C/84T) microcomputer is a single-chip control unit that utilizes high-performance silicon gate CMOS technology with the M32C/80 series CPU core. The M32C/84 group (M32C/84, M32C/84T) is available in 144-pin and 100-pin plastic molded LQFP/QFP packages.

With a 16-Mbyte address space, this microcomputer combines advanced instruction manipulation capabilities to process complex instructions by less bytes and execute instructions at higher speed.

It includes a multiplier and DMAC adequate for office automation, communication devices and industrial equipments, and other high-speed processing applications.

### 1.1 Applications

Automobiles, audio, cameras, office equipment, communications equipment, portable equipment, etc.

## 1.2 Performance Overview

Tables 1.1 and 1.2 list performance overview of the M32C/84 group (M32C/84, M32C/84T).

**Table 1.1 M32C/84 Group (M32C/84, M32C/84T) Performance (144-Pin Package)**

| Characteristic                |                                     | Performance  |   |
|-------------------------------|-------------------------------------|--|---|
|                               |                                     | M32C/84  | M32C/84T  |
| CPU                           | Basic Instructions                  | 108 instructions   |   |
|                               | Shortest Instruction Execution Time | 31.3 ns<br>(f(BCLK)=32 MHz, Vcc1=4.2 V to 5.5 V)<br>41.7 ns<br>(f(BCLK)=24 MHz, Vcc1=3.0 V to 5.5 V)   | 31.3 ns<br>(f(BCLK)=32 MHz, Vcc1=4.2 V to 5.5 V)  |
|                               | Operation Mode                      | Single-chip mode, Memory expansion mode and Microprocessor mode  | Single-chip mode  |
|                               | Address Space                       | 16 Mbytes  |   |
|                               | Memory Capacity                     | See Table 1.3  |   |
| Peripheral Function           | I/O Port                            | 123 I/O pins and 1 input pin   |   |
|                               | Multifunction Timer                 | Timer A: 16 bits x 5 channels, Timer B: 16 bits x 6 channels<br>Three-phase motor control circuit  |   |
|                               | Intelligent I/O                     | Time measurement function or Waveform generating function:<br>16 bits x 8 channels<br>Communication function (Clock synchronous serial I/O, Clock asynchronous serial I/O, HDLC data processing)   |   |
|                               | Serial I/O                          | 5 Channels<br>Clock synchronous serial I/O, Clock asynchronous serial I/O, IEBus <sup>(1)</sup> , I <sup>2</sup> C bus <sup>(2)</sup>  |   |
|                               | CAN Module                          | 1 channel Supporting CAN 2.0B specification  |   |
|                               | A/D Converter                       | 10-bit A/D converter: 1 circuit, 34 channels   |   |
|                               | D/A Converter                       | 8 bits x 2 channels  |   |
|                               | DMAC                                | 4 channels   |   |
|                               | DMAC II                             | Can be activated by all peripheral function interrupt sources<br>Immediate transfer, Calculation transfer and Chain transfer functions   |   |
|                               | CRC Calculation Circuit             | CRC-CCITT  |   |
|                               | X/Y Converter                       | 16 bits x 16 bits  |   |
|                               | Watchdog Timer                      | 15 bits x 1 channel (with prescaler)   |   |
|                               | Interrupt                           | 38 internal and 8 external sources, 5 software sources<br>Interrupt priority level: 7  |   |
|                               | Clock Generation Circuit            | 4 circuits<br>Main clock oscillation circuit(*), Sub clock oscillation circuit(*), On-chip oscillator, PLL frequency synthesizer<br>(* )Equipped with a built-in feedback resistor. Ceramic resonator or crystal oscillator must be connected externally |   |
|                               | Oscillation Stop Detect Function    | Main clock oscillation stop detect function  |   |
| Voltage Detection Circuit     | Available (optional)                | Not available <sup>(4)</sup>   |   |
| Electrical Characteristics    | Supply Voltage                      | Vcc1=4.2 V to 5.5 V, Vcc2=3.0 V to Vcc1<br>(f(BCLK)=32 MHz)<br>Vcc1=3.0 V to 5.5 V, Vcc2=3.0 V to Vcc1<br>(f(BCLK)=24 MHz)   | Vcc1=Vcc2=4.2 V to 5.5 V,<br>(f(BCLK)=32 MHz) <sup>(3)</sup>                                      |
|                               | Power Consumption                   | 28 mA (Vcc1=Vcc2=5 V,<br>f(BCLK)=32 MHz)<br>22 mA (Vcc1=Vcc2=3.3 V,<br>f(BCLK)=24 MHz)<br>10µA (Vcc1=Vcc2=5 V,<br>f(BCLK)=32 kHz, in wait mode)  | 28 mA (Vcc1=Vcc2=5 V,<br>f(BCLK)=32 MHz)<br>10µA (Vcc1=Vcc2=5 V,<br>f(BCLK)=32 kHz, in wait mode) |
| Flash Memory                  | Program/Erase Supply Voltage        | 3.3 V ± 0.3 V or 5.0 V ± 0.5 V   |   |
|                               | Program and Erase Endurance         | 100 times (all space)  |   |
| Operating Ambient Temperature |                                     | -20 to 85°C  | -40 to 85°C (T version)   |
|                               |                                     | -40 to 85°C (optional)   |   |
| Package                       | 144-pin plastic molded LQFP         |  |   |

NOTES:

1. IEBus is a trademark of NEC Electronics Corporation.
2. I<sup>2</sup>C bus is a trademark of Koninklijke Philips Electronics N. V.
3. The supply voltage of M32C/84T (High-reliability version) must be Vcc1=Vcc2.
4. The cold start-up/warm start-up determine function is available only at the user's option.

All options are on a request basis.

**Table 1.2 M32C/84 Group (M32C/84, M32C/84T) Performance (100-Pin Package)**

| Characteristic                |                                     | Performance  |  |
|-------------------------------|-------------------------------------|--|--|
|                               |                                     | M32C/84  | M32C/84T   |
| CPU                           | Basic Instructions                  | 108 instructions   |  |
|                               | Shortest Instruction Execution Time | 31.3 ns<br>(f(BCLK)=32 MHz, VCC1=4.2 V to 5.5 V)<br>41.7 ns<br>(f(BCLK)=24 MHz, VCC1=3.0 V to 5.5 V)   | 31.3 ns<br>(f(BCLK)=32 MHz, VCC1=4.2 V to 5.5 V)   |
|                               | Operation Mode                      | Single-chip mode, Memory expansion mode and Microprocessor mode  | Single-chip mode   |
|                               | Address Space                       | 16 Mbytes  |  |
|                               | Memory Capacity                     | See Table 1.3  |  |
| Peripheral Function           | I/O Port                            | 87 I/O pins and 1 input pin  |  |
|                               | Multifunction Timer                 | Timer A: 16 bits x 5 channels, Timer B: 16 bits x 6 channels<br>Three-phase motor control circuit  |  |
|                               | Intelligent I/O                     | Time measurement function or Waveform generating function:<br>16 bits x 8 channels<br>Communication function (Clock synchronous serial I/O, Clock asynchronous serial I/O, HDLC data processing)   |  |
|                               | Serial I/O                          | 5 Channels<br>Clock synchronous serial I/O, Clock asynchronous serial I/O, IEBus <sup>(1)</sup> , I <sup>2</sup> C bus <sup>(2)</sup>  |  |
|                               | CAN Module                          | 1 channel Supporting CAN 2.0B specification  |  |
|                               | A/D Converter                       | 10-bit A/D converter: 1 circuit, 26 channels   |  |
|                               | D/A Converter                       | 8 bits x 2 channels  |  |
|                               | DMAC                                | 4 channels   |  |
|                               | DMAC II                             | Can be activated by all peripheral function interrupt sources<br>Immediate transfer, Calculation transfer and Chain transfer functions   |  |
|                               | CRC Calculation Circuit             | CRC-CCITT  |  |
|                               | X/Y Converter                       | 16 bits x 16 bits  |  |
|                               | Watchdog Timer                      | 15 bits x 1 channel (with prescaler)   |  |
|                               | Interrupt                           | 38 internal and 8 external sources, 5 software sources<br>Interrupt priority level: 7  |  |
|                               | Clock Generation Circuit            | 4 circuits<br>Main clock oscillation circuit(*), Sub clock oscillation circuit(*), On-chip oscillator, PLL frequency synthesizer<br>(* )Equipped with a built-in feedback resistor. Ceramic resonator or crystal oscillator must be connected externally |  |
|                               | Oscillation Stop Detect Function    | Main clock oscillation stop detect function  |  |
|                               | Electrical Characteristics          | Supply Voltage   | VCC1=4.2 V to 5.5 V, VCC2=3.0 V to VCC1<br>(f(BCLK)=32 MHz)<br>VCC1=3.0 V to 5.5 V, VCC2=3.0 V to VCC1<br>(f(BCLK)=24 MHz) |
| Power Consumption             |                                     | 28 mA (VCC1=VCC2=5 V,<br>f(BCLK)=32 MHz)<br>22 mA (VCC1=VCC2=3.3 V,<br>f(BCLK)=24 MHz)<br>10μA (VCC1=VCC2=5 V,<br>f(BCLK)=32 kHz, in wait mode)  | 28 mA (VCC1=VCC2=5 V,<br>f(BCLK)=32 MHz)<br>10μA (VCC1=VCC2=5 V,<br>f(BCLK)=32 kHz, in wait mode)                          |
| Flash Memory                  | Program/Erase Supply Voltage        | 3.3 V ± 0.3 V or 5.0 V ± 0.5 V   |  |
|                               | Program and Erase Endurance         | 100 times (all space)  |  |
| Operating Ambient Temperature |                                     | -20 to 85°C  | -40 to 85°C (T version)  |
|                               |                                     | -40 to 85°C (optional)   |  |
| Package                       | 100-pin plastic molded LQFP/QFP     |  |  |

## NOTES:

1. IEBus is a trademark of NEC Electronics Corporation.
2. I<sup>2</sup>C bus is a trademark of Koninklijke Philips Electronics N. V.
3. The supply voltage of M32C/84T (High-reliability version) must be VCC1=VCC2.
4. The cold start-up/warm start-up determine function is available only at the user's option.

All options are on a request basis.

### 1.3 Block Diagram

Figure 1.1 shows a block diagram of the M32C/84 group (M32C/84, M32C/84T) microcomputer.

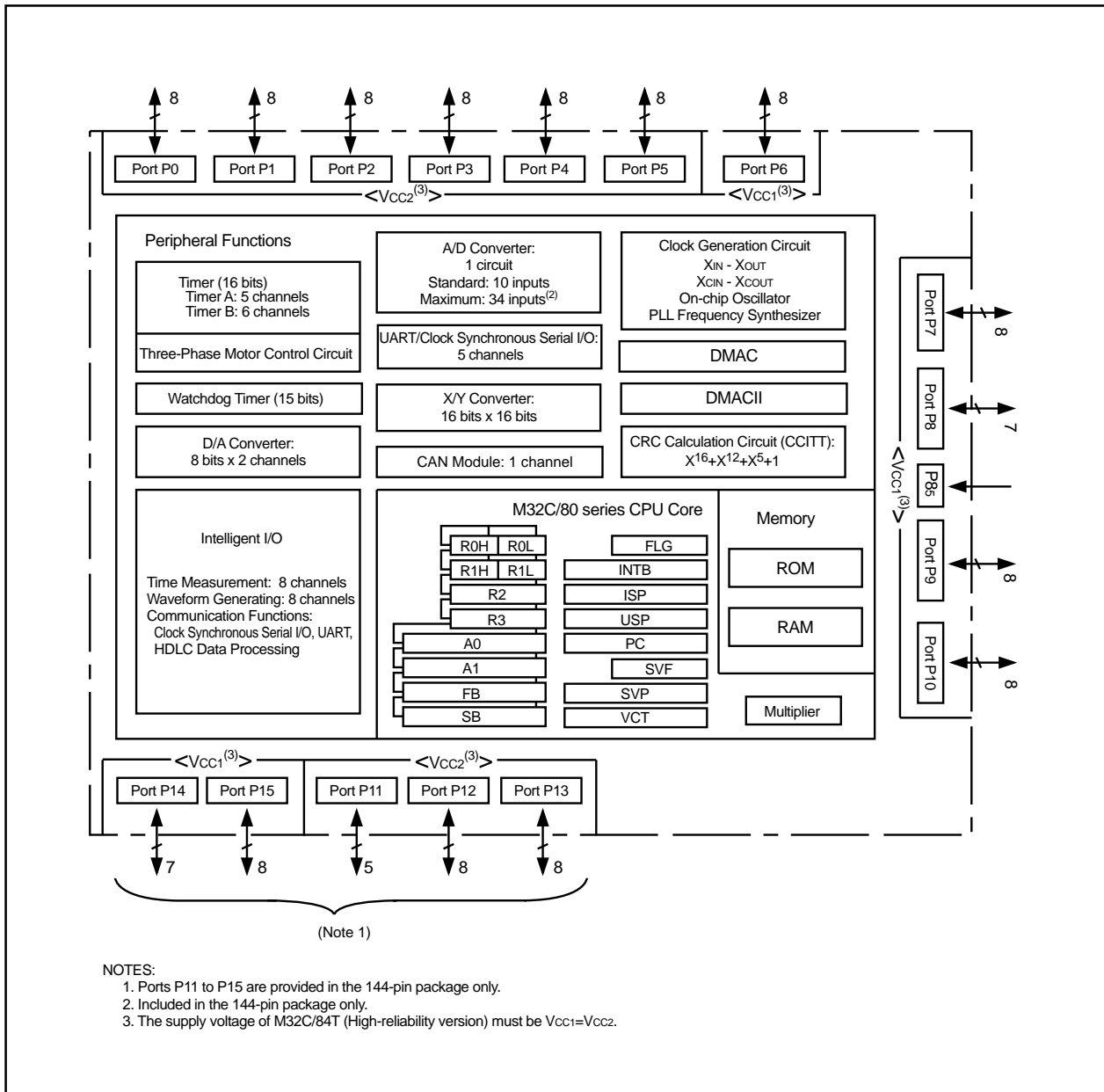


Figure 1.1 M32C/84 Group (M32C/84, M32C/84T) Block Diagram

## 1.4 Product Information

Table 1.3 lists product information. Figure 1.2 shows the product numbering system.

**Table 1.3 M32C/84 Group (1) (M32C/84)**

**As of July, 2005**

| Type Number    | Package                 | ROM Capacity | RAM Capacity | Remarks      |          |
|----------------|-------------------------|--------------|--------------|--------------|----------|
| M30845FJGP     | PLQP0144KA-A (144P6Q-A) | 512K+4K      | 24K          | Flash Memory |          |
| M30843FJGP     | PLQP0100KB-A (100P6Q-A) |              |              |              |          |
| M30843FJFP     | PRQP0100JB-A (100P6S-A) |              |              |              |          |
| M30845FHGP     | PLQP0144KA-A (144P6Q-A) | 384K+4K      |              |              |          |
| M30843FHGP     | PLQP0100KB-A (100P6Q-A) |              |              |              |          |
| M30843FHFP     | PRQP0100JB-A (100P6S-A) |              |              |              |          |
| M30845FWGP     | PLQP0144KA-A (144P6Q-A) | 320K+4K      |              | 16K          | Mask ROM |
| M30843FWGP     | PLQP0100KB-A (100P6Q-A) |              |              |              |          |
| M30845MW-XXXGP | PLQP0144KA-A (144P6Q-A) | 320K         |              |              |          |
| M30843MW-XXXGP | PLQP0100KB-A (100P6Q-A) |              |              |              |          |
| M30843MW-XXXFP | PRQP0100JB-A (100P6S-A) |              |              |              |          |
| M30842ME-XXXGP | PLQP0144KA-A (144P6Q-A) | 192K         |              |              |          |
| M30840ME-XXXGP | PLQP0100KB-A (100P6Q-A) |              |              |              |          |
| M30840ME-XXXFP | PRQP0100JB-A (100P6S-A) |              |              |              |          |
| M30842MC-XXXGP | PLQP0144KA-A (144P6Q-A) | 128K         |              |              |          |
| M30840MC-XXXGP | PLQP0100KB-A (100P6Q-A) |              |              |              |          |
| M30840MC-XXXFP | PRQP0100JB-A (100P6S-A) |              |              |              |          |
| M30842SGP (D)  | PLQP0144KA-A (144P6Q-A) | ---          | 10K          |              | ROMless  |
| M30840SGP (D)  | PLQP0100KB-A (100P6Q-A) |              |              |              |          |
| M30840SFP (D)  | PRQP0100JB-A (100P6S-A) |              |              |              |          |

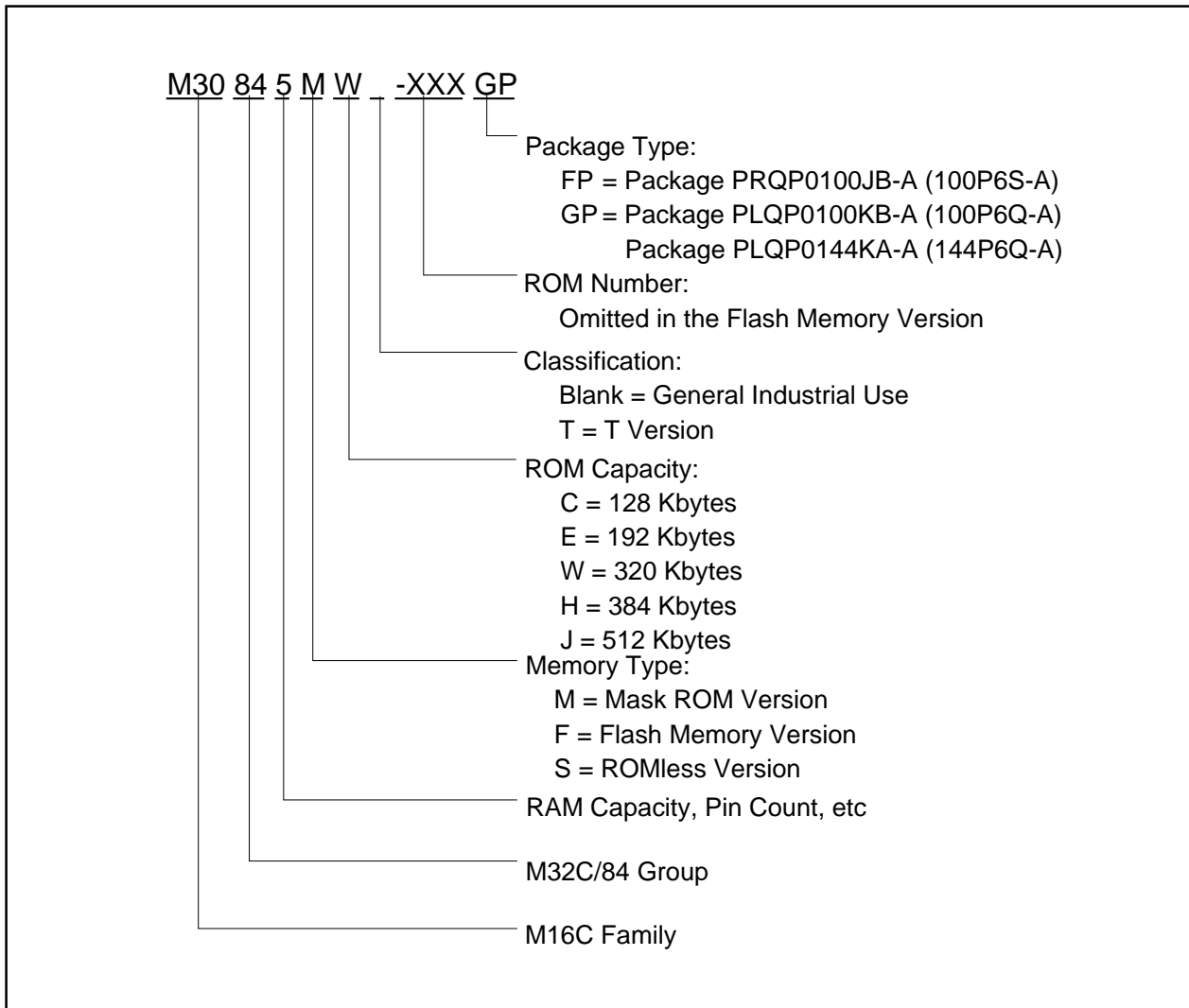
(D): Under Development

**Table 1.3 M32C/84 Group (2) (T Version, M32C/84T)**

**As of July, 2005**

| Type Number         | Package                 | ROM Capacity | RAM Capacity | Remarks  |
|---------------------|-------------------------|--------------|--------------|--|
| M30845FJTGP         | PLQP0144KA-A (144P6Q-A) | 512K+4K      | 24K          | Flash Memory<br>T Version<br>(High-releability<br>85° C Version) |
| M30843FJTGP         | PLQP0100KB-A (100P6Q-A) |              |              |  |
| M30845FHTGP         | PLQP0144KA-A (144P6Q-A) | 384K+4K      |              |  |
| M30843FHTGP         | PLQP0100KB-A (100P6Q-A) |              |              |  |
| M30843FWTGP         | PLQP0100KB-A (100P6Q-A) | 320K+4K      |              |  |
| M30842MCT-XXXGP (D) | PLQP0144KA-A (144P6Q-A) | 128K         |              |  |
| M30840MCT-XXXGP (D) | PLQP0100KB-A (100P6Q-A) |              |              |  |

(D): Under Development



**Figure 1.2 Product Numbering System**

### 1.5 Pin Assignments and Descriptions

Figures 1.3 to 1.5 show pin assignments (top view).

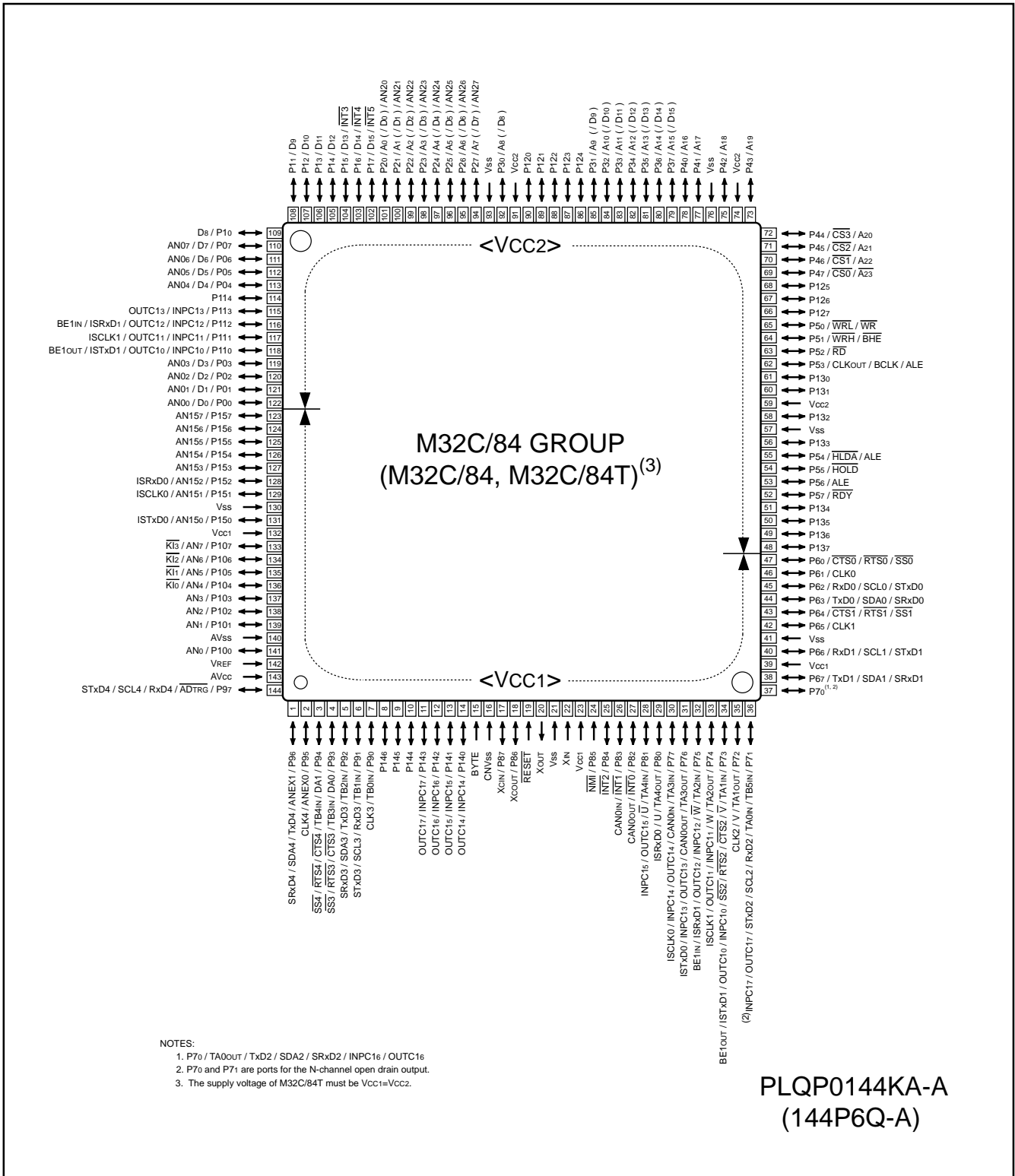


Figure 1.3 Pin Assignment for 144-Pin Package

**Table 1.4 Pin Characteristics for 144-Pin Package**

| Pin No. | Control Pin               | Port | Interrupt Pin            | Timer Pin                     | UART/CAN Pin                                    | Intelligent I/O Pin         | Analog Pin | Bus Control Pin <sup>(1)</sup> |
|---------|---------------------------|------|--------------------------|-------------------------------|---|-----------------------------|------------|--------------------------------|
| 1       |                           | P96  |                          |                               | TxD4/SDA4/SRx4                                  |                             | ANEX1      |                                |
| 2       |                           | P95  |                          |                               | CLK4  |                             | ANEX0      |                                |
| 3       |                           | P94  |                          | TB4IN                         | $\overline{\text{CTS4}}/\text{RTS4}/\text{SS4}$ |                             | DA1        |                                |
| 4       |                           | P93  |                          | TB3IN                         | $\overline{\text{CTS3}}/\text{RTS3}/\text{SS3}$ |                             | DA0        |                                |
| 5       |                           | P92  |                          | TB2IN                         | TxD3/SDA3/SRx3                                  |                             |            |                                |
| 6       |                           | P91  |                          | TB1IN                         | RxD3/SCL3/STxD3                                 |                             |            |                                |
| 7       |                           | P90  |                          | TB0IN                         | CLK3  |                             |            |                                |
| 8       |                           | P146 |                          |                               |   |                             |            |                                |
| 9       |                           | P145 |                          |                               |   |                             |            |                                |
| 10      |                           | P144 |                          |                               |   |                             |            |                                |
| 11      |                           | P143 |                          |                               |   | INPC17/OUTC17               |            |                                |
| 12      |                           | P142 |                          |                               |   | INPC16/OUTC16               |            |                                |
| 13      |                           | P141 |                          |                               |   | INPC15/OUTC15               |            |                                |
| 14      |                           | P140 |                          |                               |   | INPC14/OUTC14               |            |                                |
| 15      | BYTE                      |      |                          |                               |   |                             |            |                                |
| 16      | CNVSS                     |      |                          |                               |   |                             |            |                                |
| 17      | X <sub>CIN</sub>          | P87  |                          |                               |   |                             |            |                                |
| 18      | X <sub>COU</sub>          | P86  |                          |                               |   |                             |            |                                |
| 19      | $\overline{\text{RESET}}$ |      |                          |                               |   |                             |            |                                |
| 20      | X <sub>OUT</sub>          |      |                          |                               |   |                             |            |                                |
| 21      | V <sub>SS</sub>           |      |                          |                               |   |                             |            |                                |
| 22      | X <sub>IN</sub>           |      |                          |                               |   |                             |            |                                |
| 23      | V <sub>CC1</sub>          |      |                          |                               |   |                             |            |                                |
| 24      |                           | P85  | $\overline{\text{NMI}}$  |                               |   |                             |            |                                |
| 25      |                           | P84  | $\overline{\text{INT2}}$ |                               |   |                             |            |                                |
| 26      |                           | P83  | $\overline{\text{INT1}}$ |                               | CAN0IN  |                             |            |                                |
| 27      |                           | P82  | $\overline{\text{INT0}}$ |                               | CAN0OUT   |                             |            |                                |
| 28      |                           | P81  |                          | TA4IN/ $\overline{\text{U}}$  |   | INPC15/OUTC15               |            |                                |
| 29      |                           | P80  |                          | TA4OUT/ $\overline{\text{U}}$ |   | ISRxD0                      |            |                                |
| 30      |                           | P77  |                          | TA3IN                         | CAN0IN  | INPC14/OUTC14/ISCLK0        |            |                                |
| 31      |                           | P76  |                          | TA3OUT                        | CAN0OUT   | INPC13/OUTC13/ISTxD0        |            |                                |
| 32      |                           | P75  |                          | TA2IN/ $\overline{\text{W}}$  |   | INPC12/OUTC12/ISRxD1/BE1IN  |            |                                |
| 33      |                           | P74  |                          | TA2OUT/ $\overline{\text{W}}$ |   | INPC11/OUTC11/ISCLK1        |            |                                |
| 34      |                           | P73  |                          | TA1IN/ $\overline{\text{V}}$  | $\overline{\text{CTS2}}/\text{RTS2}/\text{SS2}$ | INPC10/OUTC10/ISTxD1/BE1OUT |            |                                |
| 35      |                           | P72  |                          | TA1OUT/ $\overline{\text{V}}$ | CLK2  |                             |            |                                |
| 36      |                           | P71  |                          | TB5IN/TA0IN                   | RxD2/SCL2/STxD2                                 | INPC17/OUTC17               |            |                                |
| 37      |                           | P70  |                          | TA0OUT                        | TxD2/SDA2/SRx2                                  | INPC16/OUTC16               |            |                                |
| 38      |                           | P67  |                          |                               | TxD1/SDA1/SRx1                                  |                             |            |                                |
| 39      | V <sub>CC1</sub>          |      |                          |                               |   |                             |            |                                |
| 40      |                           | P66  |                          |                               | RxD1/SCL1/STxD1                                 |                             |            |                                |
| 41      | V <sub>SS</sub>           |      |                          |                               |   |                             |            |                                |
| 42      |                           | P65  |                          |                               | CLK1  |                             |            |                                |
| 43      |                           | P64  |                          |                               | $\overline{\text{CTS1}}/\text{RTS1}/\text{SS1}$ |                             |            |                                |
| 44      |                           | P63  |                          |                               | TxD0/SDA0/SRx0                                  |                             |            |                                |
| 45      |                           | P62  |                          |                               | RxD0/SCL0/STxD0                                 |                             |            |                                |
| 46      |                           | P61  |                          |                               | CLK0  |                             |            |                                |
| 47      |                           | P60  |                          |                               | $\overline{\text{CTS0}}/\text{RTS0}/\text{SS0}$ |                             |            |                                |
| 48      |                           | P137 |                          |                               |   |                             |            |                                |

## NOTES:

1. Bus control pins in M32C/84T cannot be used.



Table 1.4 Pin Characteristics for 144-Pin Package (Continued)

| Pin No. | Control Pin | Port | Interrupt Pin | Timer Pin | UART/CAN Pin | Intelligent I/O Pin | Analog Pin | Bus Control Pin                     |
|---------|-------------|------|---------------|-----------|--------------|---------------------|------------|-------------------------------------|
| 49      |             | P136 |               |           |              |                     |            |                                     |
| 50      |             | P135 |               |           |              |                     |            |                                     |
| 51      |             | P134 |               |           |              |                     |            |                                     |
| 52      |             | P57  |               |           |              |                     |            | $\overline{\text{RDY}}$             |
| 53      |             | P56  |               |           |              |                     |            | $\overline{\text{ALE}}$             |
| 54      |             | P55  |               |           |              |                     |            | $\overline{\text{HOLD}}$            |
| 55      |             | P54  |               |           |              |                     |            | $\overline{\text{HLDA/ALE}}$        |
| 56      |             | P133 |               |           |              |                     |            |                                     |
| 57      | Vss         |      |               |           |              |                     |            |                                     |
| 58      |             | P132 |               |           |              |                     |            |                                     |
| 59      | Vcc2        |      |               |           |              |                     |            |                                     |
| 60      |             | P131 |               |           |              |                     |            |                                     |
| 61      |             | P130 |               |           |              |                     |            |                                     |
| 62      |             | P53  |               |           |              |                     |            | $\overline{\text{CLKout/BCLK/ALE}}$ |
| 63      |             | P52  |               |           |              |                     |            | $\overline{\text{RD}}$              |
| 64      |             | P51  |               |           |              |                     |            | $\overline{\text{WRH/BHE}}$         |
| 65      |             | P50  |               |           |              |                     |            | $\overline{\text{WRL/WR}}$          |
| 66      |             | P127 |               |           |              |                     |            |                                     |
| 67      |             | P126 |               |           |              |                     |            |                                     |
| 68      |             | P125 |               |           |              |                     |            |                                     |
| 69      |             | P47  |               |           |              |                     |            | $\overline{\text{CS0/A23}}$         |
| 70      |             | P46  |               |           |              |                     |            | $\overline{\text{CS1/A22}}$         |
| 71      |             | P45  |               |           |              |                     |            | $\overline{\text{CS2/A21}}$         |
| 72      |             | P44  |               |           |              |                     |            | $\overline{\text{CS3/A20}}$         |
| 73      |             | P43  |               |           |              |                     |            | A19                                 |
| 74      | Vcc2        |      |               |           |              |                     |            |                                     |
| 75      |             | P42  |               |           |              |                     |            | A18                                 |
| 76      | Vss         |      |               |           |              |                     |            |                                     |
| 77      |             | P41  |               |           |              |                     |            | A17                                 |
| 78      |             | P40  |               |           |              |                     |            | A16                                 |
| 79      |             | P37  |               |           |              |                     |            | A15(/D15)                           |
| 80      |             | P36  |               |           |              |                     |            | A14(/D14)                           |
| 81      |             | P35  |               |           |              |                     |            | A13(/D13)                           |
| 82      |             | P34  |               |           |              |                     |            | A12(/D12)                           |
| 83      |             | P33  |               |           |              |                     |            | A11(/D11)                           |
| 84      |             | P32  |               |           |              |                     |            | A10(/D10)                           |
| 85      |             | P31  |               |           |              |                     |            | A9(/D9)                             |
| 86      |             | P124 |               |           |              |                     |            |                                     |
| 87      |             | P123 |               |           |              |                     |            |                                     |
| 88      |             | P122 |               |           |              |                     |            |                                     |
| 89      |             | P121 |               |           |              |                     |            |                                     |
| 90      |             | P120 |               |           |              |                     |            |                                     |
| 91      | Vcc2        |      |               |           |              |                     |            |                                     |
| 92      |             | P30  |               |           |              |                     |            | A8(/D8)                             |
| 93      | Vss         |      |               |           |              |                     |            |                                     |
| 94      |             | P27  |               |           |              |                     | AN27       | A7(/D7)                             |
| 95      |             | P26  |               |           |              |                     | AN26       | A6(/D6)                             |
| 96      |             | P25  |               |           |              |                     | AN25       | A5(/D5)                             |

## NOTES:

1. Bus control pins in M32C/84T cannot be used.

**Table 1.4 Pin Characteristics for 144-Pin Package (Continued)**

| Pin No. | Control Pin | Port | Interrupt Pin | Timer Pin | UART/CAN Pin    | Intelligent I/O Pin         | Analog Pin | Bus Control Pin <sup>(1)</sup> |
|---------|-------------|------|---------------|-----------|-----------------|-----------------------------|------------|--------------------------------|
| 97      |             | P24  |               |           |                 |                             | AN24       | A4(/D4)                        |
| 98      |             | P23  |               |           |                 |                             | AN23       | A3(/D3)                        |
| 99      |             | P22  |               |           |                 |                             | AN22       | A2(/D2)                        |
| 100     |             | P21  |               |           |                 |                             | AN21       | A1(/D1)                        |
| 101     |             | P20  |               |           |                 |                             | AN20       | A0(/D0)                        |
| 102     |             | P17  | INT5          |           |                 |                             |            | D15                            |
| 103     |             | P16  | INT4          |           |                 |                             |            | D14                            |
| 104     |             | P15  | INT3          |           |                 |                             |            | D13                            |
| 105     |             | P14  |               |           |                 |                             |            | D12                            |
| 106     |             | P13  |               |           |                 |                             |            | D11                            |
| 107     |             | P12  |               |           |                 |                             |            | D10                            |
| 108     |             | P11  |               |           |                 |                             |            | D9                             |
| 109     |             | P10  |               |           |                 |                             |            | D8                             |
| 110     |             | P07  |               |           |                 |                             | AN07       | D7                             |
| 111     |             | P06  |               |           |                 |                             | AN06       | D6                             |
| 112     |             | P05  |               |           |                 |                             | AN05       | D5                             |
| 113     |             | P04  |               |           |                 |                             | AN04       | D4                             |
| 114     |             | P114 |               |           |                 |                             |            |                                |
| 115     |             | P113 |               |           |                 | INPC13/OUTC13               |            |                                |
| 116     |             | P112 |               |           |                 | INPC12/OUTC12/ISRxD1/BE1IN  |            |                                |
| 117     |             | P111 |               |           |                 | INPC11/OUTC11/ISCLK1        |            |                                |
| 118     |             | P110 |               |           |                 | INPC10/OUTC10/ISTxD1/BE1OUT |            |                                |
| 119     |             | P03  |               |           |                 |                             | AN03       | D3                             |
| 120     |             | P02  |               |           |                 |                             | AN02       | D2                             |
| 121     |             | P01  |               |           |                 |                             | AN01       | D1                             |
| 122     |             | P00  |               |           |                 |                             | AN00       | D0                             |
| 123     |             | P157 |               |           |                 |                             | AN157      |                                |
| 124     |             | P156 |               |           |                 |                             | AN156      |                                |
| 125     |             | P155 |               |           |                 |                             | AN155      |                                |
| 126     |             | P154 |               |           |                 |                             | AN154      |                                |
| 127     |             | P153 |               |           |                 |                             | AN153      |                                |
| 128     |             | P152 |               |           |                 | ISRxD0                      | AN152      |                                |
| 129     |             | P151 |               |           |                 | ISCLK0                      | AN151      |                                |
| 130     | Vss         |      |               |           |                 |                             |            |                                |
| 131     |             | P150 |               |           |                 | ISTxD0                      | AN150      |                                |
| 132     | VCC1        |      |               |           |                 |                             |            |                                |
| 133     |             | P107 | KI3           |           |                 |                             | AN7        |                                |
| 134     |             | P106 | KI2           |           |                 |                             | AN6        |                                |
| 135     |             | P105 | KI1           |           |                 |                             | AN5        |                                |
| 136     |             | P104 | KI0           |           |                 |                             | AN4        |                                |
| 137     |             | P103 |               |           |                 |                             | AN3        |                                |
| 138     |             | P102 |               |           |                 |                             | AN2        |                                |
| 139     |             | P101 |               |           |                 |                             | AN1        |                                |
| 140     | AVss        |      |               |           |                 |                             |            |                                |
| 141     |             | P100 |               |           |                 |                             | AN0        |                                |
| 142     | VREF        |      |               |           |                 |                             |            |                                |
| 143     | AVCC        |      |               |           |                 |                             |            |                                |
| 144     |             | P97  |               |           | RxD4/SCL4/STxD4 |                             | ADTRG      |                                |

## NOTES:

1. Bus control pins in M32C/84T cannot be used.

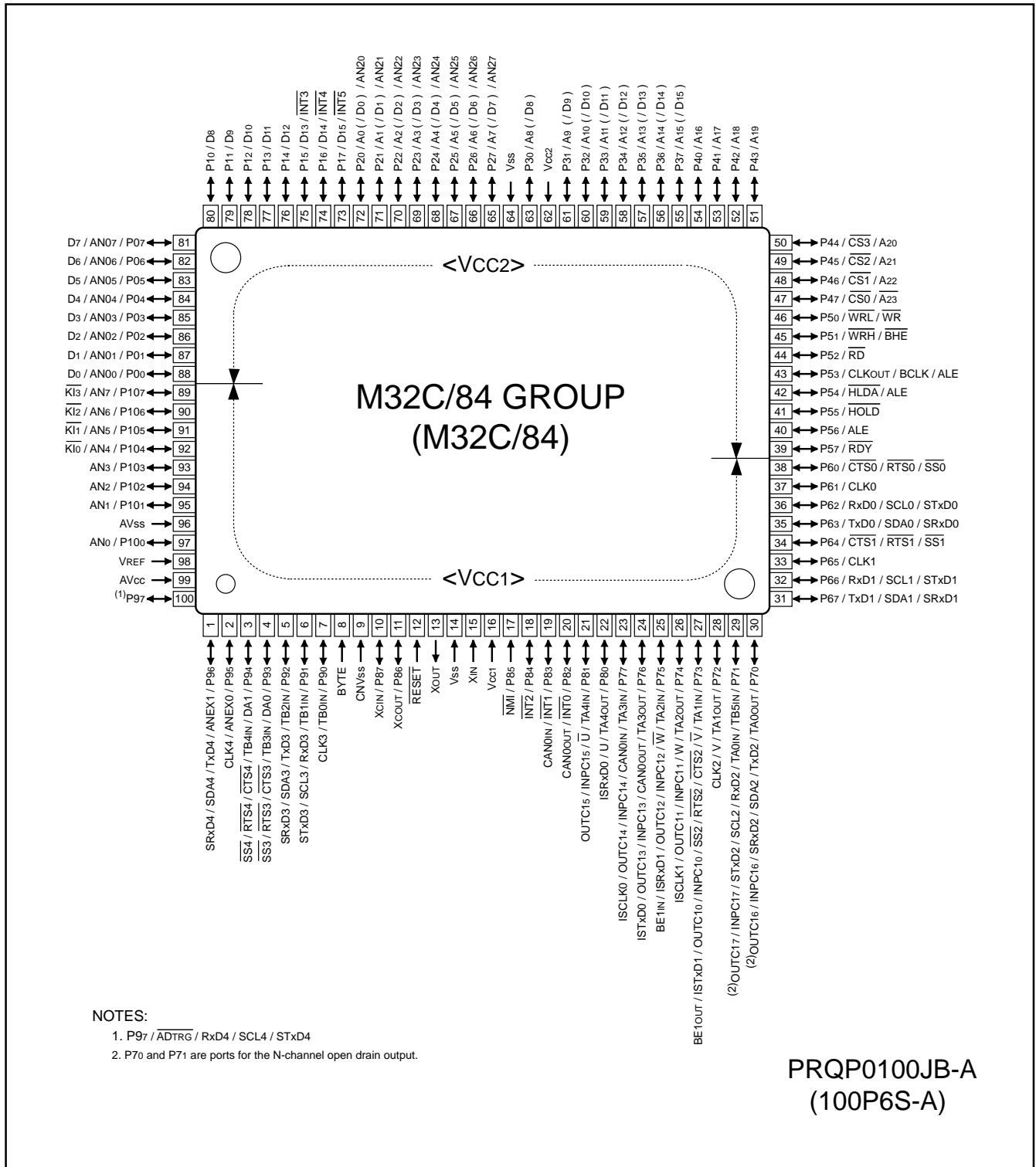


Figure 1.4 Pin Assignment for 100-Pin Package

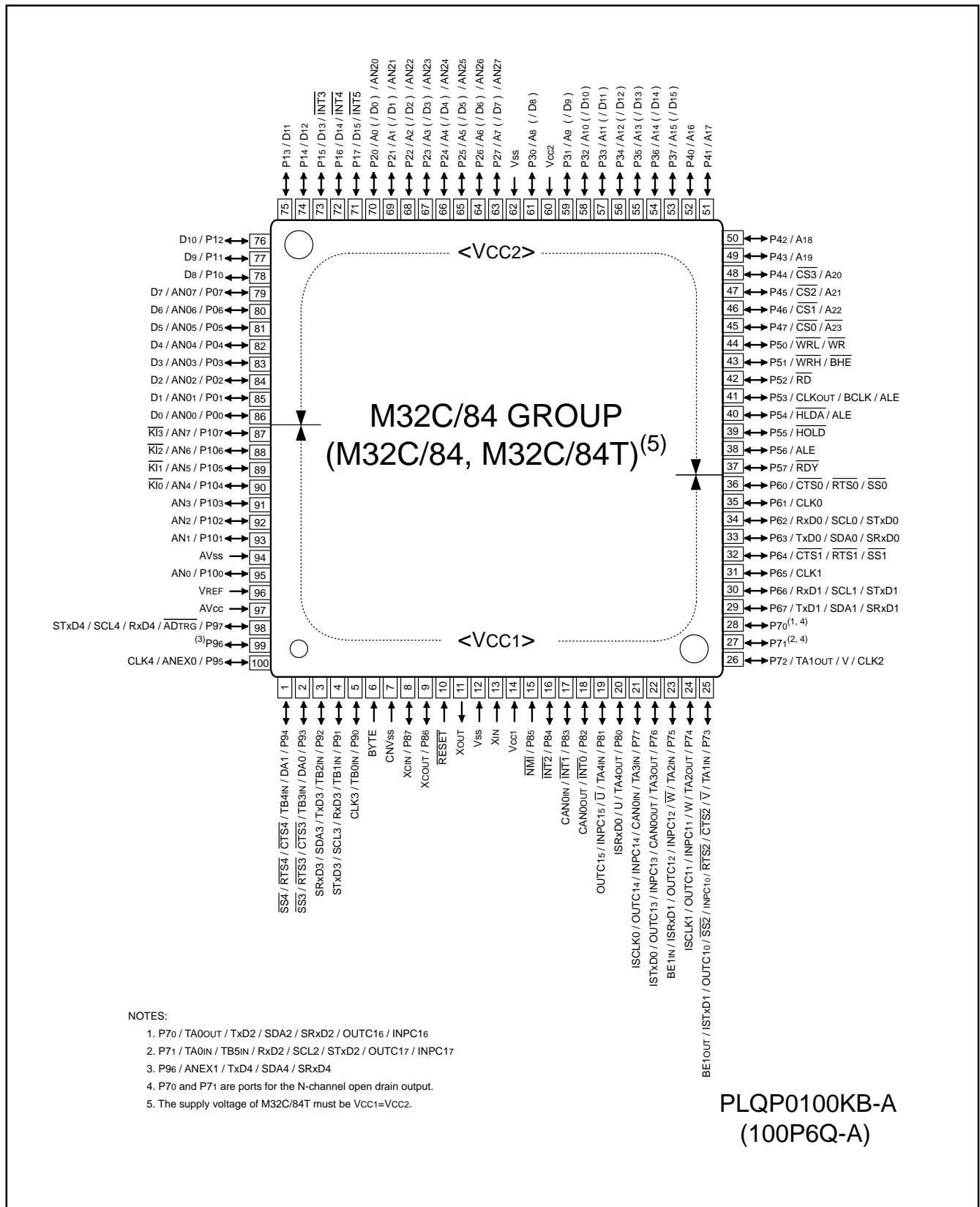


Figure 1.5 Pin Assignment for 100-Pin Package

Table 1.5 Pin Characteristics for 100-Pin Package

| Package Pin No. |     | Control Pin | Port | Interrupt Pin | Timer Pin   | UART/CAN Pin     | Intelligent I/O Pin         | Analog Pin | Bus Control Pin <sup>(1)</sup> |
|-----------------|-----|-------------|------|---------------|-------------|------------------|-----------------------------|------------|--------------------------------|
| FP              | GP  |             |      |               |             |                  |                             |            |                                |
| 1               | 99  |             | P96  |               |             | TxD4/SDA4/SRx4D4 |                             | ANEX1      |                                |
| 2               | 100 |             | P95  |               |             | CLK4             |                             | ANEX0      |                                |
| 3               | 1   |             | P94  |               | TB4IN       | CTS4/RTS4/SS4    |                             | DA1        |                                |
| 4               | 2   |             | P93  |               | TB3IN       | CTS3/RTS3/SS3    |                             | DA0        |                                |
| 5               | 3   |             | P92  |               | TB2IN       | TxD3/SDA3/SRx3D3 |                             |            |                                |
| 6               | 4   |             | P91  |               | TB1IN       | RxD3/SCL3/STxD3  |                             |            |                                |
| 7               | 5   |             | P90  |               | TB0IN       | CLK3             |                             |            |                                |
| 8               | 6   | BYTE        |      |               |             |                  |                             |            |                                |
| 9               | 7   | CNVss       |      |               |             |                  |                             |            |                                |
| 10              | 8   | XCIN        | P87  |               |             |                  |                             |            |                                |
| 11              | 9   | XCOU        | P86  |               |             |                  |                             |            |                                |
| 12              | 10  | RESET       |      |               |             |                  |                             |            |                                |
| 13              | 11  | XOUT        |      |               |             |                  |                             |            |                                |
| 14              | 12  | Vss         |      |               |             |                  |                             |            |                                |
| 15              | 13  | XIN         |      |               |             |                  |                             |            |                                |
| 16              | 14  | VCC1        |      |               |             |                  |                             |            |                                |
| 17              | 15  |             | P85  | NMI           |             |                  |                             |            |                                |
| 18              | 16  |             | P84  | INT2          |             |                  |                             |            |                                |
| 19              | 17  |             | P83  | INT1          |             | CAN0IN           |                             |            |                                |
| 20              | 18  |             | P82  | INT0          |             | CAN0OUT          |                             |            |                                |
| 21              | 19  |             | P81  |               | TA4IN/U     |                  | INPC15/OUTC15               |            |                                |
| 22              | 20  |             | P80  |               | TA4OUT/U    |                  | ISRxD0                      |            |                                |
| 23              | 21  |             | P77  |               | TA3IN       | CAN0IN           | INPC14/OUTC14/ISCLK0        |            |                                |
| 24              | 22  |             | P76  |               | TA3OUT      | CAN0OUT          | INPC13/OUTC13/ISTxD0        |            |                                |
| 25              | 23  |             | P75  |               | TA2IN/W     |                  | INPC12/OUTC12/ISRxD1/BE1IN  |            |                                |
| 26              | 24  |             | P74  |               | TA2OUT/W    |                  | INPC11/OUTC11/ISCLK1        |            |                                |
| 27              | 25  |             | P73  |               | TA1IN/V     | CTS2/RTS2/SS2    | INPC10/OUTC10/ISTxD1/BE1OUT |            |                                |
| 28              | 26  |             | P72  |               | TA1OUT/V    | CLK2             |                             |            |                                |
| 29              | 27  |             | P71  |               | TB5IN/TA0IN | RxD2/SCL2/STxD2  | INPC17/OUTC17               |            |                                |
| 30              | 28  |             | P70  |               | TA0OUT      | TxD2/SDA2/SRx2D2 | INPC16/OUTC16               |            |                                |
| 31              | 29  |             | P67  |               |             | TxD1/SDA1/SRx1D1 |                             |            |                                |
| 32              | 30  |             | P66  |               |             | RxD1/SCL1/STxD1  |                             |            |                                |
| 33              | 31  |             | P65  |               |             | CLK1             |                             |            |                                |
| 34              | 32  |             | P64  |               |             | CTS1/RTS1/SS1    |                             |            |                                |
| 35              | 33  |             | P63  |               |             | TxD0/SDA0/SRx0D0 |                             |            |                                |
| 36              | 34  |             | P62  |               |             | RxD0/SCL0/STxD0  |                             |            |                                |
| 37              | 35  |             | P61  |               |             | CLK0             |                             |            |                                |
| 38              | 36  |             | P60  |               |             | CTS0/RTS0/SS0    |                             |            |                                |
| 39              | 37  |             | P57  |               |             |                  |                             |            | RDY                            |
| 40              | 38  |             | P56  |               |             |                  |                             |            | ALE                            |
| 41              | 39  |             | P55  |               |             |                  |                             |            | HOLD                           |
| 42              | 40  |             | P54  |               |             |                  |                             |            | HLDA/ALE                       |
| 43              | 41  |             | P53  |               |             |                  |                             |            | CLKout/BCLK/ALE                |
| 44              | 42  |             | P52  |               |             |                  |                             |            | RD                             |
| 45              | 43  |             | P51  |               |             |                  |                             |            | WRH/BHE                        |
| 46              | 44  |             | P50  |               |             |                  |                             |            | WRL/WR                         |
| 47              | 45  |             | P47  |               |             |                  |                             |            | CS0/A23                        |
| 48              | 46  |             | P46  |               |             |                  |                             |            | CS1/A22                        |
| 49              | 47  |             | P45  |               |             |                  |                             |            | CS2/A21                        |
| 50              | 48  |             | P44  |               |             |                  |                             |            | CS3/A20                        |

## NOTES:

1. Bus control pins in M32C/84T cannot be used.

Table 1.5 Pin Characteristics for 100-Pin Package (Continued)

| Package Pin No. |    | Control Pin | Port | Interrupt Pin            | Timer Pin | UART/CAN Pin    | Intelligent I/O Pin | Analog Pin                | Bus Control Pin |
|-----------------|----|-------------|------|--------------------------|-----------|-----------------|---------------------|---------------------------|-----------------|
| FP              | GP |             |      |                          |           |                 |                     |                           |                 |
| 51              | 49 |             | P43  |                          |           |                 |                     |                           | A19             |
| 52              | 50 |             | P42  |                          |           |                 |                     |                           | A18             |
| 53              | 51 |             | P41  |                          |           |                 |                     |                           | A17             |
| 54              | 52 |             | P40  |                          |           |                 |                     |                           | A16             |
| 55              | 53 |             | P37  |                          |           |                 |                     |                           | A15(/D15)       |
| 56              | 54 |             | P36  |                          |           |                 |                     |                           | A14(/D14)       |
| 57              | 55 |             | P35  |                          |           |                 |                     |                           | A13(/D13)       |
| 58              | 56 |             | P34  |                          |           |                 |                     |                           | A12(/D12)       |
| 59              | 57 |             | P33  |                          |           |                 |                     |                           | A11(/D11)       |
| 60              | 58 |             | P32  |                          |           |                 |                     |                           | A10(/D10)       |
| 61              | 59 |             | P31  |                          |           |                 |                     |                           | A9(/D9)         |
| 62              | 60 | Vcc2        |      |                          |           |                 |                     |                           |                 |
| 63              | 61 |             | P30  |                          |           |                 |                     |                           | A8(/D8)         |
| 64              | 62 | Vss         |      |                          |           |                 |                     |                           |                 |
| 65              | 63 |             | P27  |                          |           |                 |                     | AN27                      | A7(/D7)         |
| 66              | 64 |             | P26  |                          |           |                 |                     | AN26                      | A6(/D6)         |
| 67              | 65 |             | P25  |                          |           |                 |                     | AN25                      | A5(/D5)         |
| 68              | 66 |             | P24  |                          |           |                 |                     | AN24                      | A4(/D4)         |
| 69              | 67 |             | P23  |                          |           |                 |                     | AN23                      | A3(/D3)         |
| 70              | 68 |             | P22  |                          |           |                 |                     | AN22                      | A2(/D2)         |
| 71              | 69 |             | P21  |                          |           |                 |                     | AN21                      | A1(/D1)         |
| 72              | 70 |             | P20  |                          |           |                 |                     | AN20                      | A0(/D0)         |
| 73              | 71 |             | P17  | $\overline{\text{INT5}}$ |           |                 |                     |                           | D15             |
| 74              | 72 |             | P16  | $\overline{\text{INT4}}$ |           |                 |                     |                           | D14             |
| 75              | 73 |             | P15  | $\overline{\text{INT3}}$ |           |                 |                     |                           | D13             |
| 76              | 74 |             | P14  |                          |           |                 |                     |                           | D12             |
| 77              | 75 |             | P13  |                          |           |                 |                     |                           | D11             |
| 78              | 76 |             | P12  |                          |           |                 |                     |                           | D10             |
| 79              | 77 |             | P11  |                          |           |                 |                     |                           | D9              |
| 80              | 78 |             | P10  |                          |           |                 |                     |                           | D8              |
| 81              | 79 |             | P07  |                          |           |                 |                     | AN07                      | D7              |
| 82              | 80 |             | P06  |                          |           |                 |                     | AN06                      | D6              |
| 83              | 81 |             | P05  |                          |           |                 |                     | AN05                      | D5              |
| 84              | 82 |             | P04  |                          |           |                 |                     | AN04                      | D4              |
| 85              | 83 |             | P03  |                          |           |                 |                     | AN03                      | D3              |
| 86              | 84 |             | P02  |                          |           |                 |                     | AN02                      | D2              |
| 87              | 85 |             | P01  |                          |           |                 |                     | AN01                      | D1              |
| 88              | 86 |             | P00  |                          |           |                 |                     | AN00                      | D0              |
| 89              | 87 |             | P107 | $\overline{\text{KI3}}$  |           |                 |                     | AN7                       |                 |
| 90              | 88 |             | P106 | $\overline{\text{KI2}}$  |           |                 |                     | AN6                       |                 |
| 91              | 89 |             | P105 | $\overline{\text{KI1}}$  |           |                 |                     | AN5                       |                 |
| 92              | 90 |             | P104 | $\overline{\text{KI0}}$  |           |                 |                     | AN4                       |                 |
| 93              | 91 |             | P103 |                          |           |                 |                     | AN3                       |                 |
| 94              | 92 |             | P102 |                          |           |                 |                     | AN2                       |                 |
| 95              | 93 |             | P101 |                          |           |                 |                     | AN1                       |                 |
| 96              | 94 | AVss        |      |                          |           |                 |                     |                           |                 |
| 97              | 95 |             | P100 |                          |           |                 |                     | AN0                       |                 |
| 98              | 96 | VREF        |      |                          |           |                 |                     |                           |                 |
| 99              | 97 | AVcc        |      |                          |           |                 |                     |                           |                 |
| 100             | 98 |             | P97  |                          |           | RxD4/SCL4/STxD4 |                     | $\overline{\text{ADTRG}}$ |                 |

## NOTES:

1. Bus control pins in M32C/84T cannot be used.

## 1.6 Pin Description

**Table 1.6 Pin Description (100-Pin and 144-Pin Packages)**

| Classification   | Symbol                      | I/O Type | Supply Voltage  | Function  |
|--|-----------------------------|----------|---|---|
| Power Supply   | VCC1, VCC2<br>VSS           | I        | –   | Apply 3.0 to 5.5V to both VCC1 and VCC2 pins. Apply 0V to the VSS pin. $VCC1 \geq VCC2^{(1, 2)}$  |
| Analog Power Supply                                    | AVCC<br>AVSS                | I        | VCC1  | Supplies power to the A/D converter. Connect the AVCC pin to VCC1 and the AVSS pin to VSS   |
| Reset Input  | RESET                       | I        | VCC1  | The microcomputer is in a reset state when "L" is applied to the RESET pin  |
| CNVSS  | CNVSS                       | I        | VCC1  | Switches processor mode. Connect the CNVSS pin to VSS to start up in single-chip mode or to VCC1 to start up in microprocessor mode   |
| Input to Switch External Data Bus Width <sup>(3)</sup> | BYTE                        | I        | VCC1  | Switches data bus width in external memory space 3. The data bus is 16 bits wide when the BYTE pin is held "L" and 8 bits wide when it is held "H". Set to either. Connect the BYTE pin to VSS to use the microcomputer in single-chip mode   |
| Bus Control Pins <sup>(3)</sup>                        | D0 to D7                    | I/O      | VCC2  | Inputs and outputs data (D0 to D7) while accessing an external memory space with separate bus   |
|  | D8 to D15                   | I/O      | VCC2  | Inputs and outputs data (D8 to D15) while accessing an external memory space with 16-bit separate bus   |
|  | A0 to A22                   | O        | VCC2  | Outputs address bits A0 to A22  |
|  | A $\bar{23}$                | O        | VCC2  | Outputs inversed address bit A23  |
|  | A0/D0 to A7/D7              | I/O      | VCC2  | Inputs and outputs data (D0 to D7) and outputs 8 low-order address bits (A0 to A7) by time-sharing while accessing an external memory space with multiplexed bus  |
|  | A8/D8 to A15/D15            | I/O      | VCC2  | Inputs and outputs data (D8 to D15) and outputs 8 middle-order address bits (A8 to A15) by time-sharing while accessing an external memory space with 16-bit multiplexed bus  |
|  | CS0 to CS3                  | O        | VCC2  | Outputs CS0 to CS3 that are chip-select signals specifying an external space  |
|  | WRL / WR<br>WRH / BHE<br>RD | O        | VCC2  | Outputs WRL, WRH, (WR, BHE) and RD signals. WRL and WRH can be switched with WR and BHE by program<br><ul style="list-style-type: none"> <li>■ WRL, WRH and RD selected:<br/>If external data bus is 16 bits wide, data is written to an even address in external memory space when WRL is held "L".<br/>Data is written to an odd address when WRH is held "L".<br/>Data is read when RD is held "L".</li> <li>■ WR, BHE and RD selected:<br/>Data is written to external memory space when WR is held "L".<br/>Data in an external memory space is read when RD is held "L".<br/>An odd address is accessed when BHE is held "L".<br/>Select WR, BHE and RD for external 8-bit data bus.</li> </ul> |
|  | ALE                         | O        | VCC2  | ALE is a signal latching the address  |
|  | HOLD                        | I        | VCC2  | The microcomputer is placed in a hold state while the HOLD pin is held "L"  |
| HLDA   | O                           | VCC2     | Outputs an "L" signal while the microcomputer is placed in a hold state |   |
| RDY  | I                           | VCC2     | Bus is placed in a wait state while the RDY pin is held "L"             |   |

I : Input    O : Output    I/O : Input and output

**NOTES:**

1. VCC1 is hereinafter referred to as VCC unless otherwise noted.
2. Apply 4.2 to 5.5V to the VCC1 and VCC2 pins when using M32C/84T.  $VCC1=VCC2$ .
3. Bus control pins in M32C/84T cannot be used.

**Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)**

| Classification                         | Symbol                                     | I/O Type | Supply Voltage | Function  |
|--|--|----------|----------------|---|
| Main Clock Input                       | XIN  | I        | VCC1           | I/O pins for the main clock oscillation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. To apply external clock, apply it to XIN and leave XOUT open |
| Main Clock Output                      | XOUT                                       | O        | VCC1           |   |
| Sub Clock Input                        | XCIN                                       | I        | VCC1           | I/O pins for the sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT. To apply external clock, apply it to XCIN and leave XCOUT open                   |
| Sub Clock Output                       | XCOUT                                      | O        | VCC1           |   |
| BCLK Output <sup>(1)</sup>             | BCLK                                       | O        | VCC2           | Outputs BCLK signal   |
| Clock Output                           | CLKOUT                                     | O        | VCC2           | Outputs the clock having the same frequency as fc, f8 or f32  |
| INT Interrupt Input                    | INT0 to INT2                               | I        | VCC1           | Input pins for the INT interrupt  |
|  | INT3 to INT5                               | I        | VCC2           |   |
| NMI Interrupt Input                    | NMI  | I        | VCC1           | Input pin for the NMI interrupt   |
| Key Input Interrupt                    | KI0 to KI3                                 | I        | VCC1           | Input pins for the key input interrupt  |
| Timer A                                | TA0OUT to TA4OUT                           | I/O      | VCC1           | I/O pins for the timer A0 to A4 (TA0OUT is a pin for the N-channel open drain output.)  |
|  | TA0IN to TA4IN                             | I        | VCC1           | Input pins for the timer A0 to A4   |
| Timer B                                | TB0IN to TB5IN                             | I        | VCC1           | Input pins for the timer B0 to B5   |
| Three-phase Motor Control Timer Output | U, $\bar{U}$ , V, $\bar{V}$ , W, $\bar{W}$ | O        | VCC1           | Output pins for the three-phase motor control timer   |
| Serial I/O                             | CTS0 to CTS4                               | I        | VCC1           | Input pins for data transmission control  |
|  | RTS0 to RTS4                               | O        | VCC1           | Output pins for data reception control  |
|  | CLK0 to CLK4                               | I/O      | VCC1           | Inputs and outputs the transfer clock   |
|  | RxD0 to RxD4                               | I        | VCC1           | Inputs serial data  |
|  | TxD0 to TxD4                               | O        | VCC1           | Outputs serial data (TxD2 is a pin for the N-channel open drain output.)  |
| I <sup>2</sup> C Mode                  | SDA0 to SDA4                               | I/O      | VCC1           | Inputs and outputs serial data (SDA2 is a pin for the N-channel open drain output.)   |
|  | SCL0 to SCL4                               | I/O      | VCC1           | Inputs and outputs the transfer clock (SCL2 is a pin for the N-channel open drain output.)  |
| Serial I/O Special Function            | STxD0 to STxD4                             | O        | VCC1           | Outputs serial data when slave mode is selected (STxD2 is a pin for the N-channel open drain output.)   |
|  | SRxD0 to SRxD4                             | I        | VCC1           | Inputs serial data when slave mode is selected  |
|  | SS0 to SS4                                 | I        | VCC1           | Input pins to control serial I/O special function   |
|  |  |          |                |   |

I : Input    O : Output    I/O : Input and output

## NOTES:

1. Bus control pins in M32C/84T cannot be used.



**Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)**

| Classification          | Symbol   | I/O Type | Supply Voltage           | Function  |
|-------------------------|--|----------|--------------------------|---|
| Reference Voltage Input | VREF   | I        | -                        | Applies reference voltage to the A/D converter and D/A converter  |
| A/D Converter           | AN0 to AN7<br>AN00 to AN07<br>AN20 to AN27                                       | I        | VCC1                     | Analog input pins for the A/D converter   |
|                         | ADTRG  | I        | VCC1                     | Input pin for an external A/D trigger   |
|                         | ANEX0  | I/O      | VCC1                     | Extended analog input pin for the A/D converter and output pin in external op-amp connection mode   |
|                         | ANEX1  | I        | VCC1                     | Extended analog input pin for the A/D converter   |
| D/A Converter           | DA0, DA1   | O        | VCC1                     | Output pin for the D/A converter  |
| Intelligent I/O         | INPC10 to INPC13   | I        | VCC1/VCC2 <sup>(1)</sup> | Input pins for the time measurement function  |
|                         | INPC14 to INPC17   | I        | VCC1                     |   |
|                         | OUTC10 to OUTC13   | O        | VCC1/VCC2 <sup>(1)</sup> | Output pins for the waveform generating function<br>(OUTC16 and OUTC17 assigned to P70 and P71 are pins for the N-channel open drain output.)   |
|                         | OUTC14 to OUTC17   | O        | VCC1                     |   |
|                         | ISCLK0   | I/O      | VCC1                     | Inputs and outputs the clock for the intelligent I/O communication function   |
|                         | ISCLK1   | I/O      | VCC1/VCC2 <sup>(1)</sup> |   |
|                         | ISRXD0   | I        | VCC1                     | Inputs data for the intelligent I/O communication function  |
|                         | ISRXD1   | I        | VCC1/VCC2 <sup>(1)</sup> |   |
|                         | ISTXD0   | O        | VCC1                     | Outputs data for the intelligent I/O communication function   |
|                         | ISTXD1   | O        | VCC1/VCC2 <sup>(1)</sup> |   |
|                         | BE1IN  | I        | VCC1/VCC2 <sup>(1)</sup> | Inputs data for the intelligent I/O communication function  |
|                         | BE1OUT   | O        | VCC1/VCC2 <sup>(1)</sup> | Outputs data for the intelligent I/O communication function   |
| CAN                     | CAN0IN   | I        | VCC1                     | Input pin for the CAN communication function  |
|                         | CAN0OUT  | O        | VCC1                     | Output pin for the CAN communication function   |
| I/O Ports               | P00 to P07<br>P10 to P17<br>P20 to P27<br>P30 to P37<br>P40 to P47<br>P50 to P57 | I/O      | VCC2                     | I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resistor available in 4-bit units |
|                         | P60 to P67<br>P70 to P77<br>P90 to P97<br>P100 to P107                           | I/O      | VCC1                     | I/O ports having equivalent functions to P0<br>(P70 and P71 are ports for the N-channel open drain output.)   |
|                         | P80 to P84<br>P86, P87   | I/O      | VCC1                     | I/O ports having equivalent functions to P0   |
|                         | Input Port   | P85      | I                        | VCC1  |

I : Input    O : Output    I/O : Input and output

## NOTES:

1. VCC2 is not available in the 100-pin package. VCC1 only available.

**Table 1.6 Pin Description (144-Pin Package only) (Continued)**

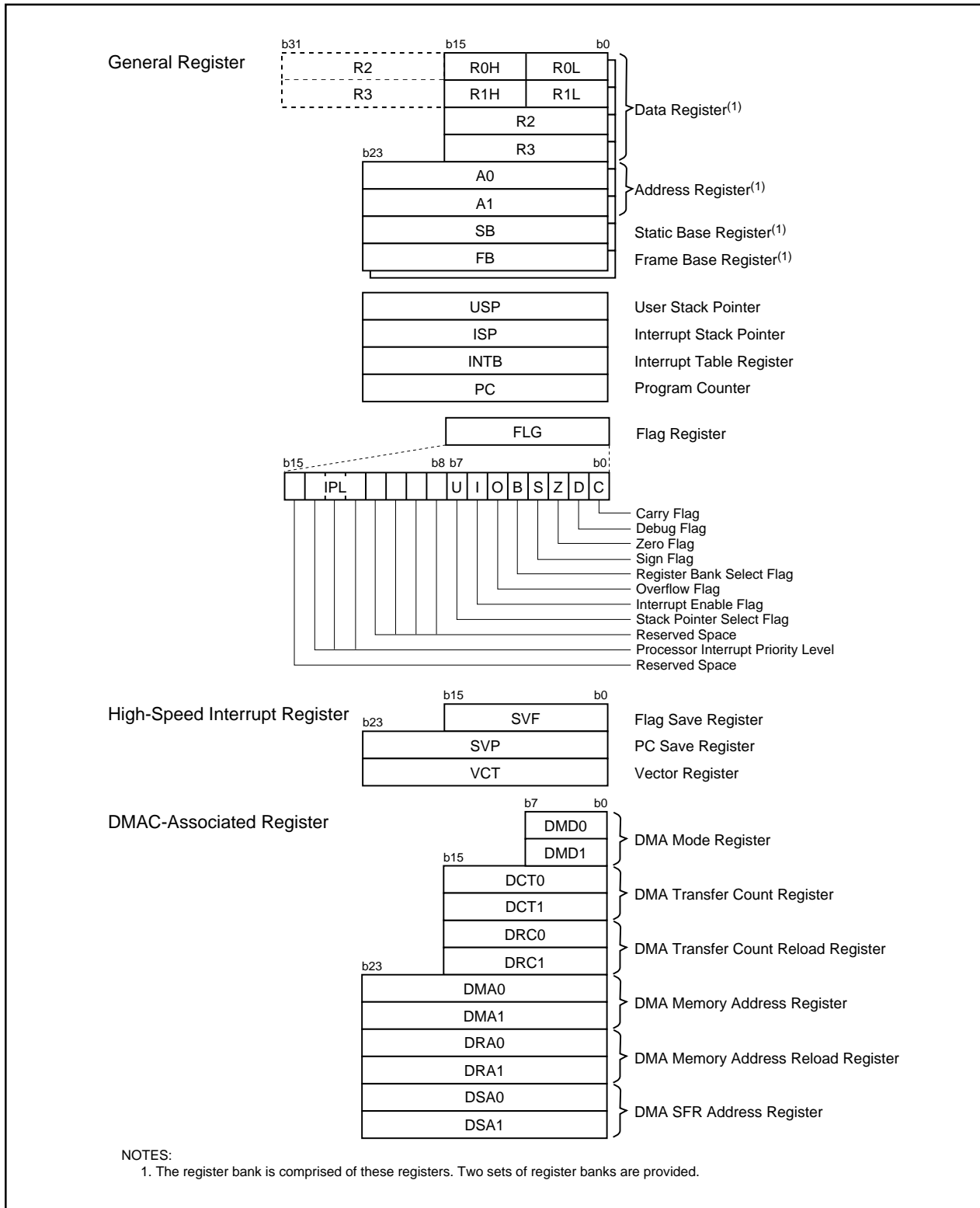
| Classification | Symbol                                       | I/O Type | Supply Voltage | Function                                    |
|----------------|--|----------|----------------|---|
| A/D Converter  | AN150 to AN157                               | I        | VCC1           | Analog input pins for the A/D converter     |
| I/O Ports      | P110 to P114<br>P120 to P127<br>P130 to P137 | I/O      | VCC2           | I/O ports having equivalent functions to P0 |
|                | P140 to P146<br>P150 to P157                 | I/O      | VCC1           | I/O ports having equivalent functions to P0 |

I : Input    O : Output    I/O : Input and output

## 2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers.

The register bank is comprised of 8 registers (R0, R1, R2, R3, A0, A1, SB and FB) out of 28 CPU registers. Two sets of register banks are provided.



**Figure 2.1 CPU Register**

## 2.1 General Registers

### 2.1.1 Data Registers (R0, R1, R2 and R3)

R0, R1, R2 and R3 are 16-bit registers for transfer, arithmetic and logic operations. R0 and R1 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R0 can be combined with R2 to be used as a 32-bit data register (R2R0). The same applies to R1 and R3.

### 2.1.2 Address Registers (A0 and A1)

A0 and A1 are 24-bit registers for A0-/A1-indirect addressing, A0-/A1-relative addressing, transfer, arithmetic and logic operations.

### 2.1.3 Static Base Register (SB)

SB is a 24-bit register for SB-relative addressing.

### 2.1.4 Frame Base Register (FB)

FB is a 24-bit register for FB-relative addressing.

### 2.1.5 Program Counter (PC)

PC, 24 bits wide, indicates the address of an instruction to be executed.

### 2.1.6 Interrupt Table Register (INTB)

INTB is a 24-bit register indicating the starting address of an relocatable interrupt vector table.

### 2.1.7 User Stack Pointer (USP), Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are 24 bits wide each. The U flag is used to switch between USP and ISP. Refer to **2.1.8 Flag Register (FLG)** for details on the U flag. Set USP and ISP to even addresses to execute an interrupt sequence efficiently.

### 2.1.8 Flag Register (FLG)

FLG is a 16-bit register indicating a CPU state.

#### 2.1.8.1 Carry Flag (C)

The C flag indicates whether carry or borrow has occurred after executing an instruction.

#### 2.1.8.2 Debug Flag (D)

The D flag is for debug only. Set to "0".

#### 2.1.8.3 Zero Flag (Z)

The Z flag is set to "1" when the value of zero is obtained from an arithmetic operation; otherwise "0".

#### 2.1.8.4 Sign Flag (S)

The S flag is set to "1" when a negative value is obtained from an arithmetic operation; otherwise "0".

### 2.1.8.5 Register Bank Select Flag (B)

The register bank 0 is selected when the B flag is set to "0". The register bank 1 is selected when this flag is set to "1".

### 2.1.8.6 Overflow Flag (O)

The O flag is set to "1" when the result of an arithmetic operation overflows; otherwise "0".

### 2.1.8.7 Interrupt Enable Flag (I)

The I flag enables a maskable interrupt.

Interrupt is disabled when the I flag is set to "0" and enabled when the I flag is set to "1". The I flag is set to "0" when an interrupt is acknowledged.

### 2.1.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to "0". USP is selected when this flag is set to "1".

The U flag is set to "0" when a hardware interrupt is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

### 2.1.8.9 Processor Interrupt Priority Level (IPL)

IPL, 3 bits wide, assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has greater priority than IPL, the interrupt is enabled.

### 2.1.8.10 Reserved Space

When writing to a reserved space, set to "0". When reading, its content is indeterminate.

## 2.2 High-Speed Interrupt Registers

Registers associated with the high-speed interrupt are as follows:

- Flag save register (SVF)
- PC save register (SVP)
- Vector register (VCT)

## 2.3 DMAC-Associated Registers

Registers associated with DMAC are as follows:

- DMA mode register (DMD0, DMD1)
- DMA transfer count register (DCT0, DCT1)
- DMA transfer count reload register (DRC0, DRC1)
- DMA memory address register (DMA0, DMA1)
- DMA SFR address register (DSA0, DSA1)
- DMA memory address reload register (DRA0, DRA1)

### 3. Memory

Figure 3.1 shows a memory map of the M32C/84 group (M32C/84, M32C/84T).

The M32C/84 group (M32C/84, M32C/84T) provides 16-Mbyte address space from addresses  $000000_{16}$  to  $FFFFFF_{16}$ .

The internal ROM is allocated lower addresses beginning with address  $FFFFFF_{16}$ . For example, a 64-Kbyte internal ROM is allocated in addresses  $FF0000_{16}$  to  $FFFFFF_{16}$ .

The fixed interrupt vectors are allocated addresses  $FFFFDC_{16}$  to  $FFFFFF_{16}$ . It stores the starting address of each interrupt routine.

The internal RAM is allocated higher addresses beginning with address  $000400_{16}$ . For example, a 10-Kbyte internal RAM is allocated addresses  $000400_{16}$  to  $002BFF_{16}$ . Besides storing data, it becomes stacks when the subroutine is called or an interrupt is acknowledged.

SFR, consisting of control registers for peripheral functions such as I/O port, A/D converter, serial I/O, and timers, is allocated addresses  $000000_{16}$  to  $0003FF_{16}$ . All blank spaces within SFR are reserved and cannot be accessed by users.

The special page vectors are allocated addresses  $FFFE00_{16}$  to  $FFFFDB_{16}$ . It is used for the JMPS instruction and JSRS instruction. Refer to the Renesas publication **M32C/80 Series Software Manual** for details. In memory expansion mode and microprocessor mode, some spaces are reserved and cannot be accessed by users.

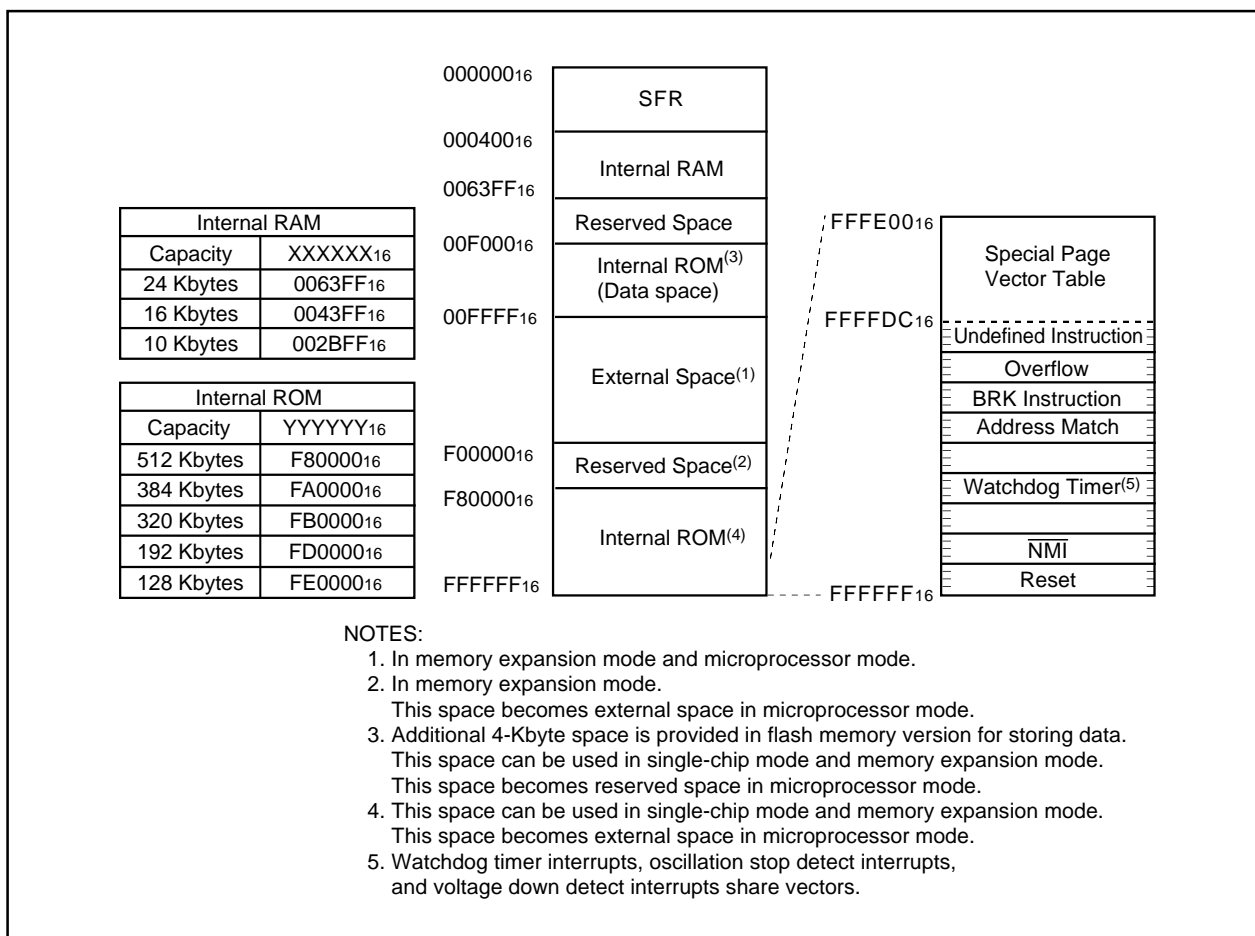


Figure 3.1 Memory Map

## 4. Special Function Registers (SFR)

| Address            | Register   | Symbol | Value after RESET  |
|--------------------|--|--------|--|
| 0000 <sub>16</sub> |  |        |  |
| 0001 <sub>16</sub> |  |        |  |
| 0002 <sub>16</sub> |  |        |  |
| 0003 <sub>16</sub> |  |        |  |
| 0004 <sub>16</sub> | Processor Mode Register 0 <sup>(1)</sup>                 | PM0    | 1000 0000 <sub>2</sub> (CNVss pin ="L")<br>0000 0011 <sub>2</sub> (CNVss pin ="H") |
| 0005 <sub>16</sub> | Processor Mode Register 1                                | PM1    | 00 <sub>16</sub>   |
| 0006 <sub>16</sub> | System Clock Control Register 0                          | CM0    | 0000 1000 <sub>2</sub>   |
| 0007 <sub>16</sub> | System Clock Control Register 1                          | CM1    | 0010 0000 <sub>2</sub>   |
| 0008 <sub>16</sub> |  |        |  |
| 0009 <sub>16</sub> | Address Match Interrupt Enable Register                  | AIER   | 00 <sub>16</sub>   |
| 000A <sub>16</sub> | Protect Register   | PRCR   | XXXX 0000 <sub>2</sub>   |
| 000B <sub>16</sub> | External Data Bus Width Control Register <sup>(2)</sup>  | DS     | XXXX 1000 <sub>2</sub> (BYTE pin ="L")<br>XXXX 0000 <sub>2</sub> (BYTE pin ="H")   |
| 000C <sub>16</sub> | Main Clock Division Register                             | MCD    | XXX0 1000 <sub>2</sub>   |
| 000D <sub>16</sub> | Oscillation Stop Detection Register                      | CM2    | 00 <sub>16</sub>   |
| 000E <sub>16</sub> | Watchdog Timer Start Register                            | WDTS   | XX <sub>16</sub>   |
| 000F <sub>16</sub> | Watchdog Timer Control Register                          | WDC    | 000X XXXX <sub>2</sub>   |
| 0010 <sub>16</sub> |  |        |  |
| 0011 <sub>16</sub> |  |        |  |
| 0012 <sub>16</sub> | Address Match Interrupt Register 0                       | RMAD0  | 000000 <sub>16</sub>   |
| 0013 <sub>16</sub> | Processor Mode Register 2                                | PM2    | 00 <sub>16</sub>   |
| 0014 <sub>16</sub> |  |        |  |
| 0015 <sub>16</sub> |  |        |  |
| 0016 <sub>16</sub> | Address Match Interrupt Register 1                       | RMAD1  | 000000 <sub>16</sub>   |
| 0017 <sub>16</sub> | Voltage Detection Register 2 <sup>(2)</sup>              | VCR2   | 00 <sub>16</sub>   |
| 0018 <sub>16</sub> |  |        |  |
| 0019 <sub>16</sub> |  |        |  |
| 001A <sub>16</sub> | Address Match Interrupt Register 2                       | RMAD2  | 000000 <sub>16</sub>   |
| 001B <sub>16</sub> | Voltage Detection Register 1 <sup>(2)</sup>              | VCR1   | 0000 1000 <sub>2</sub>   |
| 001C <sub>16</sub> |  |        |  |
| 001D <sub>16</sub> |  |        |  |
| 001E <sub>16</sub> | Address Match Interrupt Register 3                       | RMAD3  | 000000 <sub>16</sub>   |
| 001F <sub>16</sub> |  |        |  |
| 0020 <sub>16</sub> |  |        |  |
| 0021 <sub>16</sub> |  |        |  |
| 0022 <sub>16</sub> |  |        |  |
| 0023 <sub>16</sub> |  |        |  |
| 0024 <sub>16</sub> |  |        |  |
| 0025 <sub>16</sub> |  |        |  |
| 0026 <sub>16</sub> | PLL Control Register 0                                   | PLC0   | 0001 X010 <sub>2</sub>   |
| 0027 <sub>16</sub> | PLL Control Register 1                                   | PLC1   | 000X 0000 <sub>2</sub>   |
| 0028 <sub>16</sub> |  |        |  |
| 0029 <sub>16</sub> |  |        |  |
| 002A <sub>16</sub> | Address Match Interrupt Register 4                       | RMAD4  | 000000 <sub>16</sub>   |
| 002B <sub>16</sub> |  |        |  |
| 002C <sub>16</sub> |  |        |  |
| 002D <sub>16</sub> |  |        |  |
| 002E <sub>16</sub> | Address Match Interrupt Register 5                       | RMAD5  | 000000 <sub>16</sub>   |
| 002F <sub>16</sub> | Voltage Down Detection Interrupt Register <sup>(2)</sup> | D4INT  | 00 <sub>16</sub>   |

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The PM01 and PM00 bits in the PM1 register maintain values set before reset even if software reset or watchdog timer reset is performed.
2. These registers in M32C/84T cannot be used.

| Address  | Register  | Symbol | Value after RESET  |
|--|---|--------|--|
| 0030 <sub>16</sub>   |   |        |  |
| 0031 <sub>16</sub>   |   |        |  |
| 0032 <sub>16</sub>   |   |        |  |
| 0033 <sub>16</sub>   |   |        |  |
| 0034 <sub>16</sub>   |   |        |  |
| 0035 <sub>16</sub>   |   |        |  |
| 0036 <sub>16</sub>   |   |        |  |
| 0037 <sub>16</sub>   |   |        |  |
| 0038 <sub>16</sub><br>0039 <sub>16</sub><br>003A <sub>16</sub> | Address Match Interrupt Register 6                    | RMAD6  | 000000 <sub>16</sub>   |
| 003B <sub>16</sub>   |   |        |  |
| 003C <sub>16</sub><br>003D <sub>16</sub><br>003E <sub>16</sub> | Address Match Interrupt Register 7                    | RMAD7  | 000000 <sub>16</sub>   |
| 003F <sub>16</sub>   |   |        |  |
| 0040 <sub>16</sub>   |   |        |  |
| 0041 <sub>16</sub>   |   |        |  |
| 0042 <sub>16</sub>   |   |        |  |
| 0043 <sub>16</sub>   |   |        |  |
| 0044 <sub>16</sub>   |   |        |  |
| 0045 <sub>16</sub>   |   |        |  |
| 0046 <sub>16</sub>   |   |        |  |
| 0047 <sub>16</sub>   |   |        |  |
| 0048 <sub>16</sub>   | External Space Wait Control Register 0 <sup>(1)</sup> | EWCR0  | X0X0 0011 <sub>2</sub>   |
| 0049 <sub>16</sub>   | External Space Wait Control Register 1 <sup>(1)</sup> | EWCR1  | X0X0 0011 <sub>2</sub>   |
| 004A <sub>16</sub>   | External Space Wait Control Register 2 <sup>(1)</sup> | EWCR2  | X0X0 0011 <sub>2</sub>   |
| 004B <sub>16</sub>   | External Space Wait Control Register 3 <sup>(1)</sup> | EWCR3  | X0X0 0011 <sub>2</sub>   |
| 004C <sub>16</sub>   | Page Mode Wait Control Register 0 <sup>(2)</sup>      | PWCR0  | 0001 0001 <sub>2</sub>   |
| 004D <sub>16</sub>   | Page Mode Wait Control Register 1 <sup>(2)</sup>      | PWCR1  | 0001 0001 <sub>2</sub>   |
| 004E <sub>16</sub>   |   |        |  |
| 004F <sub>16</sub>   |   |        |  |
| 0050 <sub>16</sub>   |   |        |  |
| 0051 <sub>16</sub>   |   |        |  |
| 0052 <sub>16</sub>   |   |        |  |
| 0053 <sub>16</sub>   |   |        |  |
| 0054 <sub>16</sub>   |   |        |  |
| 0055 <sub>16</sub>   | Flash Memory Control Register 1                       | FMR1   | 0000 0101 <sub>2</sub>   |
| 0056 <sub>16</sub>   |   |        |  |
| 0057 <sub>16</sub>   | Flash Memory Control Register 0                       | FMRO   | 0000 0001 <sub>2</sub> (Flash memory version)<br>XXXX XXX0 <sub>2</sub> (Masked ROM version) |
| 0058 <sub>16</sub>   |   |        |  |
| 0059 <sub>16</sub>   |   |        |  |
| 005A <sub>16</sub>   |   |        |  |
| 005B <sub>16</sub>   |   |        |  |
| 005C <sub>16</sub>   |   |        |  |
| 005D <sub>16</sub>   |   |        |  |
| 005E <sub>16</sub>   |   |        |  |
| 005F <sub>16</sub>   |   |        |  |

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. These registers in M32C/84T cannot be used.
2. These registers can be used only in the ROMless version.



| Address            | Register   | Symbol            | Value after RESET |
|--------------------|--|-------------------|-------------------|
| 0060 <sub>16</sub> |  |                   |                   |
| 0061 <sub>16</sub> |  |                   |                   |
| 0062 <sub>16</sub> |  |                   |                   |
| 0063 <sub>16</sub> |  |                   |                   |
| 0064 <sub>16</sub> |  |                   |                   |
| 0065 <sub>16</sub> |  |                   |                   |
| 0066 <sub>16</sub> |  |                   |                   |
| 0067 <sub>16</sub> |  |                   |                   |
| 0068 <sub>16</sub> | DMA0 Interrupt Control Register  | DM0IC             | XXXX X0002        |
| 0069 <sub>16</sub> | Timer B5 Interrupt Control Register  | TB5IC             | XXXX X0002        |
| 006A <sub>16</sub> | DMA2 Interrupt Control Register  | DM2IC             | XXXX X0002        |
| 006B <sub>16</sub> | UART2 Receive /ACK Interrupt Control Register                                      | S2RIC             | XXXX X0002        |
| 006C <sub>16</sub> | Timer A0 Interrupt Control Register  | TA0IC             | XXXX X0002        |
| 006D <sub>16</sub> | UART3 Receive /ACK Interrupt Control Register                                      | S3RIC             | XXXX X0002        |
| 006E <sub>16</sub> | Timer A2 Interrupt Control Register  | TA2IC             | XXXX X0002        |
| 006F <sub>16</sub> | UART4 Receive /ACK Interrupt Control Register                                      | S4RIC             | XXXX X0002        |
| 0070 <sub>16</sub> | Timer A4 Interrupt Control Register  | TA4IC             | XXXX X0002        |
| 0071 <sub>16</sub> | UART0/UART3 Bus Conflict Detect Interrupt Control Register                         | BCN0IC/BCN3IC     | XXXX X0002        |
| 0072 <sub>16</sub> | UART0 Receive/ACK Interrupt Control Register                                       | S0RIC             | XXXX X0002        |
| 0073 <sub>16</sub> | A/D0 Conversion Interrupt Control Register   | AD0IC             | XXXX X0002        |
| 0074 <sub>16</sub> | UART1 Receive/ACK Interrupt Control Register                                       | S1RIC             | XXXX X0002        |
| 0075 <sub>16</sub> | Intelligent I/O Interrupt Control Register 0                                       | IIO0IC            | XXXX X0002        |
| 0076 <sub>16</sub> | Timer B1 Interrupt Control Register  | TB1IC             | XXXX X0002        |
| 0077 <sub>16</sub> | Intelligent I/O Interrupt Control Register 2                                       | IIO2IC            | XXXX X0002        |
| 0078 <sub>16</sub> | Timer B3 Interrupt Control Register  | TB3IC             | XXXX X0002        |
| 0079 <sub>16</sub> | Intelligent I/O Interrupt Control Register 4                                       | IIO4IC            | XXXX X0002        |
| 007A <sub>16</sub> | INT5 Interrupt Control Register  | INT5IC            | XX00 X0002        |
| 007B <sub>16</sub> |  |                   |                   |
| 007C <sub>16</sub> | INT3 Interrupt Control Register  | INT3IC            | XX00 X0002        |
| 007D <sub>16</sub> | Intelligent I/O Interrupt Control Register 8                                       | IIO8IC            | XXXX X0002        |
| 007E <sub>16</sub> | INT1 Interrupt Control Register  | INT1IC            | XX00 X0002        |
| 007F <sub>16</sub> | Intelligent I/O Interrupt Control Register 10/<br>CAN Interrupt 1 Control Register | IIO10IC<br>CAN1IC | XXXX X0002        |
| 0080 <sub>16</sub> |  |                   |                   |
| 0081 <sub>16</sub> | CAN Interrupt 2 Control Register   | CAN2IC            | XXXX X0002        |
| 0082 <sub>16</sub> |  |                   |                   |
| 0083 <sub>16</sub> |  |                   |                   |
| 0084 <sub>16</sub> |  |                   |                   |
| 0085 <sub>16</sub> |  |                   |                   |
| 0086 <sub>16</sub> |  |                   |                   |
| 0087 <sub>16</sub> |  |                   |                   |
| 0088 <sub>16</sub> | DMA1 Interrupt Control Register  | DM1IC             | XXXX X0002        |
| 0089 <sub>16</sub> | UART2 Transmit /NACK Interrupt Control Register                                    | S2TIC             | XXXX X0002        |
| 008A <sub>16</sub> | DMA3 Interrupt Control Register  | DM3IC             | XXXX X0002        |
| 008B <sub>16</sub> | UART3 Transmit /NACK Interrupt Control Register                                    | S3TIC             | XXXX X0002        |
| 008C <sub>16</sub> | Timer A1 Interrupt Control Register  | TA1IC             | XXXX X0002        |
| 008D <sub>16</sub> | UART4 Transmit /NACK Interrupt Control Register                                    | S4TIC             | XXXX X0002        |
| 008E <sub>16</sub> | Timer A3 Interrupt Control Register  | TA3IC             | XXXX X0002        |
| 008F <sub>16</sub> | UART2 Bus Conflict Detect Interrupt Control Register                               | BCN2IC            | XXXX X0002        |

X: Indeterminate

Blank spaces are reserved. No access is allowed.

| Address            | Register  | Symbol           | Value after RESET |
|--------------------|---|------------------|-------------------|
| 0090 <sub>16</sub> | UART0 Transmit /NACK Interrupt Control Register                                   | S0TIC            | XXXX X0002        |
| 0091 <sub>16</sub> | UART1/UART4 Bus Conflict Detect Interrupt Control Register                        | BCN1IC/BCN4IC    | XXXX X0002        |
| 0092 <sub>16</sub> | UART1 Transmit/NACK Interrupt Control Register                                    | S1TIC            | XXXX X0002        |
| 0093 <sub>16</sub> | Key Input Interrupt Control Register  | KUPIC            | XXXX X0002        |
| 0094 <sub>16</sub> | Timer B0 Interrupt Control Register   | TB0IC            | XXXX X0002        |
| 0095 <sub>16</sub> | Intelligent I/O Interrupt Control Register 1                                      | IIO1IC           | XXXX X0002        |
| 0096 <sub>16</sub> | Timer B2 Interrupt Control Register   | TB2IC            | XXXX X0002        |
| 0097 <sub>16</sub> | Intelligent I/O Interrupt Control Register 3                                      | IIO3IC           | XXXX X0002        |
| 0098 <sub>16</sub> | Timer B4 Interrupt Control Register   | TB4IC            | XXXX X0002        |
| 0099 <sub>16</sub> |   |                  |                   |
| 009A <sub>16</sub> | INT4 Interrupt Control Register   | INT4IC           | XX00 X0002        |
| 009B <sub>16</sub> |   |                  |                   |
| 009C <sub>16</sub> | INT2 Interrupt Control Register   | INT2IC           | XX00 X0002        |
| 009D <sub>16</sub> | Intelligent I/O Interrupt Control Register 9/<br>CAN Interrupt 0 Control Register | IIO9IC<br>CAN0IC | XXXX X0002        |
| 009E <sub>16</sub> | INT0 Interrupt Control Register   | INT0IC           | XX00 X0002        |
| 009F <sub>16</sub> | Exit Priority Control Register  | RLVL             | XXXX 00002        |
| 00A0 <sub>16</sub> | Interrupt Request Register 0  | IIO0IR           | 0000 000X2        |
| 00A1 <sub>16</sub> | Interrupt Request Register 1  | IIO1IR           | 0000 000X2        |
| 00A2 <sub>16</sub> | Interrupt Request Register 2  | IIO2IR           | 0000 000X2        |
| 00A3 <sub>16</sub> | Interrupt Request Register 3  | IIO3IR           | 0000 000X2        |
| 00A4 <sub>16</sub> | Interrupt Request Register 4  | IIO4IR           | 0000 000X2        |
| 00A5 <sub>16</sub> |   |                  |                   |
| 00A6 <sub>16</sub> |   |                  |                   |
| 00A7 <sub>16</sub> |   |                  |                   |
| 00A8 <sub>16</sub> | Interrupt Request Register 8  | IIO8IR           | 0000 000X2        |
| 00A9 <sub>16</sub> | Interrupt Request Register 9  | IIO9IR           | 0000 000X2        |
| 00AA <sub>16</sub> | Interrupt Request Register 10   | IIO10IR          | 0000 000X2        |
| 00AB <sub>16</sub> | Interrupt Request Register 11   | IIO11IR          | 0000 000X2        |
| 00AC <sub>16</sub> |   |                  |                   |
| 00AD <sub>16</sub> |   |                  |                   |
| 00AE <sub>16</sub> |   |                  |                   |
| 00AF <sub>16</sub> |   |                  |                   |
| 00B0 <sub>16</sub> | Interrupt Enable Register 0   | IIO0IE           | 00 <sub>16</sub>  |
| 00B1 <sub>16</sub> | Interrupt Enable Register 1   | IIO1IE           | 00 <sub>16</sub>  |
| 00B2 <sub>16</sub> | Interrupt Enable Register 2   | IIO2IE           | 00 <sub>16</sub>  |
| 00B3 <sub>16</sub> | Interrupt Enable Register 3   | IIO3IE           | 00 <sub>16</sub>  |
| 00B4 <sub>16</sub> | Interrupt Enable Register 4   | IIO4IE           | 00 <sub>16</sub>  |
| 00B5 <sub>16</sub> |   |                  |                   |
| 00B6 <sub>16</sub> |   |                  |                   |
| 00B7 <sub>16</sub> |   |                  |                   |
| 00B8 <sub>16</sub> | Interrupt Enable Register 8   | IIO8IE           | 00 <sub>16</sub>  |
| 00B9 <sub>16</sub> | Interrupt Enable Register 9   | IIO9IE           | 00 <sub>16</sub>  |
| 00BA <sub>16</sub> | Interrupt Enable Register 10  | IIO10IE          | 00 <sub>16</sub>  |
| 00BB <sub>16</sub> | Interrupt Enable Register 11  | IIO11IE          | 00 <sub>16</sub>  |
| 00BC <sub>16</sub> |   |                  |                   |
| 00BD <sub>16</sub> |   |                  |                   |
| 00BE <sub>16</sub> |   |                  |                   |
| 00BF <sub>16</sub> |   |                  |                   |

X: Indeterminate

Blank spaces are reserved. No access is allowed.

| Address                                  | Register                                | Symbol    | Value after RESET                                |
|--|---|-----------|--|
| 00C0 <sub>16</sub>                       |   |           |  |
| 00C1 <sub>16</sub>                       |   |           |  |
| 00C2 <sub>16</sub>                       |   |           |  |
| 00C3 <sub>16</sub>                       |   |           |  |
| 00C4 <sub>16</sub>                       |   |           |  |
| 00C5 <sub>16</sub>                       |   |           |  |
| 00C6 <sub>16</sub>                       |   |           |  |
| 00C7 <sub>16</sub>                       |   |           |  |
| 00C8 <sub>16</sub>                       |   |           |  |
| 00C9 <sub>16</sub>                       |   |           |  |
| 00CA <sub>16</sub>                       |   |           |  |
| 00CB <sub>16</sub>                       |   |           |  |
| 00CC <sub>16</sub>                       |   |           |  |
| 00CD <sub>16</sub>                       |   |           |  |
| 00CE <sub>16</sub>                       |   |           |  |
| 00CF <sub>16</sub>                       |   |           |  |
| 00D0 <sub>16</sub>                       |   |           |  |
| 00D1 <sub>16</sub>                       |   |           |  |
| 00D2 <sub>16</sub>                       |   |           |  |
| 00D3 <sub>16</sub>                       |   |           |  |
| 00D4 <sub>16</sub>                       |   |           |  |
| 00D5 <sub>16</sub>                       |   |           |  |
| 00D6 <sub>16</sub>                       |   |           |  |
| 00D7 <sub>16</sub>                       |   |           |  |
| 00D8 <sub>16</sub>                       |   |           |  |
| 00D9 <sub>16</sub>                       |   |           |  |
| 00DA <sub>16</sub>                       |   |           |  |
| 00DB <sub>16</sub>                       |   |           |  |
| 00DC <sub>16</sub>                       |   |           |  |
| 00DD <sub>16</sub>                       |   |           |  |
| 00DE <sub>16</sub>                       |   |           |  |
| 00DF <sub>16</sub>                       |   |           |  |
| 00E0 <sub>16</sub>                       |   |           |  |
| 00E1 <sub>16</sub>                       |   |           |  |
| 00E2 <sub>16</sub>                       |   |           |  |
| 00E3 <sub>16</sub>                       |   |           |  |
| 00E4 <sub>16</sub>                       |   |           |  |
| 00E5 <sub>16</sub>                       |   |           |  |
| 00E6 <sub>16</sub>                       |   |           |  |
| 00E7 <sub>16</sub>                       |   |           |  |
| 00E8 <sub>16</sub><br>00E9 <sub>16</sub> | SI/O Receive Buffer Register 0          | G0RB      | XXXX XXXX <sub>2</sub><br>X000 XXXX <sub>2</sub> |
| 00EA <sub>16</sub><br>00EB <sub>16</sub> | Transmit Buffer/Receive Data Register 0 | G0TB/G0DR | XX <sub>16</sub>                                 |
| 00EC <sub>16</sub>                       | Receive Input Register 0                | G0RI      | XX <sub>16</sub>                                 |
| 00ED <sub>16</sub>                       | SI/O Communication Mode Register 0      | G0MR      | 00 <sub>16</sub>                                 |
| 00EE <sub>16</sub>                       | Transmit Output Register 0              | G0TO      | XX <sub>16</sub>                                 |
| 00EF <sub>16</sub>                       | SI/O Communication Control Register 0   | G0CR      | 0000 X011 <sub>2</sub>                           |

X: Indeterminate

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| Address                                  | Register   | Symbol      | Value after RESET                    |
|--|--|-------------|--------------------------------------|
| 00F0 <sub>16</sub>                       | Data Compare Register 00                               | G0CMP0      | XX <sub>16</sub>                     |
| 00F1 <sub>16</sub>                       | Data Compare Register 01                               | G0CMP1      | XX <sub>16</sub>                     |
| 00F2 <sub>16</sub>                       | Data Compare Register 02                               | G0CMP2      | XX <sub>16</sub>                     |
| 00F3 <sub>16</sub>                       | Data Compare Register 03                               | G0CMP3      | XX <sub>16</sub>                     |
| 00F4 <sub>16</sub>                       | Data Mask Register 00                                  | G0MSK0      | XX <sub>16</sub>                     |
| 00F5 <sub>16</sub>                       | Data Mask Register 01                                  | G0MSK1      | XX <sub>16</sub>                     |
| 00F6 <sub>16</sub>                       | Communication Clock Select Register                    | CCS         | XXXX 0000 <sub>2</sub>               |
| 00F7 <sub>16</sub>                       |  |             |                                      |
| 00F8 <sub>16</sub><br>00F9 <sub>16</sub> | Receive CRC Code Register 0                            | G0RCRC      | XX <sub>16</sub><br>XX <sub>16</sub> |
| 00FA <sub>16</sub><br>00FB <sub>16</sub> | Transmit CRC Code Register 0                           | G0TCRC      | 00 <sub>16</sub><br>00 <sub>16</sub> |
| 00FC <sub>16</sub>                       | SI/O Extended Mode Register 0                          | G0EMR       | 00 <sub>16</sub>                     |
| 00FD <sub>16</sub>                       | SI/O Extended Receive Control Register 0               | G0ERC       | 00 <sub>16</sub>                     |
| 00FE <sub>16</sub>                       | SI/O Special Communication Interrupt Detect Register 0 | G0IRF       | 00 <sub>16</sub>                     |
| 00FF <sub>16</sub>                       | SI/O Extended Transmit Control Register 0              | G0ETC       | 0000 0XXX <sub>2</sub>               |
| 0100 <sub>16</sub><br>0101 <sub>16</sub> | Time Measurement/Waveform Generating Register 10       | G1TM0/G1PO0 | XX <sub>16</sub><br>XX <sub>16</sub> |
| 0102 <sub>16</sub><br>0103 <sub>16</sub> | Time Measurement/Waveform Generating Register 11       | G1TM1/G1PO1 | XX <sub>16</sub><br>XX <sub>16</sub> |
| 0104 <sub>16</sub><br>0105 <sub>16</sub> | Time Measurement/Waveform Generating Register 12       | G1TM2/G1PO2 | XX <sub>16</sub><br>XX <sub>16</sub> |
| 0106 <sub>16</sub><br>0107 <sub>16</sub> | Time Measurement/Waveform Generating Register 13       | G1TM3/G1PO3 | XX <sub>16</sub><br>XX <sub>16</sub> |
| 0108 <sub>16</sub><br>0109 <sub>16</sub> | Time Measurement/Waveform Generating Register 14       | G1TM4/G1PO4 | XX <sub>16</sub><br>XX <sub>16</sub> |
| 010A <sub>16</sub><br>010B <sub>16</sub> | Time Measurement/Waveform Generating Register 15       | G1TM5/G1PO5 | XX <sub>16</sub><br>XX <sub>16</sub> |
| 010C <sub>16</sub><br>010D <sub>16</sub> | Time Measurement/Waveform Generating Register 16       | G1TM6/G1PO6 | XX <sub>16</sub><br>XX <sub>16</sub> |
| 010E <sub>16</sub><br>010F <sub>16</sub> | Time Measurement/Waveform Generating Register 17       | G1TM7/G1PO7 | XX <sub>16</sub><br>XX <sub>16</sub> |
| 0110 <sub>16</sub>                       | Waveform Generating Control Register 10                | G1POCR0     | 0000 X000 <sub>2</sub>               |
| 0111 <sub>16</sub>                       | Waveform Generating Control Register 11                | G1POCR1     | 0X00 X000 <sub>2</sub>               |
| 0112 <sub>16</sub>                       | Waveform Generating Control Register 12                | G1POCR2     | 0X00 X000 <sub>2</sub>               |
| 0113 <sub>16</sub>                       | Waveform Generating Control Register 13                | G1POCR3     | 0X00 X000 <sub>2</sub>               |
| 0114 <sub>16</sub>                       | Waveform Generating Control Register 14                | G1POCR4     | 0X00 X000 <sub>2</sub>               |
| 0115 <sub>16</sub>                       | Waveform Generating Control Register 15                | G1POCR5     | 0X00 X000 <sub>2</sub>               |
| 0116 <sub>16</sub>                       | Waveform Generating Control Register 16                | G1POCR6     | 0X00 X000 <sub>2</sub>               |
| 0117 <sub>16</sub>                       | Waveform Generating Control Register 17                | G1POCR7     | 0X00 X000 <sub>2</sub>               |
| 0118 <sub>16</sub>                       | Time Measurement Control Register 10                   | G1TMCR0     | 00 <sub>16</sub>                     |
| 0119 <sub>16</sub>                       | Time Measurement Control Register 11                   | G1TMCR1     | 00 <sub>16</sub>                     |
| 011A <sub>16</sub>                       | Time Measurement Control Register 12                   | G1TMCR2     | 00 <sub>16</sub>                     |
| 011B <sub>16</sub>                       | Time Measurement Control Register 13                   | G1TMCR3     | 00 <sub>16</sub>                     |
| 011C <sub>16</sub>                       | Time Measurement Control Register 14                   | G1TMCR4     | 00 <sub>16</sub>                     |
| 011D <sub>16</sub>                       | Time Measurement Control Register 15                   | G1TMCR5     | 00 <sub>16</sub>                     |
| 011E <sub>16</sub>                       | Time Measurement Control Register 16                   | G1TMCR6     | 00 <sub>16</sub>                     |
| 011F <sub>16</sub>                       | Time Measurement Control Register 17                   | G1TMCR7     | 00 <sub>16</sub>                     |

X: Indeterminate

Blank spaces are reserved. No access is allowed.

| Address                                  | Register   | Symbol    | Value after RESET                                |
|--|--|-----------|--|
| 0120 <sub>16</sub><br>0121 <sub>16</sub> | Base Timer Register 1                                  | G1BT      | XX <sub>16</sub><br>XX <sub>16</sub>             |
| 0122 <sub>16</sub>                       | Base Timer Control Register 10                         | G1BCR0    | 00 <sub>16</sub>                                 |
| 0123 <sub>16</sub>                       | Base Timer Control Register 11                         | G1BCR1    | X000 000X <sub>2</sub>                           |
| 0124 <sub>16</sub>                       | Time Measurement Prescaler Register 16                 | G1TPR6    | 00 <sub>16</sub>                                 |
| 0125 <sub>16</sub>                       | Time Measurement Prescaler Register 17                 | G1TPR7    | 00 <sub>16</sub>                                 |
| 0126 <sub>16</sub>                       | Function Enable Register 1                             | G1FE      | 00 <sub>16</sub>                                 |
| 0127 <sub>16</sub>                       | Function Select Register 1                             | G1FS      | 00 <sub>16</sub>                                 |
| 0128 <sub>16</sub><br>0129 <sub>16</sub> | SI/O Receive Buffer Register 1                         | G1RB      | XXXX XXXX <sub>2</sub><br>X000 XXXX <sub>2</sub> |
| 012A <sub>16</sub><br>012B <sub>16</sub> | Transmit Buffer/Receive Data Register 1                | G1TB/G1DR | XX <sub>16</sub>                                 |
| 012C <sub>16</sub>                       | Receive Input Register 1                               | G1RI      | XX <sub>16</sub>                                 |
| 012D <sub>16</sub>                       | SI/O Communication Mode Register 1                     | G1MR      | 00 <sub>16</sub>                                 |
| 012E <sub>16</sub>                       | Transmit Output Register 1                             | G1TO      | XX <sub>16</sub>                                 |
| 012F <sub>16</sub>                       | SI/O Communication Control Register 1                  | G1CR      | 0000 X011 <sub>2</sub>                           |
| 0130 <sub>16</sub>                       | Data Compare Register 10                               | G1CMP0    | XX <sub>16</sub>                                 |
| 0131 <sub>16</sub>                       | Data Compare Register 11                               | G1CMP1    | XX <sub>16</sub>                                 |
| 0132 <sub>16</sub>                       | Data Compare Register 12                               | G1CMP2    | XX <sub>16</sub>                                 |
| 0133 <sub>16</sub>                       | Data Compare Register 13                               | G1CMP3    | XX <sub>16</sub>                                 |
| 0134 <sub>16</sub>                       | Data Mask Register 10                                  | G1MSK0    | XX <sub>16</sub>                                 |
| 0135 <sub>16</sub>                       | Data Mask Register 11                                  | G1MSK1    | XX <sub>16</sub>                                 |
| 0136 <sub>16</sub>                       |  |           |  |
| 0137 <sub>16</sub>                       |  |           |  |
| 0138 <sub>16</sub><br>0139 <sub>16</sub> | Receive CRC Code Register 1                            | G1RCRC    | XX <sub>16</sub><br>XX <sub>16</sub>             |
| 013A <sub>16</sub><br>013B <sub>16</sub> | Transmit CRC Code Register 1                           | G1TCRC    | 00 <sub>16</sub><br>00 <sub>16</sub>             |
| 013C <sub>16</sub>                       | SI/O Extended Mode Register 1                          | G1EMR     | 00 <sub>16</sub>                                 |
| 013D <sub>16</sub>                       | SI/O Extended Receive Control Register 1               | G1ERC     | 00 <sub>16</sub>                                 |
| 013E <sub>16</sub>                       | SI/O Special Communication Interrupt Detect Register 1 | G1IRF     | 00 <sub>16</sub>                                 |
| 013F <sub>16</sub>                       | SI/O Extended Transmit Control Register 1              | G1ETC     | 0000 0XXX <sub>2</sub>                           |
| 0140 <sub>16</sub>                       |  |           |  |
| 0141 <sub>16</sub>                       |  |           |  |
| 0142 <sub>16</sub>                       |  |           |  |
| 0143 <sub>16</sub>                       |  |           |  |
| 0144 <sub>16</sub>                       |  |           |  |
| 0145 <sub>16</sub>                       |  |           |  |
| 0146 <sub>16</sub>                       |  |           |  |
| 0147 <sub>16</sub>                       |  |           |  |
| 0148 <sub>16</sub>                       |  |           |  |
| 0149 <sub>16</sub>                       |  |           |  |
| 014A <sub>16</sub>                       |  |           |  |
| 014B <sub>16</sub>                       |  |           |  |
| 014C <sub>16</sub>                       |  |           |  |
| 014D <sub>16</sub>                       |  |           |  |
| 014E <sub>16</sub>                       |  |           |  |
| 014F <sub>16</sub>                       |  |           |  |

X: Indeterminate

Blank spaces are reserved. No access is allowed.

| Address  | Register                         | Symbol | Value after RESET |
|--|----------------------------------|--------|-------------------|
| 0150 <sub>16</sub>                             |                                  |        |                   |
| 0151 <sub>16</sub>                             |                                  |        |                   |
| 0152 <sub>16</sub>                             |                                  |        |                   |
| 0153 <sub>16</sub>                             |                                  |        |                   |
| 0154 <sub>16</sub>                             |                                  |        |                   |
| 0155 <sub>16</sub>                             |                                  |        |                   |
| 0156 <sub>16</sub>                             |                                  |        |                   |
| 0157 <sub>16</sub>                             |                                  |        |                   |
| 0158 <sub>16</sub>                             |                                  |        |                   |
| 0159 <sub>16</sub>                             |                                  |        |                   |
| 015A <sub>16</sub>                             |                                  |        |                   |
| 015B <sub>16</sub>                             |                                  |        |                   |
| 015C <sub>16</sub>                             |                                  |        |                   |
| 015D <sub>16</sub>                             |                                  |        |                   |
| 015E <sub>16</sub>                             |                                  |        |                   |
| 015F <sub>16</sub>                             |                                  |        |                   |
| 0160 <sub>16</sub>                             |                                  |        |                   |
| 0161 <sub>16</sub>                             |                                  |        |                   |
| 0162 <sub>16</sub>                             |                                  |        |                   |
| 0163 <sub>16</sub>                             |                                  |        |                   |
| 0164 <sub>16</sub>                             |                                  |        |                   |
| 0165 <sub>16</sub>                             |                                  |        |                   |
| 0166 <sub>16</sub>                             |                                  |        |                   |
| 0167 <sub>16</sub>                             |                                  |        |                   |
| 0168 <sub>16</sub>                             |                                  |        |                   |
| 0169 <sub>16</sub>                             |                                  |        |                   |
| 016A <sub>16</sub>                             |                                  |        |                   |
| 016B <sub>16</sub>                             |                                  |        |                   |
| 016C <sub>16</sub>                             |                                  |        |                   |
| 016D <sub>16</sub>                             |                                  |        |                   |
| 016E <sub>16</sub>                             |                                  |        |                   |
| 016F <sub>16</sub>                             |                                  |        |                   |
| 0170 <sub>16</sub>                             |                                  |        |                   |
| 0171 <sub>16</sub>                             |                                  |        |                   |
| 0172 <sub>16</sub>                             |                                  |        |                   |
| 0173 <sub>16</sub>                             |                                  |        |                   |
| 0174 <sub>16</sub>                             |                                  |        |                   |
| 0175 <sub>16</sub>                             |                                  |        |                   |
| 0176 <sub>16</sub>                             |                                  |        |                   |
| 0177 <sub>16</sub>                             |                                  |        |                   |
| 0178 <sub>16</sub>                             | Input Function Select Register   | IPS    | 00 <sub>16</sub>  |
| 0179 <sub>16</sub>                             | Input Function Select Register A | IPSA   | 00 <sub>16</sub>  |
| 017A <sub>16</sub>                             |                                  |        |                   |
| 017B <sub>16</sub>                             |                                  |        |                   |
| 017C <sub>16</sub>                             |                                  |        |                   |
| 017D <sub>16</sub><br>to<br>01DF <sub>16</sub> |                                  |        |                   |

X: Indeterminate

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| Address                                  | Register   | Symbol     | Value after RESET  |
|--|--|------------|--|
| 01E0 <sub>16</sub>                       | CAN0 Message Slot Buffer 0 Standard ID0          | C0SLOT0_0  | XX <sub>16</sub>   |
| 01E1 <sub>16</sub>                       | CAN0 Message Slot Buffer 0 Standard ID1          | C0SLOT0_1  | XX <sub>16</sub>   |
| 01E2 <sub>16</sub>                       | CAN0 Message Slot Buffer 0 Extended ID0          | C0SLOT0_2  | XX <sub>16</sub>   |
| 01E3 <sub>16</sub>                       | CAN0 Message Slot Buffer 0 Extended ID1          | C0SLOT0_3  | XX <sub>16</sub>   |
| 01E4 <sub>16</sub>                       | CAN0 Message Slot Buffer 0 Extended ID2          | C0SLOT0_4  | XX <sub>16</sub>   |
| 01E5 <sub>16</sub>                       | CAN0 Message Slot Buffer 0 Data Length Code      | C0SLOT0_5  | XX <sub>16</sub>   |
| 01E6 <sub>16</sub>                       | CAN0 Message Slot Buffer 0 Data 0                | C0SLOT0_6  | XX <sub>16</sub>   |
| 01E7 <sub>16</sub>                       | CAN0 Message Slot Buffer 0 Data 1                | C0SLOT0_7  | XX <sub>16</sub>   |
| 01E8 <sub>16</sub>                       | CAN0 Message Slot Buffer 0 Data 2                | C0SLOT0_8  | XX <sub>16</sub>   |
| 01E9 <sub>16</sub>                       | CAN0 Message Slot Buffer 0 Data 3                | C0SLOT0_9  | XX <sub>16</sub>   |
| 01EA <sub>16</sub>                       | CAN0 Message Slot Buffer 0 Data 4                | C0SLOT0_10 | XX <sub>16</sub>   |
| 01EB <sub>16</sub>                       | CAN0 Message Slot Buffer 0 Data 5                | C0SLOT0_11 | XX <sub>16</sub>   |
| 01EC <sub>16</sub>                       | CAN0 Message Slot Buffer 0 Data 6                | C0SLOT0_12 | XX <sub>16</sub>   |
| 01ED <sub>16</sub>                       | CAN0 Message Slot Buffer 0 Data 7                | C0SLOT0_13 | XX <sub>16</sub>   |
| 01EE <sub>16</sub>                       | CAN0 Message Slot Buffer 0 Time Stamp High-Order | C0SLOT0_14 | XX <sub>16</sub>   |
| 01EF <sub>16</sub>                       | CAN0 Message Slot Buffer 0 Time Stamp Low-Order  | C0SLOT0_15 | XX <sub>16</sub>   |
| 01F0 <sub>16</sub>                       | CAN0 Message Slot Buffer 1 Standard ID0          | C0SLOT1_0  | XX <sub>16</sub>   |
| 01F1 <sub>16</sub>                       | CAN0 Message Slot Buffer 1 Standard ID1          | C0SLOT1_1  | XX <sub>16</sub>   |
| 01F2 <sub>16</sub>                       | CAN0 Message Slot Buffer 1 Extended ID0          | C0SLOT1_2  | XX <sub>16</sub>   |
| 01F3 <sub>16</sub>                       | CAN0 Message Slot Buffer 1 Extended ID1          | C0SLOT1_3  | XX <sub>16</sub>   |
| 01F4 <sub>16</sub>                       | CAN0 Message Slot Buffer 1 Extended ID2          | C0SLOT1_4  | XX <sub>16</sub>   |
| 01F5 <sub>16</sub>                       | CAN0 Message Slot Buffer 1 Data Length Code      | C0SLOT1_5  | XX <sub>16</sub>   |
| 01F6 <sub>16</sub>                       | CAN0 Message Slot Buffer 1 Data 0                | C0SLOT1_6  | XX <sub>16</sub>   |
| 01F7 <sub>16</sub>                       | CAN0 Message Slot Buffer 1 Data 1                | C0SLOT1_7  | XX <sub>16</sub>   |
| 01F8 <sub>16</sub>                       | CAN0 Message Slot Buffer 1 Data 2                | C0SLOT1_8  | XX <sub>16</sub>   |
| 01F9 <sub>16</sub>                       | CAN0 Message Slot Buffer 1 Data 3                | C0SLOT1_9  | XX <sub>16</sub>   |
| 01FA <sub>16</sub>                       | CAN0 Message Slot Buffer 1 Data 4                | C0SLOT1_10 | XX <sub>16</sub>   |
| 01FB <sub>16</sub>                       | CAN0 Message Slot Buffer 1 Data 5                | C0SLOT1_11 | XX <sub>16</sub>   |
| 01FC <sub>16</sub>                       | CAN0 Message Slot Buffer 1 Data 6                | C0SLOT1_12 | XX <sub>16</sub>   |
| 01FD <sub>16</sub>                       | CAN0 Message Slot Buffer 1 Data 7                | C0SLOT1_13 | XX <sub>16</sub>   |
| 01FE <sub>16</sub>                       | CAN0 Message Slot Buffer 1 Time Stamp High-Order | C0SLOT1_14 | XX <sub>16</sub>   |
| 01FF <sub>16</sub>                       | CAN0 Message Slot Buffer 1 Time Stamp Low-Order  | C0SLOT1_15 | XX <sub>16</sub>   |
| 0200 <sub>16</sub><br>0201 <sub>16</sub> | CAN0 Control Register 0                          | C0CTRL0    | XX01 0X01 <sub>2</sub> <sup>(1)</sup><br>XXXX 0000 <sub>2</sub> <sup>(1)</sup> |
| 0202 <sub>16</sub><br>0203 <sub>16</sub> | CAN0 Status Register                             | C0STR      | 0000 0000 <sub>2</sub> <sup>(1)</sup><br>X000 0X01 <sub>2</sub> <sup>(1)</sup> |
| 0204 <sub>16</sub><br>0205 <sub>16</sub> | CAN0 Extended ID Register                        | C0IDR      | 00 <sub>16</sub> <sup>(1)</sup><br>00 <sub>16</sub> <sup>(1)</sup>             |
| 0206 <sub>16</sub><br>0207 <sub>16</sub> | CAN0 Configuration Register                      | C0CONR     | 0000 XXXX <sub>2</sub> <sup>(1)</sup><br>0000 0000 <sub>2</sub> <sup>(1)</sup> |
| 0208 <sub>16</sub><br>0209 <sub>16</sub> | CAN0 Time Stamp Register                         | C0TSR      | 00 <sub>16</sub> <sup>(1)</sup><br>00 <sub>16</sub> <sup>(1)</sup>             |
| 020A <sub>16</sub>                       | CAN0 Transmit Error Count Register               | C0TEC      | 00 <sub>16</sub> <sup>(1)</sup>  |
| 020B <sub>16</sub>                       | CAN0 Receive Error Count Register                | C0REC      | 00 <sub>16</sub> <sup>(1)</sup>  |
| 020C <sub>16</sub><br>020D <sub>16</sub> | CAN0 Slot Interrupt Status Register              | C0SISTR    | 00 <sub>16</sub> <sup>(1)</sup><br>00 <sub>16</sub> <sup>(1)</sup>             |
| 020E <sub>16</sub>                       |  |            |  |
| 020F <sub>16</sub>                       |  |            |  |

X: Indeterminate

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NOTES:

1. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) after reset and supplying the clock to the CAN module.

| Address            | Register                                | Symbol   | Value after RESET                     |
|--------------------|---|----------|---------------------------------------|
| 0210 <sub>16</sub> | CAN0 Slot Interrupt Mask Register       | C0SIMKR  | 00 <sub>16</sub> <sup>(2)</sup>       |
| 0211 <sub>16</sub> |   |          | 00 <sub>16</sub> <sup>(2)</sup>       |
| 0212 <sub>16</sub> |   |          |                                       |
| 0213 <sub>16</sub> |   |          |                                       |
| 0214 <sub>16</sub> | CAN0 Error Interrupt Mask Register      | C0EIMKR  | XXXX X000 <sub>2</sub> <sup>(2)</sup> |
| 0215 <sub>16</sub> | CAN0 Error Interrupt Status Register    | C0EISTR  | XXXX X000 <sub>2</sub> <sup>(2)</sup> |
| 0216 <sub>16</sub> | CAN0 Error Cause Register               | C0EFR    | 00 <sub>16</sub> <sup>(2)</sup>       |
| 0217 <sub>16</sub> | CAN0 Baud Rate Prescaler                | C0BRP    | 0000 0001 <sub>2</sub> <sup>(2)</sup> |
| 0218 <sub>16</sub> |   |          |                                       |
| 0219 <sub>16</sub> | CAN0 Mode Register                      | C0MDR    | XXXX XX00 <sub>2</sub> <sup>(2)</sup> |
| 021A <sub>16</sub> |   |          |                                       |
| 021B <sub>16</sub> |   |          |                                       |
| 021C <sub>16</sub> |   |          |                                       |
| 021D <sub>16</sub> |   |          |                                       |
| 021E <sub>16</sub> |   |          |                                       |
| 021F <sub>16</sub> |   |          |                                       |
| 0220 <sub>16</sub> | CAN0 Single-Shot Control Register       | C0SSCTLR | 00 <sub>16</sub> <sup>(2)</sup>       |
| 0221 <sub>16</sub> |   |          | 00 <sub>16</sub> <sup>(2)</sup>       |
| 0222 <sub>16</sub> |   |          |                                       |
| 0223 <sub>16</sub> |   |          |                                       |
| 0224 <sub>16</sub> | CAN0 Single-Shot Status Register        | C0SSSTR  | 00 <sub>16</sub> <sup>(2)</sup>       |
| 0225 <sub>16</sub> |   |          | 00 <sub>16</sub> <sup>(2)</sup>       |
| 0226 <sub>16</sub> |   |          |                                       |
| 0227 <sub>16</sub> |   |          |                                       |
| 0228 <sub>16</sub> | CAN0 Global Mask Register Standard ID0  | C0GMR0   | XXX0 0000 <sub>2</sub> <sup>(2)</sup> |
| 0229 <sub>16</sub> | CAN0 Global Mask Register Standard ID1  | C0GMR1   | XX00 0000 <sub>2</sub> <sup>(2)</sup> |
| 022A <sub>16</sub> | CAN0 Global Mask Register Extended ID0  | C0GMR2   | XXXX 0000 <sub>2</sub> <sup>(2)</sup> |
| 022B <sub>16</sub> | CAN0 Global Mask Register Extended ID1  | C0GMR3   | 00 <sub>16</sub> <sup>(2)</sup>       |
| 022C <sub>16</sub> | CAN0 Global Mask Register Extended ID2  | C0GMR4   | XX00 0000 <sub>2</sub> <sup>(2)</sup> |
| 022D <sub>16</sub> |   |          |                                       |
| 022E <sub>16</sub> |   |          |                                       |
| 022F <sub>16</sub> |   |          |                                       |
| 0230 <sub>16</sub> | CAN0 Message Slot 0 Control Register /  | C0MCTL0/ | 0000 0000 <sub>2</sub> <sup>(2)</sup> |
|                    | CAN0 Local Mask Register A Standard ID0 | C0LMAR0  | XXX0 0000 <sub>2</sub> <sup>(2)</sup> |
| 0231 <sub>16</sub> | CAN0 Message Slot 1 Control Register /  | C0MCTL1/ | 0000 0000 <sub>2</sub> <sup>(2)</sup> |
|                    | CAN0 Local Mask Register A Standard ID1 | C0LMAR1  | XX00 0000 <sub>2</sub> <sup>(2)</sup> |
| 0232 <sub>16</sub> | CAN0 Message Slot 2 Control Register /  | C0MCTL2/ | 0000 0000 <sub>2</sub> <sup>(2)</sup> |
|                    | CAN0 Local Mask Register A Extended ID0 | C0LMAR2  | XXXX 0000 <sub>2</sub> <sup>(2)</sup> |
| 0233 <sub>16</sub> | CAN0 Message Slot 3 Control Register /  | C0MCTL3/ | 00 <sub>16</sub> <sup>(2)</sup>       |
|                    | CAN0 local Mask Register A Extended ID1 | C0LMAR3  | 00 <sub>16</sub> <sup>(2)</sup>       |
| 0234 <sub>16</sub> | CAN0 Message Slot 4 Control Register /  | C0MCTL4/ | 0000 0000 <sub>2</sub> <sup>(2)</sup> |
|                    | CAN0 Local Mask Register A Extended ID2 | C0LMAR4  | XX00 0000 <sub>2</sub> <sup>(2)</sup> |
| 0235 <sub>16</sub> | CAN0 Message Slot 5 Control Register    | C0MCTL5  | 00 <sub>16</sub> <sup>(2)</sup>       |
| 0236 <sub>16</sub> | CAN0 Message Slot 6 Control Register    | C0MCTL6  | 00 <sub>16</sub> <sup>(2)</sup>       |
| 0237 <sub>16</sub> | CAN0 Message Slot 7 Control Register    | C0MCTL7  | 00 <sub>16</sub> <sup>(2)</sup>       |
| 0238 <sub>16</sub> | CAN0 Message Slot 8 Control Register /  | C0MCTL8/ | 0000 0000 <sub>2</sub> <sup>(2)</sup> |
|                    | CAN0 Local Mask Register B Standard ID0 | C0LMBR0  | XXX0 0000 <sub>2</sub> <sup>(2)</sup> |

(Note 1)

X: Indeterminate

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## NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 0220<sub>16</sub> to 023F<sub>16</sub>.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) after reset and supplying the clock to the CAN module.



| Address  | Register   | Symbol               | Value after RESET  |
|--|--|----------------------|--|
| 0239 <sub>16</sub>                             | CAN0 Message Slot 9 Control Register /<br>CAN0 Local Mask Register B Standard ID1  | C0MCTL9/<br>C0LMBR1  | 0000 0000 <sub>2</sub> <sup>(2)</sup><br>XX00 0000 <sub>2</sub> <sup>(2)</sup> |
| 023A <sub>16</sub>                             | CAN0 Message Slot 10 Control Register /<br>CAN0 Local Mask Register B Extended ID0 | C0MCTL10/<br>C0LMBR2 | 0000 0000 <sub>2</sub> <sup>(2)</sup><br>XXXX 0000 <sub>2</sub> <sup>(2)</sup> |
| 023B <sub>16</sub>                             | CAN0 Message Slot 11 Control Register /<br>CAN0 Local Mask Register B Extended ID1 | C0MCTL11/<br>C0LMBR3 | 00 <sub>16</sub> <sup>(2)</sup><br>00 <sub>16</sub> <sup>(2)</sup>             |
| 023C <sub>16</sub>                             | CAN0 Message Slot 12 Control Register /<br>CAN0 Local Mask Register B Extended ID2 | C0MCTL12/<br>C0LMBR4 | 0000 0000 <sub>2</sub> <sup>(2)</sup><br>XX00 0000 <sub>2</sub> <sup>(2)</sup> |
| 023D <sub>16</sub>                             | CAN0 Message Slot 13 Control Register  | C0MCTL13             | 00 <sub>16</sub> <sup>(2)</sup>  |
| 023E <sub>16</sub>                             | CAN0 Message Slot 14 Control Register  | C0MCTL14             | 00 <sub>16</sub> <sup>(2)</sup>  |
| 023F <sub>16</sub>                             | CAN0 Message Slot 15 Control Register  | C0MCTL15             | 00 <sub>16</sub> <sup>(2)</sup>  |
| 0240 <sub>16</sub>                             | CAN0 Slot Buffer Select Register   | C0SBS                | 00 <sub>16</sub> <sup>(2)</sup>  |
| 0241 <sub>16</sub>                             | CAN0 Control Register 1  | C0CTLR1              | X000 00XX <sub>2</sub> <sup>(2)</sup>  |
| 0242 <sub>16</sub>                             | CAN0 Sleep Control Register  | C0SLPR               | XXXX XXX0 <sub>2</sub>   |
| 0243 <sub>16</sub>                             |  |                      |  |
| 0244 <sub>16</sub>                             | CAN0 Acceptance Filter Support Register  | C0AFS                | 00 <sub>16</sub> <sup>(2)</sup>  |
| 0245 <sub>16</sub>                             |  |                      | 01 <sub>16</sub> <sup>(2)</sup>  |
| 0246 <sub>16</sub>                             |  |                      |  |
| 0247 <sub>16</sub>                             |  |                      |  |
| 0248 <sub>16</sub>                             |  |                      |  |
| 0249 <sub>16</sub>                             |  |                      |  |
| 024A <sub>16</sub>                             |  |                      |  |
| 024B <sub>16</sub>                             |  |                      |  |
| 024C <sub>16</sub>                             |  |                      |  |
| 024D <sub>16</sub>                             |  |                      |  |
| 024E <sub>16</sub>                             |  |                      |  |
| 024F <sub>16</sub>                             |  |                      |  |
| 0250 <sub>16</sub>                             |  |                      |  |
| 0251 <sub>16</sub>                             |  |                      |  |
| 0252 <sub>16</sub>                             |  |                      |  |
| 0253 <sub>16</sub>                             |  |                      |  |
| 0254 <sub>16</sub>                             |  |                      |  |
| 0255 <sub>16</sub>                             |  |                      |  |
| 0256 <sub>16</sub>                             |  |                      |  |
| 0257 <sub>16</sub>                             |  |                      |  |
| 0258 <sub>16</sub>                             |  |                      |  |
| 0259 <sub>16</sub>                             |  |                      |  |
| 025A <sub>16</sub>                             |  |                      |  |
| 025B <sub>16</sub>                             |  |                      |  |
| 025C <sub>16</sub>                             |  |                      |  |
| 025D <sub>16</sub><br>to<br>02BF <sub>16</sub> |  |                      |  |

(Note 1)

X: Indeterminate

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NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 0220<sub>16</sub> to 023F<sub>16</sub>.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) after reset and supplying the clock to the CAN module.

| Address                                  | Register                                  | Symbol    | Value after RESET                    |
|--|---|-----------|--------------------------------------|
| 02C0 <sub>16</sub><br>02C1 <sub>16</sub> | X0 Register Y0 Register                   | X0R,Y0R   | XX <sub>16</sub><br>XX <sub>16</sub> |
| 02C2 <sub>16</sub><br>02C3 <sub>16</sub> | X1 Register Y1 Register                   | X1R,Y1R   | XX <sub>16</sub><br>XX <sub>16</sub> |
| 02C4 <sub>16</sub><br>02C5 <sub>16</sub> | X2 Register Y2 Register                   | X2R,Y2R   | XX <sub>16</sub><br>XX <sub>16</sub> |
| 02C6 <sub>16</sub><br>02C7 <sub>16</sub> | X3 Register Y3 Register                   | X3R,Y3R   | XX <sub>16</sub><br>XX <sub>16</sub> |
| 02C8 <sub>16</sub><br>02C9 <sub>16</sub> | X4 Register Y4 Register                   | X4R,Y4R   | XX <sub>16</sub><br>XX <sub>16</sub> |
| 02CA <sub>16</sub><br>02CB <sub>16</sub> | X5 Register Y5 Register                   | X5R,Y5R   | XX <sub>16</sub><br>XX <sub>16</sub> |
| 02CC <sub>16</sub><br>02CD <sub>16</sub> | X6 Register Y6 Register                   | X6R,Y6R   | XX <sub>16</sub><br>XX <sub>16</sub> |
| 02CE <sub>16</sub><br>02CF <sub>16</sub> | X7 Register Y7 Register                   | X7R,Y7R   | XX <sub>16</sub><br>XX <sub>16</sub> |
| 02D0 <sub>16</sub><br>02D1 <sub>16</sub> | X8 Register Y8 Register                   | X8R,Y8R   | XX <sub>16</sub><br>XX <sub>16</sub> |
| 02D2 <sub>16</sub><br>02D3 <sub>16</sub> | X9 Register Y9 Register                   | X9R,Y9R   | XX <sub>16</sub><br>XX <sub>16</sub> |
| 02D4 <sub>16</sub><br>02D5 <sub>16</sub> | X10 Register Y10 Register                 | X10R,Y10R | XX <sub>16</sub><br>XX <sub>16</sub> |
| 02D6 <sub>16</sub><br>02D7 <sub>16</sub> | X11 Register Y11 Register                 | X11R,Y11R | XX <sub>16</sub><br>XX <sub>16</sub> |
| 02D8 <sub>16</sub><br>02D9 <sub>16</sub> | X12 Register Y12 Register                 | X12R,Y12R | XX <sub>16</sub><br>XX <sub>16</sub> |
| 02DA <sub>16</sub><br>02DB <sub>16</sub> | X13 Register Y13 Register                 | X13R,Y13R | XX <sub>16</sub><br>XX <sub>16</sub> |
| 02DC <sub>16</sub><br>02DD <sub>16</sub> | X14 Register Y14 Register                 | X14R,Y14R | XX <sub>16</sub><br>XX <sub>16</sub> |
| 02DE <sub>16</sub><br>02DF <sub>16</sub> | X15 Register Y15 Register                 | X15R,Y15R | XX <sub>16</sub><br>XX <sub>16</sub> |
| 02E0 <sub>16</sub>                       | X/Y Control Register                      | XYC       | XXXX XX00 <sub>2</sub>               |
| 02E1 <sub>16</sub>                       |   |           |                                      |
| 02E2 <sub>16</sub>                       |   |           |                                      |
| 02E3 <sub>16</sub>                       |   |           |                                      |
| 02E4 <sub>16</sub>                       | UART1 Special Mode Register 4             | U1SMR4    | 00 <sub>16</sub>                     |
| 02E5 <sub>16</sub>                       | UART1 Special Mode Register 3             | U1SMR3    | 00 <sub>16</sub>                     |
| 02E6 <sub>16</sub>                       | UART1 Special Mode Register 2             | U1SMR2    | 00 <sub>16</sub>                     |
| 02E7 <sub>16</sub>                       | UART1 Special Mode Register               | U1SMR     | 00 <sub>16</sub>                     |
| 02E8 <sub>16</sub>                       | UART1 Transmit/Receive Mode Register      | U1MR      | 00 <sub>16</sub>                     |
| 02E9 <sub>16</sub>                       | UART1 Bit Rate Register                   | U1BRG     | XX <sub>16</sub>                     |
| 02EA <sub>16</sub><br>02EB <sub>16</sub> | UART1 Transmit Buffer Register            | U1TB      | XX <sub>16</sub><br>XX <sub>16</sub> |
| 02EC <sub>16</sub>                       | UART1 Transmit/Receive Control Register 0 | U1C0      | 0000 1000 <sub>2</sub>               |
| 02ED <sub>16</sub>                       | UART1 Transmit/Receive Control Register 1 | U1C1      | 0000 0010 <sub>2</sub>               |
| 02EE <sub>16</sub><br>02EF <sub>16</sub> | UART1 Receive Buffer Register             | U1RB      | XX <sub>16</sub><br>XX <sub>16</sub> |

X: Indeterminate

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| Address            | Register  | Symbol | Value after RESET      |
|--------------------|---|--------|------------------------|
| 02F0 <sub>16</sub> |   |        |                        |
| 02F1 <sub>16</sub> |   |        |                        |
| 02F2 <sub>16</sub> |   |        |                        |
| 02F3 <sub>16</sub> |   |        |                        |
| 02F4 <sub>16</sub> | UART4 Special Mode Register 4                       | U4SMR4 | 00 <sub>16</sub>       |
| 02F5 <sub>16</sub> | UART4 Special Mode Register 3                       | U4SMR3 | 00 <sub>16</sub>       |
| 02F6 <sub>16</sub> | UART4 Special Mode Register 2                       | U4SMR2 | 00 <sub>16</sub>       |
| 02F7 <sub>16</sub> | UART4 Special Mode Register                         | U4SMR  | 00 <sub>16</sub>       |
| 02F8 <sub>16</sub> | UART4 Transmit/Receive Mode Register                | U4MR   | 00 <sub>16</sub>       |
| 02F9 <sub>16</sub> | UART4 Bit Rate Register                             | U4BRG  | XX <sub>16</sub>       |
| 02FA <sub>16</sub> | UART4 Transmit Buffer Register                      | U4TB   | XX <sub>16</sub>       |
| 02FB <sub>16</sub> |   |        | XX <sub>16</sub>       |
| 02FC <sub>16</sub> | UART4 Transmit/Receive Control Register 0           | U4C0   | 0000 1000 <sub>2</sub> |
| 02FD <sub>16</sub> | UART4 Transmit/Receive Control Register 1           | U4C1   | 0000 0010 <sub>2</sub> |
| 02FE <sub>16</sub> | UART4 Receive Buffer Register                       | U4RB   | XX <sub>16</sub>       |
| 02FF <sub>16</sub> |   |        | XX <sub>16</sub>       |
| 0300 <sub>16</sub> | Timer B3, B4, B5 Count Start Flag                   | TBSR   | 000X XXXX <sub>2</sub> |
| 0301 <sub>16</sub> |   |        |                        |
| 0302 <sub>16</sub> | Timer A1-1 Register                                 | TA11   | XX <sub>16</sub>       |
| 0303 <sub>16</sub> |   |        | XX <sub>16</sub>       |
| 0304 <sub>16</sub> | Timer A2-1 Register                                 | TA21   | XX <sub>16</sub>       |
| 0305 <sub>16</sub> |   |        | XX <sub>16</sub>       |
| 0306 <sub>16</sub> | Timer A4-1 Register                                 | TA41   | XX <sub>16</sub>       |
| 0307 <sub>16</sub> |   |        | XX <sub>16</sub>       |
| 0308 <sub>16</sub> | Three-Phase PWM Control Register 0                  | INVC0  | 00 <sub>16</sub>       |
| 0309 <sub>16</sub> | Three-Phase PWM Control Register 1                  | INVC1  | 00 <sub>16</sub>       |
| 030A <sub>16</sub> | Three-Phase Output Buffer Register 0                | IDB0   | XX11 1111 <sub>2</sub> |
| 030B <sub>16</sub> | Three-Phase Output Buffer Register 1                | IDB1   | XX11 1111 <sub>2</sub> |
| 030C <sub>16</sub> | Dead Time Timer                                     | DTT    | XX <sub>16</sub>       |
| 030D <sub>16</sub> | Timer B2 Interrupt Generation Frequency Set Counter | ICTB2  | XX <sub>16</sub>       |
| 030E <sub>16</sub> |   |        |                        |
| 030F <sub>16</sub> |   |        |                        |
| 0310 <sub>16</sub> | Timer B3 Register                                   | TB3    | XX <sub>16</sub>       |
| 0311 <sub>16</sub> |   |        | XX <sub>16</sub>       |
| 0312 <sub>16</sub> | Timer B4 Register                                   | TB4    | XX <sub>16</sub>       |
| 0313 <sub>16</sub> |   |        | XX <sub>16</sub>       |
| 0314 <sub>16</sub> | Timer B5 Register                                   | TB5    | XX <sub>16</sub>       |
| 0315 <sub>16</sub> |   |        | XX <sub>16</sub>       |
| 0316 <sub>16</sub> |   |        |                        |
| 0317 <sub>16</sub> |   |        |                        |
| 0318 <sub>16</sub> |   |        |                        |
| 0319 <sub>16</sub> |   |        |                        |
| 031A <sub>16</sub> |   |        |                        |
| 031B <sub>16</sub> | Timer B3 Mode Register                              | TB3MR  | 00XX 0000 <sub>2</sub> |
| 031C <sub>16</sub> | Timer B4 Mode Register                              | TB4MR  | 00XX 0000 <sub>2</sub> |
| 031D <sub>16</sub> | Timer B5 Mode Register                              | TB5MR  | 00XX 0000 <sub>2</sub> |
| 031E <sub>16</sub> |   |        |                        |
| 031F <sub>16</sub> | External Interrupt Cause Select Register            | IFSR   | 00 <sub>16</sub>       |

X: Indeterminate

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| Address            | Register                                  | Symbol | Value after RESET      |
|--------------------|---|--------|------------------------|
| 0320 <sub>16</sub> |   |        |                        |
| 0321 <sub>16</sub> |   |        |                        |
| 0322 <sub>16</sub> |   |        |                        |
| 0323 <sub>16</sub> |   |        |                        |
| 0324 <sub>16</sub> | UART3 Special Mode Register 4             | U3SMR4 | 00 <sub>16</sub>       |
| 0325 <sub>16</sub> | UART3 Special Mode Register 3             | U3SMR3 | 00 <sub>16</sub>       |
| 0326 <sub>16</sub> | UART3 Special Mode Register 2             | U3SMR2 | 00 <sub>16</sub>       |
| 0327 <sub>16</sub> | UART3 Special Mode Register               | U3SMR  | 00 <sub>16</sub>       |
| 0328 <sub>16</sub> | UART3 Transmit/Receive Mode Register      | U3MR   | 00 <sub>16</sub>       |
| 0329 <sub>16</sub> | UART3 Bit Rate Register                   | U3BRG  | XX <sub>16</sub>       |
| 032A <sub>16</sub> | UART3 Transmit Buffer Register            | U3TB   | XX <sub>16</sub>       |
| 032B <sub>16</sub> |   |        | XX <sub>16</sub>       |
| 032C <sub>16</sub> | UART3 Transmit/Receive Control Register 0 | U3C0   | 0000 1000 <sub>2</sub> |
| 032D <sub>16</sub> | UART3 Transmit/Receive Control Register 1 | U3C1   | 0000 0010 <sub>2</sub> |
| 032E <sub>16</sub> | UART3 Receive Buffer Register             | U3RB   | XX <sub>16</sub>       |
| 032F <sub>16</sub> |   |        | XX <sub>16</sub>       |
| 0330 <sub>16</sub> |   |        |                        |
| 0331 <sub>16</sub> |   |        |                        |
| 0332 <sub>16</sub> |   |        |                        |
| 0333 <sub>16</sub> |   |        |                        |
| 0334 <sub>16</sub> | UART2 Special Mode Register 4             | U2SMR4 | 00 <sub>16</sub>       |
| 0335 <sub>16</sub> | UART2 Special Mode Register 3             | U2SMR3 | 00 <sub>16</sub>       |
| 0336 <sub>16</sub> | UART2 Special Mode Register 2             | U2SMR2 | 00 <sub>16</sub>       |
| 0337 <sub>16</sub> | UART2 Special Mode Register               | U2SMR  | 00 <sub>16</sub>       |
| 0338 <sub>16</sub> | UART2 Transmit/Receive Mode Register      | U2MR   | 00 <sub>16</sub>       |
| 0339 <sub>16</sub> | UART2 Bit Rate Register                   | U2BRG  | XX <sub>16</sub>       |
| 033A <sub>16</sub> | UART2 Transmit Buffer Register            | U2TB   | XX <sub>16</sub>       |
| 033B <sub>16</sub> |   |        | XX <sub>16</sub>       |
| 033C <sub>16</sub> | UART2 Transmit/Receive Control Register 0 | U2C0   | 0000 1000 <sub>2</sub> |
| 033D <sub>16</sub> | UART2 Transmit/Receive Control Register 1 | U2C1   | 0000 0010 <sub>2</sub> |
| 033E <sub>16</sub> | UART2 Receive Buffer Register             | U2RB   | XX <sub>16</sub>       |
| 033F <sub>16</sub> |   |        | XX <sub>16</sub>       |
| 0340 <sub>16</sub> | Count Start Flag                          | TABSR  | 00 <sub>16</sub>       |
| 0341 <sub>16</sub> | Clock Prescaler Reset Flag                | CPSRF  | 0XXX XXXX <sub>2</sub> |
| 0342 <sub>16</sub> | One-Shot Start Flag                       | ONSF   | 00 <sub>16</sub>       |
| 0343 <sub>16</sub> | Trigger Select Register                   | TRGSR  | 00 <sub>16</sub>       |
| 0344 <sub>16</sub> | Up/Down Flag                              | UDF    | 00 <sub>16</sub>       |
| 0345 <sub>16</sub> |   |        |                        |
| 0346 <sub>16</sub> | Timer A0 Register                         | TA0    | XX <sub>16</sub>       |
| 0347 <sub>16</sub> |   |        | XX <sub>16</sub>       |
| 0348 <sub>16</sub> | Timer A1 Register                         | TA1    | XX <sub>16</sub>       |
| 0349 <sub>16</sub> |   |        | XX <sub>16</sub>       |
| 034A <sub>16</sub> | Timer A2 Register                         | TA2    | XX <sub>16</sub>       |
| 034B <sub>16</sub> |   |        | XX <sub>16</sub>       |
| 034C <sub>16</sub> | Timer A3 Register                         | TA3    | XX <sub>16</sub>       |
| 034D <sub>16</sub> |   |        | XX <sub>16</sub>       |
| 034E <sub>16</sub> | Timer A4 Register                         | TA4    | XX <sub>16</sub>       |
| 034F <sub>16</sub> |   |        | XX <sub>16</sub>       |

X: Indeterminate

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| Address                                  | Register                                       | Symbol | Value after RESET                    |
|--|--|--------|--------------------------------------|
| 0350 <sub>16</sub><br>0351 <sub>16</sub> | Timer B0 Register                              | TB0    | XX <sub>16</sub><br>XX <sub>16</sub> |
| 0352 <sub>16</sub><br>0353 <sub>16</sub> | Timer B1 Register                              | TB1    | XX <sub>16</sub><br>XX <sub>16</sub> |
| 0354 <sub>16</sub><br>0355 <sub>16</sub> | Timer B2 Register                              | TB2    | XX <sub>16</sub><br>XX <sub>16</sub> |
| 0356 <sub>16</sub>                       | Timer A0 Mode Register                         | TA0MR  | 00 <sub>16</sub>                     |
| 0357 <sub>16</sub>                       | Timer A1 Mode Register                         | TA1MR  | 00 <sub>16</sub>                     |
| 0358 <sub>16</sub>                       | Timer A2 Mode Register                         | TA2MR  | 00 <sub>16</sub>                     |
| 0359 <sub>16</sub>                       | Timer A3 Mode Register                         | TA3MR  | 00 <sub>16</sub>                     |
| 035A <sub>16</sub>                       | Timer A4 Mode Register                         | TA4MR  | 00 <sub>16</sub>                     |
| 035B <sub>16</sub>                       | Timer B0 Mode Register                         | TB0MR  | 00XX 0000 <sub>2</sub>               |
| 035C <sub>16</sub>                       | Timer B1 Mode Register                         | TB1MR  | 00XX 0000 <sub>2</sub>               |
| 035D <sub>16</sub>                       | Timer B2 Mode Register                         | TB2MR  | 00XX 0000 <sub>2</sub>               |
| 035E <sub>16</sub>                       | Timer B2 Special Mode Register                 | TB2SC  | XXXX XXX0 <sub>2</sub>               |
| 035F <sub>16</sub>                       | Count Source Prescaler Register <sup>(1)</sup> | TCSPR  | 0XXX 0000 <sub>2</sub>               |
| 0360 <sub>16</sub>                       |  |        |                                      |
| 0361 <sub>16</sub>                       |  |        |                                      |
| 0362 <sub>16</sub>                       |  |        |                                      |
| 0363 <sub>16</sub>                       |  |        |                                      |
| 0364 <sub>16</sub>                       | UART0 Special Mode Register 4                  | U0SMR4 | 00 <sub>16</sub>                     |
| 0365 <sub>16</sub>                       | UART0 Special Mode Register 3                  | U0SMR3 | 00 <sub>16</sub>                     |
| 0366 <sub>16</sub>                       | UART0 Special Mode Register 2                  | U0SMR2 | 00 <sub>16</sub>                     |
| 0367 <sub>16</sub>                       | UART0 Special Mode Register                    | U0SMR  | 00 <sub>16</sub>                     |
| 0368 <sub>16</sub>                       | UART0 Transmit/Receive Mode Register           | U0MR   | 00 <sub>16</sub>                     |
| 0369 <sub>16</sub>                       | UART0 Bit Rate Register                        | U0BRG  | XX <sub>16</sub>                     |
| 036A <sub>16</sub><br>036B <sub>16</sub> | UART0 Transmit Buffer Register                 | U0TB   | XX <sub>16</sub><br>XX <sub>16</sub> |
| 036C <sub>16</sub>                       | UART0 Transmit/Receive Control Register 0      | U0C0   | 0000 1000 <sub>2</sub>               |
| 036D <sub>16</sub>                       | UART0 Transmit/Receive Control Register 1      | U0C1   | 0000 0010 <sub>2</sub>               |
| 036E <sub>16</sub><br>036F <sub>16</sub> | UART0 Receive Buffer Register                  | U0RB   | XX <sub>16</sub><br>XX <sub>16</sub> |
| 0370 <sub>16</sub>                       |  |        |                                      |
| 0371 <sub>16</sub>                       |  |        |                                      |
| 0372 <sub>16</sub>                       |  |        |                                      |
| 0373 <sub>16</sub>                       |  |        |                                      |
| 0374 <sub>16</sub>                       |  |        |                                      |
| 0375 <sub>16</sub>                       |  |        |                                      |
| 0376 <sub>16</sub>                       |  |        |                                      |
| 0377 <sub>16</sub>                       |  |        |                                      |
| 0378 <sub>16</sub>                       | DMA0 Request Source Select Register            | DM0SL  | 0X00 0000 <sub>2</sub>               |
| 0379 <sub>16</sub>                       | DMA1 Request Source Select Register            | DM1SL  | 0X00 0000 <sub>2</sub>               |
| 037A <sub>16</sub>                       | DMA2 Request Source Select Register            | DM2SL  | 0X00 0000 <sub>2</sub>               |
| 037B <sub>16</sub>                       | DMA3 Request Source Select Register            | DM3SL  | 0X00 0000 <sub>2</sub>               |
| 037C <sub>16</sub><br>037D <sub>16</sub> | CRC Data Register                              | CRCD   | XX <sub>16</sub><br>XX <sub>16</sub> |
| 037E <sub>16</sub><br>037F <sub>16</sub> | CRC Input Register                             | CRCIN  | XX <sub>16</sub><br>XX <sub>16</sub> |

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The TCSPR register maintains values set before reset, even after software reset or watchdog timer reset has been performed.

| Address                                  | Register                | Symbol  | Value after RESET                                |
|--|-------------------------|---------|--|
| 0380 <sub>16</sub><br>0381 <sub>16</sub> | A/D0 Register 0         | AD00    | XXXX XXXX <sub>2</sub><br>0000 0000 <sub>2</sub> |
| 0382 <sub>16</sub><br>0383 <sub>16</sub> | A/D0 Register 1         | AD01    | XX <sub>16</sub><br>XX <sub>16</sub>             |
| 0384 <sub>16</sub><br>0385 <sub>16</sub> | A/D0 Register 2         | AD02    | XX <sub>16</sub><br>XX <sub>16</sub>             |
| 0386 <sub>16</sub><br>0387 <sub>16</sub> | A/D0 Register 3         | AD03    | XX <sub>16</sub><br>XX <sub>16</sub>             |
| 0388 <sub>16</sub><br>0389 <sub>16</sub> | A/D0 Register 4         | AD04    | XX <sub>16</sub><br>XX <sub>16</sub>             |
| 038A <sub>16</sub><br>038B <sub>16</sub> | A/D0 Register 5         | AD05    | XX <sub>16</sub><br>XX <sub>16</sub>             |
| 038C <sub>16</sub><br>038D <sub>16</sub> | A/D0 Register 6         | AD06    | XX <sub>16</sub><br>XX <sub>16</sub>             |
| 038E <sub>16</sub><br>038F <sub>16</sub> | A/D0 Register 7         | AD07    | XX <sub>16</sub><br>XX <sub>16</sub>             |
| 0390 <sub>16</sub>                       |                         |         |  |
| 0391 <sub>16</sub>                       |                         |         |  |
| 0392 <sub>16</sub>                       | A/D0 Control Register 4 | AD0CON4 | XXXX 00XX <sub>2</sub>                           |
| 0393 <sub>16</sub>                       |                         |         |  |
| 0394 <sub>16</sub>                       | A/D0 Control Register 2 | AD0CON2 | XX0X X000 <sub>2</sub>                           |
| 0395 <sub>16</sub>                       | A/D0 Control Register 3 | AD0CON3 | XXXX X000 <sub>2</sub>                           |
| 0396 <sub>16</sub>                       | A/D0 Control Register 0 | AD0CON0 | 00 <sub>16</sub>                                 |
| 0397 <sub>16</sub>                       | A/D0 Control Register 1 | AD0CON1 | 00 <sub>16</sub>                                 |
| 0398 <sub>16</sub>                       | D/A Register 0          | DA0     | XX <sub>16</sub>                                 |
| 0399 <sub>16</sub>                       |                         |         |  |
| 039A <sub>16</sub>                       | D/A Register 1          | DA1     | XX <sub>16</sub>                                 |
| 039B <sub>16</sub>                       |                         |         |  |
| 039C <sub>16</sub>                       | D/A Control Register    | DACON   | XXXX XX00 <sub>2</sub>                           |
| 039D <sub>16</sub>                       |                         |         |  |
| 039E <sub>16</sub>                       |                         |         |  |
| 039F <sub>16</sub>                       |                         |         |  |

X: Indeterminate

Blank spaces are reserved. No access is allowed.

## &lt;144-pin Package&gt;

| Address            | Register                    | Symbol | Value after RESET      |
|--------------------|-----------------------------|--------|------------------------|
| 03A0 <sub>16</sub> | Function Select Register A8 | PS8    | X000 0000 <sub>2</sub> |
| 03A1 <sub>16</sub> | Function Select Register A9 | PS9    | 00 <sub>16</sub>       |
| 03A2 <sub>16</sub> |                             |        |                        |
| 03A3 <sub>16</sub> |                             |        |                        |
| 03A4 <sub>16</sub> |                             |        |                        |
| 03A5 <sub>16</sub> |                             |        |                        |
| 03A6 <sub>16</sub> |                             |        |                        |
| 03A7 <sub>16</sub> | Function Select Register D1 | PSD1   | X0XX XX00 <sub>2</sub> |
| 03A8 <sub>16</sub> |                             |        |                        |
| 03A9 <sub>16</sub> |                             |        |                        |
| 03AA <sub>16</sub> |                             |        |                        |
| 03AB <sub>16</sub> |                             |        |                        |
| 03AC <sub>16</sub> | Function Select Register C2 | PSC2   | XXXX X00X <sub>2</sub> |
| 03AD <sub>16</sub> | Function Select Register C3 | PSC3   | X0XX XXXX <sub>2</sub> |
| 03AE <sub>16</sub> |                             |        |                        |
| 03AF <sub>16</sub> | Function Select Register C  | PSC    | 00X0 0000 <sub>2</sub> |
| 03B0 <sub>16</sub> | Function Select Register A0 | PS0    | 00 <sub>16</sub>       |
| 03B1 <sub>16</sub> | Function Select Register A1 | PS1    | 00 <sub>16</sub>       |
| 03B2 <sub>16</sub> | Function Select Register B0 | PSL0   | 00 <sub>16</sub>       |
| 03B3 <sub>16</sub> | Function Select Register B1 | PSL1   | 00 <sub>16</sub>       |
| 03B4 <sub>16</sub> | Function Select Register A2 | PS2    | 00X0 0000 <sub>2</sub> |
| 03B5 <sub>16</sub> | Function Select Register A3 | PS3    | 00 <sub>16</sub>       |
| 03B6 <sub>16</sub> | Function Select Register B2 | PSL2   | 00X0 0000 <sub>2</sub> |
| 03B7 <sub>16</sub> | Function Select Register B3 | PSL3   | 00 <sub>16</sub>       |
| 03B8 <sub>16</sub> |                             |        |                        |
| 03B9 <sub>16</sub> | Function Select Register A5 | PS5    | XXX0 0000 <sub>2</sub> |
| 03BA <sub>16</sub> |                             |        |                        |
| 03BB <sub>16</sub> |                             |        |                        |
| 03BC <sub>16</sub> |                             |        |                        |
| 03BD <sub>16</sub> |                             |        |                        |
| 03BE <sub>16</sub> |                             |        |                        |
| 03BF <sub>16</sub> |                             |        |                        |
| 03C0 <sub>16</sub> | Port P6 Register            | P6     | XX <sub>16</sub>       |
| 03C1 <sub>16</sub> | Port P7 Register            | P7     | XX <sub>16</sub>       |
| 03C2 <sub>16</sub> | Port P6 Direction Register  | PD6    | 00 <sub>16</sub>       |
| 03C3 <sub>16</sub> | Port P7 Direction Register  | PD7    | 00 <sub>16</sub>       |
| 03C4 <sub>16</sub> | Port P8 Register            | P8     | XX <sub>16</sub>       |
| 03C5 <sub>16</sub> | Port P9 Register            | P9     | XX <sub>16</sub>       |
| 03C6 <sub>16</sub> | Port P8 Direction Register  | PD8    | 00X0 0000 <sub>2</sub> |
| 03C7 <sub>16</sub> | Port P9 Direction Register  | PD9    | 00 <sub>16</sub>       |
| 03C8 <sub>16</sub> | Port P10 Register           | P10    | XX <sub>16</sub>       |
| 03C9 <sub>16</sub> | Port P11 Register           | P11    | XX <sub>16</sub>       |
| 03CA <sub>16</sub> | Port P10 Direction Register | PD10   | 00 <sub>16</sub>       |
| 03CB <sub>16</sub> | Port P11 Direction Register | PD11   | XXX0 0000 <sub>2</sub> |
| 03CC <sub>16</sub> | Port P12 Register           | P12    | XX <sub>16</sub>       |
| 03CD <sub>16</sub> | Port P13 Register           | P13    | XX <sub>16</sub>       |
| 03CE <sub>16</sub> | Port P12 Direction Register | PD12   | 00 <sub>16</sub>       |
| 03CF <sub>16</sub> | Port P13 Direction Register | PD13   | 00 <sub>16</sub>       |

X: Indeterminate

Blank spaces are reserved. No access is allowed.

## &lt;144-pin Package&gt;

| Address            | Register                    | Symbol | Value after RESET      |
|--------------------|-----------------------------|--------|------------------------|
| 03D0 <sub>16</sub> | Port P14 Register           | P14    | XX <sub>16</sub>       |
| 03D1 <sub>16</sub> | Port P15 Register           | P15    | XX <sub>16</sub>       |
| 03D2 <sub>16</sub> | Port P14 Direction Register | PD14   | X000 0000 <sub>2</sub> |
| 03D3 <sub>16</sub> | Port P15 Direction Register | PD15   | 00 <sub>16</sub>       |
| 03D4 <sub>16</sub> |                             |        |                        |
| 03D5 <sub>16</sub> |                             |        |                        |
| 03D6 <sub>16</sub> |                             |        |                        |
| 03D7 <sub>16</sub> |                             |        |                        |
| 03D8 <sub>16</sub> |                             |        |                        |
| 03D9 <sub>16</sub> |                             |        |                        |
| 03DA <sub>16</sub> | Pull-Up Control Register 2  | PUR2   | 00 <sub>16</sub>       |
| 03DB <sub>16</sub> | Pull-Up Control Register 3  | PUR3   | 00 <sub>16</sub>       |
| 03DC <sub>16</sub> | Pull-Up Control Register 4  | PUR4   | XXXX 0000 <sub>2</sub> |
| 03DD <sub>16</sub> |                             |        |                        |
| 03DE <sub>16</sub> |                             |        |                        |
| 03DF <sub>16</sub> |                             |        |                        |
| 03E0 <sub>16</sub> | Port P0 Register            | P0     | XX <sub>16</sub>       |
| 03E1 <sub>16</sub> | Port P1 Register            | P1     | XX <sub>16</sub>       |
| 03E2 <sub>16</sub> | Port P0 Direction Register  | PD0    | 00 <sub>16</sub>       |
| 03E3 <sub>16</sub> | Port P1 Direction Register  | PD1    | 00 <sub>16</sub>       |
| 03E4 <sub>16</sub> | Port P2 Register            | P2     | XX <sub>16</sub>       |
| 03E5 <sub>16</sub> | Port P3 Register            | P3     | XX <sub>16</sub>       |
| 03E6 <sub>16</sub> | Port P2 Direction Register  | PD2    | 00 <sub>16</sub>       |
| 03E7 <sub>16</sub> | Port P3 Direction Register  | PD3    | 00 <sub>16</sub>       |
| 03E8 <sub>16</sub> | Port P4 Register            | P4     | XX <sub>16</sub>       |
| 03E9 <sub>16</sub> | Port P5 Register            | P5     | XX <sub>16</sub>       |
| 03EA <sub>16</sub> | Port P4 Direction Register  | PD4    | 00 <sub>16</sub>       |
| 03EB <sub>16</sub> | Port P5 Direction Register  | PD5    | 00 <sub>16</sub>       |
| 03EC <sub>16</sub> |                             |        |                        |
| 03ED <sub>16</sub> |                             |        |                        |
| 03EE <sub>16</sub> |                             |        |                        |
| 03EF <sub>16</sub> |                             |        |                        |
| 03F0 <sub>16</sub> | Pull-Up Control Register 0  | PUR0   | 00 <sub>16</sub>       |
| 03F1 <sub>16</sub> | Pull-Up Control Register 1  | PUR1   | XXXX 0000 <sub>2</sub> |
| 03F2 <sub>16</sub> |                             |        |                        |
| 03F3 <sub>16</sub> |                             |        |                        |
| 03F4 <sub>16</sub> |                             |        |                        |
| 03F5 <sub>16</sub> |                             |        |                        |
| 03F6 <sub>16</sub> |                             |        |                        |
| 03F7 <sub>16</sub> |                             |        |                        |
| 03F8 <sub>16</sub> |                             |        |                        |
| 03F9 <sub>16</sub> |                             |        |                        |
| 03FA <sub>16</sub> |                             |        |                        |
| 03FB <sub>16</sub> |                             |        |                        |
| 03FC <sub>16</sub> |                             |        |                        |
| 03FD <sub>16</sub> |                             |        |                        |
| 03FE <sub>16</sub> |                             |        |                        |
| 03FF <sub>16</sub> | Port Control Register       | PCR    | XXXX XXX0 <sub>2</sub> |

X: Indeterminate

Blank spaces are reserved. No access is allowed.



## &lt;100-pin Package&gt;

| Address            | Register                                 | Symbol | Value after RESET      |
|--------------------|--|--------|------------------------|
| 03A0 <sub>16</sub> |  |        |                        |
| 03A1 <sub>16</sub> |  |        |                        |
| 03A2 <sub>16</sub> |  |        |                        |
| 03A3 <sub>16</sub> |  |        |                        |
| 03A4 <sub>16</sub> |  |        |                        |
| 03A5 <sub>16</sub> |  |        |                        |
| 03A6 <sub>16</sub> |  |        |                        |
| 03A7 <sub>16</sub> | Function Select Register D1              | PSD1   | X0XX XX00 <sub>2</sub> |
| 03A8 <sub>16</sub> |  |        |                        |
| 03A9 <sub>16</sub> |  |        |                        |
| 03AA <sub>16</sub> |  |        |                        |
| 03AB <sub>16</sub> |  |        |                        |
| 03AC <sub>16</sub> | Function Select Register C2              | PSC2   | XXXX X00X <sub>2</sub> |
| 03AD <sub>16</sub> | Function Select Register C3              | PSC3   | X0XX XXXX <sub>2</sub> |
| 03AE <sub>16</sub> |  |        |                        |
| 03AF <sub>16</sub> | Function Select Register C               | PSC    | 00X0 0000 <sub>2</sub> |
| 03B0 <sub>16</sub> | Function Select Register A0              | PS0    | 00 <sub>16</sub>       |
| 03B1 <sub>16</sub> | Function Select Register A1              | PS1    | 00 <sub>16</sub>       |
| 03B2 <sub>16</sub> | Function Select Register B0              | PSL0   | 00 <sub>16</sub>       |
| 03B3 <sub>16</sub> | Function Select Register B1              | PSL1   | 00 <sub>16</sub>       |
| 03B4 <sub>16</sub> | Function Select Register A2              | PS2    | 00X0 0000 <sub>2</sub> |
| 03B5 <sub>16</sub> | Function Select Register A3              | PS3    | 00 <sub>16</sub>       |
| 03B6 <sub>16</sub> | Function Select Register B2              | PSL2   | 00X0 0000 <sub>2</sub> |
| 03B7 <sub>16</sub> | Function Select Register B3              | PSL3   | 00 <sub>16</sub>       |
| 03B8 <sub>16</sub> |  |        |                        |
| 03B9 <sub>16</sub> |  |        |                        |
| 03BA <sub>16</sub> |  |        |                        |
| 03BB <sub>16</sub> |  |        |                        |
| 03BC <sub>16</sub> |  |        |                        |
| 03BD <sub>16</sub> |  |        |                        |
| 03BE <sub>16</sub> |  |        |                        |
| 03BF <sub>16</sub> |  |        |                        |
| 03C0 <sub>16</sub> | Port P6 Register                         | P6     | XX <sub>16</sub>       |
| 03C1 <sub>16</sub> | Port P7 Register                         | P7     | XX <sub>16</sub>       |
| 03C2 <sub>16</sub> | Port P6 Direction Register               | PD6    | 00 <sub>16</sub>       |
| 03C3 <sub>16</sub> | Port P7 Direction Register               | PD7    | 00 <sub>16</sub>       |
| 03C4 <sub>16</sub> | Port P8 Register                         | P8     | XX <sub>16</sub>       |
| 03C5 <sub>16</sub> | Port P9 Register                         | P9     | XX <sub>16</sub>       |
| 03C6 <sub>16</sub> | Port P8 Direction Register               | PD8    | 00X0 0000 <sub>2</sub> |
| 03C7 <sub>16</sub> | Port P9 Direction Register               | PD9    | 00 <sub>16</sub>       |
| 03C8 <sub>16</sub> | Port P10 Register                        | P10    | XX <sub>16</sub>       |
| 03C9 <sub>16</sub> |  |        |                        |
| 03CA <sub>16</sub> | Port P10 Direction Register              | PD10   | 00 <sub>16</sub>       |
| 03CB <sub>16</sub> | Set default value to "FF <sub>16</sub> " |        |                        |
| 03CC <sub>16</sub> |  |        |                        |
| 03CD <sub>16</sub> |  |        |                        |
| 03CE <sub>16</sub> | Set default value to "FF <sub>16</sub> " |        |                        |
| 03CF <sub>16</sub> | Set default value to "FF <sub>16</sub> " |        |                        |

X: Indeterminate

Blank spaces are reserved. No access is allowed.

## &lt;100-pin Package&gt;

| Address            | Register                                 | Symbol | Value after RESET      |
|--------------------|--|--------|------------------------|
| 03D0 <sub>16</sub> |  |        |                        |
| 03D1 <sub>16</sub> |  |        |                        |
| 03D2 <sub>16</sub> | Set default value to "FF <sub>16</sub> " |        |                        |
| 03D3 <sub>16</sub> | Set default value to "FF <sub>16</sub> " |        |                        |
| 03D4 <sub>16</sub> |  |        |                        |
| 03D5 <sub>16</sub> |  |        |                        |
| 03D6 <sub>16</sub> |  |        |                        |
| 03D7 <sub>16</sub> |  |        |                        |
| 03D8 <sub>16</sub> |  |        |                        |
| 03D9 <sub>16</sub> |  |        |                        |
| 03DA <sub>16</sub> | Pull-Up Control Register 2               | PUR2   | 00 <sub>16</sub>       |
| 03DB <sub>16</sub> | Pull-Up Control Register 3               | PUR3   | 00 <sub>16</sub>       |
| 03DC <sub>16</sub> | Set default value to "00 <sub>16</sub> " |        |                        |
| 03DD <sub>16</sub> |  |        |                        |
| 03DE <sub>16</sub> |  |        |                        |
| 03DF <sub>16</sub> |  |        |                        |
| 03E0 <sub>16</sub> | Port P0 Register                         | P0     | XX <sub>16</sub>       |
| 03E1 <sub>16</sub> | Port P1 Register                         | P1     | XX <sub>16</sub>       |
| 03E2 <sub>16</sub> | Port P0 Direction Register               | PD0    | 00 <sub>16</sub>       |
| 03E3 <sub>16</sub> | Port P1 Direction Register               | PD1    | 00 <sub>16</sub>       |
| 03E4 <sub>16</sub> | Port P2 Register                         | P2     | XX <sub>16</sub>       |
| 03E5 <sub>16</sub> | Port P3 Register                         | P3     | XX <sub>16</sub>       |
| 03E6 <sub>16</sub> | Port P2 Direction Register               | PD2    | 00 <sub>16</sub>       |
| 03E7 <sub>16</sub> | Port P3 Direction Register               | PD3    | 00 <sub>16</sub>       |
| 03E8 <sub>16</sub> | Port P4 Register                         | P4     | XX <sub>16</sub>       |
| 03E9 <sub>16</sub> | Port P5 Register                         | P5     | XX <sub>16</sub>       |
| 03EA <sub>16</sub> | Port P4 Direction Register               | PD4    | 00 <sub>16</sub>       |
| 03EB <sub>16</sub> | Port P5 Direction Register               | PD5    | 00 <sub>16</sub>       |
| 03EC <sub>16</sub> |  |        |                        |
| 03ED <sub>16</sub> |  |        |                        |
| 03EE <sub>16</sub> |  |        |                        |
| 03EF <sub>16</sub> |  |        |                        |
| 03F0 <sub>16</sub> | Pull-up Control Register 0               | PUR0   | 00 <sub>16</sub>       |
| 03F1 <sub>16</sub> | Pull-up Control Register 1               | PUR1   | XXXX 0000 <sub>2</sub> |
| 03F2 <sub>16</sub> |  |        |                        |
| 03F3 <sub>16</sub> |  |        |                        |
| 03F4 <sub>16</sub> |  |        |                        |
| 03F5 <sub>16</sub> |  |        |                        |
| 03F6 <sub>16</sub> |  |        |                        |
| 03F7 <sub>16</sub> |  |        |                        |
| 03F8 <sub>16</sub> |  |        |                        |
| 03F9 <sub>16</sub> |  |        |                        |
| 03FA <sub>16</sub> |  |        |                        |
| 03FB <sub>16</sub> |  |        |                        |
| 03FC <sub>16</sub> |  |        |                        |
| 03FD <sub>16</sub> |  |        |                        |
| 03FE <sub>16</sub> |  |        |                        |
| 03FF <sub>16</sub> | Port Control Register                    | PCR    | XXXX XXX0 <sub>2</sub> |

X: Indeterminate

Blank spaces are reserved. No access is allowed.

## 5. Electrical Characteristics

### 5.1 Electrical Characteristics (M32C/84)

**Table 5.1 Absolute Maximum Ratings**

| Symbol                              | Parameter                     |  | Condition                          | Value                                  | Unit |
|-------------------------------------|-------------------------------|--|------------------------------------|--|------|
| V <sub>CC1</sub> , V <sub>CC2</sub> | Supply Voltage                |  | V <sub>CC1</sub> =AV <sub>CC</sub> | -0.3 to 6.0                            | V    |
| V <sub>CC2</sub>                    | Supply Voltage                |  | -                                  | -0.3 to V <sub>CC1</sub>               | V    |
| AV <sub>CC</sub>                    | Analog Supply Voltage         |  | V <sub>CC1</sub> =AV <sub>CC</sub> | -0.3 to 6.0                            | V    |
| V <sub>i</sub>                      | Input Voltage                 | RESET, CNV <sub>SS</sub> , BYTE, P60-P67, P72-P77, P80-P87, P90-P97, P100-P107, P140-P146, P150-P157 <sup>(1)</sup> , V <sub>REF</sub> , X <sub>IN</sub> |                                    | -0.3 to V <sub>CC1</sub> +0.3          | V    |
|                                     |                               | P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P110-P114, P120-P127, P130-P137 <sup>(1)</sup>   |                                    | -0.3 to V <sub>CC2</sub> +0.3          |      |
|                                     |                               | P70, P71   |                                    | -0.3 to 6.0                            |      |
| V <sub>o</sub>                      | Output Voltage                | P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P140-P146, P150-P157 <sup>(1)</sup> , X <sub>OUT</sub>  |                                    | -0.3 to V <sub>CC1</sub> +0.3          | V    |
|                                     |                               | P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P110-P114, P120-P127, P130-P137 <sup>(1)</sup>   |                                    | -0.3 to V <sub>CC2</sub> +0.3          |      |
|                                     |                               | P70, P71   |                                    | -0.3 to 6.0                            |      |
| P <sub>d</sub>                      | Power Dissipation             |  | T <sub>opr</sub> =25° C            | 500                                    | mW   |
| T <sub>opr</sub>                    | Operating Ambient Temperature | during CPU operation   |                                    | -20 to 85/<br>-40 to 85 <sup>(2)</sup> | ° C  |
|                                     |                               | during flash memory program and erase operation  |                                    | 0 to 60                                |      |
| T <sub>stg</sub>                    | Storage Temperature           |  |                                    | -65 to 150                             | ° C  |

**NOTES:**

1. P11 to P15 are provided in the 144-pin package only.
2. Contact Renesas Technology Sales Co., Ltd, if temperature range of -40 to 85° C is required.

**Table 5.2 Recommended Operating Conditions**  
**(VCC1= VCC2=3.0V to 5.5V at Topr=– 20 to 85°C unless otherwise specified)**

| Symbol     | Parameter  | Standard  |         |      | Unit     |    |
|------------|--|---|---------|------|----------|----|
|            |  | Min.  | Typ.    | Max. |          |    |
| VCC1, VCC2 | Supply Voltage (VCC1≥ VCC2)                      | 3.0   | 5.0     | 5.5  | V        |    |
| AVCC       | Analog Supply Voltage                            |   | VCC1    |      | V        |    |
| VSS        | Supply Voltage                                   |   | 0       |      | V        |    |
| AVSS       | Analog Supply Voltage                            |   | 0       |      | V        |    |
| VIH        | Input High ("H") Voltage                         | P20-P27, P30-P37, P40-P47, P50-P57, P110-P114, P120-P127, P130-P137 <sup>(4)</sup>  | 0.8VCC2 |      | VCC2     | V  |
|            |  | P60-P67, P72-P77, P80-P87 <sup>(3)</sup> , P90-P97, P100-P107, P140-P146, P150-P157 <sup>(4)</sup> , XIN, RESET, CNVSS, BYTE  | 0.8VCC1 |      | VCC1     |    |
|            |  | P70, P71  | 0.8VCC1 |      | 6.0      |    |
|            |  | P00-P07, P10-P17 (in single-chip mode)  | 0.8VCC2 |      | VCC2     |    |
|            |  | P00-P07, P10-P17 (in memory expansion mode and microprocessor mode)   | 0.5VCC2 |      | VCC2     |    |
| VIL        | Input Low ("L") Voltage                          | P20-P27, P30-P37, P40-P47, P50-P57, P110-P114, P120-P127, P130-P137 <sup>(4)</sup>  | 0       |      | 0.2VCC2  | V  |
|            |  | P60-P67, P70-P77, P80-P87 <sup>(3)</sup> , P90-P97, P100-P107, P140-P146, P150-P157 <sup>(4)</sup> , XIN, RESET, CNVSS, BYTE  | 0       |      | 0.2VCC1  |    |
|            |  | P00-P07, P10-P17 (in single-chip mode)  | 0       |      | 0.2VCC2  |    |
|            |  | P00-P07, P10-P17 (in memory expansion mode and microprocessor mode)   | 0       |      | 0.16VCC2 |    |
| IOH(peak)  | Peak Output High ("H") Current <sup>(2)</sup>    | P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 <sup>(4)</sup> |         |      | -10.0    | mA |
| IOH(avg)   | Average Output High ("H") Current <sup>(1)</sup> | P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 <sup>(4)</sup> |         |      | -5.0     | mA |
| IOL(peak)  | Peak Output Low ("L") Current <sup>(2)</sup>     | P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 <sup>(4)</sup> |         |      | 10.0     | mA |
| IOL(avg)   | Average Output Low ("L") Current <sup>(1)</sup>  | P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 <sup>(4)</sup> |         |      | 5.0      | mA |

## NOTES:

- Typical values when average output current is 100ms.
- Total IOL(peak) for P0, P1, P2, P86, P87, P9, P10, P11, P14 and P15 must be 80mA or less.  
 Total IOL(peak) for P3, P4, P5, P6, P7, P80 to P84, P12 and P13 must be 80mA or less.  
 Total IOH(peak) for P0, P1, P2, and P11 must be -40mA or less.  
 Total IOH(peak) for P86, P87, P9, P10, P14 and P15 must be -40mA or less.  
 Total IOH(peak) for P3, P4, P5, P12 and P13 must be -40mA or less.  
 Total IOH(peak) for P6, P7, and P80 to P84 must be -40mA or less.
- VIH and VIL reference for P87 applies when P87 is used as a programmable input port.  
 It does not apply when P87 is used as XCIN.
- P11 to P15 are provided in the 144-pin package only.

**Table 5.2 Recommended Operating Conditions (Continued)**  
**(V<sub>CC1</sub>=V<sub>CC2</sub>=3.0V to 5.5V at Topr=-20 to 85°C unless otherwise specified)**

| Symbol               | Parameter   |                               | Standard |      |      | Unit |
|----------------------|---|-------------------------------|----------|------|------|------|
|                      |   |                               | Min.     | Typ. | Max. |      |
| f(BCLK)              | CPU Clock Frequency   | V <sub>CC1</sub> =4.2 to 5.5V | 0        |      | 32   | MHz  |
|                      |   | V <sub>CC1</sub> =3.0 to 5.5V | 0        |      | 24   | MHz  |
| f(XIN)               | Main Clock Input Frequency  | V <sub>CC1</sub> =4.2 to 5.5V | 0        |      | 32   | MHz  |
|                      |   | V <sub>CC1</sub> =3.0 to 5.5V | 0        |      | 24   | MHz  |
| f(XCIN)              | Sub Clock Frequency   |                               | 32.768   | 50   | kHz  |      |
| f(Ring)              | On-chip Oscillator Frequency (V <sub>CC1</sub> =V <sub>CC2</sub> =5.0V, Topr=25° C) |                               | 0.5      | 1    | 2    | MHz  |
| f(PLL)               | PLL Clock Frequency   | V <sub>CC1</sub> =4.2 to 5.5V | 10       |      | 32   | MHz  |
|                      |   | V <sub>CC1</sub> =3.0 to 5.5V | 10       |      | 24   | MHz  |
| t <sub>SU(PLL)</sub> | Wait Time to Stabilize PLL Frequency Synthesizer                                    | V <sub>CC1</sub> =5.0V        |          |      | 5    | ms   |
|                      |   | V <sub>CC1</sub> =3.3V        |          |      | 10   | ms   |

$V_{CC1}=V_{CC2}=5V$

**Table 5.3 Electrical Characteristics****( $V_{CC1}=V_{CC2}=4.2$  to  $5.5V$ ,  $V_{SS}=0V$  at  $T_{opr}=-20$  to  $85^{\circ}C$ ,  $f(BCLK)=32MHz$  unless otherwise specified)**

| Symbol                           | Parameter                 | Condition   | Standard                |                       |      | Unit             |     |    |
|----------------------------------|---------------------------|---|-------------------------|-----------------------|------|------------------|-----|----|
|                                  |                           |   | Min.                    | Typ.                  | Max. |                  |     |    |
| V <sub>OH</sub>                  | Output High ("H") Voltage | P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P110-P114, P120-P127, P130-P137   | I <sub>OH</sub> =-5mA   | V <sub>CC2</sub> -2.0 |      | V <sub>CC2</sub> | V   |    |
|                                  |                           | P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P140-P146, P150-P157 <sup>(1)</sup>  | I <sub>OH</sub> =-5mA   | V <sub>CC1</sub> -2.0 |      | V <sub>CC1</sub> |     |    |
|                                  | X <sub>OUT</sub>          | P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P110-P114, P120-P127, P130-P137   | I <sub>OH</sub> =-200μA | V <sub>CC2</sub> -0.3 |      | V <sub>CC2</sub> | V   |    |
|                                  |                           | P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P140-P146, P150-P157 <sup>(1)</sup>  | I <sub>OH</sub> =-200μA | V <sub>CC1</sub> -0.3 |      | V <sub>CC1</sub> |     |    |
|                                  | X <sub>COUT</sub>         |   | I <sub>OH</sub> =-1mA   | 3.0                   |      | V <sub>CC1</sub> | V   |    |
|                                  |                           |   |                         |                       |      |                  |     |    |
|                                  |                           |   |                         |                       |      |                  |     |    |
| V <sub>OL</sub>                  | Output Low ("L") Voltage  | P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 <sup>(1)</sup>   | I <sub>OL</sub> =5mA    |                       |      | 2.0              | V   |    |
|                                  |                           | P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 <sup>(1)</sup>   | I <sub>OL</sub> =200μA  |                       |      | 0.45             |     |    |
|                                  | X <sub>OUT</sub>          |   | I <sub>OL</sub> =1mA    |                       |      | 2.0              | V   |    |
|                                  | X <sub>COUT</sub>         |   | High Power              | No load applied       |      | 0                |     | V  |
|                                  |                           |   | Low Power               | No load applied       |      | 0                |     |    |
|                                  |                           |   |                         |                       |      |                  |     |    |
| V <sub>T+</sub> -V <sub>T-</sub> | Hysteresis                | HOLD, RDY, TA0IN-TA4IN, TB0IN-TB5IN, INT0-INT5, ADTRG, CTS0-CTS4, CLK0-CLK4, TA0OUT-TA4OUT, NMI, K10-K13, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4   |                         | 0.2                   |      | 1.0              | V   |    |
|                                  |                           | RESET   |                         | 0.2                   |      | 1.8              |     |    |
| I <sub>IH</sub>                  | Input High ("H") Current  | P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 <sup>(1)</sup> , X <sub>IN</sub> , RESET, CNV <sub>SS</sub> , BYTE | V <sub>I</sub> =5V      |                       |      | 5.0              | μA  |    |
| I <sub>IL</sub>                  | Input Low ("L") Current   | P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 <sup>(1)</sup> , X <sub>IN</sub> , RESET, CNV <sub>SS</sub> , BYTE | V <sub>I</sub> =0V      |                       |      | -5.0             | μA  |    |
| R <sub>PULLUP</sub>              | Pull-up Resistance        | P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 <sup>(1)</sup>   | V <sub>I</sub> =0V      | Flash Memory          | 30   | 50               | 167 | kΩ |
|                                  |                           |   |                         | Masked ROM            | 20   | 40               | 167 |    |
| R <sub>fXIN</sub>                | Feedback Resistance       | X <sub>IN</sub>   |                         |                       |      | 1.5              | MΩ  |    |
| R <sub>fXCIN</sub>               | Feedback Resistance       | X <sub>CIN</sub>  |                         |                       |      | 10               | MΩ  |    |
| V <sub>RAM</sub>                 | RAM Standby Voltage       | In stop mode  |                         |                       |      | 2.0              | V   |    |

## NOTES:

1. P11 to P15 are provided in the 144-pin package only.

$V_{CC1}=V_{CC2}=5V$

**Table 5.3 Electrical Characteristics (Continued)****( $V_{CC1}=V_{CC2}=4.2$  to  $5.5V$ ,  $V_{SS}=0V$  at  $T_{opr} = -20$  to  $85^{\circ}C$ ,  $f(BCLK)=32MHz$  unless otherwise specified)**

| Symbol                                     | Parameter            | Measurement Condition  | Standard   |              |      | Unit |    |    |
|--|----------------------|--|--|--------------|------|------|----|----|
|  |                      |  | Min.   | Typ.         | Max. |      |    |    |
| I <sub>cc</sub>                            | Power Supply Current | In single-chip mode, output pins are left open and other pins are connected to V <sub>SS</sub> . | f(BCLK)=32 MHz, Square wave, No division   |              | 28   | 45   | mA |    |
|  |                      |  | f(BCLK)=32 kHz, In low-power consumption mode, Program running on ROM                | Flash Memory |      | 430  |    | μA |
|  |                      |  |  | Masked ROM   |      | 25   |    |    |
|  |                      |  | f(BCLK)=32 kHz, In low-power consumption mode, Program running on RAM <sup>(1)</sup> |              | 25   |      | μA |    |
|  |                      |  | f(BCLK)=32 kHz, In wait mode, T <sub>opr</sub> =25° C                                |              | 10   |      | μA |    |
|  |                      |  | While clock stops, T <sub>opr</sub> =25° C   |              | 0.8  | 5    | μA |    |
| While clock stops, T <sub>opr</sub> =85° C |                      |  | 50   | μA           |      |      |    |    |

## NOTES:

- Value is obtained when setting the FMSTP bit in the FMR0 register to "1" (flash memory stopped).

$V_{CC1}=V_{CC2}=5V$

**Table 5.4 A/D Conversion Characteristics ( $V_{CC1}=V_{CC2}=AV_{CC}=V_{REF}=4.2$  to  $5.5V$ ,  $V_{SS}=AV_{SS}=0V$  at  $T_{opr}=-20$  to  $85^{\circ}C$ ,  $f(BCLK) = 32MHz$  unless otherwise specified)**

| Symbol            | Parameter                                | Measurement Condition        |   | Standard |      |                  | Unit       |
|-------------------|--|------------------------------|---|----------|------|------------------|------------|
|                   |  |                              |   | Min.     | Typ. | Max.             |            |
| -                 | Resolution                               | $V_{REF}=V_{CC1}$            |   |          |      | 10               | Bits       |
| INL               | Integral Nonlinearity Error              | $V_{REF}=V_{CC1}=V_{CC2}=5V$ | AN <sub>0</sub> to AN <sub>7</sub> , AN <sub>00</sub> to AN <sub>07</sub> , AN <sub>20</sub> to AN <sub>27</sub> , AN <sub>150</sub> to AN <sub>157</sub> , ANEX <sub>0</sub> , ANEX <sub>1</sub> |          |      | $\pm 3$          | LSB        |
|                   |  |                              | External op-amp connection mode   |          |      | $\pm 7$          | LSB        |
|                   |  |                              |   |          |      |                  |            |
| DNL               | Differential Nonlinearity Error          |                              |   |          |      | $\pm 1$          | LSB        |
| -                 | Offset Error                             |                              |   |          |      | $\pm 3$          | LSB        |
| -                 | Gain Error                               |                              |   |          |      | $\pm 3$          | LSB        |
| RLADDER           | Resistor Ladder                          | $V_{REF}=V_{CC1}$            |   | 8        |      | 40               | k $\Omega$ |
| t <sub>CONV</sub> | 10-bit Conversion Time <sup>(1, 2)</sup> |                              |   | 2.06     |      |                  | $\mu s$    |
| t <sub>CONV</sub> | 8-bit Conversion Time <sup>(1, 2)</sup>  |                              |   | 1.75     |      |                  | $\mu s$    |
| t <sub>SAMP</sub> | Sampling Time <sup>(1)</sup>             |                              |   | 0.188    |      |                  | $\mu s$    |
| V <sub>REF</sub>  | Reference Voltage                        |                              |   | 2        |      | V <sub>CC1</sub> | V          |
| V <sub>IA</sub>   | Analog Input Voltage                     |                              |   | 0        |      | V <sub>REF</sub> | V          |

## NOTES:

1. Divide  $f(X_{IN})$ , if exceeding 16 MHz, to keep  $\phi_{AD}$  frequency at 16 MHz or less.
2. With using the sample and hold function.

**Table 5.5 D/A Conversion Characteristics ( $V_{CC1}=V_{CC2}=V_{REF}=4.2$  to  $5.5V$ ,  $V_{SS}=AV_{SS}=0V$  at  $T_{opr}=-20$  to  $85^{\circ}C$ ,  $f(BCLK) = 32MHz$  unless otherwise specified)**

| Symbol            | Parameter                            | Measurement Condition |  | Standard |      |      | Unit       |
|-------------------|--------------------------------------|-----------------------|--|----------|------|------|------------|
|                   |                                      |                       |  | Min.     | Typ. | Max. |            |
| -                 | Resolution                           |                       |  |          |      | 8    | Bits       |
| -                 | Absolute Accuracy                    |                       |  |          |      | 1.0  | %          |
| t <sub>SU</sub>   | Setup Time                           |                       |  |          |      | 3    | $\mu s$    |
| R <sub>O</sub>    | Output Resistance                    |                       |  | 4        | 10   | 20   | k $\Omega$ |
| I <sub>VREF</sub> | Reference Power Supply Input Current | (Note 1)              |  |          |      | 1.5  | mA         |

## NOTES:

1. Measurement when using one D/A converter. The DA<sub>i</sub> register (i=0, 1) of the D/A converter, not being used, is set to "00<sub>16</sub>". The resistor ladder in the A/D converter is excluded.  
I<sub>VREF</sub> flows even if the VCUT bit in the AD0CON1 register is set to "0" (no V<sub>REF</sub> connection).



$V_{CC1}=V_{CC2}=5V$

**Table 5.6 Flash Memory Version Electrical Characteristics ( $V_{CC1}=4.5$  to  $5.5V$ ,  $3.3$  to  $3.6V$  at  $T_{opr}=0$  to  $60^{\circ}C$  unless otherwise specified)**

| Symbol   | Parameter  |                | Standard |      |        | Unit    |
|----------|--|----------------|----------|------|--------|---------|
|          |  |                | Min.     | Typ. | Max.   |         |
| -        | Program and Erase Endurance <sup>(2)</sup>                     |                | 100      |      |        | cycles  |
| -        | Word Program Time ( $V_{CC1}=5.0V$ , $T_{opr}=25^{\circ}C$ )   |                |          | 25   | 200    | $\mu s$ |
| -        | Lock Bit Program Time  |                |          | 25   | 200    | $\mu s$ |
| -        | Block Erase Time<br>( $V_{CC1}=5.0V$ , $T_{opr}=25^{\circ}C$ ) | 4-Kbyte Block  |          | 0.3  | 4      | s       |
|          |  | 8-Kbyte Block  |          | 0.3  | 4      | s       |
|          |  | 32-Kbyte Block |          | 0.5  | 4      | s       |
|          |  | 64-Kbyte Block |          | 0.8  | 4      | s       |
| -        | All-Unlocked-Block Erase Time <sup>(1)</sup>                   |                |          |      | 4 x // | s       |
| $t_{PS}$ | Wait Time to Stabilize Flash Memory Circuit                    |                |          |      | 15     | $\mu s$ |
| -        | Data Hold Time ( $T_{opr}=-40$ to $85^{\circ}C$ )              |                | 10       |      |        | years   |

## NOTES:

1. //denotes the number of block to be erased.

2. Number of program-erase cycles per block.

If Program and Erase Endurance is //cycle ( $// \neq 100$ ), each block can be erased and programmed //cycles.

For example, if a 4-Kbyte block A is erased after programming a word data 2,048 times, each to a different address, this counts as one program and erase endurance. Data can not be programmed to the same address more than once without erasing the block. (rewrite prohibited).

$V_{CC1}=V_{CC2}=5V$

**Table 5.7 Voltage Detection Circuit Electrical Characteristics ( $V_{CC1}=V_{CC2}=3.0$  to  $5.5V$ ,  $V_{SS}=0V$  at  $T_{opr}=25^{\circ}C$  unless otherwise specified)**

| Symbol | Parameter  | Measurement Condition   | Standard |      |      | Unit |
|--------|--|-------------------------|----------|------|------|------|
|        |  |                         | Min.     | Typ. | Max. |      |
| Vdet4  | Low Voltage Detection Voltage <sup>(1)</sup>     | $V_{CC1}=3.0$ to $5.5V$ |          | 3.8  |      | V    |
| Vdet3  | Reset Space Detection Voltage <sup>(1)</sup>     |                         |          | 3.0  |      | V    |
| Vdet3s | Low Voltage Reset Hold Voltage                   |                         | 2.0      |      |      | V    |
| Vdet3r | Low Voltage Reset Release Voltage <sup>(2)</sup> |                         |          | 3.1  |      | V    |

NOTES:

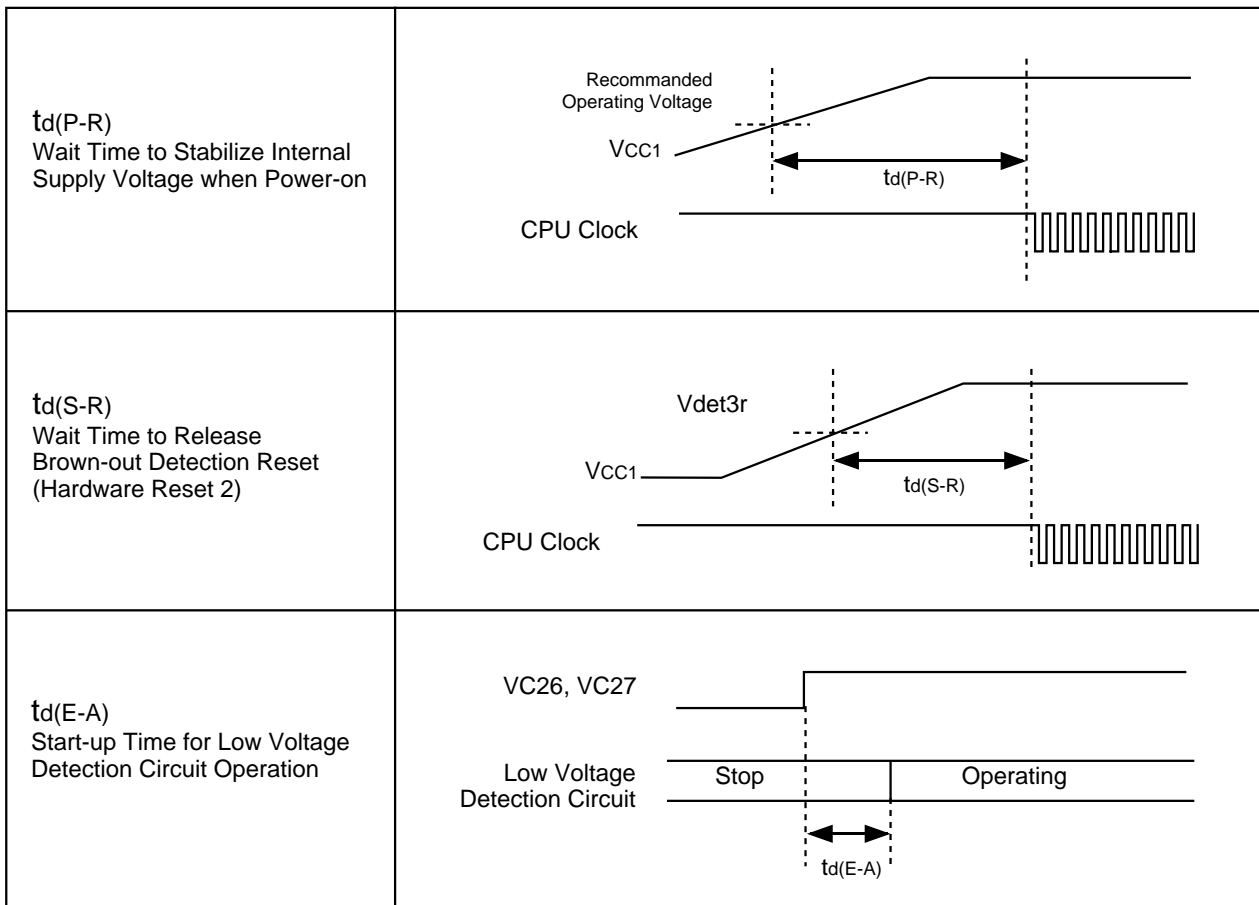
1.  $V_{det4} > V_{det3}$
2.  $V_{det3r} > V_{det3}$  is not guaranteed.

**Table 5.8 Power Supply Timing**

| Symbol  | Parameter  | Measurement Condition         | Standard |                  |      | Unit    |
|---------|--|-------------------------------|----------|------------------|------|---------|
|         |  |                               | Min.     | Typ.             | Max. |         |
| td(P-R) | Wait Time to Stabilize Internal Supply Voltage when Power-on | $V_{CC1}=3.0$ to $5.5V$       |          |                  | 2    | ms      |
| td(S-R) | Wait Time to Release Brown-out. Detection Reset              | $V_{CC1}=V_{det3r}$ to $5.5V$ |          | 6 <sup>(1)</sup> | 20   | ms      |
| td(E-A) | Start-up Time for Low Voltage Detection Circuit Operation    | $V_{CC1}=3.0$ to $5.5V$       |          |                  | 20   | $\mu s$ |

NOTES:

1.  $V_{CC1}=5V$



**Figure 5.1 Power Supply Timing Diagram**

$$V_{CC1}=V_{CC2}=5V$$

**Timing Requirements**

( $V_{CC1}=V_{CC2}=4.2$  to  $5.5V$ ,  $V_{SS}=0V$  at  $T_{opr}=-20$  to  $85^{\circ}C$  unless otherwise specified)

**Table 5.9 External Clock Input**

| Symbol     | Parameter                             | Standard |      | Unit |
|------------|---------------------------------------|----------|------|------|
|            |                                       | Min.     | Max. |      |
| $t_c$      | External Clock Input Cycle Time       | 31.25    |      | ns   |
| $t_{w(H)}$ | External Clock Input High ("H") Width | 13.75    |      | ns   |
| $t_{w(L)}$ | External Clock Input Low ("L") Width  | 13.75    |      | ns   |
| $t_r$      | External Clock Rise Time              |          | 5    | ns   |
| $t_f$      | External Clock Fall Time              |          | 5    | ns   |

**Table 5.10 Memory Expansion Mode and Microprocessor Mode**

| Symbol              | Parameter   | Standard |          | Unit |
|---------------------|---|----------|----------|------|
|                     |   | Min.     | Max.     |      |
| $t_{ac1(RD-DB)}$    | Data Input Access Time (RD standard)  |          | (Note 1) | ns   |
| $t_{ac1(AD-DB)}$    | Data Input Access Time (AD standard, CS standard)                                     |          | (Note 1) | ns   |
| $t_{ac2(RD-DB)}$    | Data Input Access Time (RD standard, when accessing a space with the multiplexrd bus) |          | (Note 1) | ns   |
| $t_{ac2(AD-DB)}$    | Data Input Access Time (AD standard, when accessing a space with the multiplexed bus) |          | (Note 1) | ns   |
| $t_{su(DB-BCLK)}$   | Data Input Setup Time   | 26       |          | ns   |
| $t_{su(RDY-BCLK)}$  | $\overline{RDY}$ Input Setup Time   | 26       |          | ns   |
| $t_{su(HOLD-BCLK)}$ | $\overline{HOLD}$ Input Setup Time  | 30       |          | ns   |
| $t_{h(RD-DB)}$      | Data Input Hold Time  | 0        |          | ns   |
| $t_{h(BCLK-RDY)}$   | $\overline{RDY}$ Input Hold Time  | 0        |          | ns   |
| $t_{h(BCLK-HOLD)}$  | $\overline{HOLD}$ Input Hold Time   | 0        |          | ns   |
| $t_{d(BCLK-HLDA)}$  | $\overline{HLDA}$ Output Delay Time   |          | 25       | ns   |

**NOTES:**

1. Values can be obtained from the following equations, according to BCLK frequency and external bus cycles. Insert a wait state or lower the operation frequency,  $f_{(BCLK)}$ , if the calculated value is negative.

$$t_{ac1(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \text{ (if external bus cycle is } a\phi + b\phi, m=(bx2)+1)$$

$$t_{ac1(AD-DB)} = \frac{10^9 \times n}{f_{(BCLK)}} - 35 \quad [\text{ns}] \text{ (if external bus cycle is } a\phi + b\phi, n=a+b)$$

$$t_{ac2(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \text{ (if external bus cycle is } a\phi + b\phi, m=(bx2)-1)$$

$$t_{ac2(AD-DB)} = \frac{10^9 \times p}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \text{ (if external bus cycle is } a\phi + b\phi, p=\{(a+b-1) \times 2\} + 1)$$

$V_{CC1}=V_{CC2}=5V$

**Timing Requirements****( $V_{CC1}=V_{CC2}=4.2$  to  $5.5V$ ,  $V_{SS}=0V$  at  $T_{op}=-20$  to  $85^{\circ}C$  unless otherwise specified)****Table 5.11 Timer A Input (Count Source Input in Event Counter Mode)**

| Symbol       | Parameter                    | Standard |      | Unit |
|--------------|------------------------------|----------|------|------|
|              |                              | Min.     | Max. |      |
| $t_{c(TA)}$  | TAiIN Input Cycle Time       | 100      |      | ns   |
| $t_{w(TAH)}$ | TAiIN Input High ("H") Width | 40       |      | ns   |
| $t_{w(TAL)}$ | TAiIN Input Low ("L") Width  | 40       |      | ns   |

**Table 5.12 Timer A Input (Gate Input in Timer Mode)**

| Symbol       | Parameter                    | Standard |      | Unit |
|--------------|------------------------------|----------|------|------|
|              |                              | Min.     | Max. |      |
| $t_{c(TA)}$  | TAiIN Input Cycle Time       | 400      |      | ns   |
| $t_{w(TAH)}$ | TAiIN Input High ("H") Width | 200      |      | ns   |
| $t_{w(TAL)}$ | TAiIN Input Low ("L") Width  | 200      |      | ns   |

**Table 5.13 Timer A Input (External Trigger Input in One-Shot Timer Mode)**

| Symbol       | Parameter                    | Standard |      | Unit |
|--------------|------------------------------|----------|------|------|
|              |                              | Min.     | Max. |      |
| $t_{c(TA)}$  | TAiIN Input Cycle Time       | 200      |      | ns   |
| $t_{w(TAH)}$ | TAiIN Input High ("H") Width | 100      |      | ns   |
| $t_{w(TAL)}$ | TAiIN Input Low ("L") Width  | 100      |      | ns   |

**Table 5.14 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)**

| Symbol       | Parameter                    | Standard |      | Unit |
|--------------|------------------------------|----------|------|------|
|              |                              | Min.     | Max. |      |
| $t_{w(TAH)}$ | TAiIN Input High ("H") Width | 100      |      | ns   |
| $t_{w(TAL)}$ | TAiIN Input Low ("L") Width  | 100      |      | ns   |

**Table 5.15 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)**

| Symbol           | Parameter                     | Standard |      | Unit |
|------------------|-------------------------------|----------|------|------|
|                  |                               | Min.     | Max. |      |
| $t_{c(UP)}$      | TAiOUT Input Cycle Time       | 2000     |      | ns   |
| $t_{w(UPH)}$     | TAiOUT Input High ("H") Width | 1000     |      | ns   |
| $t_{w(UPL)}$     | TAiOUT Input Low ("L") Width  | 1000     |      | ns   |
| $t_{su(UP-TIN)}$ | TAiOUT Input Setup Time       | 400      |      | ns   |
| $t_{h(TIN-UP)}$  | TAiOUT Input Hold Time        | 400      |      | ns   |

$V_{CC1}=V_{CC2}=5V$

**Timing Requirements****( $V_{CC1} = V_{CC2} = 4.2$  to  $5.5V$ ,  $V_{SS} = 0V$  at  $T_{opr} = -20$  to  $85^{\circ}C$  unless otherwise specified)****Table 5.16 Timer B Input (Count Source Input in Event Counter Mode)**

| Symbol       | Parameter  | Standard |      | Unit |
|--------------|--|----------|------|------|
|              |  | Min.     | Max. |      |
| $t_{c(TB)}$  | TBiIN Input Cycle Time (counted on one edge)         | 100      |      | ns   |
| $t_{w(TBH)}$ | TBiIN Input High ("H") Width (counted on one edge)   | 40       |      | ns   |
| $t_{w(TBL)}$ | TBiIN Input Low ("L") Width (counted on one edge)    | 40       |      | ns   |
| $t_{c(TB)}$  | TBiIN Input Cycle Time (counted on both edges)       | 200      |      | ns   |
| $t_{w(TBH)}$ | TBiIN Input High ("H") Width (counted on both edges) | 80       |      | ns   |
| $t_{w(TBL)}$ | TBiIN Input Low ("L") Width (counted on both edges)  | 80       |      | ns   |

**Table 5.17 Timer B Input (Pulse Period Measurement Mode)**

| Symbol       | Parameter                    | Standard |      | Unit |
|--------------|------------------------------|----------|------|------|
|              |                              | Min.     | Max. |      |
| $t_{c(TB)}$  | TBiIN Input Cycle Time       | 400      |      | ns   |
| $t_{w(TBH)}$ | TBiIN Input High ("H") Width | 200      |      | ns   |
| $t_{w(TBL)}$ | TBiIN Input Low ("L") Width  | 200      |      | ns   |

**Table 5.18 Timer B Input (Pulse Width Measurement Mode)**

| Symbol       | Parameter                    | Standard |      | Unit |
|--------------|------------------------------|----------|------|------|
|              |                              | Min.     | Max. |      |
| $t_{c(TB)}$  | TBiIN Input Cycle Time       | 400      |      | ns   |
| $t_{w(TBH)}$ | TBiIN Input High ("H") Width | 200      |      | ns   |
| $t_{w(TBL)}$ | TBiIN Input Low ("L") Width  | 200      |      | ns   |

**Table 5.19 A/D Trigger Input**

| Symbol       | Parameter                                     | Standard |      | Unit |
|--------------|---|----------|------|------|
|              |   | Min.     | Max. |      |
| $t_{c(AD)}$  | ADTRG Input Cycle Time (required for trigger) | 1000     |      | ns   |
| $t_{w(ADL)}$ | ADTRG Input Low ("L") Width                   | 125      |      | ns   |

**Table 5.20 Serial I/O**

| Symbol        | Parameter                   | Standard |      | Unit |
|---------------|-----------------------------|----------|------|------|
|               |                             | Min.     | Max. |      |
| $t_{c(CK)}$   | CLKi Input Cycle Time       | 200      |      | ns   |
| $t_{w(CKH)}$  | CLKi Input High ("H") Width | 100      |      | ns   |
| $t_{w(CKL)}$  | CLKi Input Low ("L") Width  | 100      |      | ns   |
| $t_{d(C-Q)}$  | TxDi Output Delay Time      |          | 80   | ns   |
| $t_{h(C-Q)}$  | TxDi Hold Time              | 0        |      | ns   |
| $t_{su(D-C)}$ | RxDi Input Setup Time       | 30       |      | ns   |
| $t_{h(C-Q)}$  | RxDi Input Hold Time        | 90       |      | ns   |

**Table 5.21 External Interrupt INTi Input**

| Symbol       | Parameter                   | Standard |      | Unit |
|--------------|-----------------------------|----------|------|------|
|              |                             | Min.     | Max. |      |
| $t_{w(INH)}$ | INTi Input High ("H") Width | 250      |      | ns   |
| $t_{w(INL)}$ | INTi Input Low ("L") Width  | 250      |      | ns   |

$$V_{CC1}=V_{CC2}=5V$$

### Switching Characteristics

( $V_{CC1} = V_{CC2} = 4.2$  to  $5.5V$ ,  $V_{SS} = 0V$  at  $T_{opr} = -20$  to  $85^{\circ}C$  unless otherwise specified)

**Table 5.22 Memory Expansion Mode and Microprocessor Mode  
(when accessing external memory space)**

| Symbol      | Parameter  | Measurement Condition | Standard |      | Unit |
|-------------|--|-----------------------|----------|------|------|
|             |  |                       | Min.     | Max. |      |
| td(BCLK-AD) | Address Output Delay Time  | See Figure 5.2        |          | 18   | ns   |
| th(BCLK-AD) | Address Output Hold Time (BCLK standard)                         |                       | -3       |      | ns   |
| th(RD-AD)   | Address Output Hold Time (RD standard) <sup>(3)</sup>            |                       | 0        |      | ns   |
| th(WR-AD)   | Address Output Hold Time (WR standard) <sup>(3)</sup>            |                       | (Note 1) |      | ns   |
| td(BCLK-CS) | Chip-Select Signal Output Delay Time                             |                       |          | 18   | ns   |
| th(BCLK-CS) | Chip-Select Signal Output Hold Time (BCLK standard)              |                       | -3       |      | ns   |
| th(RD-CS)   | Chip-Select Signal Output Hold Time (RD standard) <sup>(3)</sup> |                       | 0        |      | ns   |
| th(WR-CS)   | Chip-Select Signal Output Hold Time (WR standard) <sup>(3)</sup> |                       | (Note 1) |      | ns   |
| td(BCLK-RD) | RD Signal Output Delay Time                                      |                       |          | 18   | ns   |
| th(BCLK-RD) | RD Signal Output Hold Time                                       |                       | -5       |      | ns   |
| td(BCLK-WR) | WR Signal Output Delay Time                                      |                       |          | 18   | ns   |
| th(BCLK-WR) | WR Signal Output Hold Time                                       |                       | -5       |      | ns   |
| td(DB-WR)   | Data Output Delay Time (WR standard)                             |                       | (Note 2) |      | ns   |
| th(WR-DB)   | Data Output Hold Time (WR standard) <sup>(3)</sup>               |                       | (Note 1) |      | ns   |
| tW(WR)      | WR Output Width  |                       | (Note 2) |      | ns   |

#### NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

2. Values can be obtained from the following equations, according to BCLK frequency and external bus cycles.

$$t_{W(WR)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 15 \quad [ns] \quad (\text{if external bus cycle is } a\phi + b\phi, n=(bx2)-1)$$

$$t_{d(DB-WR)} = \frac{10^9 \times m}{f_{(BCLK)}} - 20 \quad [ns] \quad (\text{if external bus cycle is } a\phi + b\phi, m= b)$$

3.  $t_c$  ns is added when recovery cycle is inserted.

$$V_{CC1}=V_{CC2}=5V$$

### Switching Characteristics

( $V_{CC} = 4.2$  to  $5.5V$ ,  $V_{SS} = 0V$  at  $T_{opr} = -20$  to  $85^{\circ}C$  unless otherwise specified)

**Table 5.23 Memory Expansion Mode and Microprocessor Mode**  
(when accessing an external memory space with the multiplexed bus)

| Symbol            | Parameter  | Measurement Condition | Standard |      | Unit |
|-------------------|--|-----------------------|----------|------|------|
|                   |  |                       | Min.     | Max. |      |
| $t_{d(BCLK-AD)}$  | Address Output Delay Time  | See Figure 5.2        |          | 18   | ns   |
| $t_{h(BCLK-AD)}$  | Address Output Hold Time (BCLK standard)                         |                       | -3       |      | ns   |
| $t_{h(RD-AD)}$    | Address Output Hold Time (RD standard) <sup>(5)</sup>            |                       | (Note 1) |      | ns   |
| $t_{h(WR-AD)}$    | Address Output Hold Time (WR standard) <sup>(5)</sup>            |                       | (Note 1) |      | ns   |
| $t_{d(BCLK-CS)}$  | Chip-Select Signal Output Delay Time                             |                       |          | 18   | ns   |
| $t_{h(BCLK-CS)}$  | Chip-Select Signal Output Hold Time (BCLK standard)              |                       | -3       |      | ns   |
| $t_{h(RD-CS)}$    | Chip-Select Signal Output Hold Time (RD standard) <sup>(5)</sup> |                       | (Note 1) |      | ns   |
| $t_{h(WR-CS)}$    | Chip-Select Signal Output Hold Time (WR standard) <sup>(5)</sup> |                       | (Note 1) |      | ns   |
| $t_{d(BCLK-RD)}$  | RD Signal Output Delay Time                                      |                       |          | 18   | ns   |
| $t_{h(BCLK-RD)}$  | RD Signal Output Hold Time                                       |                       | -5       |      | ns   |
| $t_{d(BCLK-WR)}$  | WR Signal Output Delay Time                                      |                       |          | 18   | ns   |
| $t_{h(BCLK-WR)}$  | WR Signal Output Hold Time                                       |                       | -5       |      | ns   |
| $t_{d(DB-WR)}$    | Data Output Delay Time (WR standard)                             |                       | (Note 2) |      | ns   |
| $t_{h(WR-DB)}$    | Data Output Hold Time (WR standard) <sup>(5)</sup>               |                       | (Note 1) |      | ns   |
| $t_{d(BCLK-ALE)}$ | ALE Signal Output Delay Time (BCLK standard)                     |                       |          | 18   | ns   |
| $t_{h(BCLK-ALE)}$ | ALE Signal Output Hold Time (BCLK standard)                      |                       | -2       |      | ns   |
| $t_{d(AD-ALE)}$   | ALE Signal Output Delay Time (address standard)                  |                       | (Note 3) |      | ns   |
| $t_{h(ALE-AD)}$   | ALE Signal Output Hold Time (address standard)                   |                       | (Note 4) |      | ns   |
| $t_{dZ(RD-AD)}$   | Address Output Float Start Time                                  |                       |          | 8    | ns   |

#### NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$t_{h(RD-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(RD-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

2. Values can be obtained from the following equations, according to BCLK frequency and external bus cycle.

$$t_{d(DB-WR)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 25 \quad [ns] \quad (\text{if external bus cycle is } a\phi + b\phi, m = (bx2)-1)$$

3. Values can be obtained from the following equations, according to BCLK frequency and external bus cycle.

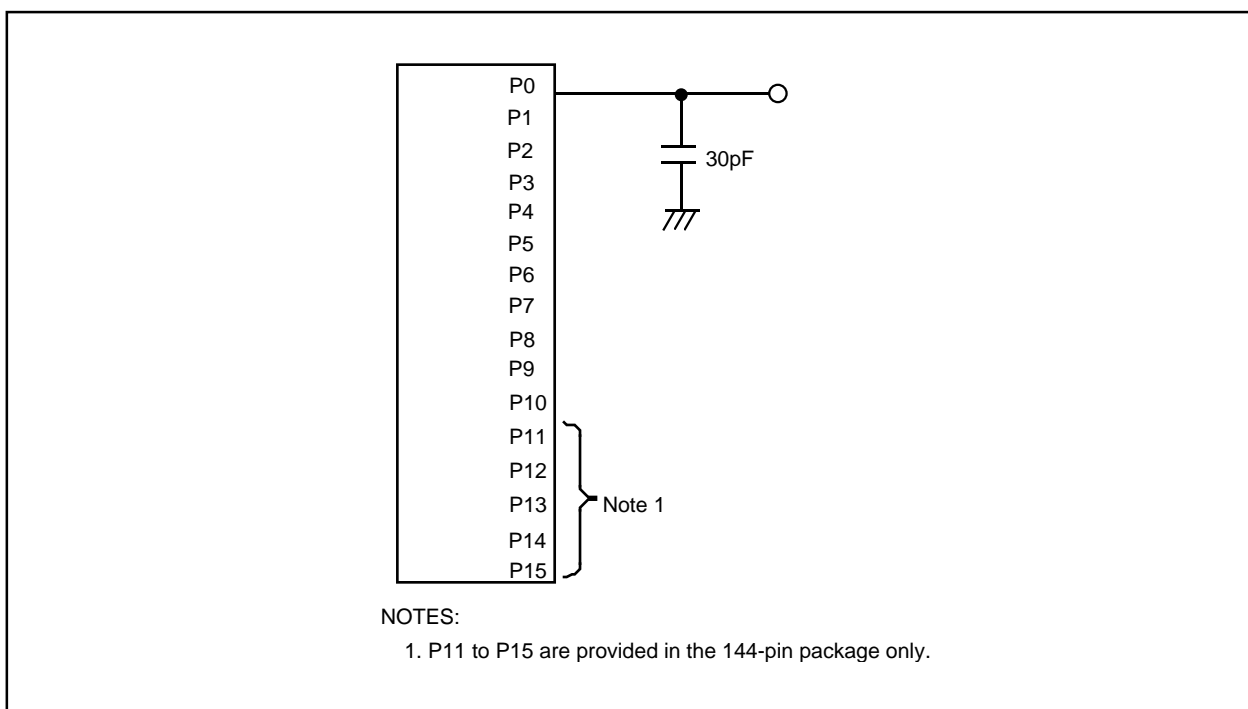
$$t_{d(AD-ALE)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 20 \quad [ns] \quad (\text{if external bus cycle is } a\phi + b\phi, n = a)$$

4. Values can be obtained from the following equations, according to BCLK frequency and external bus cycle.

$$t_{h(ALE-AD)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 10 \quad [ns] \quad (\text{if external bus cycle is } a\phi + b\phi, n = a)$$

5.  $t_{cns}$  is added when recovery cycle is inserted.

$$V_{CC1}=V_{CC2}=5V$$



**Figure 5.2 P0 to P15 Measurement Circuit**



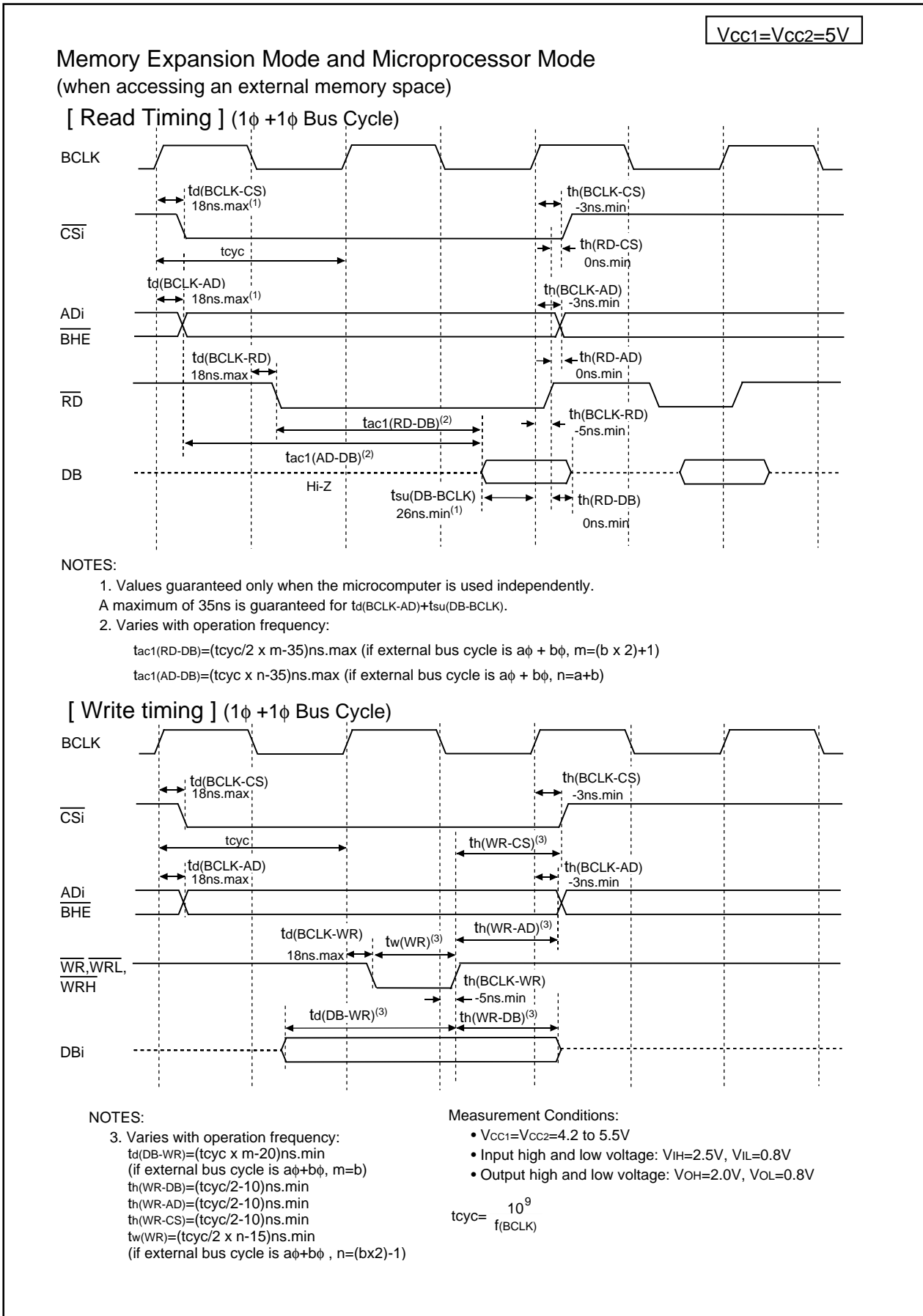


Figure 5.3 V<sub>CC1</sub>=V<sub>CC2</sub>=5V Timing Diagram (1)

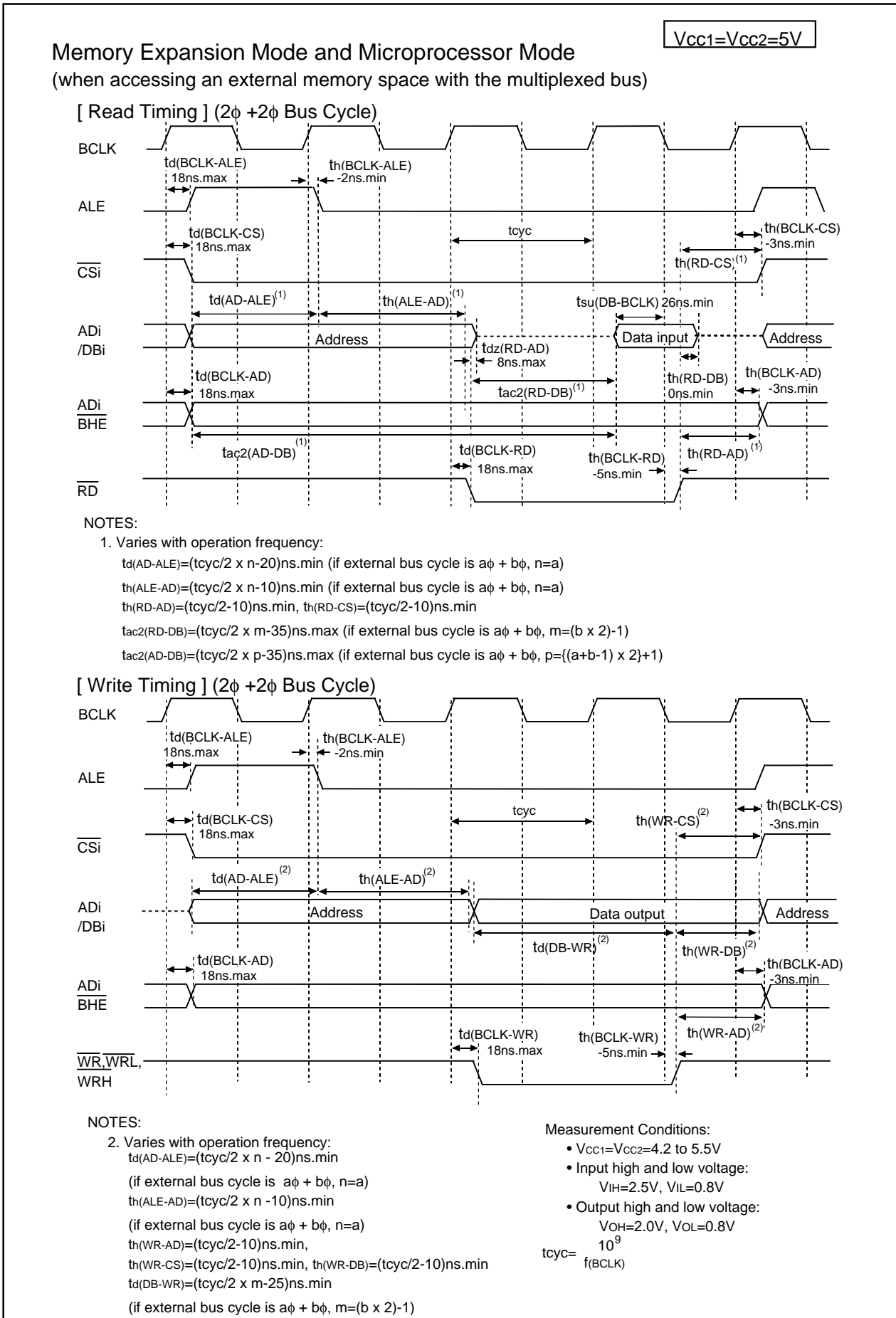


Figure 5.4 Vcc1=Vcc2=5V Timing Diagram (2)

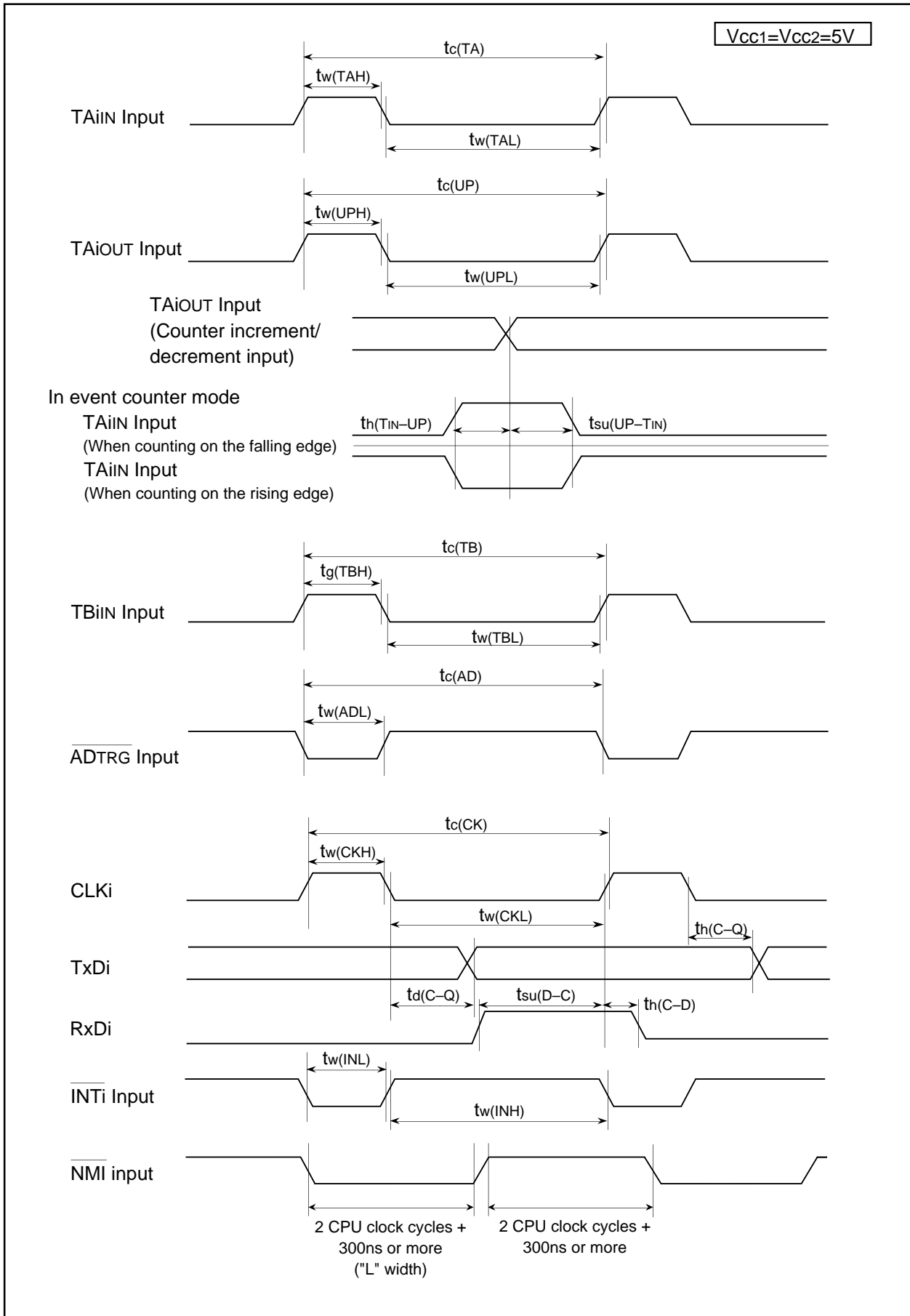


Figure 5.5 VCC1=VCC2=5V Timing Diagram (3)

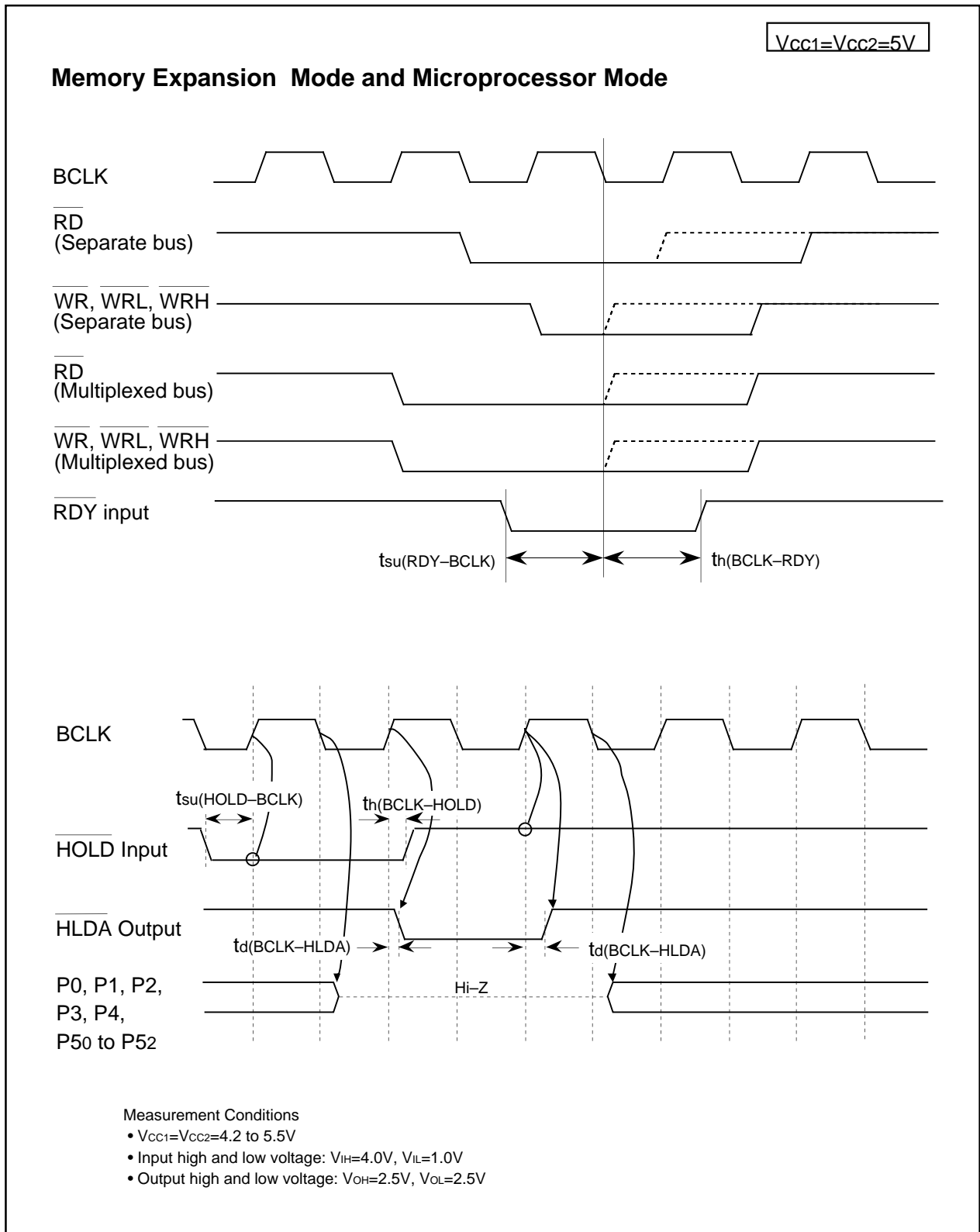


Figure 5.6  $V_{CC1}=V_{CC2}=5V$  Timing Diagram (4)

$V_{CC1}=V_{CC2}=3.3V$

**Table 5.24 Electrical Characteristics ( $V_{CC1}=V_{CC2}=3.0$  to  $3.6V$ ,  $V_{SS}=0V$  at  $T_{opr} = -20$  to  $85^{\circ}C$ ,  $f(BCLK)=24MHz$  unless otherwise specified)**

| Symbol                           | Parameter                 | Condition  | Standard  |                       |                  | Unit             |     |    |
|----------------------------------|---------------------------|--|---|-----------------------|------------------|------------------|-----|----|
|                                  |                           |  | Min.  | Typ.                  | Max.             |                  |     |    |
| V <sub>OH</sub>                  | Output High ("H") Voltage | P0 <sub>0</sub> -P0 <sub>7</sub> , P1 <sub>0</sub> -P1 <sub>7</sub> , P2 <sub>0</sub> -P2 <sub>7</sub> , P3 <sub>0</sub> -P3 <sub>7</sub> , P4 <sub>0</sub> -P4 <sub>7</sub> , P5 <sub>0</sub> -P5 <sub>7</sub> , P11 <sub>0</sub> -P11 <sub>4</sub> , P12 <sub>0</sub> -P12 <sub>7</sub> , P13 <sub>0</sub> -P13 <sub>7</sub>   | I <sub>OH</sub> =-1mA                                 | V <sub>CC2</sub> -0.6 |                  | V <sub>CC2</sub> | V   |    |
|                                  |                           | P6 <sub>0</sub> -P6 <sub>7</sub> , P7 <sub>2</sub> -P7 <sub>7</sub> , P8 <sub>0</sub> -P8 <sub>4</sub> , P8 <sub>6</sub> , P8 <sub>7</sub> , P9 <sub>0</sub> -P9 <sub>7</sub> , P10 <sub>0</sub> -P10 <sub>7</sub> , P14 <sub>0</sub> -P14 <sub>6</sub> , P15 <sub>0</sub> -P15 <sub>7</sub> <sup>(1)</sup>  |   | V <sub>CC1</sub> -0.6 |                  | V <sub>CC1</sub> | V   |    |
|                                  | X <sub>OUT</sub>          | I <sub>OH</sub> =-0.1mA  | 2.7   |                       | V <sub>CC1</sub> | V                |     |    |
|                                  | X <sub>COUT</sub>         | High Power   | No load applied                                       |                       | 2.5              |                  | V   |    |
|                                  |                           | Low Power  | No load applied                                       |                       | 1.6              |                  | V   |    |
| V <sub>OL</sub>                  | Output Low ("L") Voltage  | P0 <sub>0</sub> -P0 <sub>7</sub> , P1 <sub>0</sub> -P1 <sub>7</sub> , P2 <sub>0</sub> -P2 <sub>7</sub> , P3 <sub>0</sub> -P3 <sub>7</sub> , P4 <sub>0</sub> -P4 <sub>7</sub> , P5 <sub>0</sub> -P5 <sub>7</sub> , P6 <sub>0</sub> -P6 <sub>7</sub> , P7 <sub>0</sub> -P7 <sub>7</sub> , P8 <sub>0</sub> -P8 <sub>4</sub> , P8 <sub>6</sub> , P8 <sub>7</sub> , P9 <sub>0</sub> -P9 <sub>7</sub> , P10 <sub>0</sub> -P10 <sub>7</sub> , P11 <sub>0</sub> -P11 <sub>4</sub> , P12 <sub>0</sub> -P12 <sub>7</sub> , P13 <sub>0</sub> -P13 <sub>7</sub> , P14 <sub>0</sub> -P14 <sub>6</sub> , P15 <sub>0</sub> -P15 <sub>7</sub> <sup>(1)</sup>                 | I <sub>OL</sub> =1mA                                  |                       |                  | 0.5              | V   |    |
|                                  |                           | X <sub>OUT</sub>   | I <sub>OL</sub> =0.1mA                                |                       |                  | 0.5              | V   |    |
|                                  | X <sub>COUT</sub>         | High Power   | No load applied                                       |                       | 0                |                  | V   |    |
|                                  |                           | Low Power  | No load applied                                       |                       | 0                |                  | V   |    |
| V <sub>T+</sub> -V <sub>T-</sub> | Hysteresis                | HOLD, RDY, TA0 <sub>IN</sub> -TA4 <sub>IN</sub> , TB0 <sub>IN</sub> -TB5 <sub>IN</sub> , INT0-INT5, AD <sub>TRG</sub> , CTS0-CTS4, CLK0-CLK4, TA0 <sub>OUT</sub> -TA4 <sub>OUT</sub> , NMI, K10-K13, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4   |   | 0.2                   |                  | 1.0              | V   |    |
|                                  |                           | RESET  |   | 0.2                   |                  | 1.8              | V   |    |
| I <sub>IH</sub>                  | Input High ("H") Current  | P0 <sub>0</sub> -P0 <sub>7</sub> , P1 <sub>0</sub> -P1 <sub>7</sub> , P2 <sub>0</sub> -P2 <sub>7</sub> , P3 <sub>0</sub> -P3 <sub>7</sub> , P4 <sub>0</sub> -P4 <sub>7</sub> , P5 <sub>0</sub> -P5 <sub>7</sub> , P6 <sub>0</sub> -P6 <sub>7</sub> , P7 <sub>0</sub> -P7 <sub>7</sub> , P8 <sub>0</sub> -P8 <sub>7</sub> , P9 <sub>0</sub> -P9 <sub>7</sub> , P10 <sub>0</sub> -P10 <sub>7</sub> , P11 <sub>0</sub> -P11 <sub>4</sub> , P12 <sub>0</sub> -P12 <sub>7</sub> , P13 <sub>0</sub> -P13 <sub>7</sub> , P14 <sub>0</sub> -P14 <sub>6</sub> , P15 <sub>0</sub> -P15 <sub>7</sub> <sup>(1)</sup> , X <sub>IN</sub> , RESET, CNV <sub>SS</sub> , BYTE | V <sub>I</sub> =3V                                    |                       |                  | 4.0              | μA  |    |
| I <sub>IL</sub>                  | Input Low ("L") Current   | P0 <sub>0</sub> -P0 <sub>7</sub> , P1 <sub>0</sub> -P1 <sub>7</sub> , P2 <sub>0</sub> -P2 <sub>7</sub> , P3 <sub>0</sub> -P3 <sub>7</sub> , P4 <sub>0</sub> -P4 <sub>7</sub> , P5 <sub>0</sub> -P5 <sub>7</sub> , P6 <sub>0</sub> -P6 <sub>7</sub> , P7 <sub>0</sub> -P7 <sub>7</sub> , P8 <sub>0</sub> -P8 <sub>7</sub> , P9 <sub>0</sub> -P9 <sub>7</sub> , P10 <sub>0</sub> -P10 <sub>7</sub> , P11 <sub>0</sub> -P11 <sub>4</sub> , P12 <sub>0</sub> -P12 <sub>7</sub> , P13 <sub>0</sub> -P13 <sub>7</sub> , P14 <sub>0</sub> -P14 <sub>6</sub> , P15 <sub>0</sub> -P15 <sub>7</sub> <sup>(1)</sup> , X <sub>IN</sub> , RESET, CNV <sub>SS</sub> , BYTE | V <sub>I</sub> =0V                                    |                       |                  | -4.0             | μA  |    |
| R <sub>PULLUP</sub>              | Pull-up Resistance        | P0 <sub>0</sub> -P0 <sub>7</sub> , P1 <sub>0</sub> -P1 <sub>7</sub> , P2 <sub>0</sub> -P2 <sub>7</sub> , P3 <sub>0</sub> -P3 <sub>7</sub> , P4 <sub>0</sub> -P4 <sub>7</sub> , P5 <sub>0</sub> -P5 <sub>7</sub> , P6 <sub>0</sub> -P6 <sub>7</sub> , P7 <sub>2</sub> -P7 <sub>7</sub> , P8 <sub>0</sub> -P8 <sub>4</sub> , P8 <sub>6</sub> , P8 <sub>7</sub> , P9 <sub>0</sub> -P9 <sub>7</sub> , P10 <sub>0</sub> -P10 <sub>7</sub> , P11 <sub>0</sub> -P11 <sub>4</sub> , P12 <sub>0</sub> -P12 <sub>7</sub> , P13 <sub>0</sub> -P13 <sub>7</sub> , P14 <sub>0</sub> -P14 <sub>6</sub> , P15 <sub>0</sub> -P15 <sub>7</sub> <sup>(1)</sup>                 | V <sub>I</sub> =0V                                    | Flash Memory          | 66               | 120              | 500 | kΩ |
|                                  |                           |  |   | Masked ROM            | 40               | 70               | 500 | kΩ |
| R <sub>fXIN</sub>                | Feedback Resistance       | X <sub>IN</sub>  |   |                       |                  | 3.0              | MΩ  |    |
| R <sub>fXCIN</sub>               | Feedback Resistance       | X <sub>CIN</sub>   |   |                       |                  | 20.0             | MΩ  |    |
| V <sub>RAM</sub>                 | RAM Standby Voltage       | in stop mode   |   |                       | 2.0              |                  | V   |    |
| I <sub>CC</sub>                  | Power Supply Current      | Measurement condition: In single-chip mode, output pins are left open and other pins are connected to V <sub>SS</sub> .  | f(BCLK)=24 MHz, Square wave, No division              |                       | 22               | 35               | mA  |    |
|                                  |                           |  | f(BCLK)=32 kHz, In wait mode, T <sub>opr</sub> =25° C |                       | 10               |                  | μA  |    |
|                                  |                           |  | While clock stops, T <sub>opr</sub> =25° C            |                       | 0.8              | 5                | μA  |    |
|                                  |                           |  | While clock stops, T <sub>opr</sub> =85° C            |                       |                  | 50               | μA  |    |

## NOTES:

1. P11 to P15 are provided in the 144-pin package only.

$V_{CC1}=V_{CC2}=3.3V$

**Table 5.25 A/D Conversion Characteristics ( $V_{CC1}=V_{CC2}=AV_{CC}=V_{REF}=3.0$  to  $3.6V$ ,  $V_{SS}=AV_{SS}=0V$  at  $T_{opr} = -20$  to  $85^{\circ}C$ ,  $f(BCLK) = 24MHz$  unless otherwise specified)**

| Symbol  | Parameter                               |                | Measurement Condition          | Standard |      |           | Unit       |
|---------|---|----------------|--------------------------------|----------|------|-----------|------------|
|         |   |                |                                | Min.     | Typ. | Max.      |            |
| -       | Resolution                              |                | $V_{REF}=V_{CC1}$              |          |      | 10        | Bits       |
| INL     | Integral Nonlinearity Error             | No S&H (8-bit) | $V_{CC1}=V_{CC2}=V_{REF}=3.3V$ |          |      | $\pm 2$   | LSB        |
| DNL     | Differential Nonlinearity Error         | No S&H (8-bit) |                                |          |      | $\pm 1$   | LSB        |
| -       | Offset Error                            | No S&H (8-bit) |                                |          |      | $\pm 2$   | LSB        |
| -       | Gain Error                              | No S&H (8-bit) |                                |          |      | $\pm 2$   | LSB        |
| RLADDER | Resistor Ladder                         |                | $V_{REF}=V_{CC1}$              | 8        |      | 40        | k $\Omega$ |
| tCONV   | 8-bit Conversion Time <sup>(1, 2)</sup> |                |                                | 6.1      |      |           | $\mu s$    |
| VREF    | Reference Voltage                       |                |                                | 3        |      | $V_{CC1}$ | V          |
| VIA     | Analog Input Voltage                    |                |                                | 0        |      | $V_{REF}$ | V          |

S&amp;H: Sample and Hold

## NOTES:

1. Divide  $f(X_{IN})$ , if exceeding 10 MHz, to keep  $\phi AD$  frequency at 10 MHz or less.
2. S&H not available.

**Table 5.26 D/A Conversion Characteristics ( $V_{CC1}=V_{CC2}=V_{REF}=3.0$  to  $3.6V$ ,  $V_{SS}=AV_{SS}=0V$  at  $T_{opr} = -20$  to  $85^{\circ}C$ ,  $f(BCLK) = 24MHz$  unless otherwise specified)**

| Symbol            | Parameter                            |  | Measurement Condition | Standard |      |      | Unit       |
|-------------------|--------------------------------------|--|-----------------------|----------|------|------|------------|
|                   |                                      |  |                       | Min.     | Typ. | Max. |            |
| -                 | Resolution                           |  |                       |          |      | 8    | Bits       |
| -                 | Absolute Accuracy                    |  |                       |          |      | 1.0  | %          |
| tsu               | Setup Time                           |  |                       |          |      | 3    | $\mu s$    |
| Ro                | Output Resistance                    |  |                       | 4        | 10   | 20   | k $\Omega$ |
| I <sub>VREF</sub> | Reference Power Supply Input Current |  | (Note 1)              |          |      | 1.0  | mA         |

## NOTES:

1. Measurement results when using one D/A converter. The DA<sub>i</sub> register (i=0, 1) of the D/A converter, not being used, is set to "00<sub>16</sub>". The resistor ladder in the A/D converter is excluded.  
I<sub>VREF</sub> flows even if the VCUT bit in the AD0CON1 register is set to "0" (no V<sub>REF</sub> connection).

$$V_{CC1}=V_{CC2}=3.3V$$

### Timing Requirements

( $V_{CC1}=V_{CC2}= 3.0$  to  $3.6V$ ,  $V_{SS} = 0V$  at  $T_{opr} = -20$  to  $85^{\circ}C$  unless otherwise specified)

**Table 5.27 External Clock Input**

| Symbol     | Parameter                             | Standard |      | Unit |
|------------|---------------------------------------|----------|------|------|
|            |                                       | Min.     | Max. |      |
| $t_c$      | External Clock Input Cycle Time       | 41       |      | ns   |
| $t_{w(H)}$ | External Clock Input High ("H") Width | 18       |      | ns   |
| $t_{w(L)}$ | External Clock Input Low ("L") Width  | 18       |      | ns   |
| $t_r$      | External Clock Rise Time              |          | 5    | ns   |
| $t_f$      | External Clock Fall Time              |          | 5    | ns   |

**Table 5.28 Memory Expansion Mode and Microprocessor Mode**

| Symbol              | Parameter   | Standard |          | Unit |
|---------------------|---|----------|----------|------|
|                     |   | Min.     | Max.     |      |
| $t_{ac1(RD-DB)}$    | Data Input Access Time (RD standard)  |          | (Note 1) | ns   |
| $t_{ac1(AD-DB)}$    | Data Input Access Time (AD standard, CS standard)                                     |          | (Note 1) | ns   |
| $t_{ac2(RD-DB)}$    | Data Input Access Time (RD standard, when accessing a space with the multiplexed bus) |          | (Note 1) | ns   |
| $t_{ac2(AD-DB)}$    | Data Input Access Time (AD standard, when accessing a space with the multiplexed bus) |          | (Note 1) | ns   |
| $t_{su(DB-BCLK)}$   | Data Input Setup Time   | 30       |          | ns   |
| $t_{su(RDY-BCLK)}$  | $\overline{RDY}$ Input Setup Time   | 40       |          | ns   |
| $t_{su(HOLD-BCLK)}$ | HOLD Input Setup Time   | 60       |          | ns   |
| $t_{h(RD-DB)}$      | Data Input Hold Time  | 0        |          | ns   |
| $t_{h(BCLK-RDY)}$   | $\overline{RDY}$ Input Hold Time  | 0        |          | ns   |
| $t_{h(BCLK-HOLD)}$  | $\overline{HOLD}$ Input Hold Time   | 0        |          | ns   |
| $t_{d(BCLK-HLDA)}$  | $\overline{HLDA}$ Output Delay Time   |          | 25       | ns   |

**NOTES:**

1. Values can be obtained from the following equations, according to BCLK frequency and external bus cycles. Insert a wait state or lower the operation frequency,  $f_{(BCLK)}$ , if the calculated value is negative.

$$t_{ac1(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \text{ (if external bus cycle is } a\phi + b\phi, m=(bx2)+1)$$

$$t_{ac1(AD-DB)} = \frac{10^9 \times n}{f_{(BCLK)}} - 35 \quad [\text{ns}] \text{ (if external bus cycle is } a\phi + b\phi, n=a+b)$$

$$t_{ac2(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \text{ (if external bus cycle is } a\phi + b\phi, m=(bx2)-1)$$

$$t_{ac2(AD-DB)} = \frac{10^9 \times p}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \text{ (if external bus cycle is } a\phi + b\phi, p=\{(a+b-1)x2\}+1)$$

$V_{CC1}=V_{CC2}=3.3V$

**Timing Requirements****( $V_{CC1}=V_{CC2}= 3.0$  to  $3.6V$ ,  $V_{SS}= 0V$  at  $T_{opr} = -20$  to  $85^{\circ}C$  unless otherwise specified)****Table 5.29 Timer A Input (Count Source Input in Event Counter Mode)**

| Symbol       | Parameter                    | Standard |      | Unit |
|--------------|------------------------------|----------|------|------|
|              |                              | Min.     | Max. |      |
| $t_{C(TA)}$  | TAiIN Input Cycle Time       | 100      |      | ns   |
| $t_{W(TAH)}$ | TAiIN Input High ("H") Width | 40       |      | ns   |
| $t_{W(TAL)}$ | TAiIN Input Low ("L") Width  | 40       |      | ns   |

**Table 5.30 Timer A Input (Gate Input in Timer Mode)**

| Symbol       | Parameter                    | Standard |      | Unit |
|--------------|------------------------------|----------|------|------|
|              |                              | Min.     | Max. |      |
| $t_{C(TA)}$  | TAiIN Input Cycle Time       | 400      |      | ns   |
| $t_{W(TAH)}$ | TAiIN Input High ("H") Width | 200      |      | ns   |
| $t_{W(TAL)}$ | TAiIN Input Low ("L") Width  | 200      |      | ns   |

**Table 5.31 Timer A Input (External Trigger Input in One-Shot Timer Mode)**

| Symbol       | Parameter                    | Standard |      | Unit |
|--------------|------------------------------|----------|------|------|
|              |                              | Min.     | Max. |      |
| $t_{C(TA)}$  | TAiIN Input Cycle Time       | 200      |      | ns   |
| $t_{W(TAH)}$ | TAiIN Input High ("H") Width | 100      |      | ns   |
| $t_{W(TAL)}$ | TAiIN Input Low ("L") Width  | 100      |      | ns   |

**Table 5.32 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)**

| Symbol       | Parameter                    | Standard |      | Unit |
|--------------|------------------------------|----------|------|------|
|              |                              | Min.     | Max. |      |
| $t_{W(TAH)}$ | TAiIN Input High ("H") Width | 100      |      | ns   |
| $t_{W(TAL)}$ | TAiIN Input Low ("L") Width  | 100      |      | ns   |

**Table 5.33 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)**

| Symbol           | Parameter                     | Standard |      | Unit |
|------------------|-------------------------------|----------|------|------|
|                  |                               | Min.     | Max. |      |
| $t_{C(UP)}$      | TAiOUT Input Cycle Time       | 2000     |      | ns   |
| $t_{W(UPH)}$     | TAiOUT Input High ("H") Width | 1000     |      | ns   |
| $t_{W(UPL)}$     | TAiOUT Input Low ("L") Width  | 1000     |      | ns   |
| $t_{SU(UP-TIN)}$ | TAiOUT Input Setup Time       | 400      |      | ns   |
| $t_{H(TIN-UP)}$  | TAiOUT Input Hold Time        | 400      |      | ns   |



$V_{CC1}=V_{CC2}=3.3V$

**Timing Requirements**(V<sub>CC1</sub>=V<sub>CC2</sub>= 3.0 to 3.6V, V<sub>SS</sub> = 0V at Topr = –20 to 85°C unless otherwise specified)**Table 5.34 Timer B Input (Count Source Input in Event Counter Mode)**

| Symbol              | Parameter  | Standard |      | Unit |
|---------------------|--|----------|------|------|
|                     |  | Min.     | Max. |      |
| t <sub>c(TB)</sub>  | TB <sub>iIN</sub> Input Cycle Time (counted on one edge)         | 100      |      | ns   |
| t <sub>w(TBH)</sub> | TB <sub>iIN</sub> Input High ("H") Width (counted on one edge)   | 40       |      | ns   |
| t <sub>w(TBL)</sub> | TB <sub>iIN</sub> Input Low ("L") Width (counted on one edge)    | 40       |      | ns   |
| t <sub>c(TB)</sub>  | TB <sub>iIN</sub> Input Cycle Time (counted on both edges)       | 200      |      | ns   |
| t <sub>w(TBH)</sub> | TB <sub>iIN</sub> Input High ("H") Width (counted on both edges) | 80       |      | ns   |
| t <sub>w(TBL)</sub> | TB <sub>iIN</sub> Input Low ("L") Width (counted on both edges)  | 80       |      | ns   |

**Table 5.35 Timer B Input (Pulse Period Measurement Mode)**

| Symbol              | Parameter                                | Standard |      | Unit |
|---------------------|--|----------|------|------|
|                     |  | Min.     | Max. |      |
| t <sub>c(TB)</sub>  | TB <sub>iIN</sub> Input Cycle Time       | 400      |      | ns   |
| t <sub>w(TBH)</sub> | TB <sub>iIN</sub> Input High ("H") Width | 200      |      | ns   |
| t <sub>w(TBL)</sub> | TB <sub>iIN</sub> Input Low ("L") Width  | 200      |      | ns   |

**Table 5.36 Timer B Input (Pulse Width Measurement Mode)**

| Symbol              | Parameter                                | Standard |      | Unit |
|---------------------|--|----------|------|------|
|                     |  | Min.     | Max. |      |
| t <sub>c(TB)</sub>  | TB <sub>iIN</sub> Input Cycle Time       | 400      |      | ns   |
| t <sub>w(TBH)</sub> | TB <sub>iIN</sub> Input High ("H") Width | 200      |      | ns   |
| t <sub>w(TBL)</sub> | TB <sub>iIN</sub> Input Low ("L") Width  | 200      |      | ns   |

**Table 5.37 A/D Trigger Input**

| Symbol              | Parameter   | Standard |      | Unit |
|---------------------|---|----------|------|------|
|                     |   | Min.     | Max. |      |
| t <sub>c(AD)</sub>  | $\overline{AD}_{TRG}$ Input Cycle Time (required for trigger) | 1000     |      | ns   |
| t <sub>w(ADL)</sub> | $\overline{AD}_{TRG}$ Input Low ("L") Width                   | 125      |      | ns   |

**Table 5.38 Serial I/O**

| Symbol               | Parameter                               | Standard |      | Unit |
|----------------------|---|----------|------|------|
|                      |   | Min.     | Max. |      |
| t <sub>c(CK)</sub>   | CLK <sub>i</sub> Input Cycle Time       | 200      |      | ns   |
| t <sub>w(CKH)</sub>  | CLK <sub>i</sub> Input High ("H") Width | 100      |      | ns   |
| t <sub>w(CKL)</sub>  | CLK <sub>i</sub> Input Low ("L") Width  | 100      |      | ns   |
| t <sub>d(C-Q)</sub>  | TxD <sub>i</sub> Output Delay Time      |          | 80   | ns   |
| t <sub>h(C-Q)</sub>  | TxD <sub>i</sub> Hold Time              | 0        |      | ns   |
| t <sub>su(D-C)</sub> | RxD <sub>i</sub> Input Setup Time       | 30       |      | ns   |
| t <sub>h(C-Q)</sub>  | RxD <sub>i</sub> Input Hold Time        | 90       |      | ns   |

**Table 5.39 External Interrupt  $\overline{INT}_i$  Input**

| Symbol              | Parameter                                 | Standard |      | Unit |
|---------------------|---|----------|------|------|
|                     |   | Min.     | Max. |      |
| t <sub>w(INH)</sub> | $\overline{INT}_i$ Input High ("H") Width | 250      |      | ns   |
| t <sub>w(INL)</sub> | $\overline{INT}_i$ Input Low ("L") Width  | 250      |      | ns   |

$$V_{CC1}=V_{CC2}=3.3V$$

### Switching Characteristics

( $V_{CC1}=V_{CC2}=3.0$  to  $3.6V$ ,  $V_{SS} = 0V$  at  $T_{opr} = -20$  to  $85^{\circ}C$  unless otherwise specified)

**Table 5.40 Memory Expansion Mode and Microprocessor Mode  
(when accessing external memory space)**

| Symbol           | Parameter  | Measurement Condition | Standard |      | Unit |
|------------------|--|-----------------------|----------|------|------|
|                  |  |                       | Min.     | Max. |      |
| $t_{d(BCLK-AD)}$ | Address Output Delay Time  | See Figure 5.2        |          | 18   | ns   |
| $t_{h(BCLK-AD)}$ | Address Output Hold Time (BCLK standard)                         |                       | 0        |      | ns   |
| $t_{h(RD-AD)}$   | Address Output Hold Time (RD standard) <sup>(3)</sup>            |                       | 0        |      | ns   |
| $t_{h(WR-AD)}$   | Address Output Hold Time (WR standard) <sup>(3)</sup>            |                       | (Note 1) |      | ns   |
| $t_{d(BCLK-CS)}$ | Chip-Select Signal Output Delay Time                             |                       |          | 18   | ns   |
| $t_{h(BCLK-CS)}$ | Chip-Select Signal Output Hold Time (BCLK standard)              |                       | 0        |      | ns   |
| $t_{h(RD-CS)}$   | Chip-Select Signal Output Hold Time (RD standard) <sup>(3)</sup> |                       | 0        |      | ns   |
| $t_{h(WR-CS)}$   | Chip-Select Signal Output Hold Time (WR standard) <sup>(3)</sup> |                       | (Note 1) |      | ns   |
| $t_{d(BCLK-RD)}$ | RD Signal Output Delay Time                                      |                       |          | 18   | ns   |
| $t_{h(BCLK-RD)}$ | RD Signal Output Hold Time                                       |                       | -3       |      | ns   |
| $t_{d(BCLK-WR)}$ | WR Signal Output Delay Time                                      |                       |          | 18   | ns   |
| $t_{h(BCLK-WR)}$ | WR Signal Output Hold Time                                       |                       | 0        |      | ns   |
| $t_{d(DB-WR)}$   | Data Output Delay Time (WR standard)                             |                       | (Note 2) |      | ns   |
| $t_{h(WR-DB)}$   | Data Output Hold Time (WR standard) <sup>(3)</sup>               |                       | (Note 1) |      | ns   |
| $t_{w(WR)}$      | WR Output Width  |                       | (Note 2) |      | ns   |

#### NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 20 \quad [ns]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

2. Values can be obtained from the following equations, according to BCLK frequency and external bus cycles.

$$t_{w(WR)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 15 \quad [ns] \quad (\text{if external bus cycle is } a\phi + b\phi, n=(b \times 2)-1)$$

$$t_{d(DB-WR)} = \frac{10^9 \times m}{f_{(BCLK)}} - 20 \quad [ns] \quad (\text{if external bus cycle is } a\phi + b\phi, m=b)$$

3.  $t_{cns}$  is added when recovery cycle is inserted.

$V_{CC1}=V_{CC2}=3.3V$

**Switching Characteristics**(V<sub>CC1</sub> = V<sub>CC2</sub> = 3.0 to 3.6V, V<sub>SS</sub> = 0V at Topr = -20 to 85°C unless otherwise specified)**Table 5.41 Memory Expansion Mode and Microprocessor Mode  
(when accessing an external memory space with the multiplexed bus)**

| Symbol       | Parameter  | Measurement Condition | Standard |      | Unit |
|--------------|--|-----------------------|----------|------|------|
|              |  |                       | Min.     | Max. |      |
| td(BCLK-AD)  | Address Output Delay Time  | See Figure 5.2        |          | 18   | ns   |
| th(BCLK-AD)  | Address Output Hold Time (BCLK standard)                         |                       | 0        |      | ns   |
| th(RD-AD)    | Address Output Hold Time (RD standard) <sup>(5)</sup>            |                       | (Note 1) |      | ns   |
| th(WR-AD)    | Address Output Hold Time (WR standard) <sup>(5)</sup>            |                       | (Note 1) |      | ns   |
| td(BCLK-CS)  | Chip-Select Signal Output Delay Time                             |                       |          | 18   | ns   |
| th(BCLK-CS)  | Chip-Select Signal Output Hold Time (BCLK standard)              |                       | 0        |      | ns   |
| th(RD-CS)    | Chip-Select Signal Output Hold Time (RD standard) <sup>(5)</sup> |                       | (Note 1) |      | ns   |
| th(WR-CS)    | Chip-Select Signal Output Hold Time (WR standard) <sup>(5)</sup> |                       | (Note 1) |      | ns   |
| td(BCLK-RD)  | RD Signal Output Delay Time                                      |                       |          | 18   | ns   |
| th(BCLK-RD)  | RD Signal Output Hold Time                                       |                       | -3       |      | ns   |
| td(BCLK-WR)  | WR Signal Output Delay Time                                      |                       |          | 18   | ns   |
| th(BCLK-WR)  | WR Signal Output Hold Time                                       |                       | 0        |      | ns   |
| td(DB-WR)    | Data Output delay Time (WR standard)                             |                       | (Note 2) |      | ns   |
| th(WR-DB)    | Data Output Hold Time (WR standard) <sup>(5)</sup>               |                       | (Note 1) |      | ns   |
| td(BCLK-ALE) | ALE Signal Output Delay Time (BCLK standard)                     |                       |          | 18   | ns   |
| th(BCLK-ALE) | ALE Signal Output Hold Time (BCLK standard)                      |                       | -2       |      | ns   |
| td(AD-ALE)   | ALE Signal Output Delay Time (address standard)                  |                       | (Note 3) |      | ns   |
| th(ALE-AD)   | ALE Signal Output Hold Time (address standard)                   |                       | (Note 4) |      | ns   |
| tdz(RD-AD)   | Address Output Float Start Time                                  |                       |          | 8    | ns   |

**NOTES:**

1. Values can be obtained by the following equations, according to BCLK frequency.

$$th(RD - AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR - AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(RD - CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR - CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR - DB) = \frac{10^9}{f(BCLK) \times 2} - 20 \quad [ns]$$

2. Values can be obtained by the following equations, according to BCLK frequency and external bus cycles.

$$td(DB - WR) = \frac{10^9 \times m}{f(BCLK) \times 2} - 25 \quad [ns] \quad (\text{if external bus cycle is } a\phi + b\phi, m=(b+2)-1)$$

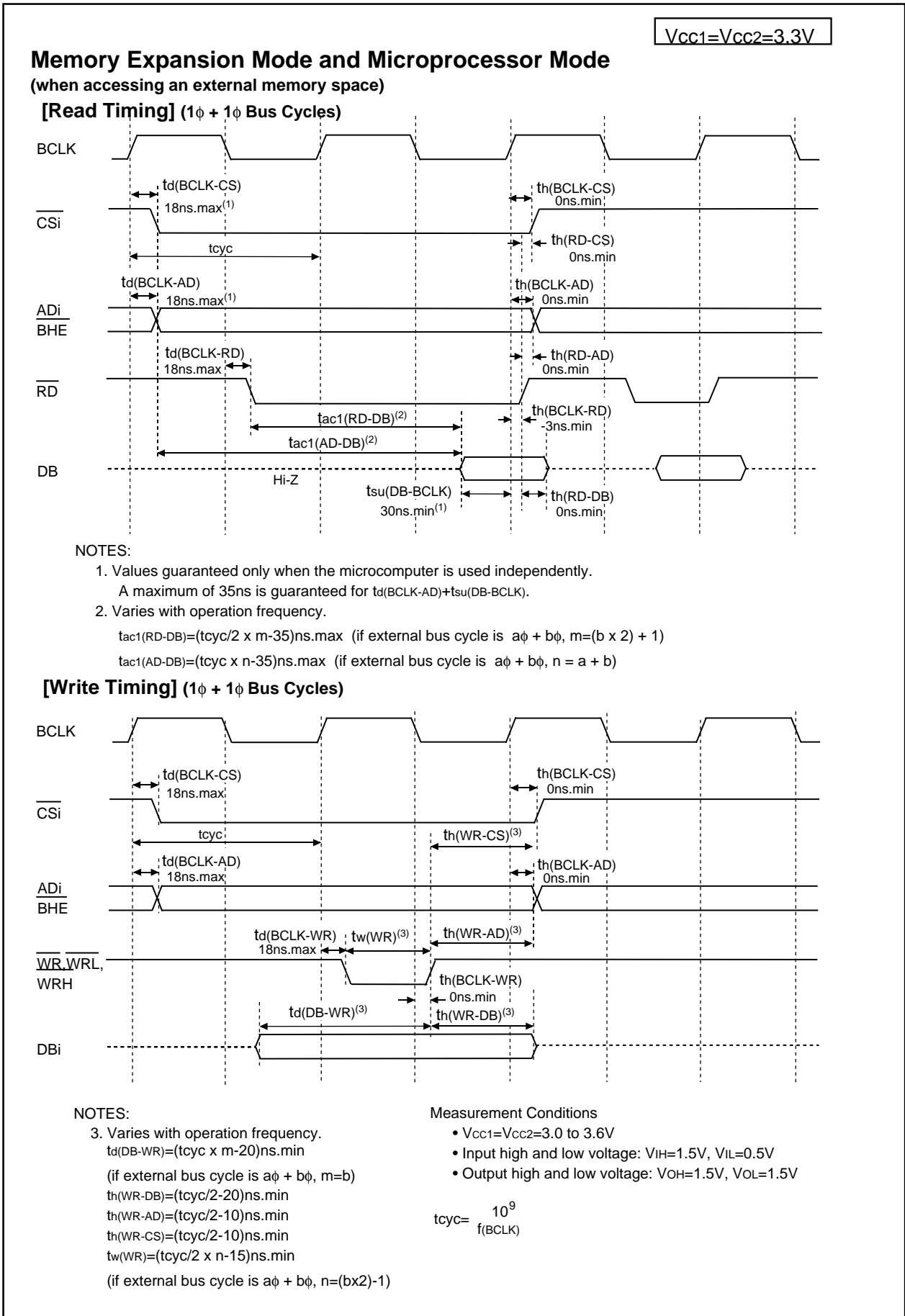
3. Values can be obtained by the following equations, according to BCLK frequency and external bus cycles.

$$td(AD - ALE) = \frac{10^9 \times n}{f(BCLK) \times 2} - 20 \quad [ns] \quad (\text{if external bus cycle is } a\phi + b\phi, n=a)$$

4. Values can be obtained by the following equations, according to BCLK frequency and external bus cycles.

$$th(ALE - AD) = \frac{10^9 \times n}{f(BCLK) \times 2} - 10 \quad [ns] \quad (\text{if external bus cycle is } a\phi + b\phi, n=a)$$

5. tc ns is added when recovery cycle is inserted.



**Figure 5.7 V<sub>CC1</sub>=V<sub>CC2</sub>=3.3V Timing Diagram (1)**

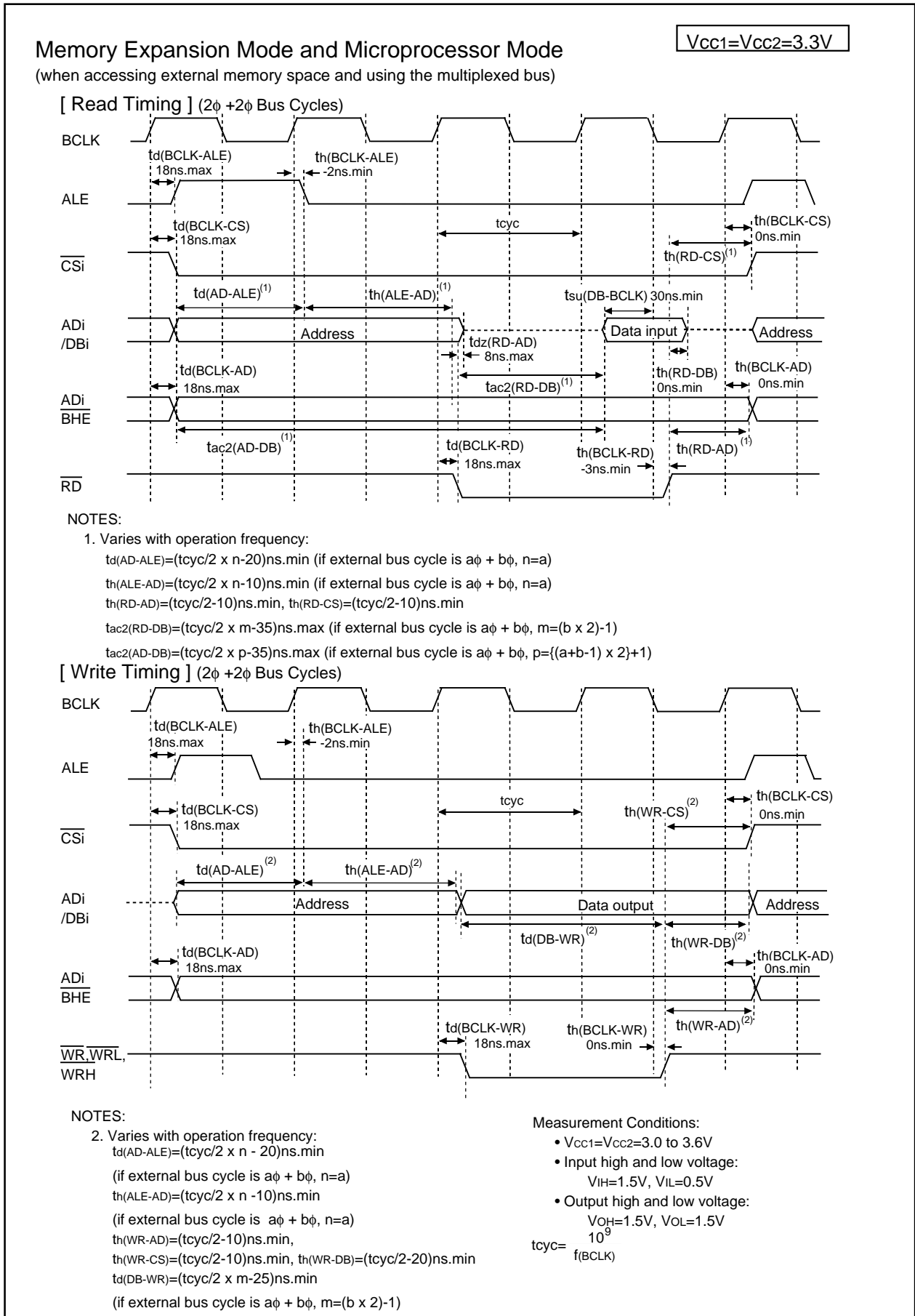


Figure 5.8 V<sub>CC1</sub>=V<sub>CC2</sub>=3.3V Timing Diagram (2)

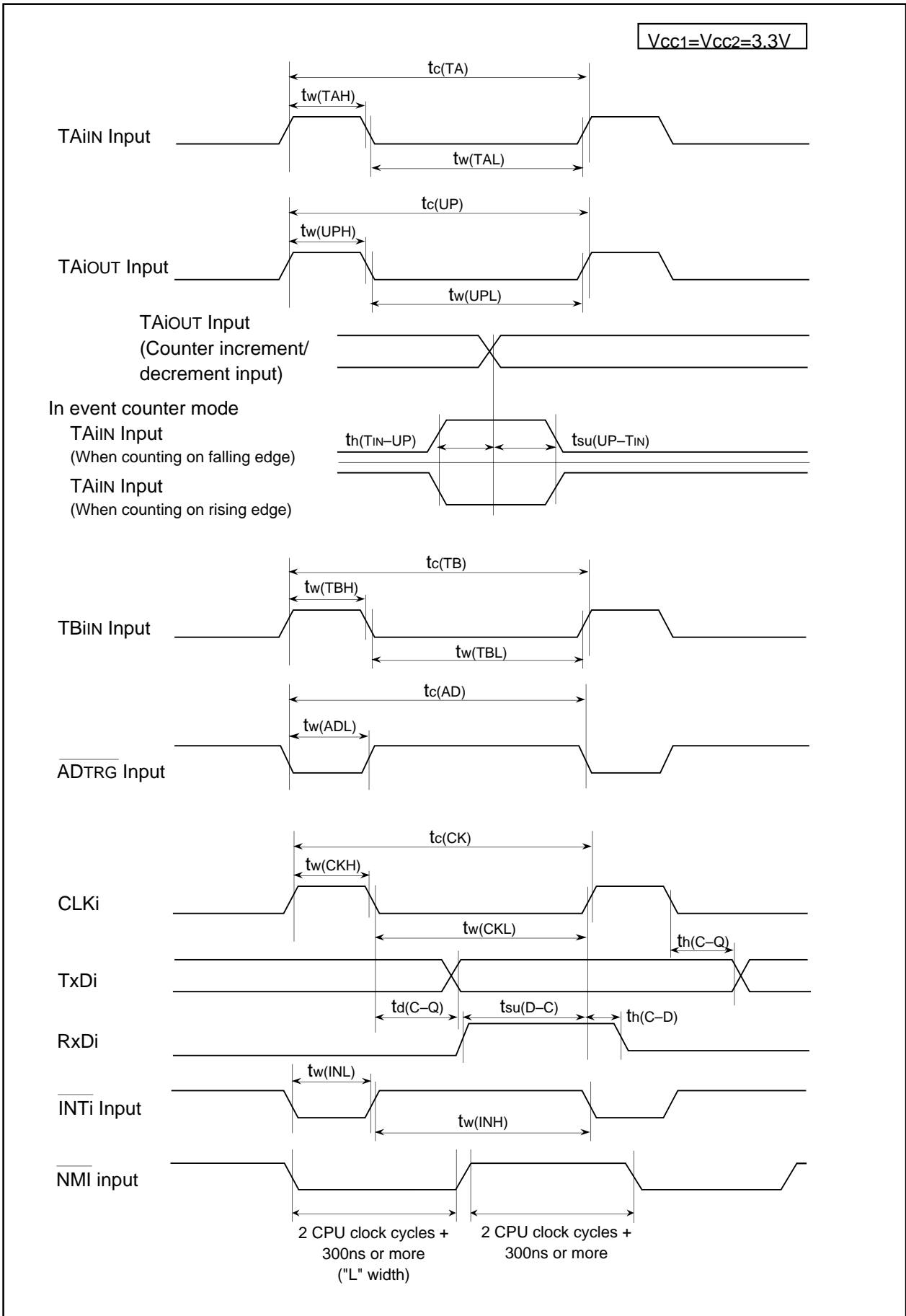
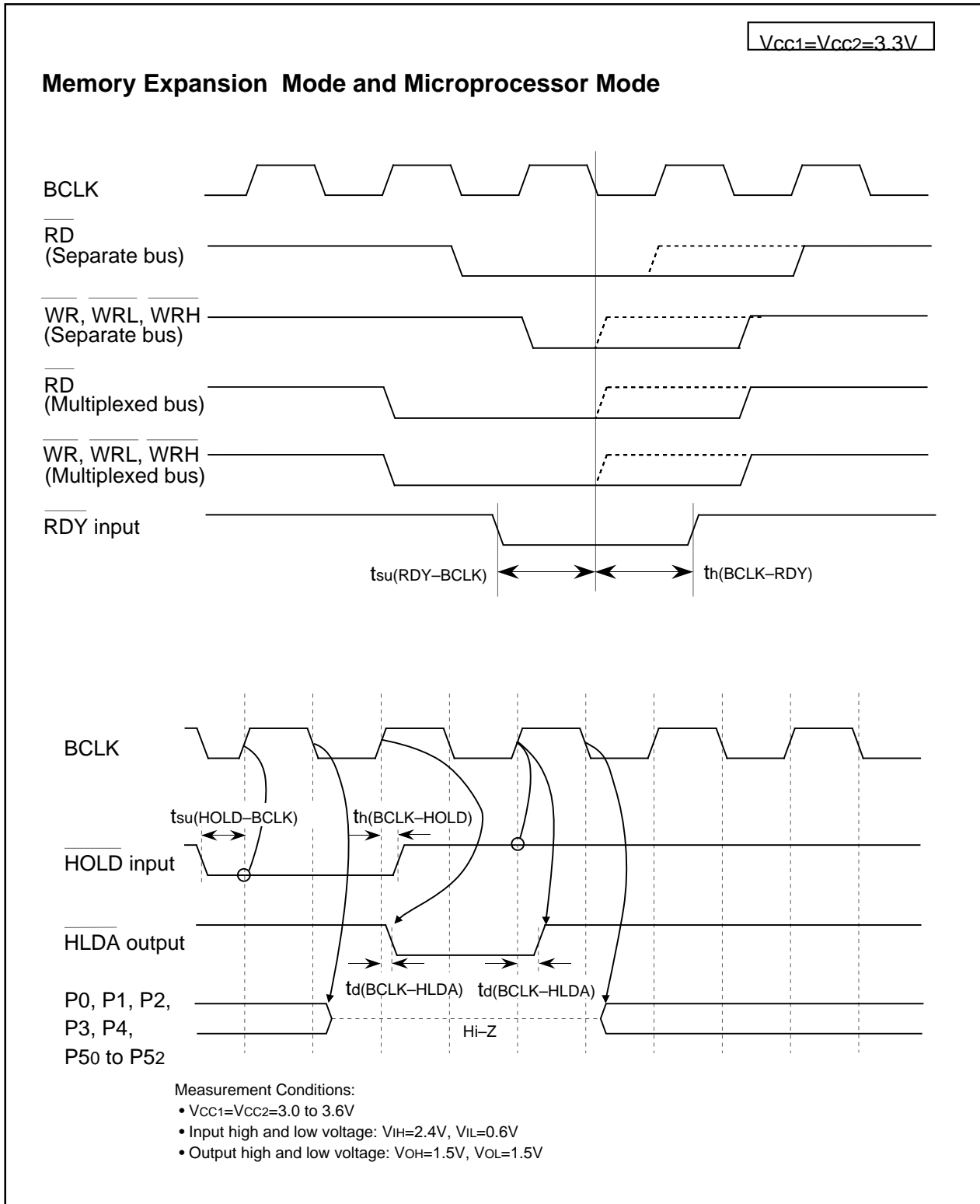


Figure 5.9 Vcc1=Vcc2=3.3V Timing Diagram (3)



**Figure 5.10**  $V_{CC1}=V_{CC2}=3.3V$  Timing Diagram (4)

## 5.2 Electrical Characteristics (M32C/84T)

**Table 5.42 Absolute Maximum Ratings**

| Symbol                              | Parameter                     |  | Condition  | Value                         | Unit |
|-------------------------------------|-------------------------------|--|--|-------------------------------|------|
| V <sub>CC1</sub> , V <sub>CC2</sub> | Supply Voltage                |  | V <sub>CC1</sub> =V <sub>CC2</sub> =AV <sub>CC</sub> | -0.3 to 6.0                   | V    |
| AV <sub>CC</sub>                    | Analog Supply Voltage         |  | V <sub>CC1</sub> =V <sub>CC2</sub> =AV <sub>CC</sub> | -0.3 to 6.0                   | V    |
| V <sub>I</sub>                      | Input Voltage                 | RESET, CNV <sub>SS</sub> , BYTE, P60-P67, P72-P77, P80-P87, P90-P97, P100-P107, P140-P146, P150-P157 <sup>(1)</sup> , V <sub>REF</sub> , X <sub>IN</sub> |  | -0.3 to V <sub>CC1</sub> +0.3 | V    |
|                                     |                               | P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P110-P114, P120-P127, P130-P137 <sup>(1)</sup>   |  | -0.3 to V <sub>CC2</sub> +0.3 |      |
|                                     |                               | P70, P71   |  | -0.3 to 6.0                   |      |
| V <sub>O</sub>                      | Output Voltage                | P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P140-P146, P150-P157 <sup>(1)</sup> , X <sub>OUT</sub>  |  | -0.3 to V <sub>CC1</sub> +0.3 | V    |
|                                     |                               | P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P110-P114, P120-P127, P130-P137 <sup>(1)</sup>   |  | -0.3 to V <sub>CC2</sub> +0.3 |      |
|                                     |                               | P70, P71   |  | -0.3 to 6.0                   |      |
| P <sub>d</sub>                      | Power Dissipation             |  | T <sub>opr</sub> =25° C                              | 500                           | mW   |
| T <sub>opr</sub>                    | Operating Ambient Temperature | during CPU operation   | T version  | -40 to 85                     | ° C  |
|                                     |                               | during flash memory program and erase operation  |  | 0 to 60                       |      |
| T <sub>stg</sub>                    | Storage Temperature           |  |  | -65 to 150                    | ° C  |

NOTES:

1. P11 to P15 are provided in the 144-pin package only.



**Table 5.43 Recommended Operating Conditions****(V<sub>CC1</sub>=V<sub>CC2</sub>=4.2 to 5.5V, V<sub>SS</sub>=0V at Topr = -40 to 85°C (T version) unless otherwise specified)**

| Symbol                              | Parameter   |   | Standard            |                  |                     | Unit |
|-------------------------------------|---|---|---------------------|------------------|---------------------|------|
|                                     |   |   | Min.                | Typ.             | Max.                |      |
| V <sub>CC1</sub> , V <sub>CC2</sub> | Supply Voltage (V <sub>CC1</sub> ≥ V <sub>CC2</sub> ) |   | 4.2                 | 5.0              | 5.5                 | V    |
| AV <sub>CC</sub>                    | Analog Supply Voltage                                 |   |                     | V <sub>CC1</sub> |                     | V    |
| V <sub>SS</sub>                     | Supply Voltage  |   |                     | 0                |                     | V    |
| AV <sub>SS</sub>                    | Analog Supply Voltage                                 |   |                     | 0                |                     | V    |
| V <sub>IH</sub>                     | Input High ("H") Voltage                              | P20-P27, P30-P37, P40-P47, P50-P57, P110-P114, P120-P127, P130-P137 <sup>(4)</sup>  | 0.8V <sub>CC2</sub> |                  | V <sub>CC2</sub>    | V    |
|                                     |   | P60-P67, P72-P77, P80-P87 <sup>(3)</sup> , P90-P97, P100-P107, P140-P146, P150-P157 <sup>(4)</sup> , X <sub>IN</sub> , RESET, CNV <sub>SS</sub> , BYTE                              | 0.8V <sub>CC1</sub> |                  | V <sub>CC1</sub>    |      |
|                                     |   | P70, P71  | 0.8V <sub>CC1</sub> |                  | 6.0                 |      |
|                                     |   | P00-P07, P10-P17  | 0.8V <sub>CC2</sub> |                  | V <sub>CC2</sub>    |      |
| V <sub>IL</sub>                     | Input Low ("L") Voltage                               | P20-P27, P30-P37, P40-P47, P50-P57, P110-P114, P120-P127, P130-P137 <sup>(4)</sup>  | 0                   |                  | 0.2V <sub>CC2</sub> | V    |
|                                     |   | P60-P67, P70-P77, P80-P87 <sup>(3)</sup> , P90-P97, P100-P107, P140-P146, P150-P157 <sup>(4)</sup> , X <sub>IN</sub> , RESET, CNV <sub>SS</sub> , BYTE                              | 0                   |                  | 0.2V <sub>CC1</sub> |      |
|                                     |   | P00-P07, P10-P17  | 0                   |                  | 0.2V <sub>CC2</sub> |      |
| I <sub>OH(peak)</sub>               | Peak Output High ("H") Current <sup>(2)</sup>         | P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 <sup>(4)</sup> |                     |                  | -10.0               | mA   |
| I <sub>OH(avg)</sub>                | Average Output High ("H") Current <sup>(1)</sup>      | P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 <sup>(4)</sup> |                     |                  | -5.0                | mA   |
| I <sub>OL(peak)</sub>               | Peak Output Low ("L") Current <sup>(2)</sup>          | P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 <sup>(4)</sup> |                     |                  | 10.0                | mA   |
| I <sub>OL(avg)</sub>                | Average Output Low ("L") Current <sup>(1)</sup>       | P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 <sup>(4)</sup> |                     |                  | 5.0                 | mA   |

## NOTES:

- Typical values when average output current is 100ms.
- Total I<sub>OL(peak)</sub> for P0, P1, P2, P86, P87, P9, P10, P11, P14 and P15 must be 80mA or less.  
Total I<sub>OL(peak)</sub> for P3, P4, P5, P6, P7, P80 to P84, P12 and P13 must be 80mA or less.  
Total I<sub>OH(peak)</sub> for P0, P1, P2, and P11 must be -40mA or less.  
Total I<sub>OH(peak)</sub> for P86, P87, P9, P10, P14 and P15 must be -40mA or less.  
Total I<sub>OH(peak)</sub> for P3, P4, P5, P12 and P13 must be -40mA or less.  
Total I<sub>OH(peak)</sub> for P6, P7, and P80 to P84 must be -40mA or less.
- V<sub>IH</sub> and V<sub>IL</sub> reference for P87 applies when P87 is used as a programmable input port.  
It does not apply when P87 is used as X<sub>CIN</sub>.
- P11 to P15 are provided in the 144-pin package only.

**Table 5.43 Recommended Operating Conditions (Continued)**  
**(V<sub>CC1</sub>=V<sub>CC2</sub>=4.2 to 5.5V, V<sub>SS</sub>=0V at Topr = -40 to 85°C (T version) unless otherwise specified)**

| Symbol   | Parameter   |                               | Standard |        |      | Unit |
|----------|---|-------------------------------|----------|--------|------|------|
|          |   |                               | Min.     | Typ.   | Max. |      |
| f(BCLK)  | CPU Input Frequency   | V <sub>CC1</sub> =4.2 to 5.5V | 0        |        | 32   | MHz  |
| f(XIN)   | Main Clock Input Frequency  | V <sub>CC1</sub> =4.2 to 5.5V | 0        |        | 32   | MHz  |
| f(XCIN)  | Sub Clock Frequency   |                               |          | 32.768 | 50   | kHz  |
| f(Ring)  | On-chip Oscillator Frequency (V <sub>CC1</sub> =V <sub>CC2</sub> =5.0V, Topr=25° C) |                               | 0.5      | 1      | 2    | MHz  |
| f(PLL)   | PLL Clock Frequency   | V <sub>CC1</sub> =4.2 to 5.5V | 10       |        | 32   | MHz  |
| tsu(PLL) | Wait Time to Stabilize PLL Frequency Synthesizer                                    | V <sub>CC1</sub> =5.0V        |          |        | 5    | ms   |

$V_{CC1}=V_{CC2}=5V$

**Table 5.44 Electrical Characteristics**

( $V_{CC1}=V_{CC2}=4.2$  to  $5.5V$ ,  $V_{SS}=0V$  at  $T_{opr} = -40$  to  $85^{\circ}C$  (T version),  
 $f(BCLK)=32MHz$  unless otherwise specified)

| Symbol                           | Parameter                 | Condition   | Standard                |                       |      | Unit             |     |    |
|----------------------------------|---------------------------|---|-------------------------|-----------------------|------|------------------|-----|----|
|                                  |                           |   | Min.                    | Typ.                  | Max. |                  |     |    |
| V <sub>OH</sub>                  | Output High ("H") Voltage | P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P110-P114, P120-P127, P130-P137   | I <sub>OH</sub> =-5mA   | V <sub>CC2</sub> -2.0 |      | V <sub>CC2</sub> | V   |    |
|                                  |                           | P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P140-P146, P150-P157 <sup>(1)</sup>  | I <sub>OH</sub> =-5mA   | V <sub>CC1</sub> -2.0 |      | V <sub>CC1</sub> |     |    |
|                                  |                           | P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P110-P114, P120-P127, P130-P137   | I <sub>OH</sub> =-200μA | V <sub>CC2</sub> -0.3 |      | V <sub>CC2</sub> | V   |    |
|                                  |                           | P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P140-P146, P150-P157 <sup>(1)</sup>  | I <sub>OH</sub> =-200μA | V <sub>CC1</sub> -0.3 |      | V <sub>CC1</sub> |     |    |
|                                  |                           | X <sub>OUT</sub>  | I <sub>OH</sub> =-1mA   | 3.0                   |      |                  | V   |    |
|                                  |                           | X <sub>COUT</sub>   | High Power              | No load applied       |      | 2.5              |     | V  |
|                                  |                           | Low Power   | No load applied         |                       | 1.6  |                  |     |    |
| V <sub>OL</sub>                  | Output Low ("L") Voltage  | P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 <sup>(1)</sup>   | I <sub>OL</sub> =5mA    |                       |      | 2.0              | V   |    |
|                                  |                           | P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 <sup>(1)</sup>   | I <sub>OL</sub> =200μA  |                       |      | 0.45             | V   |    |
|                                  |                           | X <sub>OUT</sub>  | I <sub>OL</sub> =1mA    |                       |      | 2.0              | V   |    |
|                                  |                           | X <sub>COUT</sub>   | High Power              | No load applied       |      | 0                |     | V  |
|                                  |                           |   | Low Power               | No load applied       |      | 0                |     |    |
| V <sub>T+</sub> -V <sub>T-</sub> | Hysteresis                | HOLD, RDY, TA0IN-TA4IN, TB0IN-TB5IN, INT0-INT5, ADTRG, CTS0-CTS4, CLK0-CLK4, TA0OUT-TA4OUT, NMI, KI0-KI3, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4   |                         | 0.2                   |      | 1.0              | V   |    |
|                                  |                           | RESET   |                         | 0.2                   |      | 1.8              | V   |    |
| I <sub>IH</sub>                  | Input High ("H") Current  | P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 <sup>(1)</sup> , X <sub>IN</sub> , RESET, CNV <sub>SS</sub> , BYTE | V <sub>I</sub> =5V      |                       |      | 5.0              | μA  |    |
| I <sub>IL</sub>                  | Input Low ("L") Current   | P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 <sup>(1)</sup> , X <sub>IN</sub> , RESET, CNV <sub>SS</sub> , BYTE | V <sub>I</sub> =0V      |                       |      | -5.0             | μA  |    |
| R <sub>PULLUP</sub>              | Pull-up Resistance        | P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 <sup>(1)</sup>   | V <sub>I</sub> =0V      | Flash Memory          | 30   | 50               | 167 | kΩ |
| R <sub>fXIN</sub>                | Feedback Resistance       | X <sub>IN</sub>   |                         |                       |      | 1.5              |     | MΩ |
| R <sub>fXCIN</sub>               | Feedback Resistance       | X <sub>CIN</sub>  |                         |                       |      | 10               |     | MΩ |
| V <sub>RAM</sub>                 | RAM Standby Voltage       | In stop mode  |                         |                       | 2.0  |                  |     | V  |

## NOTES:

- P11 to P15 are provided in the 144-pin package only.

$V_{CC1}=V_{CC2}=5V$

**Table 5.44 Electrical Characteristics (Continued)**  
**( $V_{CC1}=V_{CC2}=4.2$  to  $5.5V$ ,  $V_{SS}=0V$  at  $T_{opr} = -40$  to  $85^{\circ}C$  (T version),  
 $f(BCLK)=32MHz$  unless otherwise specified)**

| Symbol          | Parameter            | Measurement Condition  | Standard   |      |      | Unit |    |
|-----------------|----------------------|--|--|------|------|------|----|
|                 |                      |  | Min.   | Typ. | Max. |      |    |
| I <sub>cc</sub> | Power Supply Current | In single-chip mode, output pins are left open and other pins are connected to V <sub>ss</sub> . | f(BCLK)=32 MHz, Square wave, No division   |      | 28   | 50   | mA |
|                 |                      |  | f(BCLK)=32 kHz, In low-power consumption mode, Program running on ROM                |      | 430  |      | μA |
|                 |                      |  | f(BCLK)=32 kHz, In low-power consumption mode, Program running on RAM <sup>(1)</sup> |      | 25   |      | μA |
|                 |                      |  | f(BCLK)=32 kHz, In wait mode, T <sub>opr</sub> =25° C                                |      | 10   |      | μA |
|                 |                      |  | While clock stops, T <sub>opr</sub> =25° C   |      | 0.8  | 5    | μA |
|                 |                      |  | While clock stops, T <sub>opr</sub> =85° C   |      |      | 50   | μA |

NOTES:

1. Value is obtained when setting the FMSTP bit in the FMR0 register to "1" (flash memory stopped).

$V_{CC1}=V_{CC2}=5V$

**Table 5.45 A/D Conversion Characteristics ( $V_{CC1}=V_{CC2}=4.2$  to  $5.5V$ ,  $V_{SS}=0V$  at  $T_{opr}=-40$  to  $85^{\circ}C$  (T version),  $f(BCLK)=32MHz$  unless otherwise specified)**

| Symbol            | Parameter                                | Measurement Condition        | Standard  |      |                  | Unit |     |
|-------------------|--|------------------------------|---|------|------------------|------|-----|
|                   |  |                              | Min.  | Typ. | Max.             |      |     |
| -                 | Resolution                               | $V_{REF}=V_{CC1}$            |   |      | 10               | Bits |     |
| INL               | Integral Nonlinearity Error              | $V_{REF}=V_{CC1}=V_{CC2}=5V$ | AN <sub>0</sub> to AN <sub>7</sub> , AN <sub>00</sub> to AN <sub>07</sub> , AN <sub>20</sub> to AN <sub>27</sub> , AN <sub>150</sub> to AN <sub>157</sub> , ANEX <sub>0</sub> , ANEX <sub>1</sub> |      |                  | ±3   | LSB |
|                   |  |                              |   |      |                  |      | LSB |
|                   |  |                              | External op-amp connection mode   |      |                  | ±7   | LSB |
|                   |  |                              |   |      |                  | LSB  |     |
| DNL               | Differential Nonlinearity Error          |                              |   |      | ±1               | LSB  |     |
| -                 | Offset Error                             |                              |   |      | ±3               | LSB  |     |
| -                 | Gain Error                               |                              |   |      | ±3               | LSB  |     |
| RLADDER           | Resistor Ladder                          | $V_{REF}=V_{CC1}$            | 8   |      | 40               | kΩ   |     |
| t <sub>CONV</sub> | 10-bit Conversion Time <sup>(1, 2)</sup> |                              | 2.06  |      |                  | μs   |     |
| t <sub>CONV</sub> | 8-bit Conversion Time <sup>(1, 2)</sup>  |                              | 1.75  |      |                  | μs   |     |
| t <sub>SAMP</sub> | Sampling Time <sup>(1)</sup>             |                              | 0.188   |      |                  | μs   |     |
| V <sub>REF</sub>  | Reference Voltage                        |                              | 2   |      | V <sub>CC1</sub> | V    |     |
| V <sub>IA</sub>   | Analog Input Voltage                     |                              | 0   |      | V <sub>REF</sub> | V    |     |

## NOTES:

1. Divide  $f(X_{IN})$ , if exceeding 16 MHz, to keep  $\phi_{AD}$  frequency at 16 MHz or less.
2. With using the sample and hold function.

**Table 5.46 D/A Conversion Characteristics ( $V_{CC1}=V_{CC2}=4.2$  to  $5.5V$ ,  $V_{SS}=0V$  at  $T_{opr}=-40$  to  $85^{\circ}C$  (T version),  $f(BCLK)=32MHz$  unless otherwise specified)**

| Symbol            | Parameter                            | Measurement Condition | Standard |      |      | Unit |
|-------------------|--------------------------------------|-----------------------|----------|------|------|------|
|                   |                                      |                       | Min.     | Typ. | Max. |      |
| -                 | Resolution                           |                       |          |      | 8    | Bits |
| -                 | Absolute Accuracy                    |                       |          |      | 1.0  | %    |
| t <sub>SU</sub>   | Setup Time                           |                       |          |      | 3    | μs   |
| R <sub>O</sub>    | Output Resistance                    |                       | 4        | 10   | 20   | kΩ   |
| I <sub>VREF</sub> | Reference Power Supply Input Current | (Note 1)              |          |      | 1.5  | mA   |

## NOTES:

1. Measurement when using one D/A converter. The DA<sub>i</sub> register (i=0, 1) of the D/A converter, not being used, is set to "00<sub>16</sub>". The resistor ladder in the A/D converter is excluded.  
I<sub>VREF</sub> flows even if the VCUT bit in the AD0CON1 register is set to "0" (no V<sub>REF</sub> connection).

**Table 5.47 Flash Memory Version Electrical Characteristics**  
**(VCC1=4.5 to 5.5V, 3.3 to 3.6V at Topr= 0 to 60°C unless otherwise specified)**

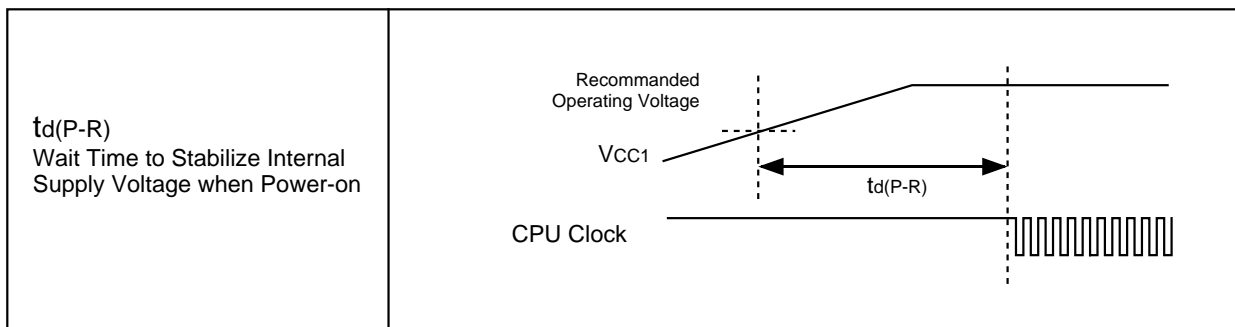
| Symbol | Parameter                                    |                | Standard |      |              | Unit   |
|--------|--|----------------|----------|------|--------------|--------|
|        |  |                | Min.     | Typ. | Max.         |        |
| -      | Program and Erase Endurance <sup>(2)</sup>   |                | 100      |      |              | cycles |
| -      | Word Program Time (VCC1=5.0V, Topr=25° C)    |                |          | 25   | 200          | µs     |
| -      | Lock Bit Program Time                        |                |          | 25   | 200          | µs     |
| -      | Block Erase Time<br>(VCC1=5.0V, Topr=25° C)  | 4-Kbyte Block  |          | 0.3  | 4            | s      |
|        |  | 8-Kbyte Block  |          | 0.3  | 4            | s      |
|        |  | 32-Kbyte Block |          | 0.5  | 4            | s      |
|        |  | 64-Kbyte Block |          | 0.8  | 4            | s      |
| -      | All-Unlocked-Block Erase Time <sup>(1)</sup> |                |          |      | 4 x <i>n</i> | s      |
| tps    | Wait Time to Stabilize Flash Memory Circuit  |                |          |      | 15           | µs     |
| -      | Data Hold Time (Topr=-40 to 85 ° C)          |                | 10       |      |              | years  |

NOTES:

- n* denotes the number of block to be erased.
- Number of program-erase cycles per block.  
 If Program and Erase Endurance is *n* cycle (*n*≠100), each block can be erased and programmed *n* cycles.  
 For example, if a 4-Kbyte block A is erased after programming a word data 2,048 times, each to a different address, this counts as one program and erase endurance. Data can not be programmed to the same address more than once without erasing the block. (rewrite prohibited).

**Table 5.48 Power Supply Timing**

| Symbol  | Parameter  | Measurement Condition | Standard |      |      | Unit |
|---------|--|-----------------------|----------|------|------|------|
|         |  |                       | Min.     | Typ. | Max. |      |
| td(P-R) | Wait Time to Stabilize Internal Supply Voltage when Power-on | VCC1=3.0 to 5.5V      |          |      | 2    | ms   |



**Figure 5.11 Power Supply Timing Diagram**

$V_{CC1}=V_{CC2}=5V$

**Timing Requirements****( $V_{CC1}=V_{CC2}=4.2$  to  $5.5V$ ,  $V_{SS}=0V$  at  $T_{opr}= -40$  to  $85^{\circ}C$  (T version) unless otherwise specified)****Table 5.49 External Clock Input**

| Symbol     | Parameter                             | Standard |      | Unit |
|------------|---------------------------------------|----------|------|------|
|            |                                       | Min.     | Max. |      |
| $t_c$      | External Clock Input Cycle Time       | 31.25    |      | ns   |
| $t_{w(H)}$ | External Clock Input High ("H") Width | 13.75    |      | ns   |
| $t_{w(L)}$ | External Clock Input Low ("L") Width  | 13.75    |      | ns   |
| $t_r$      | External Clock Rise Time              |          | 5    | ns   |
| $t_f$      | External Clock Fall Time              |          | 5    | ns   |

$V_{CC1}=V_{CC2}=5V$

**Timing Requirements****( $V_{CC1}=V_{CC2}=4.2$  to  $5.5V$ ,  $V_{SS}=0V$  at  $T_{opr} = -40$  to  $85^{\circ}C$  (T version) unless otherwise specified)****Table 5.50 Timer A Input (Count Source Input in Event Counter Mode)**

| Symbol       | Parameter                    | Standard |      | Unit |
|--------------|------------------------------|----------|------|------|
|              |                              | Min.     | Max. |      |
| $t_{c(TA)}$  | TAiIN Input Cycle Time       | 100      |      | ns   |
| $t_{w(TAH)}$ | TAiIN Input High ("H") Width | 40       |      | ns   |
| $t_{w(TAL)}$ | TAiIN Input Low ("L") Width  | 40       |      | ns   |

**Table 5.51 Timer A Input (Gate Input in Timer Mode)**

| Symbol       | Parameter                    | Standard |      | Unit |
|--------------|------------------------------|----------|------|------|
|              |                              | Min.     | Max. |      |
| $t_{c(TA)}$  | TAiIN Input Cycle Time       | 400      |      | ns   |
| $t_{w(TAH)}$ | TAiIN Input High ("H") Width | 200      |      | ns   |
| $t_{w(TAL)}$ | TAiIN Input Low ("L") Width  | 200      |      | ns   |

**Table 5.52 Timer A Input (External Trigger Input in One-Shot Timer Mode)**

| Symbol       | Parameter                    | Standard |      | Unit |
|--------------|------------------------------|----------|------|------|
|              |                              | Min.     | Max. |      |
| $t_{c(TA)}$  | TAiIN Input Cycle Time       | 200      |      | ns   |
| $t_{w(TAH)}$ | TAiIN Input High ("H") Width | 100      |      | ns   |
| $t_{w(TAL)}$ | TAiIN Input Low ("L") Width  | 100      |      | ns   |

**Table 5.53 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)**

| Symbol       | Parameter                    | Standard |      | Unit |
|--------------|------------------------------|----------|------|------|
|              |                              | Min.     | Max. |      |
| $t_{w(TAH)}$ | TAiIN Input High ("H") Width | 100      |      | ns   |
| $t_{w(TAL)}$ | TAiIN Input Low ("L") Width  | 100      |      | ns   |

**Table 5.54 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)**

| Symbol           | Parameter                     | Standard |      | Unit |
|------------------|-------------------------------|----------|------|------|
|                  |                               | Min.     | Max. |      |
| $t_{c(UP)}$      | TAiOUT Input Cycle Time       | 2000     |      | ns   |
| $t_{w(UPH)}$     | TAiOUT Input High ("H") Width | 1000     |      | ns   |
| $t_{w(UPL)}$     | TAiOUT Input Low ("L") Width  | 1000     |      | ns   |
| $t_{su(UP-TIN)}$ | TAiOUT Input Setup Time       | 400      |      | ns   |
| $t_{h(TIN-UP)}$  | TAiOUT Input Hold Time        | 400      |      | ns   |



$V_{CC1}=V_{CC2}=5V$

**Timing Requirements****( $V_{CC1}=V_{CC2}=4.2$  to  $5.5V$ ,  $V_{SS}=0V$  at  $T_{opr} = -40$  to  $85^{\circ}C$  (T version) unless otherwise specified)****Table 5.55 Timer B Input (Count Source Input in Event Counter Mode)**

| Symbol       | Parameter  | Standard |      | Unit |
|--------------|--|----------|------|------|
|              |  | Min.     | Max. |      |
| $t_{c(TB)}$  | TBiIN Input Cycle Time (counted on one edge)         | 100      |      | ns   |
| $t_{w(TBH)}$ | TBiIN Input High ("H") Width (counted on one edge)   | 40       |      | ns   |
| $t_{w(TBL)}$ | TBiIN Input Low ("L") Width (counted on one edge)    | 40       |      | ns   |
| $t_{c(TB)}$  | TBiIN Input Cycle Time (counted on both edges)       | 200      |      | ns   |
| $t_{w(TBH)}$ | TBiIN Input High ("H") Width (counted on both edges) | 80       |      | ns   |
| $t_{w(TBL)}$ | TBiIN Input Low ("L") Width (counted on both edges)  | 80       |      | ns   |

**Table 5.56 Timer B Input (Pulse Period Measurement Mode)**

| Symbol       | Parameter                    | Standard |      | Unit |
|--------------|------------------------------|----------|------|------|
|              |                              | Min.     | Max. |      |
| $t_{c(TB)}$  | TBiIN Input Cycle Time       | 400      |      | ns   |
| $t_{w(TBH)}$ | TBiIN Input High ("H") Width | 200      |      | ns   |
| $t_{w(TBL)}$ | TBiIN Input Low ("L") Width  | 200      |      | ns   |

**Table 5.57 Timer B Input (Pulse Width Measurement Mode)**

| Symbol       | Parameter                    | Standard |      | Unit |
|--------------|------------------------------|----------|------|------|
|              |                              | Min.     | Max. |      |
| $t_{c(TB)}$  | TBiIN Input Cycle Time       | 400      |      | ns   |
| $t_{w(TBH)}$ | TBiIN Input High ("H") Width | 200      |      | ns   |
| $t_{w(TBL)}$ | TBiIN Input Low ("L") Width  | 200      |      | ns   |

**Table 5.58 A/D Trigger Input**

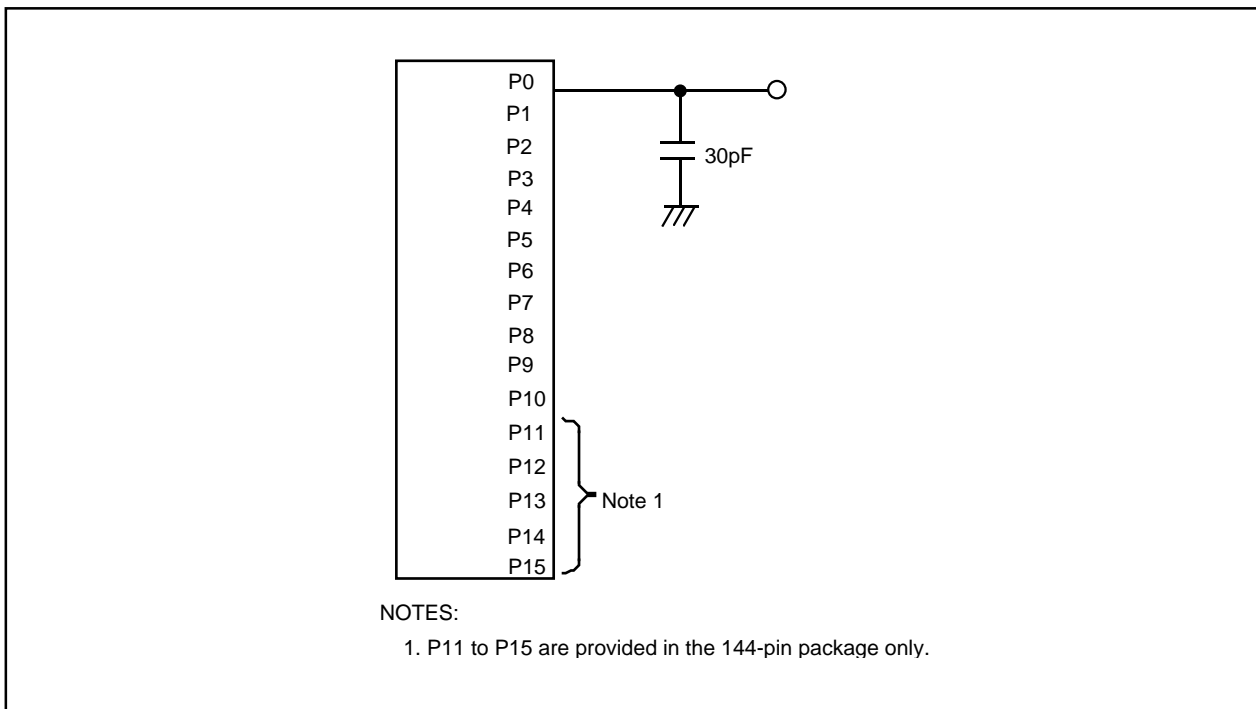
| Symbol       | Parameter                                     | Standard |      | Unit |
|--------------|---|----------|------|------|
|              |   | Min.     | Max. |      |
| $t_{c(AD)}$  | ADTRG Input Cycle Time (required for trigger) | 1000     |      | ns   |
| $t_{w(ADL)}$ | ADTRG Input Low ("L") Pulse Width             | 125      |      | ns   |

**Table 5.59 Serial I/O**

| Symbol        | Parameter                   | Standard |      | Unit |
|---------------|-----------------------------|----------|------|------|
|               |                             | Min.     | Max. |      |
| $t_{c(CK)}$   | CLKi Input Cycle Time       | 200      |      | ns   |
| $t_{w(CKH)}$  | CLKi Input High ("H") Width | 100      |      | ns   |
| $t_{w(CKL)}$  | CLKi Input Low ("L") Width  | 100      |      | ns   |
| $t_{d(C-Q)}$  | TxDi Output Delay Time      |          | 80   | ns   |
| $t_{h(C-Q)}$  | TxDi Hold Time              | 0        |      | ns   |
| $t_{su(D-C)}$ | RxDi Input Setup Time       | 30       |      | ns   |
| $t_{h(C-Q)}$  | RxDi Input Hold Time        | 90       |      | ns   |

**Table 5.60 External Interrupt INTi Input**

| Symbol       | Parameter                   | Standard |      | Unit |
|--------------|-----------------------------|----------|------|------|
|              |                             | Min.     | Max. |      |
| $t_{w(INH)}$ | INTi Input High ("H") Width | 250      |      | ns   |
| $t_{w(INL)}$ | INTi Input Low ("L") Width  | 250      |      | ns   |

**Figure 5.12 P0 to P15 Measurement Circuit**

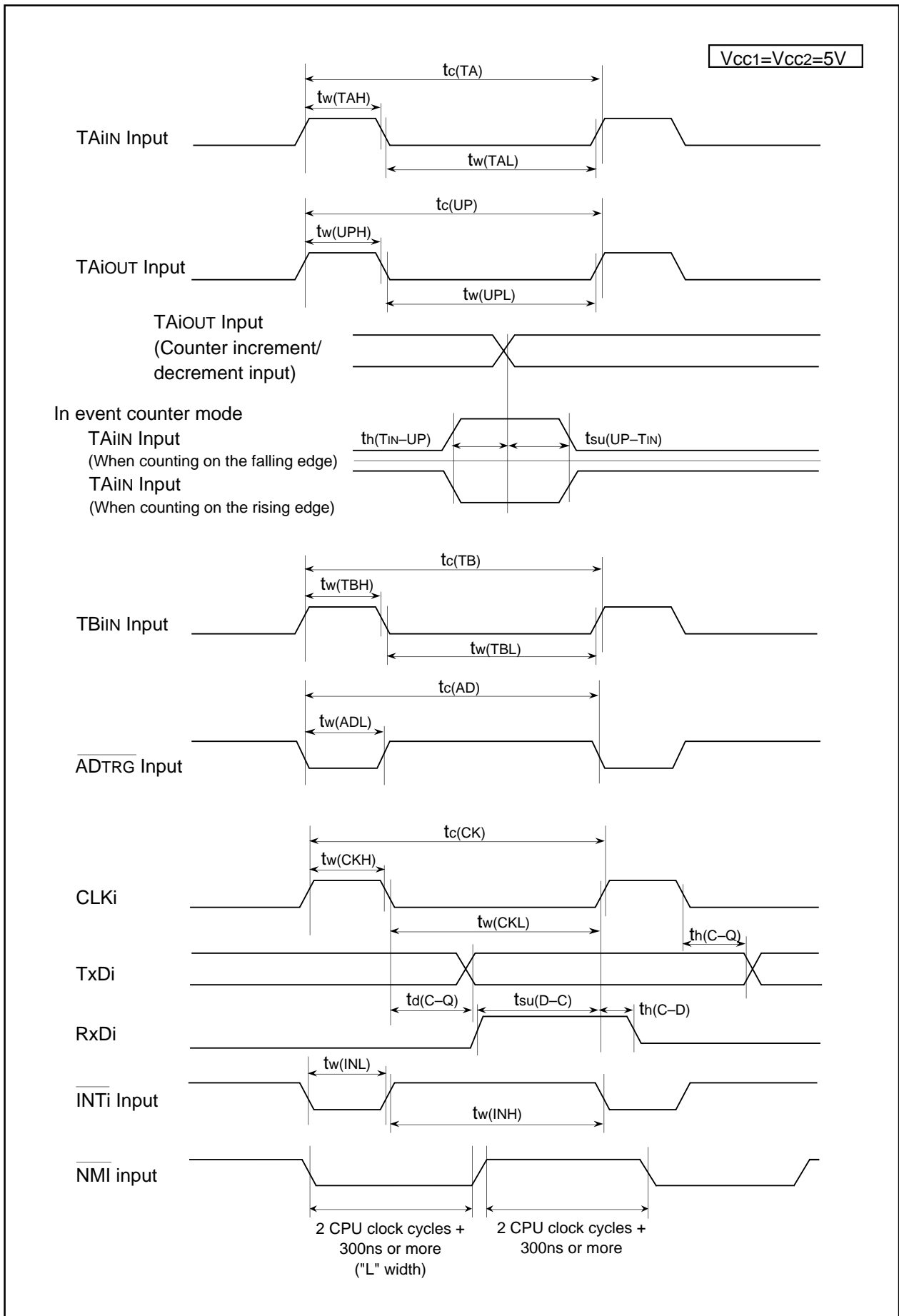


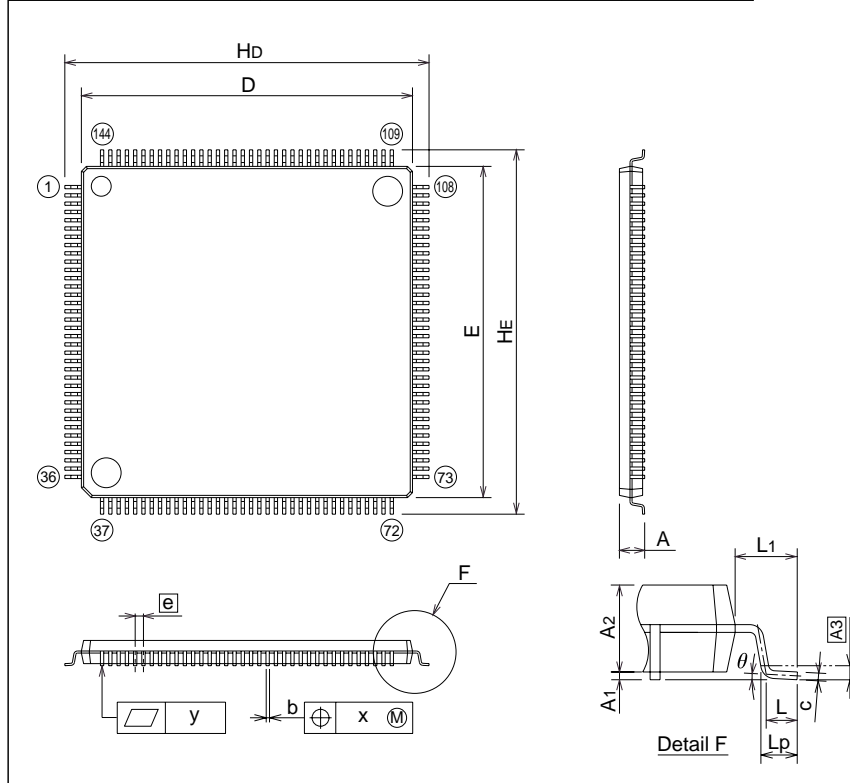
Figure 5.13 Vcc1=Vcc2=5V Timing Diagram

# Package Dimensions

## PLQP0144KA-A (144P6Q-A)

Plastic 144pin 20X20mm body LQFP

|                      |              |               |            |
|----------------------|--------------|---------------|------------|
| JEITA Package Code   | RENESAS Code | Previous Code | Mass[Typ.] |
| P-LQFP144-20x20-0.50 | PLQP0144KA-A | 144P6Q-A      | 1.2g       |



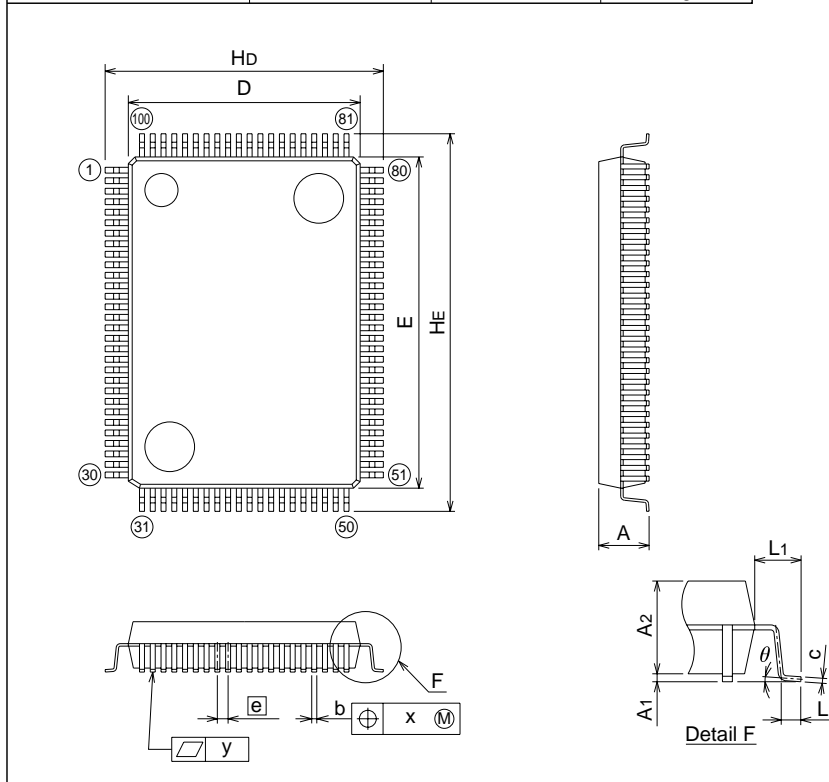
Recommended Mount Pad

| Symbol | Dimension in Millimeters |       |       |
|--------|--------------------------|-------|-------|
|        | Min                      | Nom   | Max   |
| A      | -                        | -     | 1.7   |
| A1     | 0.05                     | 0.125 | 0.2   |
| A2     | -                        | 1.4   | -     |
| b      | 0.17                     | 0.22  | 0.27  |
| c      | 0.105                    | 0.125 | 0.175 |
| D      | 19.9                     | 20.0  | 20.1  |
| E      | 19.9                     | 20.0  | 20.1  |
| e      | -                        | 0.5   | -     |
| Hd     | 21.8                     | 22.0  | 22.2  |
| HE     | 21.8                     | 22.0  | 22.2  |
| L      | 0.35                     | 0.5   | 0.65  |
| L1     | -                        | 1.0   | -     |
| Lp     | 0.45                     | 0.6   | 0.75  |
| A3     | -                        | 0.25  | -     |
| x      | -                        | -     | 0.08  |
| y      | -                        | -     | 0.1   |
| theta  | 0°                       | -     | 8°    |
| b2     | -                        | 0.225 | -     |
| l2     | 0.95                     | -     | -     |
| MD     | -                        | 20.4  | -     |
| ME     | -                        | 20.4  | -     |

## PRQP0100JB-A (100P6S-A)

Plastic 100pin 14X20mm body QFP

|                     |              |               |            |
|---------------------|--------------|---------------|------------|
| JEITA Package Code  | RENESAS Code | Previous Code | Mass[Typ.] |
| P-QFP100-14x20-0.65 | PRQP0100JB-A | 100P6S-A      | 1.6g       |



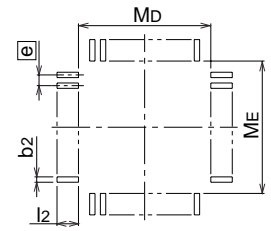
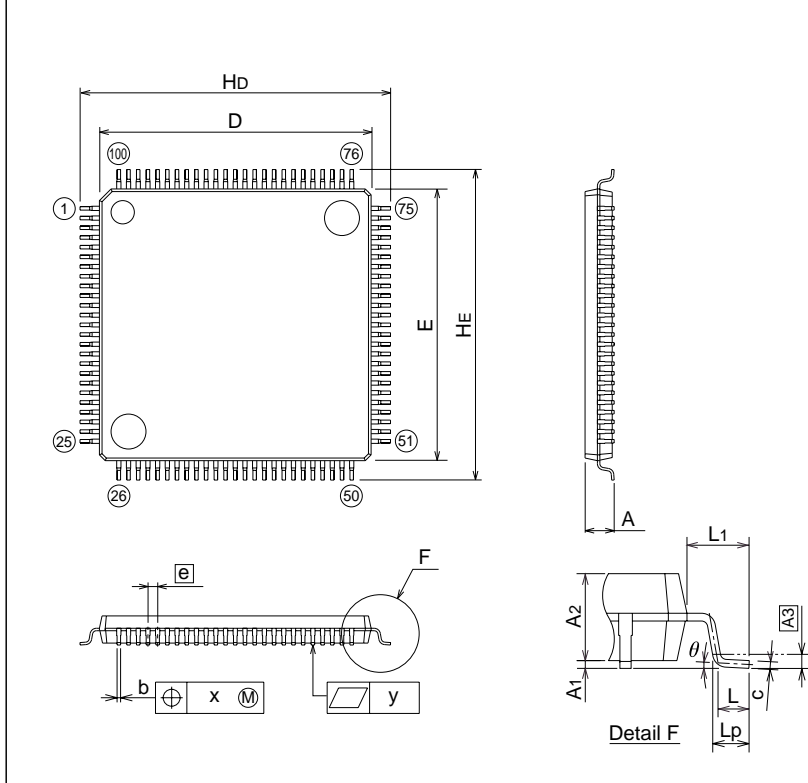
Recommended Mount Pad

| Symbol | Dimension in Millimeters |      |      |
|--------|--------------------------|------|------|
|        | Min                      | Nom  | Max  |
| A      | -                        | -    | 3.05 |
| A1     | 0                        | 0.1  | 0.2  |
| A2     | -                        | 2.8  | -    |
| b      | 0.25                     | 0.3  | 0.4  |
| c      | 0.13                     | 0.15 | 0.2  |
| D      | 13.8                     | 14.0 | 14.2 |
| E      | 19.8                     | 20.0 | 20.2 |
| e      | -                        | 0.65 | -    |
| Hd     | 16.5                     | 16.8 | 17.1 |
| HE     | 22.5                     | 22.8 | 23.1 |
| L      | 0.4                      | 0.6  | 0.8  |
| L1     | -                        | 1.4  | -    |
| x      | -                        | -    | 0.13 |
| y      | -                        | -    | 0.1  |
| theta  | 0°                       | -    | 10°  |
| b2     | -                        | 0.35 | -    |
| l2     | 1.3                      | -    | -    |
| Md     | -                        | 14.6 | -    |
| ME     | -                        | 20.6 | -    |

**PLQP0100KB-A (100P6Q-A)**

**Plastic 100pin 14X14mm body LQFP**

|                      |              |               |            |
|----------------------|--------------|---------------|------------|
| JEITA Package Code   | RENESAS Code | Previous Code | Mass[Typ.] |
| P-LQFP100-14x14-0.50 | PLQP0100KB-A | 100P6Q-A      | 0.6g       |



Recommended Mount Pad

| Symbol   | Dimension in Millimeters |       |       |
|----------|--------------------------|-------|-------|
|          | Min                      | Nom   | Max   |
| A        | -                        | -     | 1.7   |
| A1       | 0                        | 0.1   | 0.2   |
| A2       | -                        | 1.4   | -     |
| b        | 0.13                     | 0.18  | 0.28  |
| c        | 0.105                    | 0.125 | 0.175 |
| D        | 13.9                     | 14.0  | 14.1  |
| E        | 13.9                     | 14.0  | 14.1  |
| e        | -                        | 0.5   | -     |
| Hd       | 15.8                     | 16.0  | 16.2  |
| HE       | 15.8                     | 16.0  | 16.2  |
| L        | 0.3                      | 0.5   | 0.7   |
| L1       | -                        | 1.0   | -     |
| Lp       | 0.45                     | 0.6   | 0.75  |
| A3       | -                        | 0.25  | -     |
| x        | -                        | -     | 0.08  |
| y        | -                        | -     | 0.1   |
| $\theta$ | 0°                       | -     | 10°   |
| b2       | -                        | 0.225 | -     |
| l2       | 0.9                      | -     | -     |
| Md       | -                        | 14.4  | -     |
| ME       | -                        | 14.4  | -     |

REVISION HISTORY

M32C/84 Group (M32C/84, M32C/84T) Datasheet

| Rev. | Date  | Description |   |
|------|---|-------------|---|
|      |   | Page        | Summary   |
| 0.40 | Sep. 30, 2003   | –           | New Document  |
| 0.50 | Feb. 05, 2004   | 2, 3        | <b>Overview</b><br>• <b>Table 1.1 and Table 1.2 M32C/84 Group Performance</b> Values for Shortest Instruction Execution Time and Power Consumption” modified  |
|      |   | 5           | • <b>Figure 1.2 ROM/RAM Capacity</b> Products added   |
|      |   | 6           | • <b>Table 1.3 M32C/84 Group</b> Products added   |
|      |   | 6           | • <b>Figure 1.3 Product Numbering System</b> 128-Kbytes added to ROM capacity Memory  |
|      |   | 23          | • <b>Figure 3.1 Memory Map</b> Diagram modified; products added   |
|      |   | 24          | <b>SFR</b><br>• “Values after RESET” for the PM1, PM2, D4INT, G0IRF, G1IRF, IDB0 to IDB1, TA0MR to TA4MR, TCSPR, DM0SL to DM3SL registers revised<br>• The IPSA register added to address 017916<br>• NOTES added to the PM0 and TCSPR register   |
|      |   | 44          | <b>Electrical Characteristics</b><br>• Newly added  |
| 0.51 | Feb. 09, 2004   |             | <b>Electrical Characteristics</b>   |
|      |   | 50          | • <b>Table 5.6 Flash Memory Version Electrical Characteristics</b> Note 4 revised   |
|      |   | 57          | • <b>Figure 5.2 Vcc1=Vcc2=5V Timing Diagram (1)</b> Notes 1 and 2 revised   |
|      |   | 68          | • <b>Figure 5.3 Vcc1=Vcc2=5V Timing Diagram (2)</b> Notes 1, 2, and 3 revised   |
|      |   | 68          | • <b>Figure 5.6 Vcc1=Vcc2=3.3V Timing Diagram (1)</b> Notes 1, 2, and 3 revised   |
| 69   | • <b>Figure 5.7 Vcc1=Vcc2=3.3V Timing Diagram (2)</b> Notes 1 and 2 revised |             |   |
| 0.52 | Mar.12, 2004  | 2, 3        | <b>Overview</b><br>• <b>Table 1.1 and 1.2 M32C/84 Group Performance</b> Values for Power Consumption modified   |
|      |   | 48          | <b>Electrical Characteristics</b><br>• <b>Table 5.3 Electrical Characteristics</b> Maximum values for Power Supply Current modified   |
|      |   | 50          | • <b>Table 5.6 Flash Memory Version Electrical Characteristics</b> Note 1. 100-cycle Products (D3, D5, U3, U5) deleted; Note 4 modified   |
|      |   | 61          | • <b>Table 5.7 Flash Memory Version Program and Erase Voltage and Read Operation Voltage Characteristics (at Topr=0 to 60°C)</b> deleted<br>• <b>Table 5.22 Electrical Characteristics</b> Maximum values for Power Supply Consumption modified and standard values when “Topr=85°C while clock is stopped” deleted |

REVISION HISTORY

M32C/84 Group (M32C/84, M32C/84T) Datasheet

| Rev.     | Date  | Description |   |
|----------|---|-------------|---|
|          |   | Page        | Summary   |
| 1.00     | Jun.01, 2004  | -           | <b>M32C/84T (High-reliability version)</b> added  |
|          |   | All Pages   | Words standardized: On-chip oscillator, A/D converter and D/A converter                                     |
|          |   | 1           | <b>Overview</b><br>• <b>1.1 Applications</b> Automobiles added  |
|          |   | 2, 3        | • <b>Table 1.1 and Table 1.2 M32C/84 Group (M32C/84, M32C/84T) Performance</b> M32C/84T added; note 3 added |
|          |   | 4           | • <b>Figure 1.1 M32C/84 Group (M32C/84, M32C/84T) Block Diagram</b> Note 3 added                            |
|          |   | 5           | • <b>1.4 Product Information</b> Description modified   |
|          |   | 6           | • <b>Figure 1.2 ROM/RAM Capacity</b> figure modified  |
|          |   | 6           | • <b>Table 1.3 M32C/84 Group</b> M32C/84T added   |
|          |   | 6           | • <b>Figure 1.3 Product Numbering System</b> M32C/84T added   |
|          |   | 7           | • <b>Figure 1.4 Pin Assignment for 144-Pin Package</b> Note 3 added   |
| 12       | • <b>Figure 1.6 Pin Assignment for 100-Pin Package</b> Note 5 added   |             |   |
| 8 to 10  | • <b>Table 1.5 Pin Characteristics for 144-Pin Package</b> Note 1 added   |             |   |
| 13, 14   | • <b>Table 1.6 Pin Characteristics for 100-Pin Package</b> Note 1 added   |             |   |
| 15 to 18 | • <b>Table 1.7 Pin Description</b> Notes added  |             |   |
| 22       | <b>Memory</b><br>• <b>Figure 3.1 Memory Map</b> Tables of internal ROM/internal RAM modified; note 2 modified; notes 4 and 5 added  |             |   |
| 23       | <b>SFR</b><br>• Note 2 added  |             |   |
| 24       | • PWCR0 and PWCR1 registers deleted<br>• "Values after RESET" of the masked ROM version added to the FMR0 register<br>• Note 1 added  |             |   |
| 44       | <b>Electrical Characteristics</b><br>• <b>Table 5.2 Recommended Operating Conditions</b> $f_{\text{ripple}}$ , $V_{p-p(\text{ripple})}$ , $V_{CC}$ , $SV_{CC}$ and note 1 deleted       |             |   |
| 47       | • <b>Table 5.3 Electrical Characteristics</b> $R_{PULLUP}$ value for the masked ROM version added   |             |   |
| 48       | • <b>Table 5.4 A/D Conversion Characteristics</b> $t_{SMP}$ value modified; note 1 added  |             |   |
| 50       | • <b>Table 5.7 Low Voltage Detect Circuit Electrical Characteristics</b> added<br>• <b>Table 5.8 Power Supply Timing</b> added<br>• <b>Figure 5.1 Power Supply Timing Diagram</b> added |             |   |
| 55       | • <b>Table 5.23 Memory Expansion Mode and Microprocessor Mode</b> $t_{h(\text{BCLK-ALE})}$ value modified   |             |   |
| 61       | • <b>Table 5.24 Electrical Characteristics</b> $R_{PULLUP}$ value for the masked ROM version added  |             |   |
| 62       | • <b>Table 5.25 A/D Conversion Characteristics</b> $t_{CONV}$ value modified  |             |   |

REVISION HISTORY

M32C/84 Group (M32C/84, M32C/84T) Datasheet

| Rev. | Date         | Description |   |
|------|--------------|-------------|---|
|      |              | Page        | Summary   |
|      |              | 63          | • <b>Table 5.28 Memory Expansion Mode and Microprocessor Mode</b> $t_{su}(DB-BCLK)$ , $t_{su}(RDY-BCLK)$ and $t_{su}(HOLD-BCLK)$ value modified                                     |
|      |              | 66          | • <b>Table 5.40 Memory Expansion Mode and Microprocessor Mode</b> equation of $t_h(WR-DB)$ modified   |
|      |              | 67          | • <b>Table 5.41 Memory Expansion Mode and Microprocessor Mode</b> $t_h(BCLK-ALE)$ value modified; equation of $t_h(WR-DB)$ modified   |
|      |              | 72          | • <b>5.2 Electrical Characteristics (M32C/84T)</b> added  |
| 1.10 | Jun.28, 2004 | -           | <b>High-reliability version (U version)</b> deleted   |
|      |              |             | <b>Overview</b>   |
|      |              | 5           | • <b>Table 1.3 M32C/84 Group (1) (2)</b> development status modified  |
|      |              | 6           | • <b>Figure 1.2 Product Numbering System</b> figure modified  |
| 1.20 | Apr.18, 2005 |             | <b>Overview</b>   |
|      |              | 2, 3        | • <b>Table 1.1 and Table 1.2 M32C/84 Group (M32C/84, M32C/84T) Performance</b> Note 4 added   |
|      |              | 6           | • <b>Table 1.3 M32C/84 Group (1) (2)</b> Information updated  |
|      |              | 16, 17      | • <b>Table 1.6 Pin Description</b> Note 2 deleted   |
|      |              |             | <b>Memory</b>   |
|      |              | 22          | • <b>Figure 3.1 Memory Map</b> Description added to Note 3  |
|      |              |             | <b>SFR</b>  |
|      |              | 24          | • The PWCR0 and PWCR1 registers newly added to address 004C16 and 004D16<br>• “Values after RESET” for the G0RB, G1BCR1, G1RB, IDB0, IDB1, DM0SL to DM3SL and PSC registers revised |
|      |              |             | <b>Electrical Characteristics</b>   |
|      |              | 46          | • <b>Table 5.3 Electrical Characteristics</b> $I_{CC}$ standard value revised   |
|      |              | 49          | • <b>Table 5.6 Flash Memory Electrical Characteristics</b> $T_{opr}$ value modified   |
|      |              | 50          | • <b>Table 5.7 Voltage Detection Circuit Electrical Characteristics</b> $V_{CC1}$ value modified  |
|      |              | 58          | • <b>Figure 5.4 <math>V_{CC1}=V_{CC2}=5V</math> Timing Diagram (2)</b> Diagram modified   |
|      |              | 61          | • <b>Table 5.24 Electrical Characteristics</b> $I_{CC}$ standard value revised  |
|      |              | 63          | • <b>Table 5.28 Memory Expansion Mode and Microprocessor Mode</b> $t_{ac1}(AD-DB)$ expression modified  |
|      |              | 75          | • <b>Table 5.44 Electrical Characteristics</b> $I_{CC}$ standard value revised  |
|      |              | 78          | • <b>Table 5.47 Flash Memory Electrical Characteristics</b> $T_{opr}$ value modified  |
| 1.21 | Jul.08, 2005 |             | <b>Special Function Register (SFR)</b>  |
|      |              | 37          | • The TCSPR register Value after reset modified   |
|      |              |             | <b>Electrical Characteristics</b>   |
|      |              | 45          | • <b>Table 5.2 Electrical Characteristics</b> Parameter $f(BCLK)$ and its values added  |
|      |              | 51          | • <b>Table 5.10 Memory Expansion Mode and Microprocessor Mode</b> $t_{ac1}(RD-DB)$ expression on Note 1 modified; $t_{ac2}(RD-DB)$ expression on Note 1 added                       |



REVISION HISTORY

M32C/84 Group (M32C/84, M32C/84T) Datasheet

| Rev. | Date | Description |   |
|------|------|-------------|---|
|      |      | Page        | Summary   |
|      |      | 57          | <ul style="list-style-type: none"> <li>• <b>Figure 5.3 Vcc1=Vcc2=5V Timing Diagram (1)</b> <math>t_{W(ER)}</math> expression on Note 3 modified; <math>t_{CYC}</math> expression added</li> </ul>   |
|      |      | 58          | <ul style="list-style-type: none"> <li>• <b>Figure 5.4 Vcc1=Vcc2=5V Timing Diagram (2)</b> <math>t_{AC2(AD-DB)}</math> expression on Note 1 modified; <math>t_{H(ALE-AD)}</math> expressions on Notes 1 and 2 modified; <math>t_{CYC}</math> expression added</li> </ul>  |
|      |      | 63          | <ul style="list-style-type: none"> <li>• <b>Table 5.28 Memory Expansion Mode and Microprocessor Mode</b> <math>t_{AC1(RD-DB)}</math> expression on Note 1 modified; <math>t_{AC2(RD-DB)}</math> expression on Note 1 added</li> </ul>   |
|      |      | 68          | <ul style="list-style-type: none"> <li>• <b>Figure 5.7 Vcc1=Vcc2=3.3V Timing Diagram (1)</b> <math>t_{W(ER)}</math> expression on Note 3 modified; <math>t_{CYC}</math> expression added</li> </ul>   |
|      |      | 69          | <ul style="list-style-type: none"> <li>• <b>Figure 5.8 Vcc1=Vcc2=3.3V Timing Diagram (2)</b> <math>t_{AC2(RD-DB)}</math> expression on Note 1 modified; <math>t_{H(ALE-AD)}</math> expressions on Notes 1 and 2 modified; <math>t_{H(WR-CS)}</math> expression on Note 2 modified; <math>t_{CYC}</math> expression added</li> </ul> |
|      |      | 74          | <ul style="list-style-type: none"> <li>• <b>Table 5.43 Electrical Characteristics</b> Parameter <math>f(BCLK)</math> and its values added</li> </ul>  |
|      |      | 78          | <ul style="list-style-type: none"> <li>• <b>Table 5.47 Flash Memory Version Electrical Characteristics</b> Measurement condition changed</li> </ul>   |
|      |      |             |   |