

September 1983 Revised January 2005

# MM74HCT14 Hex Inverting Schmitt Trigger

### **General Description**

The MM74HCT14 utilizes advanced silicon-gate CMOS technology to achieve the low power dissipation and high noise immunity of standard CMOS, as well as the capability to drive 10 LS-TTL loads.

The 74HCT logic family is functionally and pinout compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### **Features**

- Typical propagation delay: 13 ns
- Wide power supply range: 2–6V
- Low quiescent current: 10 µA maximum
- Low input current: 1 µA maximum
- Fanout of 10 LS-TTL loads
- $\blacksquare$  Typical hysteresis voltage: 0.9V at  $V_{CC} = 4.5V$
- TTL, LS pin-out and input threshold compatible

### **Ordering Codes:**

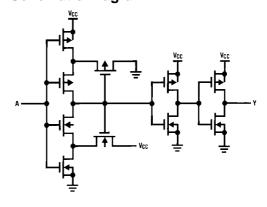
Order Number	Package	Package Description			
	Number				
MM74HCT14M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow			
MM74HCT14MX_NL	M14A	Pb-Free 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow			
MM74HCT14SJ	M14D	Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide			
MM74HCT14MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide			
MM74HCT14N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide			

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code. Pb-Free package per JEDEC J-STD-020B.

### **Connection Diagram**

# Pin Assignments for DIP, SOIC, SOP and TSSOP VCC A6 Y6 A5 Y5 A4 Y4 14 13 112 11 10 9 8 1 1 2 3 4 5 6 7 A1 Y1 A2 Y2 A3 Y3 GND Top View

### **Schematic Diagram**



### **Absolute Maximum Ratings**(Note 1)

(Note 2)

Supply Voltage (V<sub>CC</sub>) -0.5 to +7.0V DC Input Voltage (V<sub>IN</sub>) -1.5 to  $V_{CC} + 1.5V$ DC Output Voltage (V<sub>OUT</sub>) -0.5 to  $V_{CC} + 0.5V$ Clamp Diode Current ( $I_{IK}$ ,  $I_{OK}$ )  $\pm$  20 mA DC Output Current, per pin (I<sub>OUT</sub>) ± 25 mA DC  $V_{CC}$  or GND Current, per pin ( $I_{CC}$ )  $\pm$  50 mA Storage Temperature Range (T<sub>STG</sub>) -65°C to +150°C Lead Temperature (T<sub>L</sub>)

(Soldering 10 seconds)

### **Recommended Operating Conditions**

Units Max Supply Voltage (V<sub>CC</sub>) 6 V DC Input or Output Voltage 0  $\mathsf{V}_{\mathsf{CC}}$ ٧  $(V_{IN}, V_{OUT})$ °С Operating Temperature Range  $(T_A)$  -40+85

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

### DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	V <sub>CC</sub>	T <sub>A</sub> = 25°C		T <sub>A</sub> = -40 to 85°C	Units
		Conditions	*cc	Тур	Guar	anteed Limits	Units
$V_{T+}$	Positive Going	Minimum	4.5V	1.5	1.2	1.2	V
	Threshold Voltage		5.5V	1.7	1.4	1.4	V
		Maximum	4.5V	1.5	1.9	1.9	V
			5.5V	1.7	2.1	2.1	V
V <sub>T-</sub>	Negative Going	Minimum	4.5V	0.9	0.5	0.5	V
	Threshold Voltage		5.5V	1.0	0.6	0.6	V
		Maximum	4.5V	0.9	1.2	1.2	V
			5.5V	1.0	1.4	1.4	V
V <sub>H</sub>	Hysteresis Voltage	Minimum	4.5V	0.6	0.4	0.4	V
			5.5V	0.7	0.4	0.4	V
		Maximum	4.5V	0.6	1.4	1.4	V
			5.5V	0.7	1.5	1.5	V
V <sub>OH</sub>	Minimum HIGH Level	$V_{IN} = V_{IL}$					
	Output Voltage	$ I_{OUT}  = 20 \mu A$		V <sub>CC</sub>	V <sub>CC</sub> - 0.1	V <sub>CC</sub> - 0.1	V
		$ I_{OUT}  = 4.0 \text{ mA}, V_{CC} = 4.5 \text{V}$		4.2	3.98	3.84	V
		$ I_{OUT}  = 4.8 \text{ mA}, V_{CC} = 5.5 \text{V}$		5.2	4.98	4.98	V
V <sub>OL</sub>	Maximum LOW Level	$V_{IN} = V_{IH}$					
	Voltage	$ I_{OUT}  = 20 \mu A$		0	0.1	0.1	V
		$ I_{OUT}  = 4.0 \text{ mA}, V_{CC} = 4.5 \text{V}$		0.2	0.26	0.33	V
		$ I_{OUT}  = 4.8 \text{ mA}, V_{CC} = 5.5 \text{V}$		0.2	0.26	0.33	V
I <sub>IN</sub>	Maximum Input Current	V <sub>IN</sub> = V <sub>CC</sub> or GND			±0.1	±1.0	
		V <sub>IH</sub> or V <sub>IL</sub>			±0.1	±1.0	μΑ
I <sub>CC</sub>	Maximum Quiescent	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5V		1.0	10	μА
	Supply Current	$I_{OUT} = 0 \mu A$	3.57		1.0	10	μΑ
		V <sub>IN</sub> =2.4V or 0.5V (Note 3)	5.5V		2.4	2.4	mA

260°C

Note 3: For a power supply of 5V  $\pm$  10% the worst case output voltages ( $V_{OH}$ , and  $V_{OL}$ ) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case  $V_{IH}$  and  $V_{IL}$  occur at  $V_{CC}$  = 5.5V and 4.5V respectively. (The  $V_{IH}$  value at 5.5V is 3.85V.) The worst case leakage current ( $I_{IN}$ ,  $I_{CC}$ , and  $I_{OZ}$ ) occur for CMOS at the higher voltage and so the 6.0V values should be used.

### **AC Electrical Characteristics**

 $\mbox{V}_{CC} = 5\mbox{V}, \ \mbox{T}_{A} = 25\mbox{°C}, \ \mbox{C}_{L} = 15 \ \mbox{pF}, \ \mbox{t}_{r} = \mbox{t}_{f} = \mbox{6 ns}$ 

Symbol	Parameter	Conditions	Тур	Guaranteed Limit	Units
t <sub>PHL</sub> , t <sub>PLH</sub>	Maximum Propagation Delay		10	18	ns

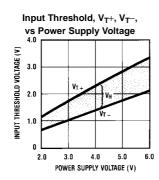
### **AC Electrical Characteristics**

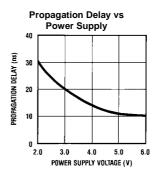
 $\text{V}_{CC}\text{=}5\text{V}\pm10\%,~C_{L}\text{=}50~\text{pF},~t_{f}\text{=}t_{f}\text{=}6~\text{ns}$  (unless otherwise specified)

Symbol	Parameter	Conditions	T <sub>A</sub> = 25°		T <sub>A</sub> = -40 to 85°C	Units
Gymbol	r arameter		Тур	Gua	ranteed Limits	Oints
t <sub>PHL</sub> , t <sub>PLH</sub>	Maximum Propagation Delay			20	25	ns
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Rise and Fall Time		9	15	19	ns
C <sub>PD</sub>	Power Dissipation	(per gate)		25		pF
	Capacitance (Note 4)					
C <sub>IN</sub>	Maximum Input Capacitance		5	10	10	pF

Note 4:  $C_{PD}$  determines the no load dynamic power consumption,  $P_D = C_{PD} \ V_{CC} 2 \ f + I_{CC} \ V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} \ V_{CC} f + I_{CC}$ .

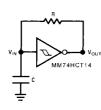
### **Typical Performance Characteristics**





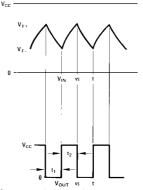
## **Typical Applications**

### Low Power Oscillator

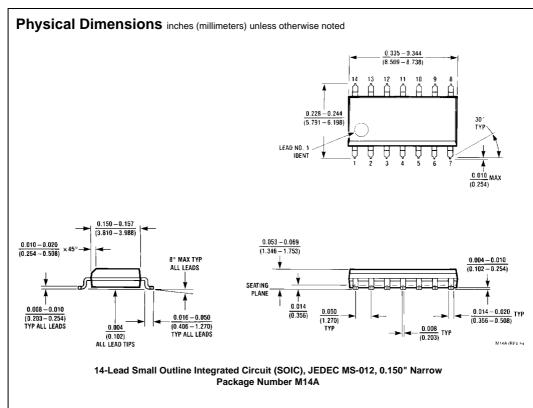


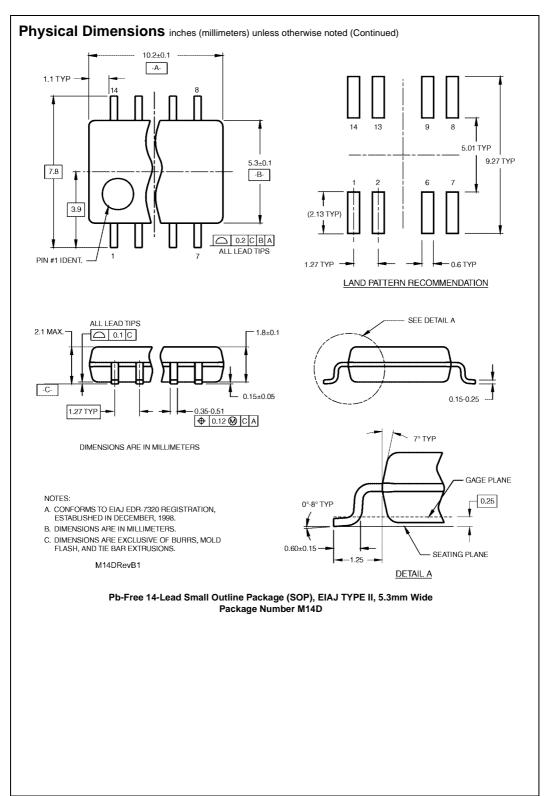
$$t_2 \approx RC \ln \frac{V_{CC} - V_{T-}}{V_{CC} - V_{T+}}$$

$$f \approx \frac{1}{RC \ln \frac{V_{T+}(V_{CC} - V_{T-})}{V_{T-}(V_{CC} - V_{T+})}}$$

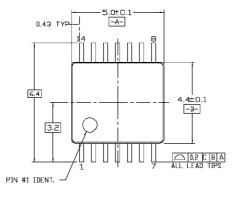


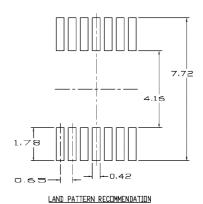
Note: The equations assume  $t_1 + t_2 >> t_{pd0} + t_{pd1}$ 

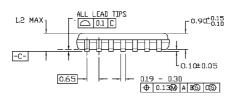


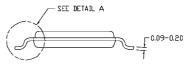


# Physical Dimensions inches (millimeters) unless otherwise noted (Continued)





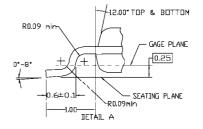




### NOTES:

- A CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB-REF NOTE 6, DATED 7/93 B. DIMENSIONS ARE IN MILLIMETERS
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
  D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982

MTC14revD



14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC14

### Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 0.740 - 0.770 (18.80 - 19.56)(2.286) 14 13 12 14 13 12 11 10 9 8 INDEX AREA 0.250 ± 0.010 (6.350 ± 0.254) PIN NO. 1 IDENT 1 2 3 4 5 6 7 1 2 3 $\frac{0.092}{(2.337)}$ DIA $\frac{0.030}{(0.762)}$ MAX OPTION 1 OPTION 02 $\frac{0.135 \pm 0.005}{(3.429 \pm 0.127)}$ 0.300 - 0.320(7.620 - 8.128) 0.065 0.145 - 0.2000.060 4° TYP Optional (3.683 - 5.080)(1.524) \* 95° ±5° $\frac{0.008 - 0.016}{(0.203 - 0.406)} \text{ TYP}$ ก ก่อก 0.125 - 0.150(3.175 - 3.810) $\frac{0.075 \pm 0.015}{(1.905 \pm 0.381)}$ 0.280 0.014 - 0.023 TYP (7.112)-MIN $\frac{0.100 \pm 0.010}{(2.540 \pm 0.254)} \text{ TYP}$ $\frac{0.050 \pm 0.010}{(1.270 - 0.254)} \text{ TYP}$ $0.325 ^{\,+\,0.040}_{\,-\,0.015}$ $\left(8.255 + 1.016 \atop -0.381\right)$

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

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