microelectronics group

Lucent Technologies
Bell Labs Innovations

TTRN0110G
10 Gbits/s Clock Synthesizer, 16:1 Data Multiplexer

Features

- Fully-integrated 10 GHz clock synthesizer; 16:1 data multiplexer

- Supports standard OC-192/STM-64 data rate of 9.9532 GHz as well as FEC rate of 10.6642 GHz

- Supported clocking modes include the following:
  — Supports forward directional clocking for parallel transfer of input data with 311 MHz or 622 MHz data clocks
  — Supports contradirectional clocking for parallel transfer of input data based on a 622 MHz output clock
  — Supports a clockless data transfer mode

- Allows a 155.52 MHz or 622.08 MHz reference clock with common PLL loop filter components for both frequencies

- Additional 10 Gbits/s CML serial data output for system loopback

- Supports 10 GHz clock output for clocked laser driver applications

- Loss of lock indication

- Single 3.3 V supply

- LVDS 622.08 Mbits/s digital I/O

- Power dissipation as low as 1.2 W

- Available in a 198 BGA package

- Jitter generation and jitter transfer compliant with the following:
  — *Telcordia Technologies** GR-1377 CORE
  — ITU-T G.825
  — ITU-T G.958

- Fully compatible with the Optical Interface Forum specification OIF99.102.5

* *Telcordia Technologies* is a registered trademark of Bell Communications Research, Inc.

Applications

- SONET/SDH optical modules

- SONET/SDH line origination equipment

- SONET/SDH add/drop multiplexers

- SONET/SDH cross connects

- SONET/SDH test equipment
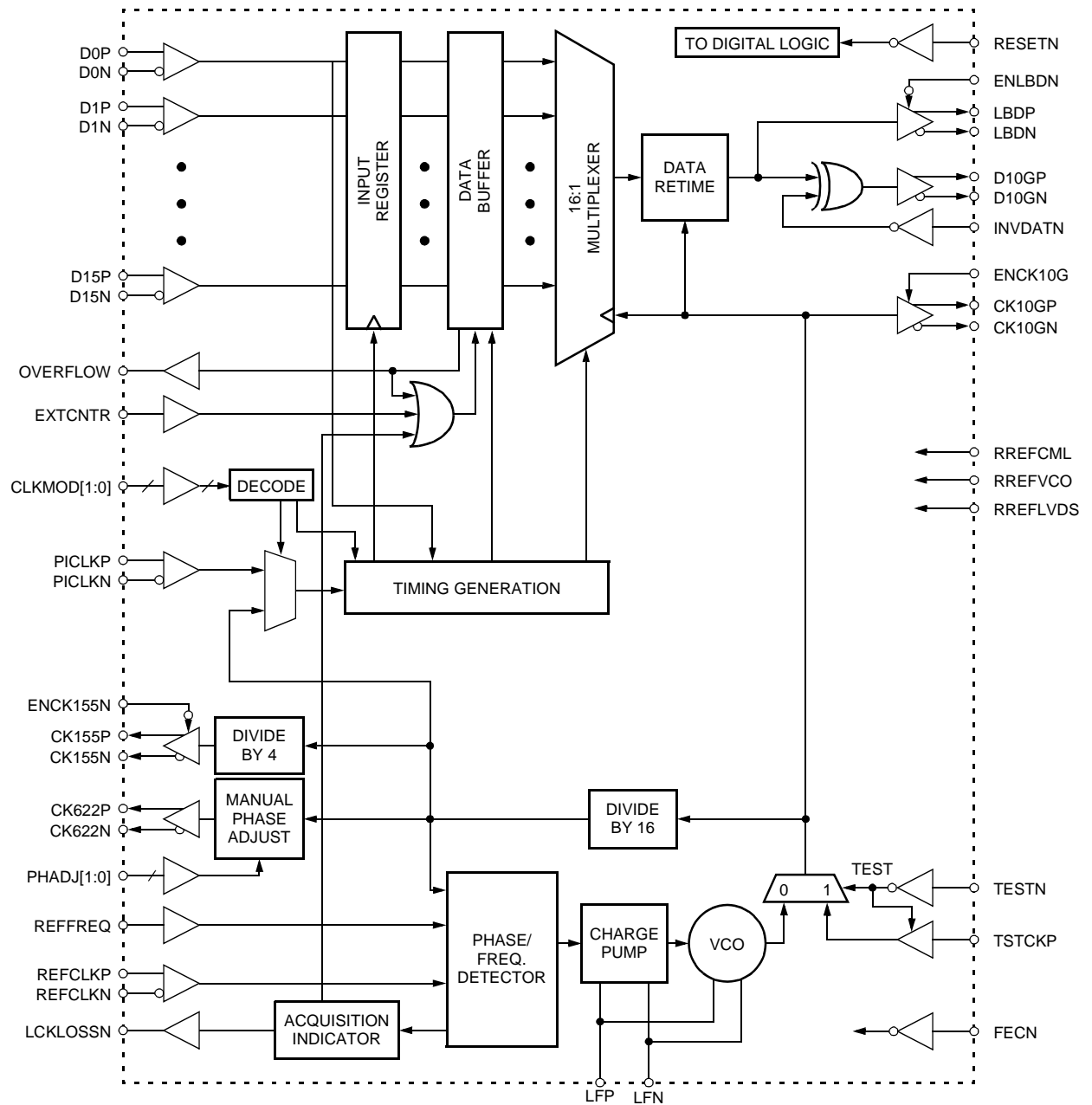
- Digital video transmission

Description

The Lucent Technologies Microelectronics Group TTRN0110G device provides a 16:1 multiplexer, accepts 16 differential LVDS data inputs and a 155.52 MHz or 622.08 MHz reference clock, and generates a CML 10 Gbits/s clock and data output. Both forward directional and contradirectional clocking schemes are supported for transferring data across the parallel interface. When contraclocking is used, the TTRN0110G provides one of four phases of a 622.08 MHz clock output back upstream to the data chip. The device also supports a clockless parallel data transfer mode. The TTRN0110G can be operated at either the standard OC-192/STM-64 data rate of 9.9532 GHz or at the FEC rate of 10.6642 GHz.

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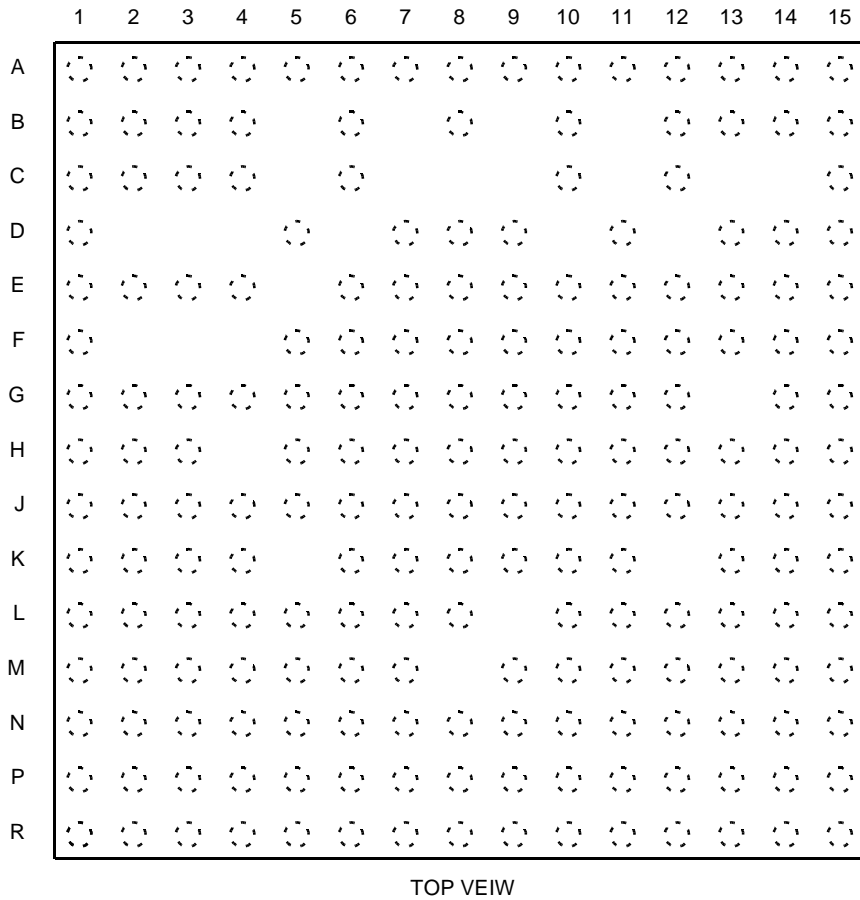
Description (continued)

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Note: Diagram is representative of device functionality and conceptual signal flow. Internal implementation details may be different than shown.

Figure 1. Functional Block Diagram of TTRN0110G

Pin Information

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Figure 2. Pin Diagram of 198-Pin BGA

Pin Information (continued)

Table 1. Pin Assignments for 198-Pin BGA by Pin Number Order

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	GND	C1	GND	E1	GND	G1	GND
A2	GND	C2	GND	E2	GND	G2	GND
A3	GND	C3	GND	E3	GND	G3	GND
A4	GND	C4	V$_{CCD}$	E4	GND	G4	GND
A5	CK10GN	C5	—	E5	—	G5	V$_{CCD}$
A6	GND	C6	GND	E6	GND	G6	GND
A7	CK10GP	C7	—	E7	INVDATN	G7	GND
A8	GND	C8	—	E8	GND	G8	GND
A9	D10GN	C9	—	E9	TESTN	G9	GND
A10	GND	C10	GND	E10	GND	G10	GND
A11	D10GP	C11	—	E11	GND	G11	GND
A12	GND	C12	GND	E12	GND	G12	LCKLOSSN
A13	GND	C13	—	E13	V$_{CCA}$	G13	—
A14	GND	C14	—	E14	V$_{CCA}$	G14	V$_{CCD}$
A15	GND	C15	TSTCKP	E15	LFN	G15	V$_{CCA}$
B1	GND	D1	LBDP	F1	LBDN	H1	V$_{CCD}$
B2	GND	D2	—	F2	—	H2	GND
B3	GND	D3	—	F3	—	H3	GND
B4	GND	D4	—	F4	—	H4	—
B5	—	D5	GND	F5	GND	H5	GND
B6	GND	D6	—	F6	GND	H6	GND
B7	—	D7	V$_{CCD}$	F7	ENLBDN	H7	GND
B8	GND	D8	RREFCML	F8	GND	H8	GND
B9	—	D9	V$_{CCD}$	F9	ENCK10G	H9	GND
B10	GND	D10	—	F10	GND	H10	GND
B11	—	D11	GND	F11	GND	H11	GND
B12	GND	D12	—	F12	RREFLVDS	H12	GND
B13	V$_{CCD}$	D13	GND	F13	V$_{CCA}$	H13	GND
B14	GND	D14	GND	F14	RREFVCO	H14	RESETN
B15	GND	D15	GND	F15	LFP	H15	CLKMOD[0]

Note: — refers to no ball. A ball has been removed for routing purposes.

Pin Information (continued)

Table 1. Pin Assignments for 198-Pin BGA by Pin Number Order (continued)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
J1	D0P	K13	ENCK155N	M9	GND	P5	D8P
J2	GND	K14	FECN	M10	D15P	P6	D9P
J3	GND	K15	EXTCNTR	M11	GND	P7	D10P
J4	GND	L1	D1P	M12	GND	P8	D12N
J5	V$_{CCD}$	L2	GND	M13	GND	P9	D13N
J6	V$_{CCD}$	L3	GND	M14	REFCLKN	P10	D14N
J7	GND	L4	GND	M15	PHADJ[0]	P11	CK155N
J8	GND	L5	GND	N1	D2P	P12	PICLKN
J9	GND	L6	V$_{CCD}$	N2	D3P	P13	CK622N
J10	GND	L7	GND	N3	D4N	P14	GND
J11	GND	L8	V$_{CCD}$	N4	GND	P15	GND
J12	GND	L9	—	N5	D7N	R1	GND
J13	V$_{CCD}$	L10	GND	N6	GND	R2	D5P
J14	OVRFLW	L11	GND	N7	D10N	R3	D5N
J15	CLKMOD[1]	L12	GND	N8	D12P	R4	D6N
K1	D0N	L13	GND	N9	GND	R5	D8N
K2	GND	L14	PHADJ[1]	N10	D15N	R6	D9N
K3	GND	L15	REFFREQ	N11	GND	R7	D11P
K4	GND	M1	D1N	N12	GND	R8	D11N
K5	—	M2	GND	N13	GND	R9	D13P
K6	GND	M3	D4P	N14	REFCLKP	R10	D14P
K7	GND	M4	GND	N15	GND	R11	CK155P
K8	GND	M5	D7P	P1	D2N	R12	PICLKP
K9	V$_{CCD}$	M6	GND	P2	D3N	R13	CK622P
K10	GND	M7	GND	P3	GND	R14	GND
K11	V$_{CCD}$	M8	—	P4	D6P	R15	GND
K12	—						

Note: — refers to no ball. A ball has been removed for routing purposes.

Pin Information (continued)

Note: In Table 2, when operating the TTRN0110G device at the OC-192/STM-64 rate, 10 Gbits/s should be interpreted as 9.9532 Gbits/s. When operating the TTRN0110G device at the RS FEC OC-192/STM-64 rate, 10 Gbits/s should be interpreted as 10.6642 Gbits/s.

Table 2. Pin Descriptions—10 Gbits/s and Related Signals

Pin	Symbol*	Type†	Level	Name/Description
A11	D10GP	O	CML	**Data Output (10 Gbits/s NRZ).** 10 Gbits/s differential data output. Note that this data rate will scale by 15/14 when operating at the FEC rate.
A9	D10GN			
D1	LBDP	O	CML	**Loopback Data Output.** Additional 10 Gbits/s differential data output for system loopback. Note that this data rate will scale by 15/14 when operating at the FEC rate.
F1	LBDN			
A7	CK10GP	O	CML	**Clock Output (10 GHz).** 10 GHz differential clock output. Note that this clock frequency will scale by 15/14 when operating at the FEC rate.
A5	CK10GN			
K14	FECN	I^u	CMOS	**FEC Rate (Active-Low).** Selects the normal OC-192/STM-64 rate of 9.9532 GHz or the FEC rate of 10.6642 GHz. 0 = FEC rate of 10.6642 GHz 1 or no connection = OC-192/STM-64 rate of 9.9532 GHz Note that all input and output clock and data rates are scaled by 15/14 when operating at the FEC rate.
D8	RREFCML	I	Analog	**Resistor Reference CML.** CML current bias reference resistor. (See Table 16, page 23 for values.)
F9	ENCK10G	I^u	CMOS	**Enable CK10GP/N Clock Output.** 0 = CK10GP/N buffer powered off 1 or no connection = CK10GP/N buffer enabled
F7	ENLBDN	I^u	CMOS	**Enable LBDP/N Data Output (Active-Low).** 0 = LBDP/N buffer enabled 1 or no connection = LBDP/N buffer powered off
E7	INVDATN	I^u	CMOS	**Invert D10G Data Output (Active-Low).** 0 = invert 1 or no connection = noninvert
C15	TSTCKP	I	CML	**Test Clock Input.** (Buffer is powered down when TESTN = 1.)
E9	TESTN	I^u	CMOS	**Select Test Clock (Active-Low).** 0 = select test clock 1 or no connection = select VCO
F14	RREFVCO	I	Analog	**Resistor Reference VCO.** VCO bias reference resistor. Connect a **TBD** kΩ resistor to V_CCD.

* Differential pairs are indicated by P and N suffixes. For nondifferential pins, N at the end of the symbol name designates active-low.
† I = input, O = output. I^u indicates an internal pull-up resistor on this pin. I^d indicates an internal pull-down resistor on this pin.

Pin Information (continued)

Note: In Table 3, when operating the TTRN0110G device at the OC-192/STM-64 rate, 155 Mbits/s should be interpreted as 155.52 Mbits/s. When operating the TTRN0110G device at the RS FEC OC-192/STM-64 rate, 155 Mbits/s should be interpreted as 166.62 Mbits/s.

Table 3. Pin Descriptions—622.08 Mbits/s and Related Signals

Pin	Symbol*	Type†	Level	Name/Description
M10	D15P	I	LVDS	**Data Input (622 Mbits/s).** 622 Mbits/s differential data input. D15 is the most significant bit and is transmitted first on the D10GP/N output. Note that the data rate will scale by 15/14 when operating at the FEC rate.
N10	D15N			
R10	D14P		LVDS	
P10	D14N			
R9	D13P		LVDS	
P9	D13N			
N8	D12P		LVDS	
P8	D12N			
R7	D11P		LVDS	
R8	D11N			
P7	D10P		LVDS	
N7	D10N			
P6	D9P		LVDS	
R6	D9N			
P5	D8P		LVDS	
R5	D8N			
M5	D7P		LVDS	
N5	D7N			
P4	D6P		LVDS	
R4	D6N			
R2	D5P		LVDS	
R3	D5N			
M3	D4P		LVDS	
N3	D4N			
N2	D3P		LVDS	
P2	D3N			
N1	D2P		LVDS	
P1	D2N			
L1	D1P		LVDS	
M1	D1N			
J1	D0P		LVDS	
K1	D0N			

* Differential pairs are indicated by P and N suffixes. For nondifferential pins, N at the end of the symbol name designates active-low.
† I = input, O = output. I^u indicates an internal pull-up resistor on this pin. I^d indicates an internal pull-down resistor on this pin.

Pin Information (continued)

Table 3. Pin Descriptions—622.08 Mbits/s and Related Signals (continued)

Pin	Symbol*	Type†	Level	Name/Description
R13 P13	CK622P CK622N	O	LVDS	**Clock Output (622 MHz).** 622 MHz differential clock output. Note that this clock frequency will scale by 15/14 when operating at the FEC rate.
M15 L14	PHADJ[0] PHADJ[1]	I^t	CMOS	**Phase Adjust.** Adjusts phase of CK622 in 90 degree steps.
R11 P11	CK155P CK155N	O	LVDS	**Clock Output (155 MHz).** 155 MHz differential clock output. Note that this clock frequency will scale by 15/14 when operating at the FEC rate.
K13	ENCK155N	I^u	CMOS	**Enable CK155P/N Clock Output (Active-Low).** 0 = CK155P/N buffer enabled 1 or no connection = CK155P/N buffer powered off
R12 P12	PICLKP PICLKN	I	LVDS	**Parallel Input Clock (622 MHz).** 622 MHz differential clock input used to register parallel data when using forward directional clocking mode. Note that this clock frequency will scale by 15/14 when operating at the FEC rate.
H15 J15	CLKMOD[0] CLKMOD[1]	I^u	CMOS	**Clock Mode Select.** Selects clocking method for data transfer mode. 00 = forward directional clocking 01 = clockless transfer 11 or no connections = contraclocking
G12	LCKLOSSN	O	CMOS	**Loss of Lock (Active-Low).** 0 = PLL out of lock
K15	EXTCNTR	I^d	CMOS	**External Center.** Centers the pointers in the parallel data storage element.
J14	OVRFLW	O	CMOS	**Data Storage Overflow.** Indicates (active high) when an overflow has occurred in the parallel data storage element.
N14 M14	REFCLKP REFCLKN	I	LVDS	**Reference Clock Input (622.08 MHz or 155.52 MHz).** Note that this clock frequency must scale by 15/14 when operating the device at the FEC rate.
L15	REFFREQ	I^u	CMOS	**Reference Clock Frequency.** Selects frequency of REFCLKP/N. 0 = 155 MHz 1 or no connection = 622 MHz
F15 E15	LFP LFN	I	Analog	**Loop Filter PLL.** Connect LFP and LFN to loop filter (see Figure 3, page 11).
F12	RREFLVDS	I	Analog	**Resistor Reference LVDS.** LVDS bias reference resistor. Connect a **TBD** kΩ resistor to V$_{CCD}$.

* Differential pairs are indicated by P and N suffixes. For nondifferential pins, N at the end of the symbol name designates active-low.
† I = input, O = output. I^u indicates an internal pull-up resistor on this pin. I^d indicates an internal pull-down resistor on this pin.

Table 4. Pin Descriptions—Reset

Pin	Symbol*	Type†	Level	Name/Description
H14	RESETN	I^u	CMOS	**Reset (Active-Low).** Resets all synchronous logic. During a reset, the true data outputs are in the low state and the barred data outputs are in the high state. Reset must be held active low for a minimum of 6.4 ns while the internal oscillator is active. 0 = reset 1 or no connection = normal operation

* Differential pairs are indicated by P and N suffixes. For nondifferential pins, N at the end of the symbol name designates active-low.
† I = input, O = output. I^u indicates an internal pull-up resistor on this pin. I^d indicates an internal pull-down resistor on this pin.

Pin Information (continued)

Table 5. Pin Descriptions—Power and Ground

Note: V_{CCA} and V_{CCD} have the same dc value, which is represented as V_{CC} unless otherwise specified. However, high-frequency filtering is suggested between the individual supplies.

Pin	Symbol*	Type†	Level	Name/Description
E13, E14, F13, G15	V_{CCA}	I	Power	**Analog Power Supply (3.3 V).**
B13, C4, D7, D9, G5, G14, H1, J5, J6, J13, K9, K11, L6, L8	V_{CCD}	I	Power	**Digital Power Supply (3.3 V).**
A1—A4, A6, A10, A12—A15, B1—B4, B6, B8, B10, B12, B14, B15, C1—C3, C6, C10, C12, D5, D11, D13—D15, E1—E4, E6, E8, E10—E12, F5, F6, F8, F10, F11, G1—G4, G6—G11, H2, H3, H5—H13, J2—J4, J7—J12, K2—K4, K6—K8, K10, L2—L5, L7, L10—L13, M2, M4, M6, M7, M9, M11—M13, N4, N6, N9, N11—N13, N15, P3, P14, P15, R1, R14, R15	GND	I	Ground	**Ground.**

* Differential pairs are indicated by P and N suffixes. For nondifferential pins, N at the end of the symbol name designates active-low.

† I = input, O = output. I^u indicates an internal pull-up resistor on this pin. I^d indicates an internal pull-down resistor on this pin.

Functional Overview

The TTRN0110G performs the clock synthesis and 16:1 data multiplexing operations required to support 10 Gbits/s* OC-192/STM-64 applications compliant with *Telcordia Technologies* and ITU standards. Parallel 622 Mbits/s data is clocked into an input register. Both forward directional and contradirectional clocking modes are supported as well as a clockless data transfer mode. The data is then multiplexed into a 10 Gbits/s serial stream and output buffered for interfacing to a laser driver. A 10 GHz clock is synthesized from a reference clock and is used to retime the serial data. The 10 GHz clock is optionally available as an output.

FEC Rate Support

The TTRN0110G will support both the normal OC-192/STM-64 rate of 9.9532 GHz and the forward error correction (FEC) rate of 10.6642 GHz. The FECN pin selects the rate at which the part is operating. Throughout this document, most specifications are given in terms of the normal operating rate only. All frequency-based specifications are to be multiplied by 15/14 when operating at the FEC rate and all time-based specifications, with the exception of electrical signal rise and fall times, are to be multiplied by 14/15 when operating at the FEC rate. For example, the reference clock would need to be applied at 166.628 MHz or 666.515 MHz and the parallel data interface would operate at 666.515 MHz when FECN = 0.

Clock Synthesizer Operation

The clock synthesizer uses a PLL to synthesize a 10 GHz clock from a reference frequency. A 622 MHz clock derived from the 10 GHz synthesized clock may be used to clock in the parallel data in contradirectional clocking applications.
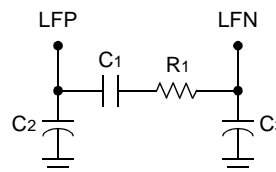
Clock Synthesizer Loop Filter

A typical loop filter that provides adequate damping for less than 0.1 dB of jitter peaking is shown in Figure 3. Connect the filter components to LFP and LFN. The component values can be varied to adjust the loop dynamic response (see Table 6).

Table 6. Clock Synthesizer Loop Filter Component Values

Components	Values for 8 MHz Loop Bandwidth
C1†	**TBD** μF ± 10%
C2, C3	**TBD** pF ± 20%
R1	**TBD** Ω ± 5%

† Capacitor C1 should be either ceramic or nonpolar.

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Figure 3. Clock Synthesizer Loop Filter Components

* The OC-192/STM-64 data rate of 9.95328 Gbits/s is typically approximated as 10 Gbits/s in this document when referring to the application rate. Similarly, the low-speed parallel interface data rate of 622.08 Mbits/s is typically approximated as 622 Mbits/s. The exact frequencies are used only when necessary for clarity.

Clock Synthesizer Operation (continued)

Clock Synthesizer Settling Time

The clock synthesizer will acquire phase/frequency lock after a valid REFCLKP/N signal is applied. The actual time to acquire lock is a function of the loop bandwidth selected. The loop will acquire lock within 5 ms when using the external loop bandwidth components corresponding to a corner of less than 8 MHz.

Loss of Lock Indicator (LCKLOSSN)

The LCKLOSSN pin indicates (active-low) when the clock synthesizer has exceeded phase-lock limits with the incoming REFCLKP/N phase. The lock detect function compares the phases of the input 155 MHz or 622 MHz clock at the REFCLKP/N pins with the internally generated 622 MHz output clock at the CK622P/N pin. When the phase difference in the two signals is close to zero as determined by a second internal phase detector and filter, the lock detect signal LCKLOSSN is set to a logic high. When the phase difference between the two signals is changing at a rate exceeding the filter's cutoff frequency, the TTRN0110G is declared out of lock and LCKLOSSN is set to a logic low. If a set of highly damped phase-locked loop parameters is chosen, LCKLOSSN may exhibit more than one positive edge transition during the acquisition process before a steady logic-high state is achieved.

Upon a transition from the out-of-lock condition to the in-lock condition, the parallel data storage element pointers are centered.

Clock Synthesizer Generated Jitter

The clock synthesizer's generated jitter performance meets the requirements shown in Table 7. These specifications apply to the jitter generated at the 10 GHz clock pins CK10GP/N when the jitter on the reference clock REFCLKP/N is within the specifications given in Table 10 on page 20, and the loop filter components are chosen to provide a loop bandwidth of less than 8 MHz.

**Table 7. Clock Synthesizer Generated Jitter Specifications**

Parameter	Typical	Max (Device)*	Unit

Generated Jitter (p-p) SONET Rate:
    Measured with 50 kHz to 80 MHz Bandpass Filter
    1 UI = 1/9.95328 GHz
	TBD	0.09	UIp-p

Generated Jitter (p-p) FEC Rate:
    Measured with **??** kHz to **??** MHz Bandpass Filter
    1 UI = (14/15)(9.95328 GHz)
	TBD	0.09	UIp-p

* This denotes the device specification for system SONET/SDH compliance when the loop filter in Table 6 and Figure 3 is used.

Clock Synthesizer Operation (continued)

Clock Synthesizer Jitter Transfer

The clock synthesizer's jitter transfer performance meets the requirement shown in Figure 4 when the loop filter values shown in Table 6 on page 11 are used.
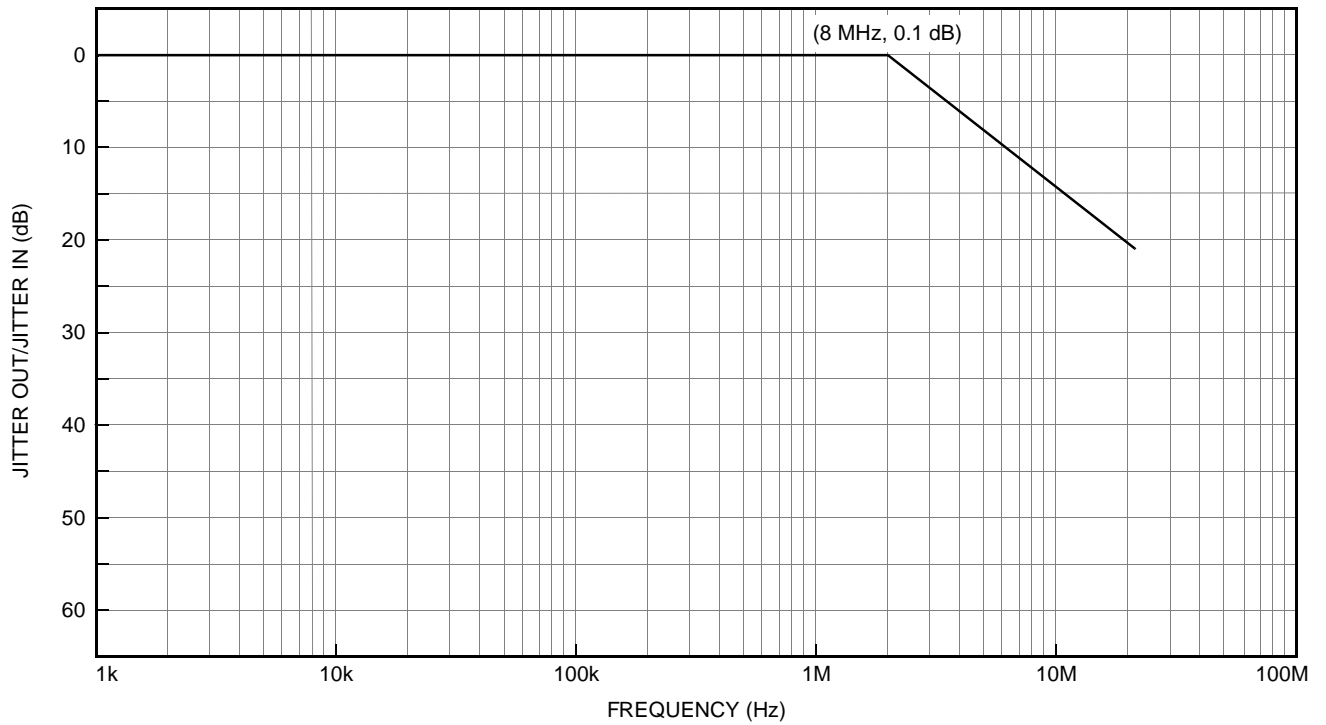
Figure 4. Clock Synthesizer Jitter Transfer

Multiplexer Operation

The parallel 622 Mbits/s data is clocked into an input buffer then clocked into a 16:1 multiplexer. The relationship between the parallel D[15:0]P/N input data and the serial output data D10GP/N is given in Figure 5. The D15 bit is the most significant bit (MSB) and is shifted out first in time in the serial output stream.
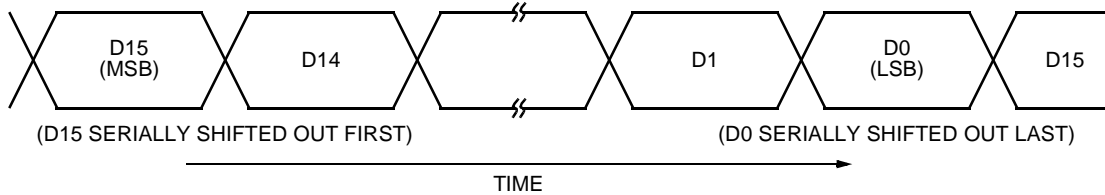
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Figure 5. Parallel Input to Serial Output Data Relationship

10 GHz Clock Output Enable (ENCK10G)

The 10 GHz clock output CK10GP/N may be disabled by setting the ENCK10G pin to logic low. ENCK10G is an active-high CMOS input with a pull-up resistor so the default condition will enable the CK10GP/N output and a ground or logic-low signal must be applied to disable the CK10GP/N output. When disabled, the CK10GP/N pins should be either left floating or be connected to a load which returns to Vcc. The output must not be connected directly to ground when it is disabled.

Loopback 10 GHz Data Output (LBDP/N, ENLBDN)

An alternate 10 Gbits/s CML data output is available on the LBDP/N pin. This pin is provided for use in system loopback testing and avoids the need for off-chip signal splitting of the data signal path. The alternate 10 Gbits/s loopback data output may be enabled by setting the ENLBDN pin to logic low. ENLBDN enable is an active-low CMOS input with a pull-up resistor so the default condition will disable the LBDP/N output, and a ground or logic-low signal must be applied to enable the loopback output. When disabled, the LBDP/N pin should be either left floating, or be connected to a load which returns to Vcc. The output must not be connected directly to ground when it is disabled.

Reset (RESETN)

The RESETN signal must be held active low for a minimum of 6.4 ns when the internal VCO is active and running, in order for the internal logic to be completely reset.

Clocking Modes and Timing Adjustments

The TTRN0110G supports four timing modes for the 622 Mbits/s data input: forward directional 622, forward directional 311, contradirectional, and clockless transfer, as selected by the CLKMOD[1:0] pins.

Forward Directional 622 Clocking Mode (CLKMOD[1:0] = 00, EXTCNTR, PICLKP/N, OVRFLW)

In forward directional 622 clocking mode (CLKMOD[1:0] = 00), data is clocked into a 16-bit wide input register on the TTRN0110G device by the PICLKP/N parallel input clock. The setup and hold times for the data relative to PICLK are given in Figure 8 on page 24 and Table 18 on page 26. An internal data buffer is used to absorb timing drift between PICLK and the internal clocks derived from the 10 GHz internal oscillator. A PICLK phase drift of up to ±1600 ps relative to the internal clocks can be absorbed by the buffer, as long as the bandwidth of this phase drift is less than 16 MHz. Note that the read and write addresses for the data buffer must be initially reset in order for the buffer to absorb the full range of PICLK phase drift.

The read and write addresses for the data buffer are reset at the time the PLL acquires lock and the loss of lock indicator transitions from the out-of-lock condition to the in-lock condition. After LCKLOSSN goes high the buffer will be centered and data integrity will be obtained within approximately 2 μs.

The data buffer can also be recentered by applying EXTCNTR (active high) for a minimum of 6.4 ns. After EXTCNTR goes low the buffer will be centered and data integrity will be lost and subsequently restored within approximately 2 μs.

If the timing drift exceeds ±1600 ps, the data buffer will indicate overflow with a logic-high signal on the OVRFLW pin for a minimum of 6.4 ns. After a time interval of 4.8 ns after OVRFLW goes low, the buffer will be recentered and data integrity will be lost and subsequently restored within approximately 2 μs. During the 11.2 ns between the rising edge of OVRFLW and the recentering of the buffer, data integrity may be lost if the timing drift exceeds ±2000 ps.

If the output clock CK622P/N is not used when in CLKMOD[1:0] = 00, it can be left unconnected to conserve power.

Forward Directional 311 Clocking Mode (CLKMOD[1:0] = 10, EXTCNTR, PICLKP/N, OVRFLW)

In forward directional 311 clocking mode (CLKMOD[1:0] = 10), data is clocked into a 16-bit wide input register on the TTRN0110G device by the PICLKP/N parallel input clock. In contrast to forward directional 622 mode, the PICLK signal is at half the data rate (311 MHz instead of 622 MHz). The setup and hold times for the data relative to PICLK are given in Figure 9 on page 24 and Table 18 on page 26. An internal data buffer is used to absorb timing drift between PICLK and the internal clocks derived from the 10 GHz internal oscillator. A PICLK phase drift of up to ±1600 ps relative to the internal clocks can be absorbed by the buffer, as long as the bandwidth of this phase drift is less than 500 kHz. Note that the read and write addresses for the data buffer must be initially reset in order for the buffer to absorb the full range of PICLK phase drift.

The read and write addresses for the data buffer are reset at the time the PLL acquires lock and the loss of lock indicator transitions from the out-of-lock condition to the in-lock condition. After LCKLOSSN goes high, the buffer will be centered and data integrity will be obtained within approximately 2 μs.

The data buffer can also be recentered by applying EXTCNTR (active high) for a minimum of 6.4 ns. After EXTCNTR goes low, the buffer will be centered and data integrity will be lost and subsequently restored within approximately 2 μs.

If the timing drift exceeds ±1600 ps, the data buffer will indicate overflow with a logic-high signal on the OVRFLW pin for a minimum of 6.4 ns. After a time interval of 4.8 ns after OVRFLW goes low, the buffer will be recentered and data integrity will be lost and subsequently restored within approximately 2 μs. During the 11.2 ns between the rising edge of OVRFLW and the recentering of the buffer, data integrity may be lost if the timing drift exceeds ±2000 ps.

If the output clock CK622P/N is not used when in CLKMOD[1:0] = 10 it can be left unconnected to conserve power.

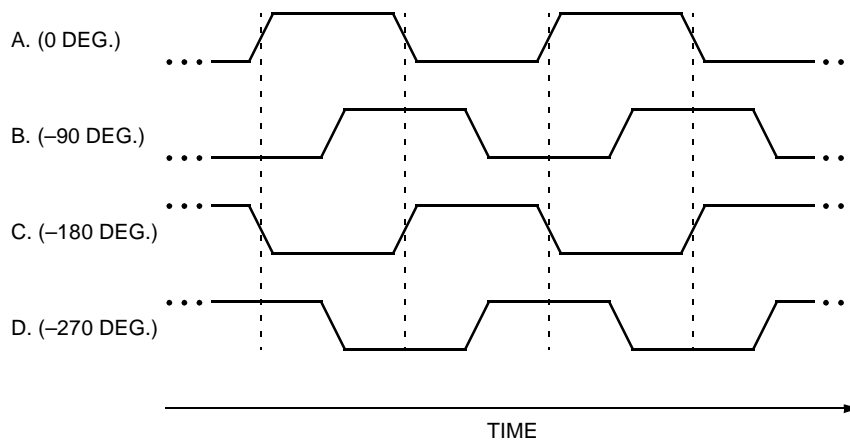## Clocking Modes and Timing Adjustments (continued)

Contradirectional Clocking Mode (CLKMOD[1:0] = 01, PHADJ[1:0], EXTCNTR)

In the contradirectional clocking mode (CLKMOD[1:0] = 01) the TTRN0110G device sends a 622 MHz clock with one of four user-selectable phases out to the upstream device for clocking the data toward the TTRN0110G. The user can program PHADJ[1:0] to adjust the phase of CK622P/N as a function of PWB layout and upstream device propagation delay in order to meet the setup and hold time of the 622 Mbits/s data input to the TTRN0110G. PHADJ[1:0] changes the phase of the CK622P/N clock without changing the input data sampling time. PHADJ[1:0] setting information is given in Table 8, and the phase relationship of CK622P/N for each PHADJ[1:0] setting is shown in Figure 6.

Table 8. PHADJ Settings for CK622 Output Clock (Contraclocking Mode)

Input Pins		Phase
PHADJ[1]	**PHADJ[0]**	
0	0	(See part A of Figure 6.)
1	1	(See part B of Figure 6.)
1	0	(See part C of Figure 6.)
0	1	(See part D of Figure 6.)

In this mode, the TTRN0110G input data still passes though the data buffer described in the forward directional clocking sections, however, there will no longer be any phase drift or overflow since the CK622P/N output serves as the master clock for the upstream device. The read and write addresses for the data buffer are initially reset at the time the PLL acquires lock and the loss of lock indicator transitions from the out-of-lock condition to the in-lock condition. After LCKLOSSN goes high the buffer will be recentered and data integrity will be obtained within approximately 2 μs.

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Figure 6. CK622 Phase Relation vs. PHADJ Setting

Clocking Modes and Timing Adjustments (continued)

Clockless Transfer Mode (CLKMOD[1:0]= 11, EXTCNTR)

In clockless transfer mode (CLKMOD[1:0] = 11), data may be sent to the TTRN0110G device without providing PICLKP/N. An internal delay-locked loop (DLL) automatically produces a 622 MHz clock that is aligned to the parallel data based on the phase of the D0P/N data input. The skew of all data bits D[15:1]P/N relative to D0P/N must be less than 650 ps as shown in Figure 11 on page 25.

An internal data buffer is used to absorb timing drift between D0 and the internal clocks derived from the 10 GHz internal oscillator. A D0 phase drift of up to ±1600 ps relative to the internal clocks can be absorbed by the buffer, as long as the bandwidth of this phase drift is less than 500 kHz. Note that the read and write addresses for the data buffer must be initially reset in order for the buffer to absorb the full range of D[15:0]P/N phase drift.

The read and write addresses for the data buffer are reset at the time the PLL acquires lock and the loss of lock indicator transitions from the out-of-lock condition to the in-lock condition. After LCKLOSSN goes high the buffer will be centered and data integrity will be obtained within approximately 2 μs.

The data buffer can also be recentered by applying EXTCNTR (active high) for a minimum of 6.4 ns. After EXTCNTR goes low the buffer will be centered and data integrity will be lost and subsequently restored within approximately 2 μs.

If the timing drift exceeds ±1600 ps, the data buffer will indicate overflow with a logic-high signal on the OVRFLW pin for a minimum of 6.4 ns. After a time interval of 4.8 ns after OVRFLW goes low the buffer will be recentered and data integrity will be lost and subsequently restored within approximately 2 μs. During the 11.2 ns between the rising edge of OVRFLW and the recentering of the buffer, data integrity may be lost if the timing drift exceeds ±2000 ps.

If the output clock CK622P/N is not used when in CLKMOD[1:0] = 11, it can be left unconnected to conserve power.

Because the clockless data transfer mode uses the transitions on the D0 data bit as a phase reference for clocking the data, a constraint of a maximum number of consecutive zeroes of less than **TBD** data periods is placed on the D0 bit when operating in the clockless data transfer mode.

CML Output Structure (Used on Pins D10GP/N, CK10GP/N, LBDP/N)

The CML architecture is essentially a current-steering mechanism combined with an amplifier. This makes the output swing of the signal a function of the termination resistor and the output current. The on-chip, 50 Ω termination resistor provides a back termination and the output may be direct or ac-coupled to the load. For the direct coupled case, the 50 Ω load should be referenced to the positive 3.3 V supply, V$_{CC}$. This will ensure dc levels that comply with the limits set in Table 16 and Table 17 on page 23. The value for RREFCML is also given in these tables.
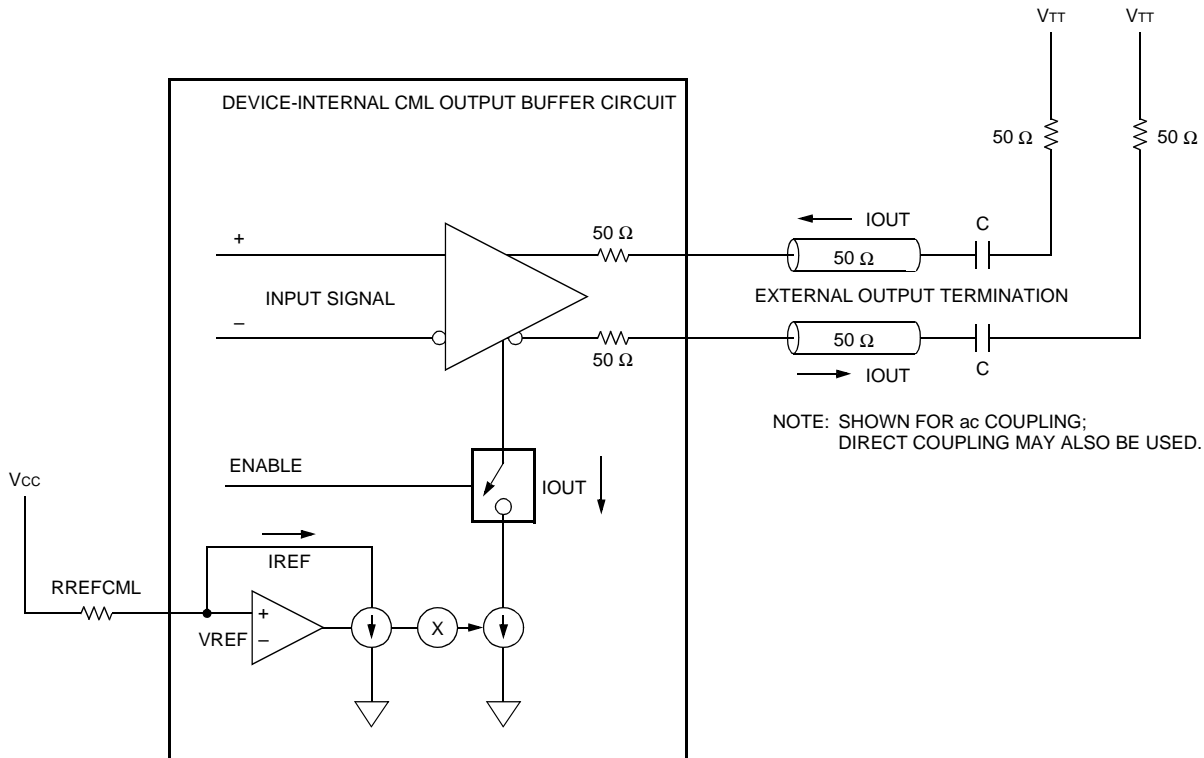
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Figure 7. Typical CML Output Structure

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Min	Max	Unit
Power Supply Voltage (V_{CC})	—	—	V
Storage Temperature	−40	125	°C
Pin Voltage	GND − 0.5	V_{CC} + 0.5	V

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Lucent employs a human-body model (HBM) and charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used in the defined model. No industrywide standard has been adopted for the CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes:

Device	Voltage
TTRN0110G	**TBD**

Operating Conditions

Table 9. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply (dc voltage)	—	3.135	3.3	3.465	V
Ground	—	—	—	—	V

Input Voltage:
    Low
    High
	V_{IL}
	V_{IH}
		See Table 13,
		Table 14.
			See Table 13,
			Table 14.
				See Table 13,
				Table 14.
					V
					V

Temperature: Ambient	—	−40	—	85	°C

Power Dissipation:
    D10G Active, CK10G Disabled,
    LBD Disabled
	P_D	—	1.2	**TBD**	W

Power Dissipation:
    D10G Active, CK10G Active,
    LBD Disabled
	P_D	—	1.7	**TBD**	W

Power Dissipation:
    D10G Active, CK10G Active,
    LBD Active
	P_D	—	1.9	**TBD**	W

Electrical Characteristics

Reference Frequency (REFCLKP/N, REFFREQ) (Standard SONET Rate)

The device requires a 155.52 MHz or a 622.08 MHz differential LVDS reference clock input. Table 10 provides the characteristics of the REFCLKP/N input.

Table 10. Reference Frequency Characteristics (standard SONET)

Parameter	Min	Typ	Max	Unit
Reference Frequency (REFCLKP/N):				
When REFFREQ = 0	—	155.52	—	MHz
When REFFREQ = 1	—	622.08	—	MHz
Reference Frequency Tolerance*	−20	—	20	ppm
Duty Cycle	40	—	60	%
Phase Jitter†	—	—	**TBD**	ps(rms)
Temperature‡	−40	—	85	°C
Supply Voltage‡	3.00	—	3.60	V

* Includes effects of power supply variation, temperature, electrical loading, and aging. The ±20 ppm tolerance is required
  to meet SONET/SDH requirements. For non-SONET/SDH compliant systems, looser tolerances may apply.
† Measured under one 3.3 V LVDS load. Includes frequency components up to 8 MHz.
‡ Specified range is to be compatible with environmental specification of TTRN0110G. Applications requiring a reduced
  temperature range may specify the reference frequency oscillator accordingly.

Reference Frequency (REFCLKP/N, REFFREQ) (FEC Rate)

The device requires a (15/14)155.52 MHz or a (15/14)622.08 MHz differential LVDS reference clock input. Table 11 provides the characteristics of the REFCLKP/N input.

Table 11. Reference Frequency Characteristics (FEC rate)

Parameter	Min	Typ	Max	Unit
Reference Frequency (REFCLKP/N):				
When REFFREQ = 0	—	(15/14)155.52	—	MHz
When REFFREQ = 1	—	(15/14)622.08	—	MHz
Reference Frequency Tolerance*	−20	—	20	ppm
Duty Cycle	40	—	60	%
Phase Jitter†	—	—	**TBD**	ps(rms)
Temperature‡	−40	—	85	°C
Supply Voltage‡	3.00	—	3.60	V

* Includes effects of power supply variation, temperature, electrical loading, and aging. The ±20 ppm tolerance is required
  to meet SONET/SDH requirements. For non-SONET/SDH compliant systems, looser tolerances may apply.
† Measured under one 3.3 V LVDS load. Includes frequency components up to 8 MHz.
‡ Specified range is to be compatible with environmental specification of TTRN0110G. Applications requiring a reduced
  temperature range may specify the reference frequency oscillator accordingly.

Electrical Characteristics (continued)

LVDS, CMOS, CML Output Pins

Notes:
1. For Table 12 through Table 19, VCC = 3.3 V ± 5%, Tambient = –40 °C to +85 °C.

2. For more information on interpreting CML specifications, see the CML Output Structure (Used on Pins D10GP/N, CK10GP/N, LBDP/N) section on page 18.

Table 12. LVDS Output Pin Parametrics

Applicable Pins	Symbol	Parameter	Conditions	Min	Typ	Max	Units
CK622P/N, CK155P/N	Voh	Output Voltage High, Voa or Vob	Rload = 100 Ω ± 1%	—	—	1475	mV
	Vol	Output Voltage Low, Voa or Vob	Rload = 100 Ω ± 1%	925	—	—	mV
	|Vod|	Output Differential Voltage	Rload = 100 Ω ± 1%	250	—	400	mV
	Vos	Output Offset Voltage	Rload = 100 Ω ± 1%	1125	—	1275	mV
	Ro	Differential Output Impedance	Vcm = 1.0 V and 1.4 V	80	100	280	Ω
	ΔRo	Ro Mismatch Between A & B	Vcm = 1.0 V and 1.4 V	—	—	10	%
	|ΔVod|	Change in |Vod| Between Logic 0 and Logic 1	Rload = 100 Ω ± 1%	—	—	25	mV
	|ΔVos|	Change in |Vos| Between Logic 0 and Logic 1	Rload = 100 Ω ± 1%	—	—	25	mV
	Isa, Isb	Output Current	Driver shorted to GND	—	—	24	mA
	Isab	Output Current	Drivers shorted together	—	—	12	mA
	|Ixa|,|Ixb|	Power-Off Output Leakage	—	—	—	TBD	mA
	trised tfalld	Data Vod: Rise Time, 20% to 80% Fall Time, 20% to 80%	Zload = 100 Ω ± 1% Zload = 100 Ω ± 1%	200 200	— —	450 450	ps ps
	trisec tfallc	Clock Vod: Rise Time, 20% to 80% Fall Time, 20% to 80%	Zload = 100 Ω ± 1% Zload = 100 Ω ± 1%	100 100	— —	450 450	ps ps
	tskew1	Differential Skew*	—	—	—	TBD	ps
	tskew2	Channel to Channel*	—	—	—	200	ps

* As defined in the *IEEE*[†] standard 1596.3 -1996.
† *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.

Electrical Characteristics (continued)

LVDS, CMOS, CML Output Pins (continued)

Table 13. LVDS Input Pin Parametrics

Applicable Pins	Symbol	Parameter	Conditions	Min	Typ	Max	Units
D[15:0]P/N, REFCLKP/N PICLKP/N	Vcm	Input Common Mode Voltage Range	Avg(Via,Vib)	0	1200	2400	mV
	Vdiff	Input Peak Differential Voltage	|Via-Vib|	100	—	800	mV
	Vhyst	Threshold Hysteresis*	(+Vid) – (–Vid)	—	—	—	mV
	Rin	Differential Input Impedance†	f = 250 MHz	80	100	120	Ω

* Buffer will not produce output transitions when input is open-circuited.
† Looser than ICORE/IEEE spec of ±10 Ω.

Table 14. CMOS Input Pin Characteristics

Applicable Pins	Symbol	Parameter	Conditions	Min	Max	Unit
RESETN, FECN, PHADJ[1:0], CLKMOD[1:0], REFFREQ, ENCK10G, ENLBDN, ENCK155N, TESTN	VIH	Input Voltage High	—	VCC – 1.0	VCC	V
	VIL	Input Voltage Low	—	GND	1.0	V
	IIH	Input Current High Leakage	VIN = VCC	—	10	μA
	IIL	Input Current Low Leakage	VIN = GND	–225	—	μA
EXTCNTR	VIH	Input Voltage High	—	VCC – 1.0	VCC	V
	VIL	Input Voltage Low	—	GND	1.0	V
	IIH	Input Current High Leakage	VIN = VCC	—	225	μA
	IIL	Input Current Low Leakage	VIN = GND	–10	—	μA

Table 15. CMOS Output Pin Characteristics

Applicable Pins	Symbol	Parameter	Conditions	Min	Max	Unit
LCKLOSSN OVRFLW	VOH	Output Voltage High	IOH = –4.0 mA	VCC – 0.5	VCC	V
	VOL	Output Voltage Low	IOL = 4.0 mA	GND	0.5	V
	CI	Output Load Capacitance	—	—	15	pF

Electrical Characteristics (continued)

LVDS, CMOS, CML Output Pins (continued)

Table 16. CML Output Pin dc Characteristics

Applicable Pins	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
D10GP/N, LBDP/N, CK10GP/N	V_{OL}	Output Voltage Low	$R_L = 50\ \Omega$, Referenced to VCC	$V_{CC} - 1.2$	—	—	V
	V_{OH}	Output Voltage High		—	—	$V_{CC} + 0.3$	V
	V_{AMP}	Voltage Amplitude Single-Ended	RREFCML = **TBD** kΩ	400	500	600	mV

Table 17. CML Output Pin dc Characteristics (High Amplitude Data Swing)

Applicable Pins	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
D10GP/N, LBDP/N	V_{OL}	Output Voltage Low	$R_L = 50\ \Omega$, Referenced to VCC	$V_{CC} - 1.6$	—	—	V
	V_{OH}	Output Voltage High		—	—	$V_{CC} + 0.3$	V
	V_{AMP}	Voltage Amplitude Single-Ended	RREFCML = **TBD** kΩ	600	700	800	mV
CK10GP/N	V_{OL}	Output Voltage Low		$V_{CC} - 1.2$	—	—	V
	V_{OH}	Output Voltage High		—	—	$V_{CC} + 0.3$	V
	V_{AMP}	Voltage Amplitude Single-Ended		400	500	600	mV

Timing Characteristics

Note that all timing diagrams involving differential signals represent the positive signal as a solid line and the negative signal as a dashed line. This is especially important when referencing the rising or falling edge of a differential signal.

Transmit Timing

Figure 8 shows the required timing relationships between the input clock PICLKP/N and the input data D[15:0]P/N in forward directional 622 clocking mode.
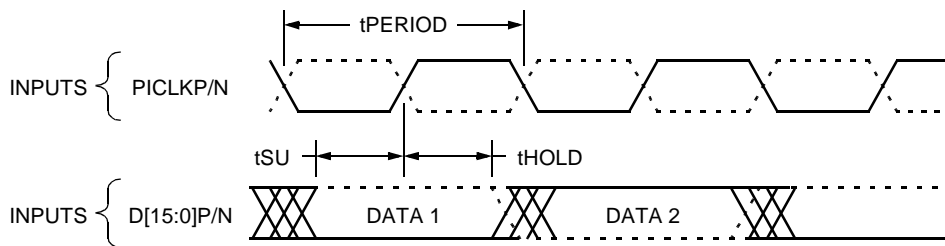

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Figure 8. Transmit Timing Waveforms (Forward Directional 622 Clocking Mode)

Figure 9 shows the timing relationships between the input clock PICLKP/N and the input data D[15:0]P/N in forward directional 311 clocking mode.
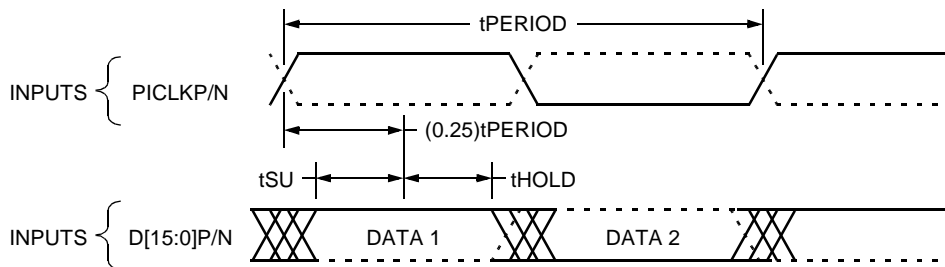
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Figure 9. Transmit Timing Waveform (Forward Directional 311 Clocking Mode)

Timing Characteristics (continued)

Transmit Timing (continued)

Figure 10 shows the timing relationships between the output clock CK622P/N and the input data D[15:0]P/N. This relationship is true for both the contraclocking mode and the clockless transfer mode.
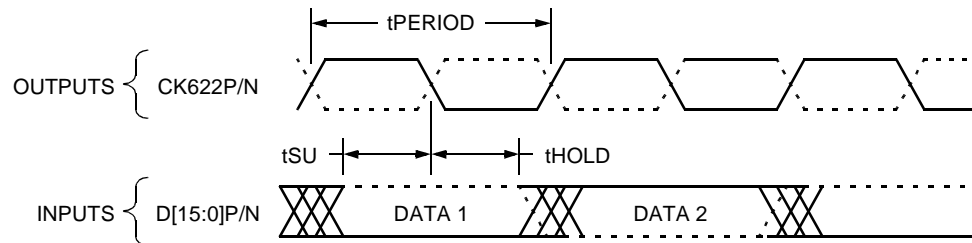
0361(F)r.1

Note: T_{SU} and T_{HOLD} only apply in contraclocking mode when CLKMOD[1:0] = 01.

Figure 10. Transmit Timing Waveform (Contradirectional Clocking Mode)

Figure 11 shows the skew relationship between the D0P/N data remainder of the D[15:1]P/N data bus required to support clockless data transfer.
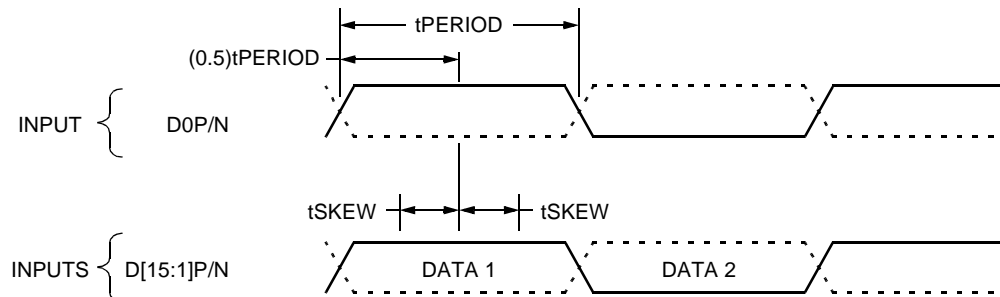
0362(F)r.1

Figure 11. Transmit Timing Waveform (Clockless Transfer Mode)

Timing Characteristics (continued)

Transmit Timing (continued)

The output 622 MHz clock and data signals are specified in Table 18.

Table 18. LVDS Input/Output Pin ac Timing Characteristics

Applicable Pins	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CK622P/N PICLKP/N forward directional 622	—	Duty Cycle	All signals differential	40	50	60	%
	tPERIOD	Clock Period		—	1.6	—	ns
PICLKP/N forward directional 311	—	Duty Cycle	All signals differential	45	50	55	%
	tPERIOD	Clock Period		—	3.2	—	ns
Input Timing							
D[15:0]P/N, CK622P/N PICLKP/N	tSU	Setup from Clock Edge to D[15:0]P/N	CLKMOD = 01, All signals differential	**TBD**	—	—	ns
	tHOLD	Hold from Clock Edge to D[15:0]P/N	CLKMOD = 01, All signals differential	**TBD**	—	—	ns
	tRISE, tFALL	Rise, Fall Times: 20%—80%	All signals differential	**TBD**	**TBD**	**TBD**	ps
	tSKEW	Transition Skew Rise to Fall		**−TBD**	0	**TBD**	ps

Timing Characteristics (continued)

Transmit Timing (continued)

Figure 12 shows the timing relationships between the output 10 GHz clock CK10GP/N and the output 10 Gbits/s data D10GP/N.
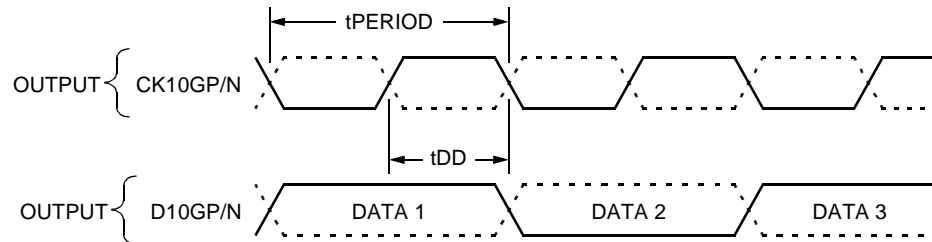
0357(F)r.1

Figure 12. Transmit Timing Waveform with 10 GHz Clock

The output 10 GHz clock and data signals from Figure 12 are characterized in Table 19.

Table 19. CML Output Pin ac Timing Characteristics

Applicable Pins	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CK10GP/N	—	Duty Cycle	RREFCML = TBD kΩ	40	50	60	%
	t_{PERIOD}	CK10GP/N Clock Period		—	100	—	ps
D10GP/N, CK10GP/N	t_{DD}	Time Delay from Clock Edge to Data Edge	R_L = 50 Ω	30	50	70	ps
CK10GP/N D10GP/N, LBDP/N	t_{RISE}, t_{FALL}	Rise, Fall Times: 20%—80%		15	25	35	ps
	t_{SKEW}	Transition Skew Rise to Fall		−20	0	20	ps
	R_{LOSS}	Output Return Loss: 10 GHz < 7 GHz	— —	— —	12 15	— —	dB dB

Outline Diagram

198-Pin BGA

Note: Dimensions are in millimeters. Tolerance is ±0.076 mm unless otherwise noted.
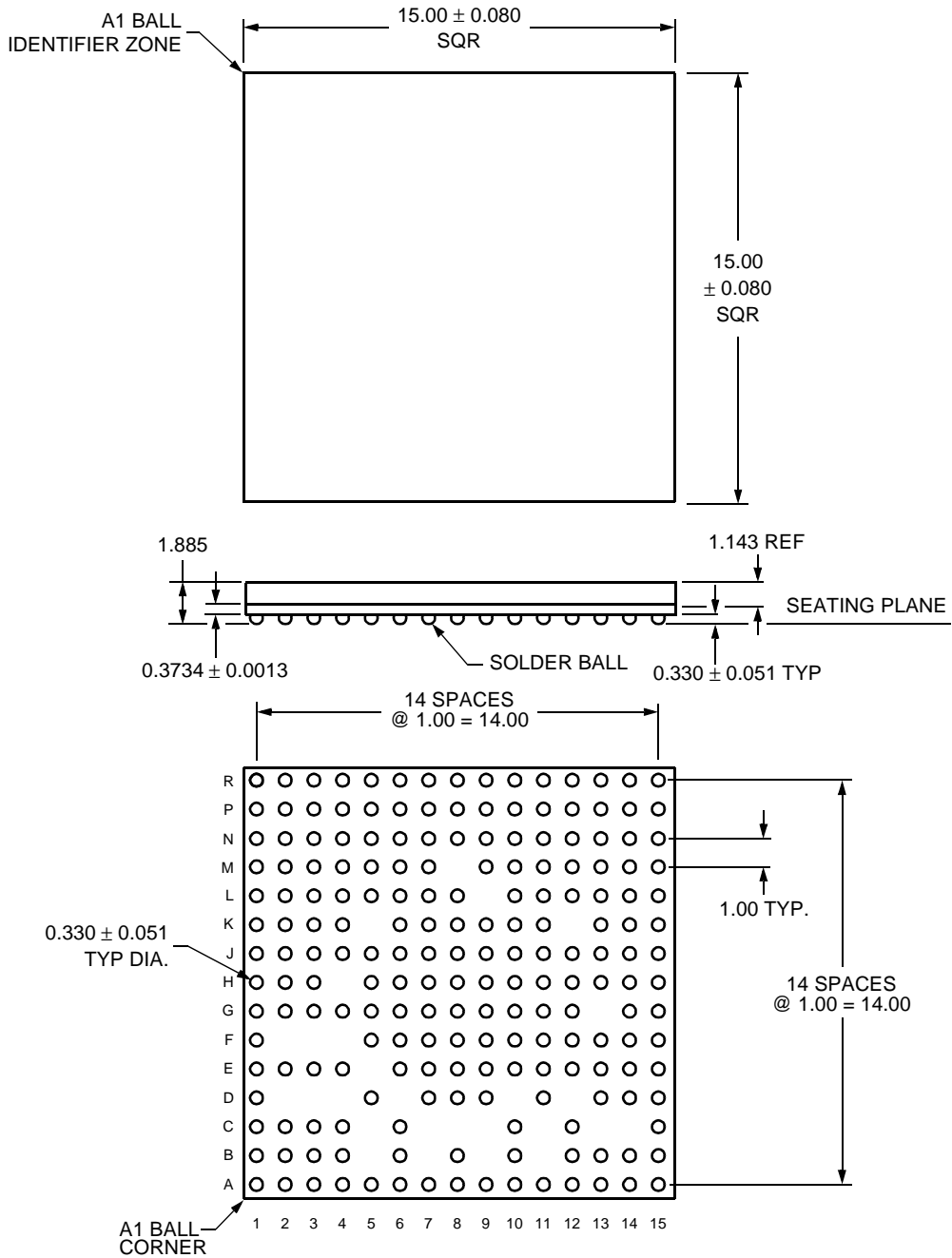
Ordering Information

Device Code	Package	Temperature	Comcode (Ordering Number)
TTRN0110G	198-pin BGA	–40 °C to +85 °C	108698465
—	—	—	—
—	—	—	—

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