

## 5th Generation Hi-Speed USB Flash Media and IrDA Controller with Integrated Card Power FETs

### PRODUCT FEATURES

Datasheet

#### IrDA Controller

- IrDA v1.1 FIR and SIR Compliant Controller, with 9.6K, 19.2K, 38.4K, 57.6K, 115.2K, 0.576Mbps, 1.152Mbps and 4Mbps data rate support.

#### Flash Media Controller

- Complete System Solution for interfacing SmartMedia<sup>TM</sup> (SM) or xD Picture Card<sup>TM</sup> (xD)<sup>1</sup>, Memory Stick<sup>TM</sup> (MS), High Speed Memory Stick (HSMS), Memory Stick PRO (MSPRO), MS Duo<sup>TM</sup>, Secure Digital (SD), High Speed SD, Mini-Secure Digital (Mini-SD), TransFlash (SD), MultiMediaCard<sup>TM</sup> (MMC), Reduced Size MultiMediaCard (RS-MMC), NAND Flash, Compact Flash<sup>TM</sup> (CF) and CF Ultra<sup>TM</sup> I & II, and CF form-factor ATA hard drives to Hi-Speed USB
  - Supports USB Bulk Only Mass Storage Compliant Bootable BIOS
- Support for simultaneous operation of all above devices. (only one at a time of each of the following groups supported: CF or ATA drive, SM or XD or NAND, SD or MMC)
- On-Chip 4-Bit High Speed Memory Stick and MS PRO Hardware Circuitry
- On-Chip firmware reads and writes High Speed Memory Stick and MS PRO
- 1-bit ECC correction performed in hardware for maximum efficiency
- Hardware support for SD Security Command Extensions
- On-chip power FETs with short circuit protection for supplying flash media card power
- USB Bus Power Certified
- 3.3 Volt I/O with 5V input tolerance on VBUS/GPIO3
- Complete USB Specification 2.0 Compatibility for Bus Powered Operation
  - Includes Hi-Speed USB Transceiver
  - A Bi-directional Control and two Bi-directional Bulk Endpoints are provided.
- 8051 8 bit microprocessor
  - Provides low speed control functions
  - 30 Mhz execution speed at 1 clock per instruction cycle average
  - 12K Bytes of internal SRAM for general purpose scratchpad
- 768 Bytes of internal SRAM for general purpose scratchpad or program execution while re-flashing external ROM
- Two, Double Buffered Bulk Endpoints
- Two, Bi-directional 512 Byte Buffers for Bulk Endpoints
- 64 Byte RX Control Endpoint Buffer
- 64 Byte TX Control Endpoint Buffer
- Internal or External Program Memory Interface
  - 76K Byte Internal Code Space or Optional 128K Byte External Code Space using Flash, SRAM or EPROM memory.
- On Board 24Mhz Crystal Driver Circuit
- Can be clocked by 48MHz external source
- On-Chip 1.8V Regulator for Low Power Core Operation
- Internal PLL for 480Mhz Hi-Speed USB Sampling, Configurable MCU clock
- Supports firmware upgrade via USB bus if “boot block” Flash program memory is used
- 12 GPIOs for special function use: LED indicators, button inputs, power control to memory devices, etc.
  - Inputs capable of generating interrupts with either edge sensitivity
- Attribute bit controlled features:
  - Activity LED polarity/operation/blink rate
  - Full or Partial Card compliance checking
  - Bus or Self Powered
  - LUN configuration and assignment
  - Write Protect Polarity
  - SmartDetach<sup>TM</sup> - Detach from USB when no Card Inserted for Notebook apps
  - Cover Switch operation for xD compliance
  - Inquiry Command operation
  - SD Write Protect operation
  - Older CF card support
  - Force USB 1.1 reporting
  - Internal or External Power FET operation
- Compatible with Microsoft WinXP, WinME, Win2K SP3, Apple OS10, Softconnex, and Linux Multi-LUN Mass Storage Class Drivers
- Win2K, Win98/98SE and Apple OS8.6 and OS9 Multi-LUN Mass Storage Class Drivers available from SMSC
- 128 Pin TQFP Package (1.0mm height, 14mmx14mm footprint); green, lead-free package also available

<sup>1</sup>.xD Picture Card not applicable to USB2229.

**ORDER NUMBER(S):****USB2229/USB2230-NE-XX FOR 128 PIN, TQFP PACKAGE; USB2229/USB2230-NU-XX FOR 128 PIN, TQFP PACKAGE (GREEN, LEAD-FREE) PACKAGE**

80 Arkay Drive  
Hauppauge, NY 11788  
(631) 435-6000  
FAX (631) 273-3123

Copyright © 2006 SMSC or its subsidiaries. All rights reserved.

Circuit diagrams and other information relating to SMSC products are included as a means of illustrating typical applications. Consequently, complete information sufficient for construction purposes is not necessarily given. Although the information has been checked and is believed to be accurate, no responsibility is assumed for inaccuracies. SMSC reserves the right to make changes to specifications and product descriptions at any time without notice. Contact your local SMSC sales office to obtain the latest specifications before placing your product order. The provision of this information does not convey to the purchaser of the described semiconductor devices any licenses under any patent rights or other intellectual property rights of SMSC or others. All sales are expressly conditional on your agreement to the terms and conditions of the most recently dated version of SMSC's standard Terms of Sale Agreement dated before the date of your order (the "Terms of Sale Agreement"). The product may contain design defects or errors known as anomalies which may cause the product's functions to deviate from published specifications. Anomaly sheets are available upon request. SMSC products are not designed, intended, authorized or warranted for use in any life support or other application where product failure could cause or contribute to personal injury or severe property damage. Any and all such uses without prior written approval of an Officer of SMSC and further testing and/or modification will be fully at the risk of the customer. Copies of this document or other SMSC literature, as well as the Terms of Sale Agreement, may be obtained by visiting SMSC's website at <http://www.smc.com>. SMSC is a registered trademark of Standard Microsystems Corporation ("SMSC"). Product names and company names are the trademarks of their respective holders.

**SMSC DISCLAIMS AND EXCLUDES ANY AND ALL WARRANTIES, INCLUDING WITHOUT LIMITATION ANY AND ALL IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, TITLE, AND AGAINST INFRINGEMENT AND THE LIKE, AND ANY AND ALL WARRANTIES ARISING FROM ANY COURSE OF DEALING OR USAGE OF TRADE. IN NO EVENT SHALL SMSC BE LIABLE FOR ANY DIRECT, INCIDENTAL, INDIRECT, SPECIAL, PUNITIVE, OR CONSEQUENTIAL DAMAGES; OR FOR LOST DATA, PROFITS, SAVINGS OR REVENUES OF ANY KIND; REGARDLESS OF THE FORM OF ACTION, WHETHER BASED ON CONTRACT; TORT; NEGLIGENCE OF SMSC OR OTHERS; STRICT LIABILITY; BREACH OF WARRANTY; OR OTHERWISE; WHETHER OR NOT ANY REMEDY OF BUYER IS HELD TO HAVE FAILED OF ITS ESSENTIAL PURPOSE, AND WHETHER OR NOT SMSC HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.**

## Table of Contents

<b>Chapter 1</b>	<b>General Description</b> .....	<b>6</b>
<b>Chapter 2</b>	<b>Acronyms</b> .....	<b>7</b>
<b>Chapter 3</b>	<b>Pin Table</b> .....	<b>8</b>
3.1	128-Pin Package .....	8
3.2	128-Pin List Table.....	9
<b>Chapter 4</b>	<b>Block Diagram</b> .....	<b>11</b>
<b>Chapter 5</b>	<b>Pin Configuration</b> .....	<b>12</b>
<b>Chapter 6</b>	<b>Pin Descriptions</b> .....	<b>13</b>
6.1	PIN Descriptions .....	13
6.2	Buffer Type Descriptions .....	20
<b>Chapter 7</b>	<b>DC Parameters</b> .....	<b>22</b>
7.1	Maximum Guaranteed Ratings .....	22
7.2	DC Electrical Characteristics .....	22
7.3	Capacitance .....	25
<b>Chapter 8</b>	<b>Packaging</b> .....	<b>26</b>
<b>Chapter 9</b>	<b>GPIO Usage</b> .....	<b>27</b>

## List of Figures

Figure 5.1	USB2229/USB2230 128-Pin TQFP .....	12
Figure 8.1	USB2229/USB2230 128-Pin TQFP Package Outline .....	26



Datasheet

## List of Tables

Table 3.1	USB2229/USB2230 128-Pin Package	8
Table 3.2	USB2229/USB2230 128-Pin TQFP	9
Table 6.1	USB2229/USB2230 Pin Descriptions	13
Table 6.2	USB2229/USB2230 Buffer Type Descriptions	20
Table 8.1	USB2229/USB2230 128-Pin TQFP Package Parameters	26
Table 9.1	GPIO Usage (ROM Rev 0x00)	27

## Chapter 1 General Description

The USB2229/USB2230 is a Hi-Speed USB IrDA and Bulk Only Mass Storage Class Peripheral Controller. The Bulk Only Mass Storage Class Peripheral Controller supports CompactFlash (CF) in True IDE Mode only, SmartMedia (SM), Memory Stick (MS) including both serial and parallel interface and Secure Digital/MultiMediaCard (SD/MMC) flash memory devices. It provides a single chip solution for the most popular flash memory cards in the market. In addition, the IrDA controller consists of the SMSC IrCC block, which includes a Synchronous Communications Engine (SCE).

The IrCC SCE supports FIR and SIR IrDA. The IrCC offers flexible signal routing and programmable output control through the Raw mode interface, General Purpose Data pins and Output Multiplexer. Chip-level address decoding is required to access the IrCC register set.

The device consists of a USB2.0 PHY and SIE, buffers, Fast 8051 microprocessor with expanded scratchpad, and program SRAM, and IrDA, CF, MS, SM and SD controllers. The SD controller supports both SD and MMC devices.

Provisions for external Flash Memory up to 128K bytes for program storage is provided (note: when Bank switching is enabled the upper 64K will map into the 8051 ROM space, otherwise, only the first 64K bytes is used).

12K bytes of scratchpad SRAM and 768Bytes of program SRAM are also provided.

Twelve GPIO pins are provided for indicators, external serial EEPROM for OEM ID and system configuration information, and other special functions.

Internal power FETs are provided to directly supply power to the xD/SM, MMC/SD and MS/MSPro cards.

The internal ROM program is capable of implementing any combination of single or multi-LUN CF/SD/MMC/SM/MS reader functions with individual card power control and activity indication. SMSC also provides licenses\*\* for Win98 and Win2K drivers and setup utilities. Note: Please check with SMSC for precise features and capabilities for the current ROM code release.

\*Note: In order to develop, make, use, or sell readers and/or other products using or incorporating any of the SMSC devices made the subject of this document or to use related SMSC software programs, technical information and licenses under patent and other intellectual property rights from or through various persons or entities, including without limitation media standard companies, forums, and associations, and other patent holders may be required. These media standard companies, forums, and associations include without limitation the following: Sony Corporation (Memory Stick, Memory Stick Pro); SD3 LLC (Secure Digital); MultiMedia Card Association (MultiMediaCard); the SSFDC Forum (SmartMedia); the Compact Flash Association (Compact Flash); and Fuji Photo Film Co., Ltd., Olympus Optical Co., Ltd., and Toshiba Corporation (xD-Picture Card). SMSC does not make such licenses or technical information available; does not promise or represent that any such licenses or technical information will actually be obtainable from or through the various persons or entities (including the media standard companies, forums, and associations), or with respect to the terms under which they may be made available; and is not responsible for the accuracy or sufficiency of, or otherwise with respect to, any such technical information.

SMSC's obligations (if any) under the Terms of Sale Agreement, or any other agreement with any customer, or otherwise, with respect to infringement, including without limitation any obligations to defend or settle claims, to reimburse for costs, or to pay damages, shall not apply to any of the devices made the subject of this document or any software programs related to any of such devices, or to any combinations involving any of them, with respect to infringement or claimed infringement of any existing or future patents related to solid state disk or other flash memory technology or applications ("Solid State Disk Patents"). By making any purchase of any of the devices made the subject of this document, the customer represents, warrants, and agrees that it has obtained all necessary licenses under then-existing Solid State Disk Patents for the manufacture, use and sale of solid state disk and other flash memory products and that the customer will timely obtain at no cost or expense to SMSC all necessary licenses under Solid State Disk Patents; that the manufacture and testing by or for SMSC of the units of any of the devices made the subject of this document which may be sold to the customer, and any sale by SMSC of such units to the customer, are valid exercises of the customer's rights and licenses under such Solid State Disk Patents; that SMSC shall have no obligation for royalties or otherwise under any Solid State Disk Patents by reason of any such manufacture, use, or sale of such units; and that SMSC shall have no obligation for any costs or expenses related to the customer's obtaining or having obtained rights or licenses under any Solid State Disk Patents.

**SMSC MAKES NO WARRANTIES, EXPRESS, IMPLIED, OR STATUTORY, IN REGARD TO INFRINGEMENT OR OTHER VIOLATION OF INTELLECTUAL PROPERTY RIGHTS. SMSC DISCLAIMS AND EXCLUDES ANY AND ALL WARRANTIES AGAINST INFRINGEMENT AND THE LIKE.**

No license is granted by SMSC expressly, by implication, by estoppel or otherwise, under any patent, trademark, copyright, mask work right, trade secret, or other intellectual property right.

\*\*To obtain this software program the appropriate SMSC Software License Agreement must be executed and in effect. Forms of these Software License Agreements may be obtained by contacting SMSC.

## Chapter 2 Acronyms

- SM:** SmartMedia
- SMC:** SmartMedia Controller
- FM:** Flash Media
- FMC:** Flash Media Controller
- CF:** Compact Flash
- CFC:** CompactFlash Controller
- SD:** Secure Digital
- SDC:** Secure Digital Controller
- MMC:** MultiMediaCard
- MS:** Memory Stick
- MSC:** Memory Stick Controller
- TPC:** Transport Protocol Code.
- ECC:** Error Checking and Correcting
- CRC:** Cyclic Redundancy Checking

## Chapter 3 Pin Table

### 3.1 128-Pin Package

**Table 3.1 USB2229/USB2230 128-Pin Package**

<b>CompactFlashINTERFACE (28 Pins)</b>			
CF_D0	CF_D1	CF_D2	CF_D3
CF_D4	CF_D5	CF_D6	CF_D7
CF_D8	CF_D9	CF_D10	CF_D11
CF_D12	CF_D13	CF_D14	CF_D15
CF_nIOR	CF_nIOW	CF_IRQ	CF_nRESET
CF_IORDY	CF_nCS0	CF_nCS1	CF_SA0
CF_SA1	CF_SA2	CF_nCD1	CF_nCD2
<b>SmartMedia INTERFACE (17 Pins)</b>			
SM_D0	SM_D1	SM_D2	SM_D3
SM_D4	SM_D5	SM_D6	SM_D7
SM_ALE	SM_CLE	SM_nRE	SM_nWE
SM_nWP	SM_nB/R	SM_nCE	SM_nCD
SM_nWPS			
<b>Memory Stick INTERFACE (7 Pins)</b>			
MS_BS	MS_SDIO/MS_D0	MS_SCLK	MS_INS
MS_D1	MS_D2	MS_D3	
<b>SD INTERFACE (7 Pins)</b>			
SD_CMD	SD_CLK	SD_DAT0	SD_DAT1
SD_DAT2	SD_DAT3	SD_nWP	
<b>USB INTERFACE (10 Pins)</b>			
USBDP	USBDM	ATEST	RBIAS
VDD18PLL	VSSPLL	VDDA33	VSSA
XTAL1/CLKIN	XTAL2		



**Table 3.1 USB2229/USB2230 128-Pin Package (continued)**

<b>MEMORY/IO INTERFACE (27 Pins)</b>			
MA0/CLK_SEL0	MA1/CLK_SEL1	MA2/SEL_CLKDRV	MA3/TX_POL
MA4	MA5	MA6	MA7
MA8	MA9	MA10	MA11
MA12	MA13	MA14	MA15
MD0	MD1	MD2	MD3
MD4	MD5	MD6	MD7
nMRD	nMWR	nMCE	
<b>MISC (15 Pins)</b>			
GPIO1	GPIO2	GPIO3	GPIO4
GPIO5	GPIO6/ROMEN/MA16	GPIO7	GPIO8/ CRD_PWR0
GPIO9	GPIO10/ CRD_PWR1	GPIO11/ CRD_PWR2	GPIO12
nTEST0	nTEST1	nRESET	
<b>IrDA (3 PINS)</b>			
IR_TXD/TX	IR_RXD/RX	IR_MODE	
<b>DIGITAL, POWER, GROUND &amp; NC (14 Pins)</b>			
(5)VDD33	(2)VDD18	(7)VSS	
<b>Total 128</b>			

## 3.2 128-Pin List Table

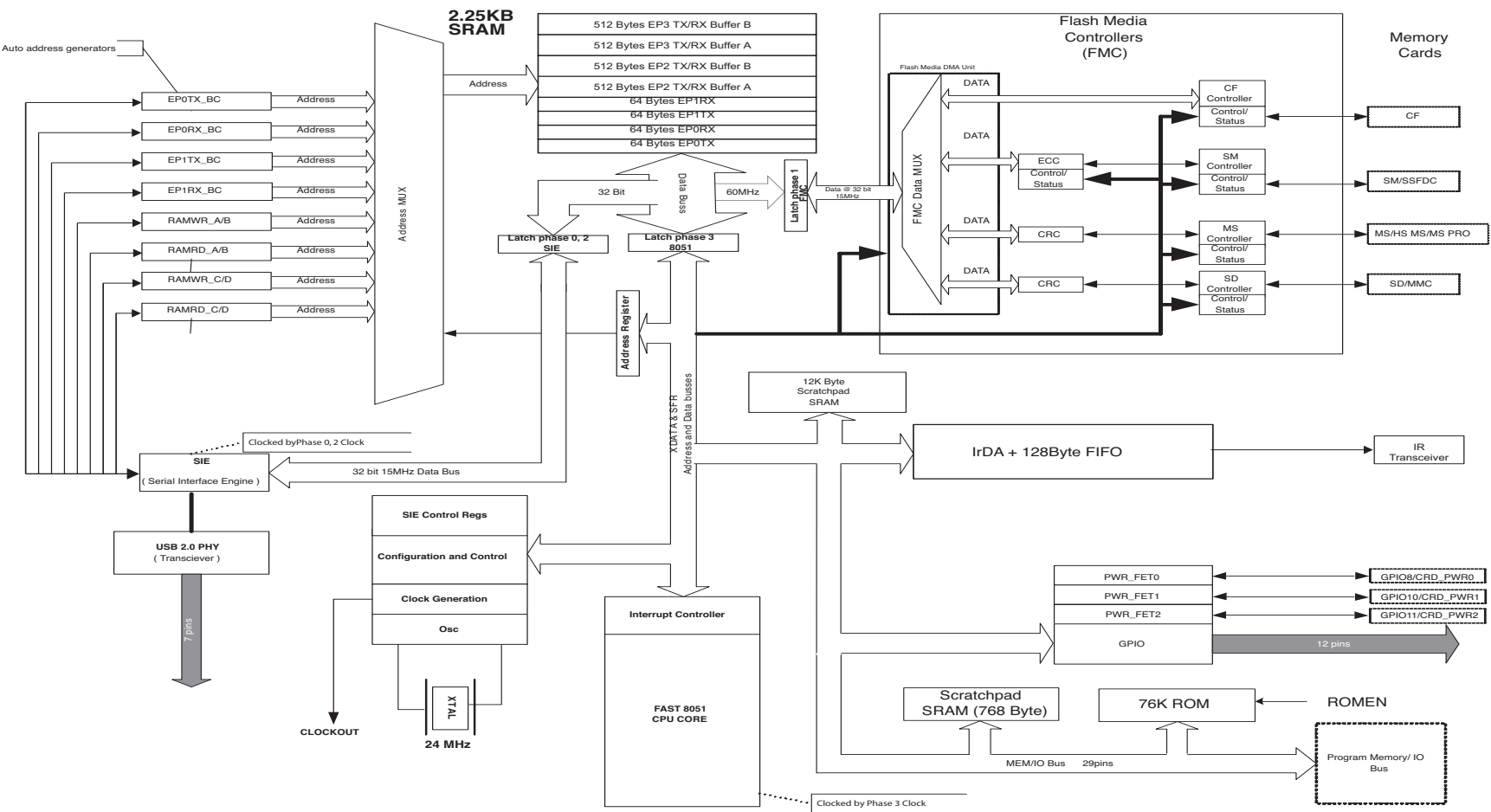
**Table 3.2 USB2229/USB2230 128-Pin TQFP**

PIN #	NAME	MA	PIN #	NAME	MA	PIN #	NAME	MA	PIN #	NAME	MA
1	MA13	8	33	CF_D1	8	65	SM_D0	8	97	VSS	-
2	MA14	8	34	CF_D2	8	66	SM_D1	8	98	RBIAS	-
3	VDD33	-	35	CF_D3	8	67	SM_D2	8	99	ATEST	-
4	MA15	8	36	CF_D4	8	68	SM_D3	8	100	VDD33	-
5	MD0	8	37	CF_D5	8	69	SM_D4	8	101	VDD18PLL	-
6	MD1	8	38	CF_D6	8	70	SM_D5	8	102	XTAL1/ CLKIN	-
7	MD2	8	39	CF_D7	8	71	SM_D6	8	103	XTAL2	-
8	MD3	8	40	CF_D8	8	72	SM_D7	8	104	VSSPLL	-

**Table 3.2 USB2229/USB2230 128-Pin TQFP (continued)**

PIN #	NAME	MA	PIN #	NAME	MA	PIN #	NAME	MA	PIN #	NAME	MA
9	MD4	8	41	CF_D9	8	73	SM_ALE	8	105	GPIO9	8
10	MD5	8	42	GPIO8/ CRD_PWR0	8	74	SM_nWP	8	106	VDD18	-
11	MD6	8	43	VDD33	-	75	SM_CLE	8	107	GPIO7	8
12	MD7	8	44	GPIO11/ CRD_PWR2	8	76	SM_nWPS	-	108	VDD33	-
13	nMRD	8	45	CF_D10	8	77	SM_nB/R	-	109	GPIO6/ ROMEN/ MA16	8
14	nMWR	8	46	CF_D11	8	78	SM_nCD	-	110	GPIO5	8
15	VSS	-	47	VSS	-	79	GPIO10/ CRD_PWR1	8	111	GPIO4	8
16	VSS	-	48	CF_D12	8	80	VDD33	-	112	VSS	-
17	nMCE	8	49	VDD18	-	81	SM_nRE	8	113	nRESET	8
18	MS_INS	-	50	CF_D13	8	82	SM_nWE	8	114	GPIO2	8
19	MS_D0/ MS_SDIO	8	51	CF_D14	8	83	SM_nCE	8	115	GPIO1	-
20	MS_D1	8	52	CF_D15	8	84	VSS	-	116	MA0/ CLK_SEL0	8
21	MS_D2	8	53	CF_nCD1	-	85	VSS	-	117	MA1/ CLK_SEL1	8
22	MS_D3	8	54	CF_nCD2	-	86	VSSA	-	118	MA2/ SEL CLKDRV	8
23	MS_SCLK	8	55	CF_IRQ	8	87	USBDM	-	119	MA3/ TX_POL	8
24	MS_BS	8	56	CF_IORDY	8	88	USBDP	-	120	MA4	8
25	SD_nWP	-	57	CF_nIOR	8	89	VDDA33	-	121	MA5	8
26	SD_DAT0	8	58	CF_nIOW	8	90	IR_MODE	8	122	MA6	8
27	SD_DAT1	8	59	CF_nRESET	8	91	IR_RXD/RX	8	123	MA7	8
28	SD_DAT2	8	60	CF_nCS0	8	92	IR_TXD/TX	8	124	MA8	8
29	SD_DAT3	8	61	CF_nCS1	8	93	GPIO12	8	125	MA9	8
30	SD_CMD	8	62	CF_SA0	8	94	GPIO3	8	126	MA10	8
31	SD_CLK	-	63	CF_SA1	8	95	nTEST1	-	127	MA11	8
32	CF_D0	8	64	CF_SA2	-	96	nTEST0	-	128	MA12	8

# Chapter 4 Block Diagram



# Chapter 5 Pin Configuration

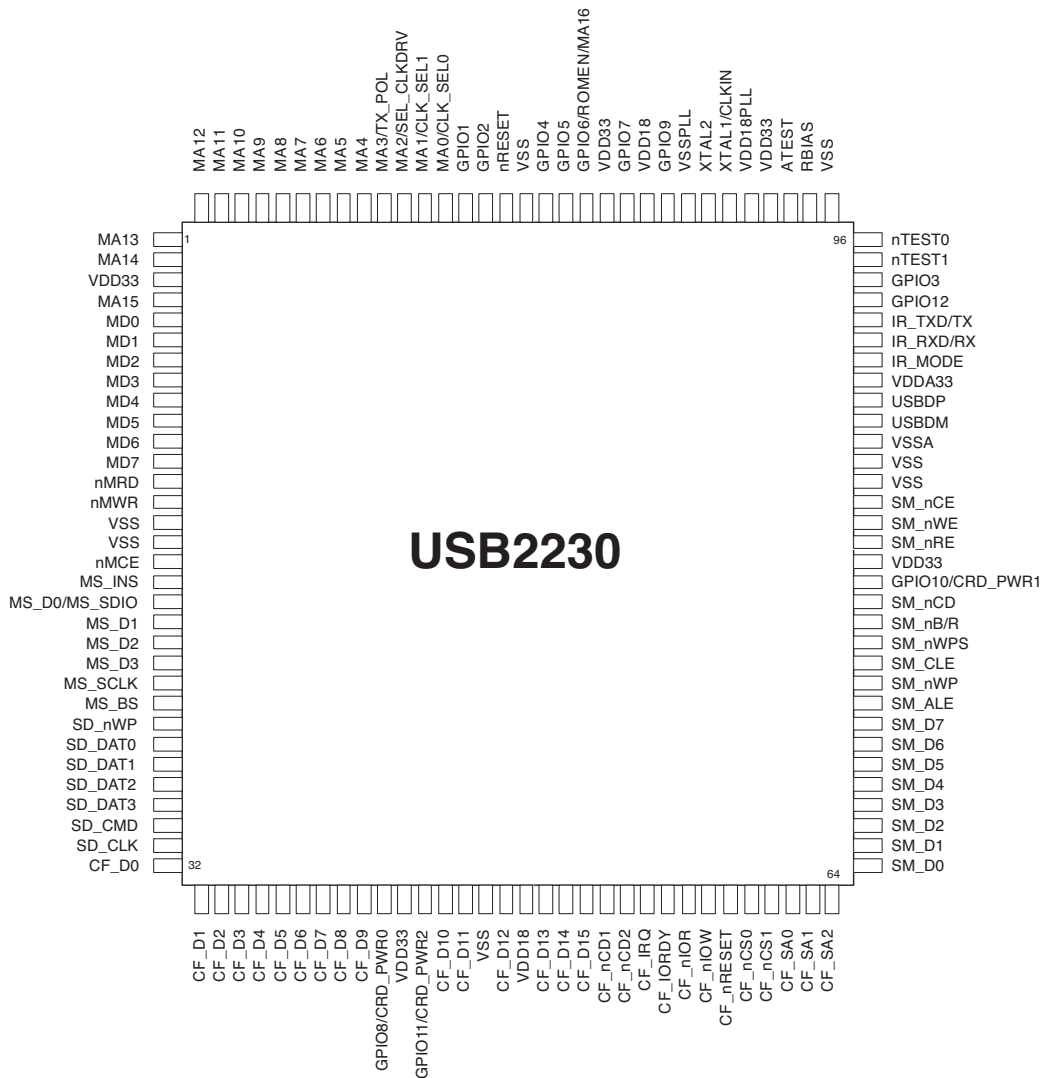


Figure 5.1 USB2229/USB2230 128-Pin TQFP

## Chapter 6 Pin Descriptions

This section provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface.

The “n” symbol in the signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When “n” is not present before the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of “active low” and “active high” signal. The term assert, or assertion indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation indicates that a signal is inactive.

### 6.1 PIN Descriptions

**Table 6.1 USB2229/USB2230 Pin Descriptions**

NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
<b>CompactFlash (In True IDE mode) INTERFACE</b>			
CF Chip Select 1	CF_nCS1	O8PU	This pin is the active low chip select 1 signal for the CF ATA device
CF Chip Select 0	CF_nCS0	O8PU	This pin is the active low chip select 0 signal for the task file registers of CF ATA device in the True IDE mode.
CF Register Address 2	CF_SA2	O8	This pin is the register select address bit 2 for the CF ATA device.
CF Register Address 1	CF_SA1	O8	This pin is the register select address bit 1 for the CF ATA device
CF Register Address 0	CF_SA0	O8	This pin is the register select address bit 0 for the CF ATA device.
CF Interrupt	CF_IRQ	IPD	This is the active high interrupt request signal from the CF device.
CF Data 15-8	CF_D[15:8]	I/O8PD	The bi-directional data signals CF_D15-CF_D8 in True IDE mode data transfer.  In the True IDE Mode, all of task file register operation occur on the CF_D[7:0], while the data transfer is on CF_D[15:0].  The bi-directional data signal has an internal weak pull-down resistor.
CF Data7-0	CF_D[7:0]	I/O8PD	The bi-directional data signals CF_D7-CF_D0 in the True IDE mode data transfer. In the True IDE Mode, all of task file register operation occur on the CF_D[7:0], while the data transfer is on CF_D[15:0].  The bi-directional data signal has an internal weak pull-down resistor.
IO Ready	CF_IORDY	IPU	This pin is active high input signal.  This pin has an internally controlled weak pull-up resistor.

**Table 6.1 USB2229/USB2230 Pin Descriptions**

NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
CF Card Detection2	CF_nCD2	IPU	This card detection pin is connected to the ground on the CF device, when the CF device is inserted.  This pin has an internally controlled weak pull-up resistor.
CF Card Detection1	CF_nCD1	IPU	This card detection pin is connected to ground on the CF device, when the CF device is inserted.  This pin has an internally controlled weak pull-up resistor.
CF Hardware Reset	CF_nRESET	O8	This pin is an active low hardware reset signal to CF device.
CF IO Read	CF_nIOR	O8	This pin is an active low read strobe signal for CF device.
CF IO Write Strobe	CF_nIOW	O8	This pin is an active low write strobe signal for CF device.
<b>SmartMedia INTERFACE</b>			
SM Write Protect	SM_nWP	O8PD	This pin is an active low write protect signal for the SM device.  This pin has a weak pull-down resistor that is permanently enabled
SM Address Strobe	SM_ALE	O8PD	This pin is an active high Address Latch Enable signal for the SM device.  This pin has a weak pull-down resistor that is permanently enabled
SM Command Strobe	SM_CLE	O8PD	This pin is an active high Command Latch Enable signal for the SM device.  This pin has a weak pull-down resistor that is permanently enabled
SM Data7-0	SM_D[7:0]	I/O8PD	These pins are the bi-directional data signal SM_D7-SM_D0.  The bi-directional data signal has an internal weak pull-down resistor.
SM Read Enable	SM_nRE	O8PU	This pin is an active low read strobe signal for SM device.  When using the internal FET, this pin has an internal weak pull-up resistor that is tied to the output of the internal Power FET.
		O8	If an external FET is used (Internal FET is disabled), then the internal pull-up is not available (external pull-ups must be used, and should be connected to the applicable Card Power Supply).

**Table 6.1 USB2229/USB2230 Pin Descriptions**

<b>NAME</b>	<b>SYMBOL</b>	<b>BUFFER TYPE</b>	<b>DESCRIPTION</b>
SM Write Enable	SM_nWE	O8PU	This pin is an active low write strobe signal for SM device.  When using the internal FET, this pin has an internal weak pull-up resistor that is tied to the output of the internal Power FET.
		O8	If an external FET is used (Internal FET is disabled), then the internal pull-up is not available (external pull-ups must be used, and should be connected to the applicable Card Power Supply).
SM Write Protect Switch	SM_nWPS	IPU	A write-protect seal is detected, when this pin is low.  This pin has an internally controlled weak pull-up resistor.
SM Busy or Data Ready	SM_nB/R	I	This pin is connected to the BSY/RDY pin of the SM device.  An external pull-up resistor is required on this signal. The pull-up resistor must be pulled up to the same power source that powers the SM/NAND flash device.
SM Chip Enable	SM_nCE	O8PU	This pin is the active low chip enable signal to the SM device.  When using the internal FET, this pin has an internal weak pull-up resistor that is tied to the output of the internal Power FET.
		O8	If an external FET is used (Internal FET is disabled), then the internal pull-up is not available (external pull-ups must be used, and should be connected to the applicable Card Power Supply).
SM Card Detection	SM_nCD	IPU	This is the card detection signal from SM device to indicate if the device is inserted.  This pin has an internally controlled weak pull-up resistor.
<b>MEMORY STICK INTERFACE</b>			
MS Bus State	MS_BS	O8	This pin is connected to the BS pin of the MS device.  It is used to control the Bus States 0, 1, 2 and 3 (BS0, BS1, BS2 and BS3) of the MS device.
MS System Data In/Out	MS_SDIO/MS_D0	I/O8PD	This pin is a bi-directional data signal for the MS device.  Most significant bit (MSB) of each byte is transmitted first by either MSC or MS device.  The bi-directional data signal has an internal weak pull-down resistor.
MS System Data In/Out	MS_D[3:1]	I/O8PD	This pin is a bi-directional data signal for the MS device.  The bi-directional data signals have internal weak pull-down resistors.

**Table 6.1 USB2229/USB2230 Pin Descriptions**

NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
MS Card Insertion	MS_INS	IPU	This pin is the card detection signal from the MS device to indicate, if the device is inserted.  This pin has an internally controlled weak pull-up resistor.
MS System CLK	MS_SCLK	O8	This pin is an output clock signal to the MS device.  The clock frequency is software configurable.
<b>SD INTERFACE</b>			
SD Data3-0	SD_DAT[3:0]	I/O8PU	These are bi-directional data signals.  These pins have internally controlled weak pull-up resistors.
SD Clock	SD_CLK	O8	This is an output clock signal to SD/MMC device.  The clock frequency is software configurable.
SD Command	SD_CMD	I/O8PU	This is a bi-directional signal that connects to the CMD signal of SD/MMC device.  This pin has an internally controlled weak pull-up resistor.
SD Write Protected	SD_nWP	IPD	This pin is an input signal with an internal weak pull-down.  This pin has an internally controlled weak pull-down resistor.
<b>USB INTERFACE</b>			
USB Bus Data	USBDM USBDP	IO-U	These pins connect to the USB bus data signals.
USB Transceiver Bias	RBIAS	I	A 12.0k $\Omega$ , $\pm$ 1.0% resistor is attached from VSSA to this pin, in order to set the transceiver's internal bias currents.
Analog Test	ATEST	AIO	This signal is used for testing the analog section of the chip and should be connected to VDDA33 for normal operation.
1.8v PLL Power	VDD18PLL		1.8v Power for the PLL
PLL Ground Reference	VSSPLL		Ground Reference for 1.8v PLL power
3.3v Analog Power	VDDA33		3.3v Analog Power
Analog Ground Reference	VSSA		Analog Ground Reference for 3.3v Analog Power.
Crystal Input/External Clock Input	XTAL1/ CLKIN	ICLKx	24Mhz Crystal or external 24/48 MHz clock input. This pin can be connected to one terminal of the crystal or can be connected to an external 24/48Mhz clock when a crystal is not used.  <b>Note:</b> The 'MA[2:0] pins will be sampled while nRESET is asserted, and the value will be latched upon nRESET negation. This will determine the clock source and value.



Table 6.1 USB2229/USB2230 Pin Descriptions

NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
Crystal Output	XTAL2	OCLKx	24Mhz Crystal This is the other terminal of the crystal, or left open when an external clock source is used to drive XTAL1/CLKIN. It may not be used to drive any external circuitry other than the crystal circuit.
<b>MEMORY/IO INTERFACE</b>			
Memory Data Bus	MD[7:0]	IO8	When ROMEN bit of GPIO_IN1 register = 0, these signals are used to transfer data between the internal CPU and the external program memory.  These pins have internally controlled weak pull-up resistors.
Memory Address Bus	MA[15:3]	O8	These signals address memory locations within the external memory.
Memory Address Bus	MA3/ TX_POL	I/O8PU	MA3 Addresses memory locations within the external memory.
			During nRESET assertion, TX_POL will select the operating polarity of the IR LED (active high or active low) and the weak pull-up resistor will be enabled. When nRESET is negated, the value on this pin will be internally latched and this pin will revert to MA3 functionality, the internal pull-up will be disabled.
Memory Address Bus	MA2/ SEL_CLKDRV	I/O8PD	MA2 Addresses memory locations within the external memory.
			SEL_CLKDRV. During nRESET assertion, this pins will select the operating clock mode (crystal or externally driven clock source), and a weak pull-down resistor is enabled. When nRESET is negated, the value will be internally latched and this pin will revert to MA2 functionality, the internal pull-down will be disabled.  '0' = Crystal operation (24MHz only) '1' = Externally driven clock source (24MHz or 48MHz) <b>Note:</b> If the latched value is '1', then the MA2 pin is tri-stated when the following conditions are true: <ol style="list-style-type: none"><li>1. IDLE bit (PCON.0) is 1.</li><li>2. INT2 is negated</li><li>3. SLEEP bit of CLOCK_SEL is 1.</li></ol> If the latched value is '0', then the MA2 pin will function identically to the MA[15:3] pins at all times (other than during nRESET assertion).

**Table 6.1 USB2229/USB2230 Pin Descriptions**

NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
Memory Address Bus	MA[1:0]/CLK_SEL[1:0]	I/O8PD	MA[1:0]. These signals address memory locations within the external memory.
			SEL[1:0]. During nRESET assertion, these pins will select the operating frequency of the external clock, and the corresponding weak pull-down resistors are enabled. When nRESET is negated, the value on these pins will be internal latched and these pins will revert to MA[1:0] functionality, the internal pull-downs will be disabled.  SEL[1:0] = '00'. 24MHz SEL[1:0] = '01'. RESERVED SEL[1:0] = '10'. RESERVED SEL[1:0] = '11'. 48MHz  <b>Note:</b> If the latched value is '1', then the corresponding MA pin is tri-stated when the following conditions are true: <ol style="list-style-type: none"> <li>1. IDLE bit (PCON.0) is 1.</li> <li>2. INT2 is negated</li> <li>3. SLEEP bit of CLOCK_SEL is 1.</li> </ol> If the latched value is '0', then the corresponding MA pin will function identically to the MA[15:3] pins at all times (other than during nRESET assertion).
Memory Write Strobe	nMWR	O8	Program Memory Write; active low
Memory Read Strobe	nMRD	O8	Program Memory Read; active low
Memory Chip Enable	nMCE	O8	Program Memory Chip Enable; active low.  This signal is asserted, when any of the following conditions are no longer met: <ol style="list-style-type: none"> <li>1. IDLE bit (PCON.0) is 1.</li> <li>2. INT2 is negated</li> <li>3. SLEEP bit of CLOCK_SEL is 1.</li> </ol> <b>Note:</b> This signal is held to a logic 'high' while nRESET is asserted.
<b>MISC</b>			
General Purpose I/O	GPIO1	I/O8	This pin may be used either as input, edge sensitive interrupt input, or output.
General Purpose I/O	GPIO2	I/O8	This pin may be used either as input, edge sensitive interrupt input, or output.
General Purpose I/O	GPIO3	I/O8	This pin may be used either as input, edge sensitive interrupt input, or output.
General Purpose I/O	GPIO4	I/O8	This pin may be used either as input, edge sensitive interrupt input, or output.
General Purpose I/O	GPIO5	I/O8	This pin may be used either as input, edge sensitive interrupt input, or output.

**Table 6.1 USB2229/USB2230 Pin Descriptions**

NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
GPIO6, ROMEN, Memory Address 16	GPIO6/ROMEN /MA16	I/P	<p>This pin has an internal weak pull-up resistor that is enabled or disabled by the state of nRESET. The pull-up is enabled when nRESET is active. The pull-up is disabled, when the nRESET is inactive (some clock cycles later, after the rising edge of nRESET).</p> <p>The state of this pin is latched internally on the rising edge of nRESET to determine if internal or external program memory is used. The state latched is stored in ROMEN bit of GPIO_IN1 register.</p>
		I/O8	<p>After the rising edge of nRESET, this pin may be used as GPIO6 or RXD.</p> <p>When pulled low via an external weak pull-down resistor, an external program memory should be connected to the memory data bus. The USB2229/USB2230 uses this external bus for program execution.</p> <p>When this pin is left unconnected or pulled high by a weak pull-up resistor, the USB2229/USB2230 uses the internal ROM for program execution.</p>
		I/O8	For Bank Switching support, MA16 addresses the external 128k memory above the standard 64k range (the upper 64k is mapped into the 64k addressable ROM space)
General Purpose I/O	GPIO7	I/O8	This pin may be used either as input, edge sensitive interrupt input, or output.
General Purpose I/O Or Card Power	GPIO8/ CRD_PWR0	I/O8	GPIO: This pin may be used either as input, edge sensitive interrupt input, or output.
			CRD_PWR: Card Power drive of 3.3V @ 100mA.
General Purpose I/O	GPIO9	I/O8	This pin may be used either as input, edge sensitive interrupt input, or output.
General Purpose I/O Or Card Power	GPIO10/ CRD_PWR1	I/O8	GPIO: This pin may be used either as input, edge sensitive interrupt input, or output.
			CRD_PWR: Card Power drive of 3.3V @ 100mA.
General Purpose I/O Or Card Power	GPIO11/ CRD_PWR2	I/O8	GPIO: This pin may be used either as input, edge sensitive interrupt input, or output.
			CRD_PWR: Card Power drive of 3.3V @ 200mA.
General Purpose I/O	GPIO12	I/O8	These pins may be used either as input, or output.
RESET input	nRESET	IS	This active low signal is used by the system to reset the chip. The active low pulse should be at least 1 $\mu$ s wide.
TEST Input	nTEST[1:0]	I	These signals are used for testing the chip. User should normally tie them high externally, if the test function is not used.

**Table 6.1 USB2229/USB2230 Pin Descriptions**

NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
<b>IrDA</b>			
IR MODE	IR_MODE	O8	IR_MODE, declares the operating speed of the IR link.
IR Receive Data or UART RX	IR_RXD/RX	I	IR_RXD, can be used as IR receiver or as the UART RX line.
IR Transmit Data or UART TX	IR_TXD/TX	O8	IR_TXD, can be used as IR transmitter or as the UART TX line.
<b>DIGITAL POWER, GROUNDS, and NO CONNECTS</b>			
1.8v Digital Core Power	VDD18		+1.8V Core power All VDD18 pins must be connected together on the circuit board.
3.3v Power & Voltage Regulator Input	VDD33		3.3V Power & Regulator Input. Pins 100 & 108 supply 3.3V power to the internal 1.8V regulators.
Ground	VSS		Ground Reference

**Notes:**

- Hot-insertion capable card connectors are required for all flash media. It is required for SD connector to have Write Protect switch. This allows the chip to detect MMC card.
- nMCE is normally asserted except when the 8051 is in standby mode.

## 6.2 Buffer Type Descriptions

**Table 6.2 USB2229/USB2230 Buffer Type Descriptions**

BUFFER	DESCRIPTION
I	Input
IPU	Input with internal weak pull-up resistor.
IPD	Input with internal weak pull-down resistor.
IS	Input with Schmitt trigger
I/O8	Input/Output buffer with 8mA sink and 8mA source.
I/O8PU	Input/Output buffer with 8mA sink and 8mA source, with an internal weak pull-up resistor.
I/O8PD	Input/Output buffer with 8mA sink and 8mA source, with an internal weak pull-down resistor.
O8	Output buffer with 8mA sink and 8mA source.
O8PU	Output buffer with 8mA sink and 8mA source, with an internal weak pull-up resistor.
O8PD	Output buffer with 8mA sink and 8mA source, with an internal weak pull-down resistor.
ICLKx	XTAL clock input

**Datasheet****Table 6.2 USB2229/USB2230 Buffer Type Descriptions (continued)**

<b>BUFFER</b>	<b>DESCRIPTION</b>
OCLKx	XTAL clock output
I/O-U	Analog Input/Output Defined in USB specification
AIO	Analog Input/Output

## Chapter 7 DC Parameters

### 7.1 Maximum Guaranteed Ratings

Operating Temperature Range .....	0°C to +70°C
Storage Temperature Range.....	-55° to +150°C
Lead Temperature Range (soldering, 10 seconds).....	+325°C
Positive Voltage on GPIO3, with respect to Ground.....	5.5V
Positive Voltage on any signal pin, with respect to Ground .....	4.6V
Positive Voltage on XTAL1, with respect to Ground .....	4.0V
Positive Voltage on XTAL2, with respect to Ground .....	2.5V
Negative Voltage on GPIO8, 10 & 11, with respect to Ground (see <a href="#">Note 7.2</a> ).....	-0.5V
Negative Voltage on any pin, with respect to Ground .....	-0.5V
Maximum $V_{DD18}$ , $V_{DD18PLL}$ .....	+2.5V
Maximum $V_{DD33}$ , $V_{DDA33}$ .....	+4.6V

\*Stresses above the specified parameters could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

**Note 7.1** When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. When this possibility exists, it is suggested that a clamp circuit be used.

**Note 7.2** When internal power FET operation of these pins is enabled, these pins may be simultaneously shorted to ground or any voltage up to 3.63V indefinitely, without damage to the device as long as  $V_{DD33}$  and  $V_{DDA33}$  are less than 3.63V and  $T_A$  is less than 70°C.

### 7.2 DC Electrical Characteristics

( $T_A = 0^\circ\text{C} - 70^\circ\text{C}$ ,  $V_{DD33}$ ,  $V_{DDA33} = +3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{DD18}$ ,  $V_{DD18PLL} = +1.8\text{ V} \pm 10\%$ .)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
<b>I,I<sub>PU</sub> &amp; IPD Type Input Buffer</b>						
Low Input Level	$V_{ILI}$			0.8	V	TTL Levels
High Input Level	$V_{IHI}$	2.0			V	
Pull Down	PD		72		$\mu\text{A}$	
Pull Up	PU		58		$\mu\text{A}$	

## Datasheet

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
<b>IS Type Input Buffer</b>						
Low Input Level	$V_{ILI}$			0.8	V	TTL Levels
High Input Level	$V_{IHI}$	2.0			V	
Hysteresis	$V_{HYSI}$		500		mV	
<b>ICLK Input Buffer</b>						
Low Input Level	$V_{ILCK}$			0.4	V	
High Input Level	$V_{IHCK}$	2.2			V	
<b>Input Leakage (All I and IS buffers)</b>						
Low Input Leakage	$I_{IL}$	-10		+10	$\mu$ A	$V_{IN} = 0$
High Input Leakage	$I_{IH}$	-10		+10	mA	$V_{IN} = V_{DD33}$
<b>O8, O8PU &amp; O8PD Type Buffer</b>						
Low Output Level	$V_{OL}$			0.4	V	$I_{OL} = 8 \text{ mA @ } V_{DD33} = 3.3\text{V}$
High Output Level	$V_{OH}$	$V_{DD33} - 0.4$			V	$I_{OH} = -8\text{mA @ } V_{DD33} = 3.3\text{V}$
Output Leakage	$I_{OL}$	-10		+10	$\mu$ A	$V_{IN} = 0 \text{ to } V_{DD33}$ (Note 7.3)
Pull Down	PD		72		$\mu$ A	
Pull Up	PU		58		$\mu$ A	
<b>I/O8, I/O8PU &amp; I/O8PD Type Buffer</b>						
Low Output Level	$V_{OL}$			0.4	V	$I_{OL} = 8 \text{ mA @ } V_{DD33} = 3.3\text{V}$
High Output Level	$V_{OH}$	$V_{DD33} - 0.4$			V	$I_{OH} = -8 \text{ mA @ } V_{DD33} = 3.3\text{V}$
Output Leakage	$I_{OL}$	-10		+10	$\mu$ A	$V_{IN} = 0 \text{ to } V_{DD33}$ (Note 7.3)
Pull Down	PD		72		$\mu$ A	
Pull Up	PU		58		$\mu$ A	

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
<b>IO-U</b> (Note 7.4)						
<b>Integrated Power FET for GPIO8 &amp; GPIO10</b>						
Output Current	$I_{OUT}$	100			mA	GPIO8 or 10; $V_{dropFET} = 0.23V$
Short Circuit Current Limit	$I_{SC}$			140	mA	GPIO8 or 10; $V_{outFET} = 0V$
On Resistance	$R_{DSON}$			2.1	$\Omega$	GPIO8 or 10; $I_{FET} = 70mA$
Output Voltage Rise Time	$t_{DSON}$			800	$\mu s$	GPIO8 or 10; $C_{LOAD} = 10\mu F$
<b>Integrated Power FET for GPIO11)</b>						
Output Current	$I_{OUT}$	200			mA	GPIO11; $V_{dropFET} = 0.46V$
Short Circuit Current Limit	$I_{SC}$			181	mA	GPIO11; $V_{outFET} = 0V$
On Resistance	$R_{DSON}$			2.1	$\Omega$	GPIO11; $I_{FET} = 70mA$
Output Voltage Rise Time	$t_{DSON}$			800	$\mu s$	GPIO11; $C_{LOAD} = 10\mu F$
Supply Current Unconfigured	$I_{CCINIT}$		45	60	mA	@ $V_{DD18}, V_{DD18PLL} = 1.8V$
			10	20	mA	@ $V_{DD33}, V_{DDA33} = 3.3V$
Supply Current Active (Full Speed)	$I_{CC}$		35	60	mA	@ $V_{DD18}, V_{DD18PLL} = 1.8V$
			15	30	mA	@ $V_{DD33}, V_{DDA33} = 3.3V$
Supply Current Active (High Speed)	$I_{CC}$		45	70	mA	@ $V_{DD18}, V_{DD18PLL} = 1.8V$
			15	30	mA	@ $V_{DD33}, V_{DDA33} = 3.3V$
Supply Current Standby	$I_{CSBY}$		160	180	$\mu A$	@ $V_{DD18}, V_{DD18PLL} = 1.8V$
			215	240	$\mu A$	@ $V_{DD33}, V_{DDA33} = 3.3V$

**Note 7.3** Output leakage is measured with the current pins in high impedance.

**Note 7.4** See Appendix A for USB DC electrical characteristics.

**Note 7.5** The Maximum power dissipation parameters of the package should not be exceeded



**Datasheet**

**Note 7.6** The assignment of each Integrated Card Power FET to a designated Card Connector is controlled by both firmware and the specific board implementation. Firmware will default to the settings listed in [Table 9.1, "GPIO Usage \(ROM Rev 0x00\),"](#) on page 27

## 7.3 Capacitance

$T_A = 25^\circ\text{C}$ ;  $f_c = 1\text{MHz}$ ;  $V_{DD18}, V_{DD18PLL} = 1.8\text{V}$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN	TYP	MAX		
Clock Input Capacitance	$C_{IN}$			20	pF	All pins except USB pins (and pins under test tied to AC ground)
Input Capacitance	$C_{IN}$			10	pF	
Output Capacitance	$C_{OUT}$			20	pF	

# Chapter 8 Packaging

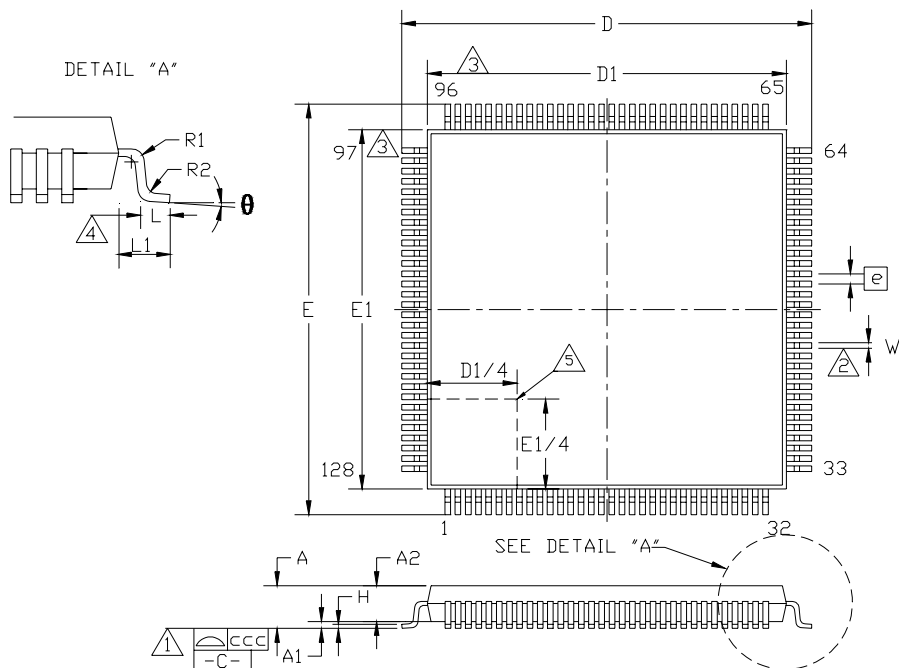


Figure 8.1 USB2229/USB2230 128-Pin TQFP Package Outline

Table 8.1 USB2229/USB2230 128-Pin TQFP Package Parameters

	MIN	NOMINAL	MAX	REMARKS
A	~	~	1.20	Overall Package Height
A1	0.05	~	0.15	Standoff
A2	0.95	~	1.05	Body Thickness
D	15.80	~	16.20	X Span
D1	13.80	~	14.20	X body Size
E	15.80	~	16.20	Y Span
E1	13.80	~	14.20	Y body Size
H	0.09	~	0.20	Lead Frame Thickness
L	0.45	0.60	0.75	Lead Foot Length
L1	~	1.00	~	Lead Length
e	0.40 Basic			Lead Pitch
q	0°	~	7°	Lead Foot Angle
W	0.13	0.18	0.23	Lead Width
R1	0.08	~	~	Lead Shoulder Radius
R2	0.08	~	0.20	Lead Foot Radius
ccc	~	~	0.08	Coplanarity

**Notes:**

- Controlling Unit: millimeter.
- Tolerance on the true position of the leads is  $\pm 0.035$  mm maximum.  
Package body dimensions D1 and E1 do not include the mold protrusion.
- Maximum mold protrusion is 0.25 mm.
- Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.
- Details of pin 1 identifier are optional but must be located within the zone indicated.

## Chapter 9 GPIO Usage

**Table 9.1 GPIO Usage (ROM Rev 0x00)**

NAME	ACTIVE LEVEL	SYMBOL	DESCRIPTION AND NOTE
GPIO1	H	Flash Media Activity LED/ xD_Door	Indicates media activity. Media or USB cable must not be removed with LED lit. Also may be used for xD Door functionality
GPIO2	H	EE_CS	Serial EE PROM chip select
GPIO3	H	V_BUS	USB V bus detect
GPIO4	H	EE_DIN/EE_DOUT/xDID	Serial EE PROM input/output and xD Identify
GPIO5	H	HS_IND/SD_CD	HS Indicator LED or SD Card Detect Switch input
GPIO6	H	A16/ROMEN	A16 address line connect for DFU or debug LED indicator optional.
GPIO7	H	EE_CLK/ UNCONF_LED	Serial EE PROM clock output or Unconfigured LED.
GPIO8	L	MS_PWR_CTRL/ CRD_PWR0	Memory Stick Card Power Control, or Internal Power FET0.
GPIO9	L	CF_PWR_CTRL	CompactFlash Card Power Control
GPIO10	L	SM_PWR_CTRL/ CRD_PWR1	SmartMedia Card Power Control, or Internal Power FET1.
GPIO11	L	SD/MMC_PWR_CTRL/ CRD_PWR2	SD/MMC Card Power Control, or Internal Power FET2.
GPIO12	H	MS_ACT_IND/ Media Activity	Memory Stick Activity Indicator, or Media Activity LED.