HFC - S mini

ISDN HDLC FIFO controller

with

S/T interface and integrated FIFOs

Revision History

Date	Remarks
July 2003	The data sheet has completely been revised. Section "Processor interface modes" moved into section "Microprocessor interface", "List of registers" moved to the document preamble, information has been added to FIFO initialization, transformer list, processor interface timings, PCM data rate restrictions, electrical characteristics, clock synchronization, cascade-connected HFC-S mini with only one quartz circuitry and the following registers: INC_RES_F, RAM_DATA, FIFO, F_USAGE, F_FILL, FIF_DATA_NOINC, F_THRES, INT_S1, INT_M1, INT_M2, CON_HDLC, STATUS, MST_MODE0, MST_MODE1, MST_MODE2, ST_RD_STA, ST_WR_STA, CLKDEL.
September 2001	Information added to: MST_MODE0 and CON_HDLC register description.
August 2001	Chapters added: Timing diagrams for Motorala mode (mode2), sample circuitries.
July 2001	Information added to: Register description.
January 2001	Information added to: Microprocessor access, PCM / GCI / IOM2 timing.

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List of Registers sorted by name

> ☞ **Please note !**
>
> Register addresses are assigned independently for write and read access; i.e. in some cases there are different registers for write and read access with the same address. Only registers with the same meaning and bitmap structure in both write and read directions are declared to be read / write.

Write only registers:

Address	Name	Page
0x26	AUX1_RSL	47
0x22	AUX1_SSL	45
0x27	AUX2_RSL	47
0x23	AUX2_SSL	45
0x24	B1_RSL	46
0x3C	B1_SEND	60
0x20	B1_SSL	44
0x25	B2_RSL	46
0x3D	B2_SEND	60
0x21	B2_SSL	44
0xF4	CH_MASK	41
0xFC	CHANNEL	42
0x00	CIRM	29
0x37	CLKDEL	59
0xFA	CON_HDLC	40
0x3E	D_SEND	61
0x0B	F_CROSS	29
0x0D	F_MODE	30
0x0C	F_THRES	34
0x0F	FIFO	31
0xFB	HDLC_PAR	39
0x0E	INC_RES_F	30
0x1A	INT_M1	38
0x1B	INT_M2	38
0x14	MST_MODE0	50
0x15	MST_MODE1	51
0x16	MST_MODE2	52
0x09	RAM_ADR_H	31
0x08	RAM_ADR_L	30
0x32	SCTRL_E	57
0x33	SCTRL_R	57
0x31	SCTRL	56
0x34	SQ_SEND	58
0x30	ST_WR_STA	55
0x1C	TIME_SEL	43

Read only registers:

Address	Name	Page
0x3C	B1_REC	59
0x3D	B2_REC	60
0x16	CHIP_ID	42
0x3E	D_REC	60
0x3F	E_REC	61
0x1B	F_FILL	35
0x1A	F_USAGE	32
0x19	F0_CNT_H	53
0x18	F0_CNT_L	52
0x0C	FIF_F1	32
0x0D	FIF_F2	33
0x04	FIF_Z1	33
0x06	FIF_Z2	33
0x10	INT_S1	36
0x11	INT_S2	37
0x34	SQ_REC	58
0x30	ST_RD_STA	54
0x1C	STATUS	43
0x29	TRxR	53

Read / Write registers:

Address	Name	Page
0x2E	AUX1_D	48
0x2F	AUX2_D	49
0x2C	B1_D	48
0x2D	B2_D	48
0x28	C/I	53
0x84	FIF_DATA_NOINC	32
0x80	FIF_DATA	32
0x2A	MON1_D	54
0x2B	MON2_D	54
0xC0	RAM_DATA	31

List of Registers sorted by address

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> Register addresses are assigned independently for write and read access; i.e. in some cases there are different registers for write and read access with the same address. Only registers with the same meaning and bitmap structure in both write and read directions are declared to be read / write.

Write only registers:

Address	Name	Page
0x00	CIRM	29
0x08	RAM_ADR_L	30
0x09	RAM_ADR_H	31
0x0B	F_CROSS	29
0x0C	F_THRES	34
0x0D	F_MODE	30
0x0E	INC_RES_F	30
0x0F	FIFO	31
0x14	MST_MODE0	50
0x15	MST_MODE1	51
0x16	MST_MODE2	52
0x1A	INT_M1	38
0x1B	INT_M2	38
0x1C	TIME_SEL	43
0x20	B1_SSL	44
0x21	B2_SSL	44
0x22	AUX1_SSL	45
0x23	AUX2_SSL	45
0x24	B1_RSL	46
0x25	B2_RSL	46
0x26	AUX1_RSL	47
0x27	AUX2_RSL	47
0x30	ST_WR_STA	55
0x31	SCTRL	56
0x32	SCTRL_E	57
0x33	SCTRL_R	57
0x34	SQ_SEND	58
0x37	CLKDEL	59
0x3C	B1_SEND	60
0x3D	B2_SEND	60
0x3E	D_SEND	61
0xF4	CH_MASK	41
0xFA	CON_HDLC	40
0xFB	HDLC_PAR	39
0xFC	CHANNEL	42

Read only registers:

Address	Name	Page
0x04	FIF_Z1	33
0x06	FIF_Z2	33
0x0C	FIF_F1	32
0x0D	FIF_F2	33
0x10	INT_S1	36
0x11	INT_S2	37
0x16	CHIP_ID	42
0x18	F0_CNT_L	52
0x19	F0_CNT_H	53
0x1A	F_USAGE	32
0x1B	F_FILL	35
0x1C	STATUS	43
0x29	TRxR	53
0x30	ST_RD_STA	54
0x34	SQ_REC	58
0x3C	B1_REC	59
0x3D	B2_REC	60
0x3E	D_REC	60
0x3F	E_REC	61

Read / Write registers:

Address	Name	Page
0x28	C/I	53
0x2A	MON1_D	54
0x2B	MON2_D	54
0x2C	B1_D	48
0x2D	B2_D	48
0x2E	AUX1_D	48
0x2F	AUX2_D	49
0x80	FIF_DATA	32
0x84	FIF_DATA_NOINC	32
0xC0	RAM_DATA	31

1 General description

The HFC-S mini is a single-chip ISDN S/T HDLC basic rate controller for embedded applications. The S/T interface, HDLC controllers, FIFOs and a microprocessor interface are integrated in the HFC-S mini. A PCM128 / PCM64 / PCM30 interface is also implemented which can be connected to many telecom serial busses. CODECs are usually connected to this interface. All ISDN channels (2 B + 1 D) and the PCM interface are served fully duplex by the 8 integrated FIFOs. HDLC controllers are implemented in hardware so there is no need to implement HDLC on the host processor.

1.1 Features

- single chip ISDN S/T controller with B- and D-channel HDLC support

- integrated S/T interface

- full I.430 ITU S/T ISDN support in TE and NT mode for 3.3 V and 5 V power supply

- independent read and write HDLC channels for two ISDN B-channels, one ISDN D-channel and one additional PCM time slot (or E-channel)

- B1- and B2-channel transparent mode independently selectable

- integrated FIFOs for B1-channel, B2-channel, D-channel and an additional PCM (or E-channel) channel

- FIFO size: 128 bytes per channel and direction; up to 7 HDLC frames per FIFO

- 56 kbit/s restricted mode for U.S. ISDN lines selectable by software

- PCM128 / PCM64 / PCM30 interface configurable to interface MITEL ST^{TM} bus (MVIP^{TM}), Siemens IOM2^{TM} or GCI^{TM} for interface to U-chip or external CODECs

- H.100 data rate supported

- microprocessor interface compatible to Motorola bus and Intel bus

- Timer with interrupt capability

- CMOS technology, 3 V . . 5 V

- PQFP 48 package

1.2 Block diagram
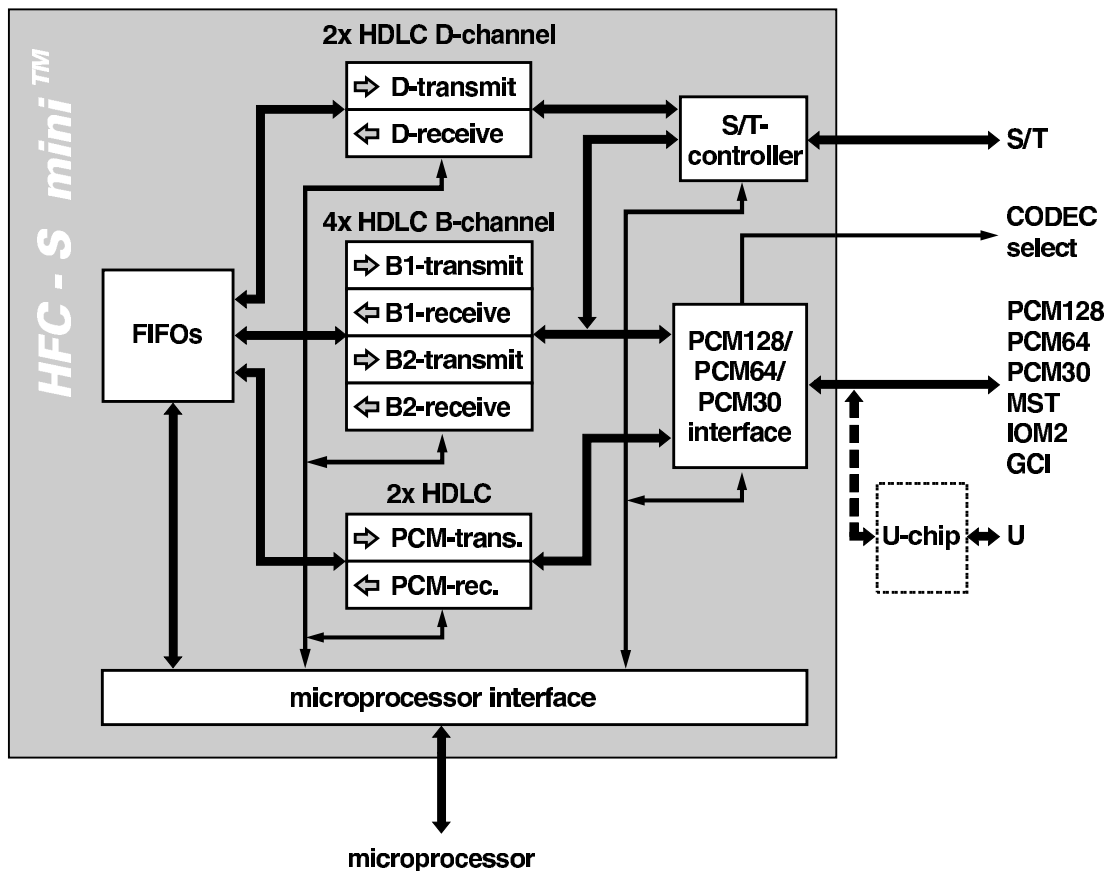
Figure 1: *HFC-S mini block diagram*

1.3 Applications

The HFC-S mini can be used for all kinds of ISDN equipment with ISDN basic rate S/T interface.

- ISDN terminal adapters (for internet access)
- ISDN terminal adapters (with POTS interfaces)
- ISDN PABX
- ISDN SoHo PABX (switching done by HFC-S mini)
- ISDN telephones
- ISDN video conferencing equipment
- ISDN dialers and LCR (Least Cost Routers)
- ISDN LAN routers
- ISDN protocol analyzers
- ISDN smart NTs

2   Pin description
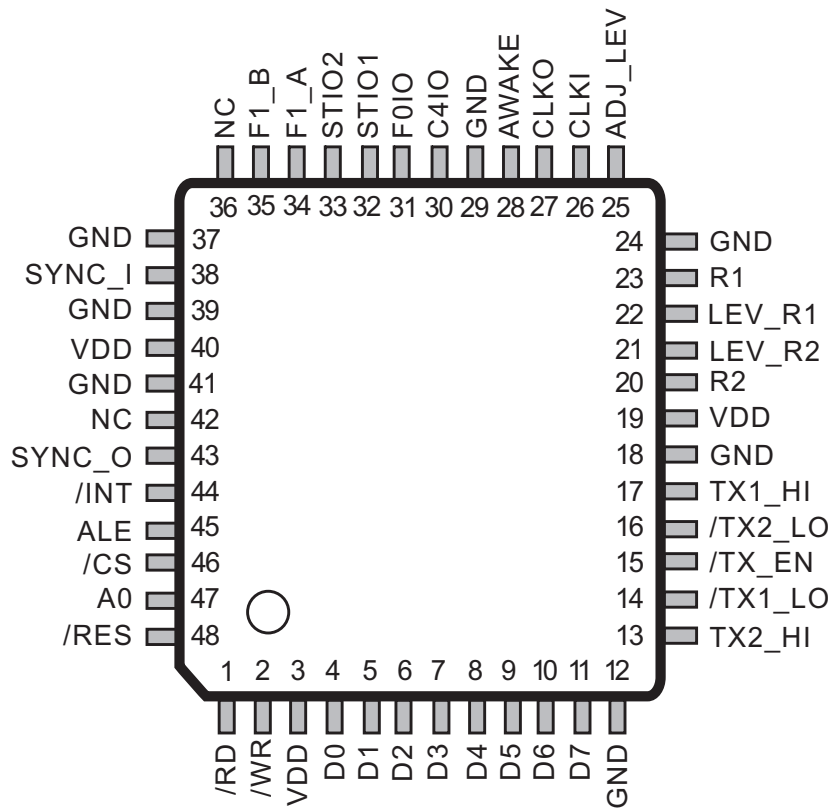
Figure 2: *Pin Connection*

Pin	Interface	Name	I/O	Description
1	1st function	/RD	I	Read signal from external processor (low active)
	2nd function	/DS	I	I/O data strobe
2	1st function	/WR	I	Write signal from external processor (low active)
	2nd function	R/W	I	Read/Write select (WR = '0')
3		VDD		VDD (3.3V or 5V)
4		D0	IOr	Data bus (bit 0)
5		D1	IOr	Data bus (bit 1)
6		D2	IOr	Data bus (bit 2)
7		D3	IOr	Data bus (bit 3)
8		D4	IOr	Data bus (bit 4)
9		D5	IOr	Data bus (bit 5)
10		D6	IOr	Data bus (bit 6)
11		D7	IOr	Data bus (bit 7)

(continued on next page)

Pin	Interface	Name	I/O	Description
12		GND		GND
13		TX2_HI	O	Transmit output 2
14		/TX1_LO	O	GND driver for transmitter 1
15		/TX_EN	O	Transmit enable
16		/TX2_LO	O	GND driver for transmitter 2
17		TX1_HI	O	Transmit output 1
18		GND		GND
19		VDD		VDD (3.3V or 5V)
20		R2	I	Receive data 2
21		LEV_R2	I	Level detect for R2
22		LEV_R1	I	Level detect for R1
23		R1	I	Receive data 1
24		GND		GND
25		ADJ_LEV	O	Level generator
26		CLKI	I	24.576 MHz clock input or 24.576 MHz crystal
27		CLKO	O	24.576 MHz clock output or 24.576 MHz crystal
28		AWAKE	I	Awake input pin for external awake circuitry
29		GND		GND
30		C4IO	IOpu	Double bit clock 4.096 MHz / 8.192 MHz / 16.384 MHz
31		F0IO	IOpu	Frame synchronization, 8 kHz pulse for PCM/GCI/IOM2 bus frame synchronization
32		STIO1	IOpu	PCM/GCI/IOM2 bus data line 1
33		STIO2	IOpu	PCM/GCI/IOM2 bus data line 2
34		F1_A	O	Enable signal for external CODEC A or C2IO clock (bit clock), programmable as positive (reset default) or negative pulse
35		F1_B	O	Enable signal for external CODEC B, programmable as positive (reset default) or negative pulse
36		NC		Must not be connected
38		SYNC_I	I	8 kHz synchronization input
39		GND		GND
40		VDD		VDD (3.3V or 5V)
41		GND		GND

Pin	Interface	Name	I/O	Description
42		NC		Must not be connected
43		SYNC_O	O	8 kHz synchronization output
44		/INT	Ood	Interrupt request for external processor (low active)
45		ALE	Ipu	Address latch enable ALE is also used for mode selection during reset
46		/CS	Ipu	Chip select (low active)
47		A0	I	Address bit 0 from external processor
48		/RES	Istpu	Reset (low active)

Legend:

I	Input pin
O	Output pin
IO	Bidirectional pin
Ipu	Input pin with internal pull-up resistor of app. $100\,k\Omega$ to VDD
IOpu	Bidirectional pin with internal pull-up resistor of app. $100\,k\Omega$ to VDD
Istpu	Input pin with Schmitt trigger characteristic and internal pull-up resistor of app. $100\,k\Omega$ to VDD
IOr	Tristated during reset
Ood	Output pin with open drain
NC	Not connected

Unused input pins should be connected to ground.

3 Functional description

3.1 Microprocessor interface

The HFC-S mini has an integrated 8 bit microprocessor interface. It is compatible with Motorola bus and Intel bus. The different microprocessor interface modes are selected during reset by ALE.

In mode 2 (Motorola bus mode) and mode 3 (de-multiplexed Intel bus mode) pin A0 is the address input. The data bus is D7..D0.

In mode 4 (multiplexed Intel bus mode) D[7:0] is the multiplexed address/data bus. A0 must be '0' in this mode.

3.1.1 Processor interface modes

Mode 2: Motorola bus with control signals /CS, R/W, /DS is selected by setting ALE to VDD.

Mode 3: Intel bus with seperated address bus (A0) and data bus (D7..D0) and control signals /CS, /WR, /RD is selected by setting ALE to GND.

Mode 4: Intel bus with multiplexed address bus and data bus with control signals /CS, /WR, /RD, ALE. The first rising edge on ALE switches into this mode. A0 must be '0'. ALE latches the address. The multiplexed address/data bus is D7..D0.

In mode 4 all internal registers can be directly accessed. In mode 2 and mode 3 first the address of the desired register must be written to the address with A0 = '1'. Afterwards data can be read/written from/to that register by reading/writing the address with A0 = '0'. In mode 4 A0 must always be '0'.

3.1.2 Register access

In mode 2 and mode 3 the HFC-S mini has 2 addresses. The lower address (A0 = '0') is used for data read/write. The higher address (A0 = '1') is write only and is used for register selection. Registers are selected by first setting A0 to '1' and then writing the address of the desired register to the data bus D7..D0. All following accesses to the HFC-S mini with A0 = '0' are read/write operations concerning this register.

In mode 4 all registers can be directly accessed by their address. The function of the control signals is shown in Table 2. Except in mode 4, ALE is assumed to be stable after reset.

Table 2: *Function of the microprocessor interface control signals (X = don't care)*

/RD /DS	/WR R/W	/CS	ALE	Operation	Mode
X	X	1	X	no data access	all
1	1	X	X	no data access	all
0	1	0	1	read data	2
0	0	0	1	write data	2
0	1	0	0	read data	3
1	0	0	0	write data	3
0	1	0	0 *	read data	4
1	0	0	0 *	write data	4

(*: 1-pulse latches register address)

☞ **Please note !**

Every asynchronous register read access should be done multiple times until two consecutive read accesses result in the same value. Only this way it is ensured that the read bits are stable.
This information applies to the following registers:

F_USAGE (0x1A),	RAM_DATA (0xC0),	FIF_DATA (0x80),
FIF_DATA_NOINC (0x84),	FIF_F1 (0x0C),	FIF_F2 (0x0D),
FIF_Z1 (0x04),	FIF_Z2 (0x06),	B1_D (0x2C),
B2_D (0x2D),	AUX1_D (0x2E),	AUX2_D (0x2F),
F0_CNT_L (0x18),	F0_CNT_H (0x19),	C/I (0x28),
MON1_D (0x2A),	MON2_D (0x2B),	SQ_REC (0x34).

3.2 FIFOs

There is a transmit and a receive FIFO with HDLC controller for each of the two B-channels, for the D-channel and for the PCM interface in the HFC-S mini. As an alternative the PCM receive controller can be used for the E-channel. Every FIFO has a length of 128 bytes in each direction. Up to 7 frames can be stored in every FIFO.

The HDLC circuits are located on the S/T device side of the HFC-S mini. So always plain data is stored in the FIFOs. Zero insertion and CRC checksum processing for receive and transmit data is done by the HFC-S mini automatically.

A FIFO can be selected for access by writing its number in the FIFO select register FIFO.

The FIFOs are ring buffers. To control them there are some counters. *Z1* is the FIFO input counter and *Z2* is the FIFO output counter.

Each counter points to a byte position in the SRAM. On a FIFO input operation $Z1$ is incremented. On an output operation $Z2$ is incremented.

After every pulse of the F0IO signal two HDLC bytes for the B1- and the B2-channel are written into the S/T interface (FIFOs with even numbers) and two HDLC-bytes are read from the S/T interface (FIFOs with odd numbers).

D-channel data is handled in a similar way but only 2 bits are processed.

☞ **Important !**

Instead of the S/T interface the PCM bus is also selectable for each B-channel (see CON_HDLC register).

If $Z1 = Z2$ the FIFO is empty.

Additionally there are two counters $F1$ and $F2$ for every FIFO channel (3 bits for each channel). They count the HDLC frames in the FIFOs and form a ring buffer as $Z1$ and $Z2$ do, too.

$F1$ is incremented when a complete frame has been received and stored in the FIFO. $F2$ is incremented when a complete frame has been read from the FIFO.

If $F1 = F2$ there is no complete frame in the FIFO.

When the /RES line is active or software reset is active $Z1$, $Z2$, $F1$ and $F2$ are all initialized to all '1's (so Z-counters are initialized to 0x7F and F-counters are initialized to 0x07).

The access to a FIFO is selected by writing the FIFO number into the FIFO select register FIFO.

☞ **Important !**

FIFO change, FIFO reset and $F1/F2$ incrementation:

Changing the FIFO, resetting the FIFO or incrementing the frame counters causes a short BUSY period of the HFC-S mini. This means an access to FIFO control registers and data registers is *not* allowed until BUSY status is reset (bit 0 of STATUS register). This has a maximum duration of 25 clock cycles ($2\,\mu$s).

Status, interrupt and control registers can be read or written at any time.

☞ **Important !**

The counter state 0x00 of the Z-counters follows counter state 0x7F in all FIFOs.
The counter state 0x00 of the F-counters follows counter state 0x07 in all FIFOs.

3.2.1   FIFO channel operation

3.2.1.1   Send channels (B1, B2, D and PCM transmit)

The send channels send data from the host bus interface to the FIFO and the HFC-S mini converts the data into HDLC code and tranfers it from the FIFO into the S/T or / and the PCM bus interface write registers.

The HFC-S mini checks $Z1$ and $Z2$. If $Z1 = Z2$ (FIFO empty) the HFC-S mini generates a HDLC flag '0111 1110' or idle pattern '1111 1111' and sends it to the S/T device. In this case $Z2$ is not incremented. If also $F1 = F2$ only HDLC flags are sent to the S/T interface and all counters remain unchanged. If the frame counters are unequal $F2$ is incremented and the HFC-S mini tries to send the next frame to the output device. After the end of a frame ($Z2$ reaches $Z1$) it automatically generates the 16 bit CRC checksum and adds the ending flag. If there is another frame in the FIFO ($F1 \neq F2$) the $F2$ counter is incremented.

With every byte being sent from the host bus side to the FIFO, $Z1$ is incremented automatically. If a complete frame has been sent, $F1$ must be incremented to send the next frame. If the frame counter $F1$ is incremented, also the Z-counters may change because $Z1$ and $Z2$ are functions of $F1$ and $F2$. So there are $Z1(F1)$, $Z2(F1)$, $Z1(F2)$ and $Z2(F2)$ (see Figure 3).

Figure 3: *FIFO Organization*

$Z1(F1)$ is used for the frame which is just written from the microprocessor bus side. $Z2(F2)$ is used for the frame which is just beeing transmitted to the S/T device side of the HFC-S mini. $Z1(F2)$ is the end of frame pointer of the current output frame.

In the send channels $F1$ is only changed from the microprocessor interface side if the software driver wants to say "end of send frame". If bit 0 in INC_RES_F register is set, the current value of $Z1$ is stored, $F1$ is incremented and $Z1$ is used as start address of the next frame automatically. $Z1(F2)$ and $Z2(F2)$ can not be accessed.

☞ **Important !**

The HFC-S mini begins to transmit the bytes from a FIFO at the moment the FIFO is changed or the $F1$ counter is incremented. Also changing to the FIFO that is already selected starts the transmission. So by selecting the same FIFO again transmission can be started. This is required if a HDLC frame is longer than 128 bytes.

3.2.1.2 Automatically D-channel frame repetition

The D-channel send FIFO has a special feature. If the S/T interface signals a D-channel contention before the CRC is sent, the $Z2$ counter is set to the starting address of the current frame and the HFC-S mini tries to repeat the frame automatically.

3.2.1.3 FIFO full condition in send channel

There are two different FIFO full conditions. The first one is met when the FIFO contents comes up to 7 frames. There is no possibility for the HFC-S mini to manage more HDLC frames even if the frames are very small. The driver software must check that there are never more than 7 HDLC frames in a FIFO.

The second limitation is the size of the FIFO (128 bytes each). FIFO full condition can be checked by reading the F_USAGE register. It shows the actually occupied FIFO space in bytes.

Furthermore a threshold value can be set for all transmit and receive FIFOs in the F_THRES register. Then the F_FILL register shows an indication of the filling level for each FIFO. After data processing from or to a FIFO, the F_FILL register must be updated with a change FIFO or an increment FIFO counter operation. After this it takes up to $250\,\mu$s until the bit value in the F_FILL register of the processed FIFO represents the actual state of the FIFO filling level.

3.2.1.4 Receive Channels (B1, B2, D and PCM or E receive)

The receive channels receive data from the S/T or PCM bus interface read registers. The data is converted from HDLC into plain data and sent to the FIFO. Then the data can be read via the microprocessor bus interface.

The HFC-S mini checks the HDLC data coming in. If it finds a flag or more than 5 consecutive '1's it does not generate any output data. In this case $Z1$ is not incremented. Proper HDLC data being received is converted by the HFC-S mini into plain data. After the ending flag of a frame the HFC-S mini checks the HDLC CRC checksum. If it is correct one STAT byte (see Figure 4) with all '0's is inserted behind the CRC data in the FIFO. This last byte of a frame in the FIFO is different from all '0's if there is no correct CRC field at the end of the frame.

The ending flag of a HDLC-frame can also be the starting flag of the next frame.

After a frame is received completely, $F1$ is incremented by the HFC-S mini automatically and the next frame can be received.

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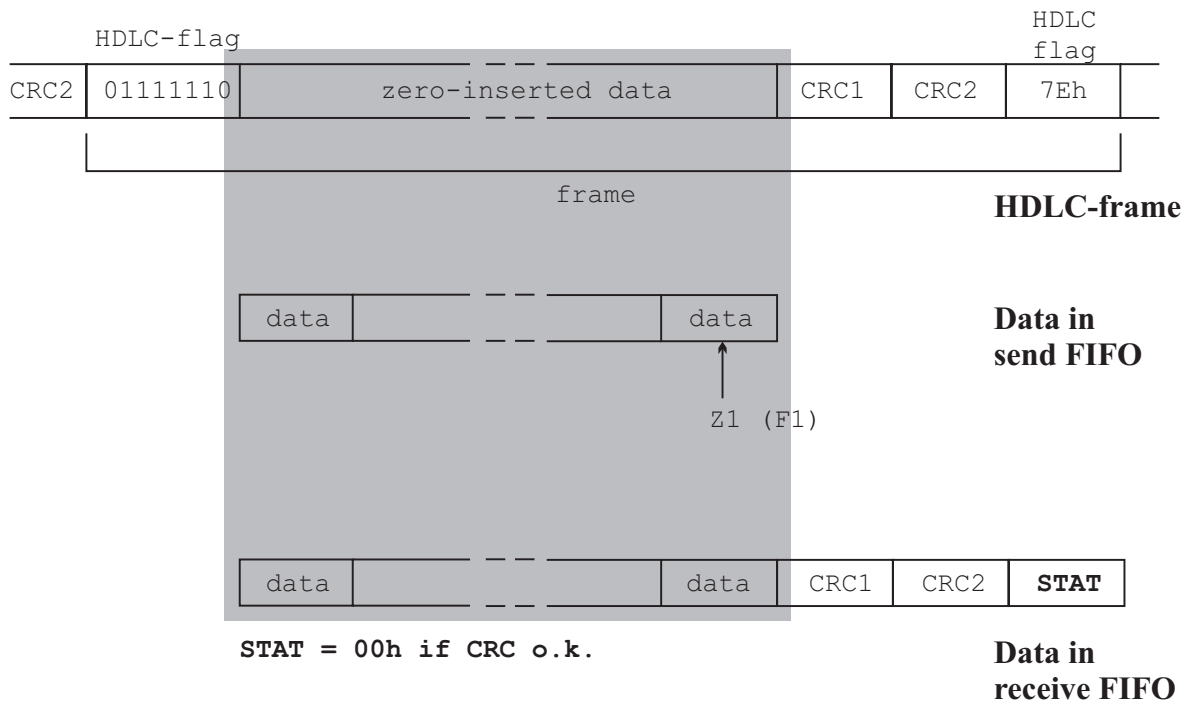
Figure 4: *FIFO Data Organization*

After reading a frame via the microprocessor bus interface, $F2$ must be incremented. If the frame counter $F2$ is incremented, also the Z-counters may change because $Z1$ and $Z2$ are functions of $F1$ and $F2$. So there are $Z1(F1)$, $Z2(F1)$, $Z1(F2)$ and $Z2(F2)$ (see Figure 3).
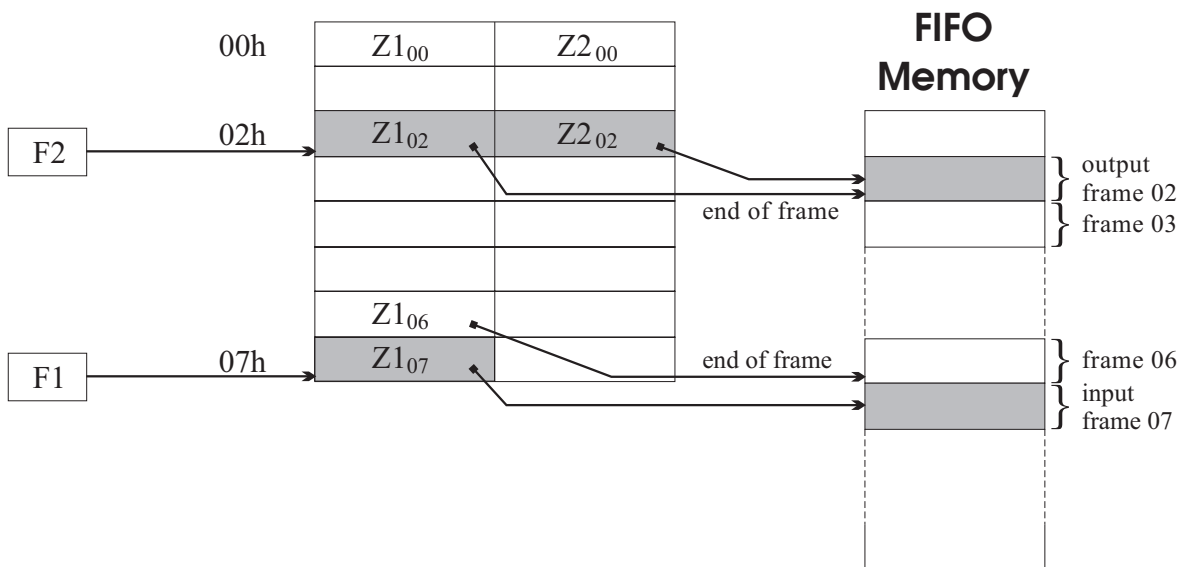
$Z1(F1)$ is used for the frame which is just received from the S/T device side of the HFC-S mini. $Z2(F2)$ is used for the frame which is just beeing transmitted to the microprocessor bus interface. $Z1(F2)$ is the end of frame pointer of the current output frame.

To calculate the length of the current receive frame the software has to evaluate $Z1 - Z2 + 1$. When $Z2$ reaches $Z1$ the complete frame has been read.

In the receive channels $F2$ must be incremented from the microprocessor bus interface side after the software detects an *end of receive frame* ($Z1 = Z2$) and $F1 \neq F2$. Then the current value of $Z2$ is stored, $F2$ is incremented and $Z2$ is copied as start address of the next frame. If $Z1 = Z2$ and $F1 = F2$ the FIFO is totally empty. $Z1(F1)$ can not be accessed.

☞ **Important !**

Before reading a FIFO, a change FIFO operation (see also: FIFO register) must be done even if the desired FIFO is already selected. The change FIFO operation is required to update the internal buffer of the HFC-S mini. Otherwise the first byte of the FIFO will be taken from the internal buffer and may be invalid.

3.2.1.5 FIFO full condition in receive channels

Because the ISDN B-channels and the ISDN D-channels have no hardware based flow control there is no possibility to stop input data if a receive FIFO is full.

So there is no FIFO full condition implemented in the HFC-S mini. The HFC-S mini assumes that the FIFOs are so deep, that the host processors hardware and software is able to avoid any overflow of the receive FIFOs. Overflow conditions are again more than 7 input frames or a real overflow of the FIFO because of excessive data (more than 128 bytes).

Because HDLC procedures only know a window size of 7 frames no more than 7 frames are sent without software intervention.

The register F_FILL indicates if the fill level of some FIFOs exceeds the number of bytes defined in the F_THRES register. A byte overflow can be avoided by polling this register. After data processing from or to a FIFO, the F_FILL register must be updated with a change FIFO or an increment FIFO counter operation. After this it takes up to $250\,\mu s$ until the bit value in the F_FILL register of the processed FIFO represents the actual state of the FIFO filling level.

The register F_USAGE shows the actually occupied FIFO space in bytes. A byte overflow can be avoided by polling this register.

However to avoid any undetected FIFO overflows the software driver should check the number of frames in the FIFO which is $F1 - F2$. An overflow exists if the number $F1 - F2$ is less than the number in the last reading even if there was no reading of a frame in between.

After a detected FIFO overflow condition this FIFO must be reset by setting the FIFO reset bit in the INC_RES_F register.

3.2.2 FIFO initialization

All FIFOs are disabled after reset. To enable a FIFO, at least one of the bits[4:1] of the CON_HDLC register for the corresponding FIFO must be set to '1'.

For D-channel FIFOs the inter frame fill bit (bit 0 of CON_HDLC register) must be set to '1'. The HDLC_PAR register must be set to 0x02 ('0000 0010').

Even for a data transmission between S/T interface and PCM interface where no FIFO data is involved, the data transmission capability is only activated if the corresponding FIFO is enabled.

3.2.3 FIFO reset

All counters $Z1$, $Z2$, $F1$ and $F2$ of all FIFOs are initialized to all '1's after a reset. Then the result is $Z1 = Z2 = 0x7F$ and $F1 = F2 = 0x07$.

The same initialisation is done if the bit 3 in the CIRM register is set (soft reset).

Single FIFOs can be reset by setting bit 1 of INC_RES_F register.

3.3 Transparent mode of HFC-S mini

You can switch off HDLC operation for each B-channel independently. There is one bit for each B-channel in the CON_HDLC control register. If this bit is set, data in the FIFO is sent directly to the

S/T or PCM bus interface and data from the S/T or PCM bus interface is sent directly to the FIFO.

The FIFOs should be empty when switching into transparent mode ($F1 = F2$).

If a send FIFO channel changes to FIFO empty condition no CRC is generated and the last data byte in the FIFO memory is repeated until there is new data. If the last data byte which was written to the selected FIFO should be repeated, the last byte must be written without increment of Z-counter (FIF_DATA_NOINC register, address 84).

In receive channels there is no check on flags or correct CRCs and no status byte is added.

The byte boundaries are not arbitrary like in HDLC mode where byte synchronisation is achieved with HDLC flags. The data is just the same as it comes from the S/T or PCM bus interface or is sent to this.

Send and receive transparent data can be handled in two ways. The usual way is transporting B-channel data with the LSB first as it is usual in HDLC mode. The second way is sending the bytes in reverse bit order as it is usual for PWM data. So the first bit is the MSB. The bit order can be reversed by setting the corresponding bit in the F_CROSS register.

3.4   Correspondency between FIFOs, CHANNELs and SLOTs

For the data processing of the HFC-S mini you must distinguish between FIFOs, CHANNELs and SLOTs.

The FIFOs are buffers between the microprocessor interface and the data interfaces PCM and/or S/T. The HDLC controllers are located on the non host bus side of the FIFOs.

The CHANNELs are either mapped to the data channels on the S/T interface (then the CHANNEL selects the S/T channel as shown in Table 3) or they can be connected to arbitrary time slots on the PCM interface. SLOTs are 8 bit time slots on the PCM interface. The following values (registers) characterise FIFOs, CHANNELs and SLOTs:

FIFO: FIFO

CHANNEL: CHANNEL

SLOT: B1_RSL, B1_SSL, B2_RSL, B2_SSL, AUX1_RSL, AUX1_SSL, AUX2_RSL and AUX2_SSL

Even numbers (LSB = '0') always belong to a transmit FIFO, transmit CHANNEL (see Table 4).

Odd numbers (LSB = '1') always belong to a receive FIFO, receive CHANNEL (see Table 4).

In Simple Mode (F_MODE register bit 7 = '0', SM) the CHANNEL number equals the FIFO number. But it is possible to connect each FIFO to a PCM time slot instead of the S/T interface in this mode (see Table 3).

In Channel Select Mode (F_MODE register bit 7 = '1', CSM) FIFOs can be associated with arbitrary CHANNELs.

FIFOs are selected by writing their number in the FIFO register. All FIFOs are disabled after initialization (reset). By setting at least one of the CON_HDLC register bits 3 . . 1 to '1' the selected FIFO is enabled.

The connection between a FIFO and a CHANNEL can be established by the CHANNEL register for each FIFO if Channel Select Mode is enabled (F_MODE register bit 7 = '1', CSM). Otherwise the CHANNEL number equals the FIFO number.

Table 3: *Possible connections of FIFO and CHANNELs in Simple Mode (SM)*

FIFO no. FIFO[2..0]	CHANNEL after reset	Possible connections in Simple Mode (SM) CON_HDLC[7..5]
'000'	transmit B1-channel (S/T)	transmit B1-channel (S/T) transmit PCM time slot selected by B1_SSL
'001'	receive B1-channel (S/T)	receive B1-channel (S/T) receive PCM time slot selected by B1_RSL
'010'	transmit B2-channel (S/T)	transmit B2-channel (S/T) transmit PCM time slot selected by B2_SSL
'011'	receive B2-channel (S/T)	receive B2-channel (S/T) receive PCM time slot selected by B2_RSL
'100'	transmit D-channel (S/T)	transmit D-channel (S/T) transmit PCM time slot selected by AUX1_SSL
'101'	receive D-channel (S/T)	receive D-channel (S/T) receive PCM time slot selected by AUX1_RSL
'110'	invalid (E is receive only)	– transmit PCM time slot selected by AUX2_SSL
'111'	receive E-channel (S/T)	receive E-channel (S/T) receive PCM time slot selected by AUX2_RSL

The channels on the S/T interface (B1, B2, D and E) and PCM interface (B1, B2, AUX1 and AUX2) are numbered as shown in Table 4.

Table 4: *CHANNEL numbers on the S/T interface and PCM interface*

CHANNEL no. CHANNEL[2..0]	ISDN channel on the S/T interface	ISDN channel on the PCM interface
'000'	B1 transmit	B1 transmit
'001'	B1 receive	B1 receive
'010'	B2 transmit	B2 transmit
'011'	B2 receive	B2 receive
'100'	D transmit	AUX1 transmit
'101'	D receive	AUX1 receive
'110'	invalid (E is receive only)	AUX2 transmit
'111'	E receive	AUX2 receive

The data flow between the HFC part (FIFOs), S/T interface and PCM interface can be selected by the CON_HDLC register (bits 7..5) for each FIFO.

The PCM time slot for B1, B2, AUX1 and AUX2 can be set by the time slot assigner (registers B1_RSL, B1_SSL, B2_RSL, B2_SSL, AUX1_RSL, AUX1_SSL, AUX2_RSL and AUX2_SSL).

Data of a CHANNEL can furthermore be looped over the PCM interface (and the time slot assigner).
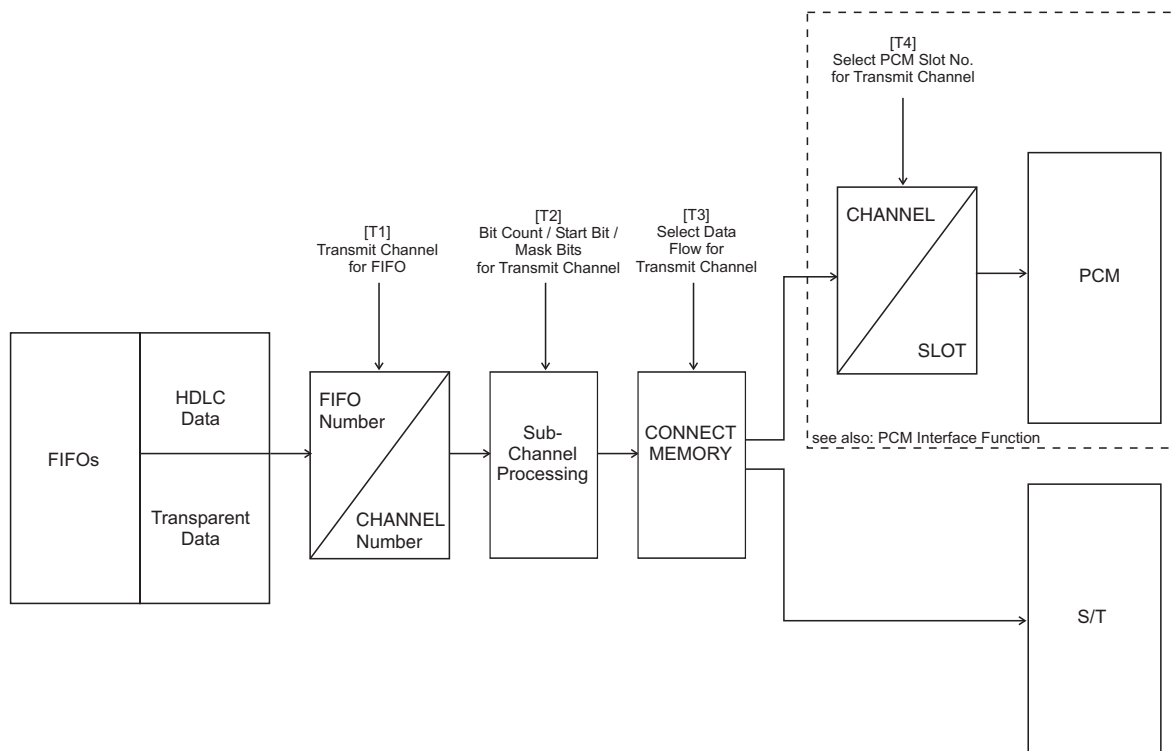
Figure 5: *FIFOs, CHANNELs and SLOTs in transmit Direction*

[T1] In Simple Mode (SM) the CHANNEL number is the same as the FIFO number. If Channel Select Mode (CSM) is enabled the transmit CHANNEL for a FIFO can be selected by

1. writing the FIFO number $(0 .. 7)$ in the FIFO register
2. writing the desired CHANNEL number $(0 .. 7)$ to the CHANNEL register (bits $2 .. 0$)

Please note that transmit CHANNELs are even numbered (bit 0 of CHANNEL register = '0').

[T2] The bit values for the not processed bits of the transmit CHANNEL are read from the CH_MASK register. The processed bits are taken from the FIFO (see also Section 3.5). Please note that more than one FIFO can transmit data to the same CHANNEL. This is useful to combine subchannels and transmit them in one ISDN channel.

[T3] Data can either be transmitted to the S/T interface or the PCM interface.

1. write the FIFO number $(0 .. 7)$ in the FIFO register
2. write the desired connection to the CON_HDLC register bits $7 .. 5$

The CON_HDLC register bits $7 .. 5$ settings must be the same for corresponding receive and transmit FIFOs.

[T4] A PCM SLOT can be connected to a CHANNEL (see Table 5 on Page 26).

The PCM SLOT number for a CHANNEL can be selected by writing the desired SLOT number to its time slot selection register as shown in Table 5. Please note that the .._SSL registers are for transmit slots.
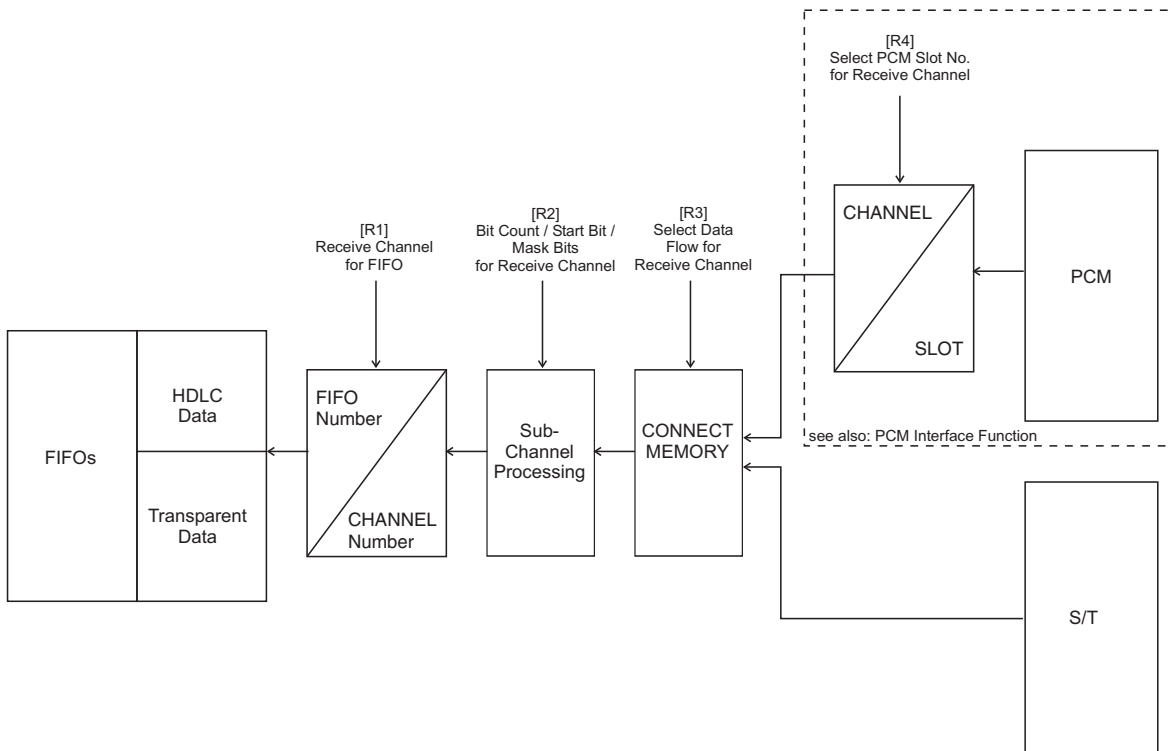
Figure 6: *FIFOs, CHANNELs and SLOTs in receive direction*

[R1] In Simple Mode (SM) the CHANNEL number is the same as the FIFO number. If Channel Select Mode (CSM) is enabled the transmit CHANNEL for a FIFO can be selected by

1. writing the FIFO number $(0 \ldots 7)$ in the FIFO register
2. writing the desired CHANNEL number $(0 \ldots 7)$ to the CHANNEL register (bits $2 \ldots 0$)

Please note that receive CHANNELs are odd numbered (bit 0 of CHANNEL register = '1').

[R2] The bit values of the not processed bits of the receive CHANNEL are ignored. The processed bits are taken from the CHANNEL (see also Section 3.5). Please note that more than one FIFO can receive data from the same CHANNEL (e.g. bits $1 \ldots 0$ are processed by FIFO 1 and bits $3 \ldots 2$ by FIFO 3). This is useful to split subchannels that have been combined to be transmitted in one ISDN channel.

[R3] Data can either be received from the S/T interface or the PCM interface.

1. write the FIFO number $(0 \ldots 7)$ in the FIFO register
2. write the desired connection to the CON_HDLC register bits $7 \ldots 5$

The CON_HDLC register bits $7 \ldots 5$ settings must be the same for corresponding receive and transmit FIFOs.

[R4] A PCM SLOT can be connected to a CHANNEL (see Table 5).

The PCM SLOT number for a CHANNEL can be selected by writing the desired SLOT number to its time slot selection selection register as shown in Table 5. Please note that only the .._RSL registers are for receive slots.

Table 5: *FIFO to S/T channel assignment (In Simple Mode the FIFO number is used as CHANNEL number; in Channel Select Mode the CHANNEL number can be selected for each FIFO in the register CHANNEL.)*

CHANNEL no. (FIFO[2..0] or CHANNEL[2..0]	Register for time slot selection
'000'	B1_SSL
'001'	B1_RSL
'010'	B2_SSL
'011'	B2_RSL
'100'	AUX1_SSL
'101'	AUX1_RSL
'110'	AUX2_SSL
'111'	AUX2_RSL

3.5 Subchannel Processing

The following example shows how subchannel processing can be configured by the HDLC_PAR register. Bits are shown on the PCM interface.
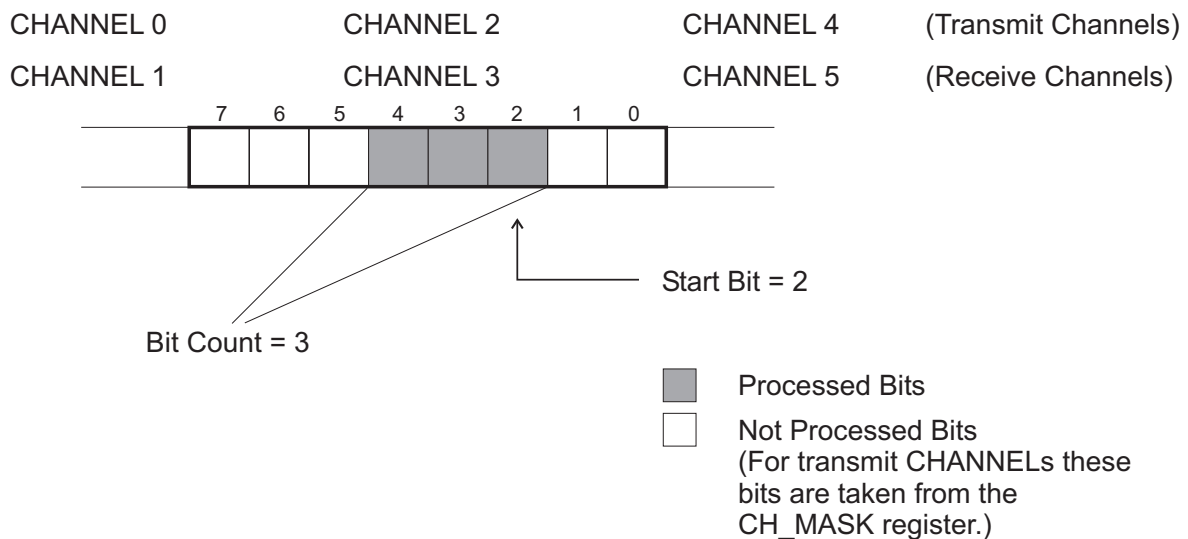
Figure 7: *Example for Subchannel Processing*

The start bit can be selected by bits 5..3 of the HDLC_PAR register. The number of bits to process can be selected by bits 2..0 of the HDLC_PAR register. By default (HDLC_PAR = 0x00) all 8 bits are processed. In the given example the start bit is bit 2 and the number of bits to process is 3. The not processed bits are set to the value given in the CH_MASK register. Please note that the HDLC_PAR register settings can be different for each channel.

3.6 PCM Interface Function
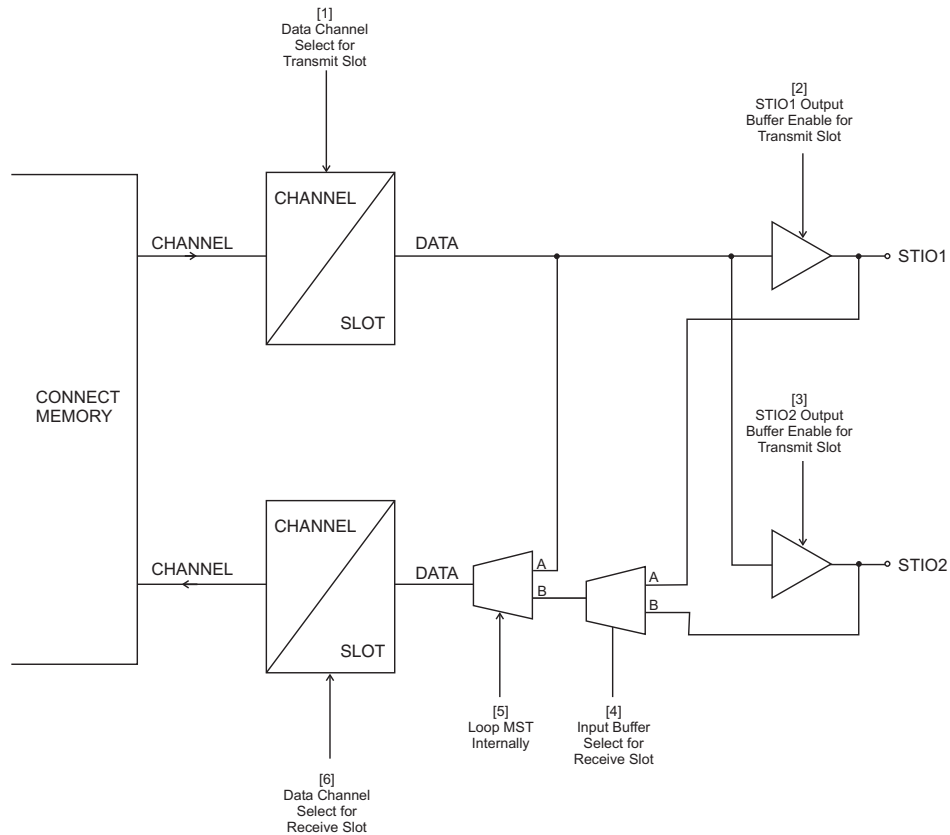
Figure 8: *PCM Interface Function Block Diagram*

Table 6: *PCM interface control options*

Number	Function	B1_SSL, B2_SSL, AUX1_SSL and AUX2_SSL register bits
[1]	Data channel select for transmit slot	Bits[4:0] are for time slot selection
[2]	STIO1 Output buffer enable for transmit slot	Bits[7:6] = '10' (STIO1 output buffer enable)
[3]	STIO2 output buffer enable for transmit slot	Bits[7:6] = '11' (STIO2 output buffer enable)
Number	**Function**	**B1_RSL, B2_RSL, AUX1_RSL and AUX2_RSL register bits**
[4]	Input buffer select for receive slot	Bit 6 = '0' (data in from STIO2 [MUX input B]) Bit 6 = '1' (data in from STIO1 [MUX input A])
[5]	Loop MST internally	Bit 6 of MST_MODE1 register '0' MUX input B (normal operation) '1' MUX input A (internal loop)
[6]	Data channel select for receive slot	Bits[4:0] are for time slot selection

3.7   Configuring test loops

For electrical tests of layer 1 it is useful to create a S/T test loop for the B1 / B2 channel. The test loop described here transmits the data that has been received on the B1- or B2-channel of the S/T interface to the same transmit channel back on the S/T interface. To configure the test loop the following settings have to implemented:

write 0x0F to register CLKDEL (0x37)	// Adjust the phase offset between receive and
	// transmit direction (the value depends on the external
	// circuitry).

write 0x43 to register SCTRL (0x31)	// 0x03 is to enable B1, B2 at the S/T interface for
	// transmission
	// Bit 6 could be set for /TX1_LO and /TX2_LO setup
	// (non-capacitive line mode), this depends on the
	// external S/T circuitry

write 0x00 to register ST_RD_STA (0x30)	// Release S/T state machine for activation over the // S/T interface by incoming INFO 2 or INFO 4.
write 0x03 to register SCTRL_R (0x33)	// Configure S/T B1- and B2-channel to normal // receive operation.
write 0x00 to register FIFO (0x0F)	// Select B1 transmit
write 0xC4 to register CON_HDLC (0xFA)	// Configure transmit B1-channel for test loop
write 0x01 to register FIFO (0x0F)	// Select B1 receive
write 0xC4 to register CON_HDLC (0xFA)	// Configure receive B1-channel for test loop
write 0x02 to register FIFO (0x0F)	// Select B2 transmit
write 0xC4 to register CON_HDLC (0xFA)	// Configure transmit B2-channel for test loop
write 0x03 to register FIFO (0x0F)	// Select B2 receive
write 0xC4 to register CON_HDLC (0xFA)	// Configure receive B2-channel for test loop
write 0x80 to register B1_SSL (0x20)	// Enable transmit channel for PCM / GCI / IOM2 bus, // pin STIO1 is used as output, use time slot #0.
write 0xC0 to register B1_RSL (0x24)	// Enable receive channel for PCM / GCI / IOM2 bus, // pin STIO1 is used as input, use time slot #0.
write 0x81 to register B2_SSL (0x21)	// Enable transmit channel for PCM / GCI / IOM2 bus, // pin STIO1 is used as output, use transmission slot #1.
write 0xC1 to register B2_RSL (0x25)	// Enable receive channel for PCM / GCI / IOM2 bus, // pin STIO1 is used as input, use time slot #1.
write 0x01 to register MST_MODE0 (0x14)	// Configure HFC-S mini as PCM / GCI / IOM2 bus master.

4 Register description

4.1 FIFO, interrupt, status and control registers

CIRM	**(write only)**	**0x00**
Soft reset		

Bits	**Description**
2..0	unused, must be '0'
3	The reset is active until the bit is cleared. '0' deactivate reset (reset default) '1' activate reset
7..4	unused, must be '0'

F_CROSS	**(write only)**	**0x0B**
Select bit order for FIFO data '0' normal bit order (LSB first, reset default) '1' reverse bit order (MSB first)		

Bits	**Description**
0	B1 transmit
1	B1 receive
2	B2 transmit
3	B2 receive
4	D transmit
5	D receive
6	PCM transmit
7	PCM receive

F_MODE	**(write only)**	0x0D
Channel Select Mode (CSM)		

Bits	Description
6..0	must be '0'
7	enable CSM

INC_RES_F [FIFO]	**(write only)**	0x0E
F-counter increment and reset		

Bits	Description
0	Increment F-counter of selected FIFO '1' = increment This bit is automatically cleared.
1	Reset selected FIFO '1' = reset FIFO This bit is automatically cleared.
7..2	unused, should be '0'

RAM_ADR_L [FIFO]	**(write only)**	0x08
Low byte of RAM address		

Bits	Description
7..0	Address bits 7..0 for direct RAM access

RAM_ADR_H	(write only)	0x09
High byte of RAM address		

Bits	Description
2..0	Address bits 10..8 for direct RAM access
5..3	must be '0'
6	'1' reset address This bit is automatically cleared.
7	'1' increment address after each read or write access to RAM_DATA

RAM_DATA	(read / write)	0xC0
Read/write RAM data		

Bits	Description
7..0	FIFOs should be disabled before accessing the RAM directly.

The registers RAM_ADR_H, RAM_ADR_L and RAM_DATA can be used or direct accesses to the internal FIFO RAM. They are normally not used.

The FIFOs are located in the address range from 0x000 to 0x3FF. Bits 2..0 of the address select the FIFO number, bits 10..4 are used to address the FIFO data.

Before reading / writing data from / to a memory region all FIFOs using this region must be disabled.

FIFO	(write only)	0x0F
FIFO select		

Bits	Description
2..0	'000' B1 transmit '001' B1 receive '010' B2 transmit '011' B2 receive '100' D transmit '101' D receive '110' PCM transmit '111' PCM receive or E receive
7..3	unused, should be '0'

F_USAGE [FIFO]	(read only)	0x1A
FIFO usage		

Bits	Description
7..0	fill level of FIFO in bytes

FIF_DATA [FIFO]	(read / write)	0x80
FIFO data register		

Bits	Description
7..0	Read/write data from/to the FIFO selected in the FIFO register and increment Z-counter

FIF_DATA_NOINC [FIFO]	(read / write)	0x84
FIFO data register		

Bits	Description
7..0	Read/write data from/to the FIFO selected in the FIFO register without incrementing Z-counter

FIF_F1 [FIFO]	(read only)	0x0C
FIFO input HDLC frame counter $F1$		

Bits	Description
7..0	Up to 7 HDLC frames can be stored in each FIFO.

FIF_F2 [FIFO]	(read only)	0x0D
FIFO output HDLC frame counter $F2$		

Bits	Description
7..0	Up to 7 HDLC frames can be stored in each FIFO.

FIF_Z1 [FIFO]	(read only)	0x04
FIFO input counter $Z1$		

Bits	Description
7..0	Up to 128 bytes can be stored in one FIFO so the maximum value of the $Z1$ counter is 0x7F.

FIF_Z2 [FIFO]	(read only)	0x06
FIFO output counter $Z2$		

Bits	Description
7..0	Up to 128 bytes can be stored in one FIFO so the maximum value of the $Z2$ counter is 0x7F.

F_THRES	(write only)	0x0C
FIFO threshold		

Bits	Description
3..0	Threshold for B1 transmit, B2 transmit, D transmit and PCM transmit (see also F_FILL) '0000' 0 bytes '0001' 8 bytes (reset default) '0010' 16 bytes (reset default) : : '1111' 120 bytes The corresponding bit(s) in the F_FILL register are set if the number of bytes in a transmit FIFO is greater or equal than this value.
7..4	Threshold for B1 receive, B2 receive, D receive and PCM receive (see also F_FILL) '0000' 0 bytes '0001' 8 bytes (reset default) '0010' 16 bytes (reset default) : : '1111' 120 bytes The corresponding bit(s) in the F_FILL register are set if the number of bytes in a receive FIFO is greater or equal than this value.

F_FILL	(read only)	0x1B

'0' Number of bytes in the following FIFOs is lower than the value defined in the F_THRES register.

'1' Number of bytes in the following FIFOs is greater or equal than the value defined in the F_THRES register.

Bits	Description
0	B1 transmit
1	B1 receive
2	B2 transmit
3	B2 receive
4	D transmit
5	D receive
6	PCM transmit
7	PCM receive

☞ **Important !**

After data reading from or writing to a FIFO, the F_FILL register must be updated with a change FIFO or an increment FIFO counter operation. After this it takes up to $250\,\mu$s until the bit value in the register F_FILL of the processed FIFO represents the actual state of the FIFO filling level.

INT_S1	(read only)	0x10

FIFO interrupt status

Bits	Description
0	B1 FIFO interrupt status in transmit direction '1' a complete frame has been transmitted, the frame counter $F2$ has been incremented
1	B1 FIFO interrupt status in receive direction '1' a complete frame has been transmitted, the frame counter $F1$ has been incremented
2	B2 FIFO interrupt status in transmit direction '1' a complete frame has been transmitted, the frame counter $F2$ has been incremented
3	B2 FIFO interrupt status in receive direction '1' a complete frame has been transmitted, the frame counter $F1$ has been incremented
4	D FIFO interrupt status in transmit direction '1' a complete frame was transmitted, the frame counter $F2$ has been incremented
5	D FIFO interrupt status in receive direction '1' a complete frame was transmitted, the frame counter $F1$ has been incremented
6	PCM FIFO interrupt status in transmit direction '1' a complete frame was transmitted, the frame counter $F2$ has been incremented
7	PCM FIFO interrupt status in receive direction '1' a complete frame was transmitted, the frame counter $F1$ has been incremented

☞ **Please note !**

The interrupts indicated in the INT_S1 register are frame interrupts which occur in HDLC mode. In transparent mode an interrupt can be generated on a regular basis. Interrupt frequency can be selected in the CON_HDLC register.

INT_S2	(read only)	0x11
Interrupt status		

Bits	Description
0	TE/NT state machine interrupt status '1' state of state machine changed
1	Timer interrupt status '1' timer is elapsed
2	Processing/non processing transition interrupt status '1' The HFC-S mini has changed from processing to non processing state.
3	GCI I-change interrupt '1' a different I-value on GCI was detected
4	Receiver ready (RxR) of monitor channel '1' 2 monitor bytes have been received
7..5	unused, '0'

☞ **Important !**

Reading the INT_S1 or INT_S2 register resets all active read interrupts in the INT_S1 or INT_S2 register respectively. New interrupts may occur during read. These interrupts are reported at the next read of INT_S1 or INT_S2.

All interrupt bits are reported regardless of the mask registers settings (INT_M1 and INT_M2). The mask registers settings only influence the interrupt output condition.

The interrupt output goes inactive during the read of INT_S1 or INT_S2. If interrupts occur during this read the interrupt line goes active immediately after the read is finished. So processors with level or transition triggered interrupt inputs can be connected.

INT_M1	**(write only)**	0x1A

Interrupt mask
For mask bits of this register a '1' enables and a '0' disables the interrupt. Reset clears all bits to '0'.

Bits	Description
0	interrupt mask for B1-channel in transmit direction
1	interrupt mask for B1-channel in receive direction
2	interrupt mask for B2-channel in transmit direction
3	interrupt mask for B2-channel in receive direction
4	interrupt mask for D-channel in transmit direction
5	interrupt mask for D-channel in receive direction
6	interrupt mask for PCM-channel in transmit direction
7	interrupt mask for PCM-channel in receive direction

INT_M2	**(write only)**	0x1B

Interrupt mask
For mask bits of this register a '1' enables and a '0' disables the interrupt. Reset clears all bits to '0'.

Bits	Description
0	interrupt mask for TE/NT state machine state change
1	interrupt mask for timer
2	interrupt mask for processing/non processing transition
3	interrupt mask for GCI I-change
4	interrupt mask for receiver ready (RxR) of monitor channel
5	unused, must be '0'
6	interrupt output is reversed
7	enable interrupt output

Bits	Description
HDLC_PAR [FIFO] (write only) 0xFB	

Bits	Description
2..0	Bit count for HDLC and transparent mode (number of bits to process) '000' process 8 bits (64 kbit/s) (reset default) '001' process 1 bit : : '111' process 7 bits (56 kbit/s)
5..3	Start bit for HDLC and transparent mode '000' start processing with bit 0 (reset default) : : '111' start processing with bit 7
6	FIFO loop '0' normal operation (reset default) '1' repeat current frame
7	Invert data enable/disable '0' normal read/write data (reset default) '1' invert data

☞ **Important !**

For normal B-channel operation, the HDLC_PAR register must be set to 0x00. To use 56 kbit/s restricted mode the HDLC_PAR register must be set to 0x07 for B-channels.

For D-channels the HDLC_PAR register must be set to 0x02.

CON_HDLC [FIFO]	(write only)	0xFA

Bits	Description
0	Inter frame fill '0' write HDLC flags 0x7E as inter frame fill (reset default) '1' write all '1's as inter frame fill (must be set for D-channel)
1	HDLC mode/transparent mode select '0' HDLC mode (reset default) '1' transparent mode select **If bits 3..1 are** '000' **the FIFO is disabled (reset default).**
3..2	Transparent mode interrupt frequency select '00' every 8 bytes '01' every 16 bytes '10' every 32 bytes '11' every 64 bytes **In HDLC mode, set this bitmap** $\neq 0$ **to enable the FIFO.**
4	must be '0'

7..5	Select data flow for selected FIFO
	B1-channel (FIFO0 and FIFO1):
	bit 5: '0' FIFO1 ← B1-S/T
	          '1' FIFO1 ← B1-PCM
	bit 6: '0' B1-S/T ← FIFO0
	          '1' B1-S/T ← B1-PCM
	bit 7: '0' B1-PCM ← FIFO0
	          '1' B1-PCM ← B1-S/T
	B2-channel (FIFO2 and FIFO3):
	bit 5: '0' FIFO3 ← B2-S/T
	          '1' FIFO3 ← B2-PCM
	bit 6: '0' B2-S/T ← FIFO2
	          '1' B2-S/T ← B2-PCM
	bit 7: '0' B2-PCM ← FIFO2
	          '1' B2-PCM ← B2-S/T
	D-channel and PCM (FIFO4 and FIFO5):
	bit 5: '0' FIFO5 ← D-S/T *
	          '1' FIFO5 ← AUX1
	bit 6: '0' D-S/T ← FIFO4
	          '1' D-S/T ← AUX1
	bit 7: '0' AUX1 ← FIFO4
	          '1' AUX1 ← D-S/T
	E-channel and PCM (FIFO6 and FIFO7):
	bit 5: '0' FIFO7 ← E-S/T
	          '1' FIFO7 ← AUX2
	bit 6: '0' E-S/T ← FIFO6
	          '1' E-S/T ← AUX2
	bit 7: '0' AUX2 ← FIFO6
	          '1' AUX2 ← E-S/T
	*: (not available if MST_MODE1[7] is set)
	CON_HDLC register bits[7:5] must be the same for corresponding receive and transmit FIFOs.

☞ **Please note !**

In any case the FIFO must be enabled to activate the data transmission selected
with bits 7 . . 5 of the CON_HDLC register.

☞ **Important !**

FIFO5 for the D-channel does not work properly if GCI mode is selected (bit 7 of
MST_MODE1 = '1'). In this case, the AUX2 receive time slot can be configured
to the receive time slot 3 which is related to FIFO 7 in this case for D-channel
receive (HDLC_PAR = 0x02 and CON_HDLC = 0x25).
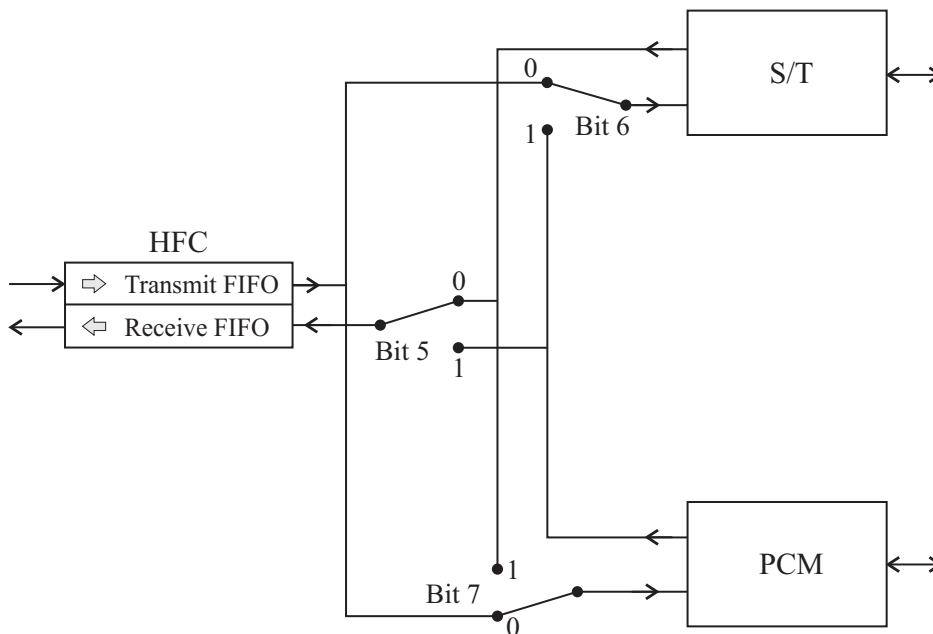
Figure 9: *Function of CON_HDLC register bits 7 . . 5*

CH_MASK [FIFO]	(write only)	0xF4
Bit value for not processed bits of a channel. All not processed bits of a channel are set to the value defined in this register.		

Bits	Description
7..0	Mask value

CHANNEL [FIFO]	(write only)	0xFC
Link selected FIFO to ISDN channel (only in Channel Select Mode, see F_MODE register)		

Bits	Description
2..0	Link FIFO to S/T channel '000' B1-transmit '001' B1-receive '010' B2-transmit '011' B2-receive '100' D-transmit '101' D-receive '110' invalid (E is receive only) '111' E-receive
7..3	unused, must be '0'

CHIP_ID	(read only)	0x16
Chip identification		

Bits	Description
3..0	unused, '0'
7..4	'0101' HFC-S mini

STATUS	(read only)	0x1C

Bits	Description
0	BUSY/NOBUSY status '1' the HFC-S mini is BUSY after initializing, reset FIFO, increment F or change FIFO '0' the HFC-S mini is not busy, all accesses are allowed **Note:** Accesses to FIFO registers are not allowed during busy period.
1	Processing/non processing status '1' the HFC-S mini is in processing phase (every $125\,\mu$s) '0' the HFC-S mini is not in processing phase
2	unused, '0'
3	AWAKE input signal
4	SYNC_I input signal
5	unused, '0'
6	an interrupt (with enabled mask bit) indicated in the INT_S2 register has occured
7	FRAME interrupt with enabled mask bit has occured (any FIFO interrupt) All masked B-, D- and PCM-channel interrupts are 'ored' (see register INT_S1)

Reading the STATUS register clears no bit.

TIME_SEL	(write only)	0x1C
Select interrupt frequency of timer interrupt		

Bits	Description
3..0	'0000' every $250\,\mu$s '0001' every $500\,\mu$s '0010' every 1 ms '0011' every 2 ms '0100' every 4 ms '0101' every 8 ms '0110' every 16 ms '0111' every 32 ms '1000' every 64 ms '1001' every 128 ms '1010' every 256 ms '1011' every 512 ms '1100' every 1024 ms '1101' every 2048 ms '1110' every 4096 ms '1111' every 8192 ms
7..4	unused, must be '0'

4.2 PCM/GCI/IOM2 bus section registers

4.2.1 Time slots for transmit direction

B1_SSL	**(write only)**	**0x20**

Bits	Description
4..0	select PCM/GCI/IOM2 bus transmission slot (0..31, 32..63, 64..95, 96..127, see MST_MODE2 register bits 5..4)
5	unused
6	select PCM/GCI/IOM2 bus data lines '0' STIO1 output '1' STIO2 output
7	select PCM/GCI/IOM2 bus data lines '0' STIO1 output '1' STIO2 output

B2_SSL	**(write only)**	**0x21**

Bits	Description
4..0	select PCM/GCI/IOM2 bus transmission slot (0..31, 32..63, 64..95, 96..127, see MST_MODE2 register bits 5..4)
5	unused
6	select PCM/GCI/IOM2 bus data lines '0' STIO1 output '1' STIO2 output
7	transmit channel enable for PCM/GCI/IOM2 bus '0' disable (reset default) '1' enable

AUX1_SSL	(write only)	0x22

Bits	Description
4..0	select PCM/GCI/IOM2 bus transmission slot (0..31, 32..63, 64..95, 96..127, see MST_MODE2 register bits 5..4)
5	unused
6	select PCM/GCI/IOM2 bus data lines '0' STIO1 output '1' STIO2 output
7	transmit channel enable for PCM/GCI/IOM2 bus '0' disable (reset default) '1' enable

AUX2_SSL	(write only)	0x23

Bits	Description
4..0	select PCM/GCI/IOM2 bus transmission slot (0..31, 32..63, 64..95, 96..127, see MST_MODE2 register bits 5..4)
5	unused
6	select PCM/GCI/IOM2 bus data lines '0' STIO1 output '1' STIO2 output
7	transmit channel enable for PCM/GCI/IOM2 bus '0' disable (reset default) '1' enable

☞ **Important !**

Enabling more than one channel on the same slot causes undefined output data.

4.2.2 Time slots for receive direction

B1_RSL	**(write only)**	0x24

Bits	Description
4..0	select PCM/GCI/IOM2 bus receive slot (0..31, 32..63, 64..95,96..127, see MST_MODE2 register bits 5..4)
5	unused
6	select PCM/GCI/IOM2 bus data lines '0' STIO2 is input '1' STIO1 is input
7	receive channel enable for PCM/GCI/IOM2 bus '0' disable (reset default) '1' enable

B2_RSL	**(write only)**	0x25

Bits	Description
4..0	select PCM/GCI/IOM2 bus receive slot (0..31, 32..63, 64..95,96..127, see MST_MODE2 register bits 5..4)
5	unused
6	select PCM/GCI/IOM2 bus data lines '0' STIO2 is input '1' STIO1 is input
7	receive channel enable for PCM/GCI/IOM2 bus '0' disable (reset default) '1' enable

AUX1_RSL	(write only)	0x26

Bits	Description
4..0	select PCM/GCI/IOM2 bus receive slot (0..31, 32..63, 64..95,96..127, see MST_MODE2 register bits 5..4)
5	unused
6	select PCM/GCI/IOM2 bus data lines '0' STIO2 is input '1' STIO1 is input
7	receive channel enable for PCM/GCI/IOM2 bus '0' disable (reset default) '1' enable

AUX2_RSL	(write only)	0x27

Bits	Description
4..0	select PCM/GCI/IOM2 bus receive slot (0..31, 32..63, 64..95,96..127, see MST_MODE2 register bits 5..4)
5	unused
6	select PCM/GCI/IOM2 bus data lines '0' STIO2 is input '1' STIO1 is input
7	receive channel enable for PCM/GCI/IOM2 bus '0' disable (reset default) '1' enable

4.2.3 PCM data registers

B1_D	(read / write)	0x2C

Bits	Description
7..0	read/write data registers for selected time slot data

B2_D	(read / write)	0x2D

Bits	Description
7..0	read/write data registers for selected time slot data

AUX1_D	(read / write)	0x2E

Bits	Description
7..0	read/write data registers for selected time slot data

AUX2_D	(read / write)	0x2F

Bits	Description
7..0	read/write data registers for selected time slot data

All PCM data registers are read / written automatically by the HDLC FIFO controller (HFC) or PCM controller and need not be accessed by the user. To read / write data the FIFO registers should be used.

> ☞ **Please note !**
>
> **Auxiliary channel handling**
>
> To support an automatic CODEC to CODEC connection AUX1_D and AUX2_D can be set into mirror mode. In this case, if the data registers AUX1_D and AUX2_D are not overwritten, the transmisson slots AUX1_SSL and AUX2_SSL mirror the data received in AUX1_RSL and AUX2_RSL slots. This is useful for an internal connection between two CODECs. This mirroring is enabled by setting bits 1 . . 0 in MST_MODE1 register.

4.2.4 Configuration and status registers

MST_MODE0	(write only)	0x14

Bits	Description
0	PCM/GCI/IOM2 bus mode '0' slave (reset default) (C4IO and F0IO are inputs) '1' master (C4IO and F0IO are outputs)
1	polarity of C4IO and C2O clock '0' F0IO is sampled on negative clock transition '1' F0IO is sampled on positive clock transition
2	polarity of F0IO signal '0' F0IO positive pulse '1' F0IO negative pulse
3	duration of F0IO signal '0' F0IO active for one C4IO clock (244 ns at 2 Mbit/s) (reset default) '1' F0IO active for two C4IO clocks (488 ns at 2 Mbit/s)
5..4	time slot for CODEC-A signal F1_A '00' B1 receive slot '01' B2 receive slot '10' AUX1 receive slot '11' signal C2O. pin F1_A (C2O is 1/2 C4IO)
7..6	time slot for CODEC-B signal F1_B '00' B1 receive slot '01' B2 receive slot '10' AUX1 receive slot '11' AUX2 receive slot

The pulse shape and polarity of the CODEC signals F1_A and F1_B is the same as the pulse shape of the F0IO signal. The polarity of C2O can be changed by bit 1.

/RES clears registers MST_MODE0, MST_MODE1 and MST_MODE2 to all '0's.

☞ **Important !**

There is always a clock signal required at the pins C4IO and F0IO. If no external clock source is connected to these pins (PCM slave mode), bit 0 of MST_MODE0 must be set for PCM master mode.

MST_MODE1	(write only)	0x15

Bits	Description
0	enable/disable AUX1 channel mirroring '0' disable AUX1 channel data mirroring (reset default) '1' mirror AUX1 receive to AUX1 transmit
1	enable/disable AUX2 channel mirroring '0' disable AUX2 channel data mirroring (reset default) '1' mirror AUX2 receive to AUX2 transmit
3..2	DPLL adjust speed '00' C4IO clock is adjusted in the last time slot of MST frame 4 times by one half clock cycle of CLKI '01' C4IO clock is adjusted in the last time slot of MST frame 3 times by one half clock cycle of CLKI '10' C4IO clock is adjusted in the last time slot of MST frame twice by one half clock cycle of CLKI '11' C4IO clock is adjusted in the last time slot of MST frame once by one half clock cycle of CLKI
5..4	PCM data rate '00' 2 MBit/s (PCM30) '01' 4 MBit/s (PCM64), long F0IO signal required ($> 170\,ns$, bit 3 of MST_MODE0 must be set) '10' 8 MBit/s (PCM128), only in PCM slave mode and with long F0IO signal ($> 170\,ns$, bit 3 of MST_MODE0 must be set) '11' unused
6	MST test loop When set MST output data is looped to the MST inputs.
7	enable GCI/IOM2 write slots '0' disable PCM/GCI/IOM2 write slots; slot #2 and slot #3 may be used for normal data '1' enables slot #2 and slot #3 as master, D- and C/I-channel

☞ **Important !**

As the F0IO pulse must be 170 ns at least in all cases where the S/T interface is used, the following restrictions must be fulfilled:

- In master mode bit 3 of MST_MODE0 must be '1' at 4 Mbit/s. A data rate of 8 Mbit/s is not available.

- In slave mode any data rate of MST_MODE1[4..5] is selectable if F0IO $>$ 170 ns (bit 3 of MST_MODE0 = '1').

MST_MODE2	(write only)	0x16

Bits	Description
0	'1' generate frame signal for OKI^{TM} CODECs on F1_A
1	'1' generate frame signal for OKI^{TM} CODECs on F1_B
2	select PCM DPLL synchronization source '0' S/T receive frame (only in TE mode and valid frame synchronization (F6 or F7) a synchronization signal is generated) '1' SYNC_I input 8 kHz
3	select SYNC_O output '0' S/T receive frame 8 kHz (only in TE mode and valid frame synchronization (F6 or F7) a synchronization signal is generated) '1' SYNC_I is connected to SYNC_O
5..4	PCM/GCI/IOM2 slot select for higher data rates '00' slots 31..0 accessable '01' slots 63..32 accessable '10' slots 95..64 accessable '11' slots 127..96 accessable
6	This bit is only valid if bit 7 is set. '0' PCM frame time is reduced as selected by bits 3..2 of the MST_MODE1 register '1' PCM frame time is increased as selected by bits 3..2 of the MST_MODE1 register
7	'0' normal operation '1' enable PCM PLL adjust according to bit 6 if no synchronization source is available. This is used to synchronize by software.

F0_CNT_L	(read only)	0x18
F0IO pulse count		

Bits	Description
7..0	16 bit 125 μs time counter (low byte)

F0_CNT_H	(read only)	0x19
F0IO pulse count		

Bits	Description
7..0	16 bit 125 μs time counter (high byte)

C/I	(read / write)	0x28
C/I channel data of GCI		

Bits	Description
3..0	on read: indication on write: command
7..4	unused

TRxR	(read only)	0x29

Bits	Description
0	'1' Monitor receiver ready (2 monitor bytes have been received)
1	'1' Monitor transmitter ready Writing on MON2_D starts transmisssion and resets this bit.
5..2	reserved
6	value of STIO2 input pin
7	value of STIO1 input pin

MON1_D	(read / write)	0x2A

Bits	Description
7..0	first monitor byte

MON2_D	(read / write)	0x2B

Bits	Description
7..0	second monitor byte

4.3   S/T section registers

ST_RD_STA	(read only)	0x30
S/T interface state register		

Bits	Description
3..0	binary value of actual state (NT: Gx, TE: Fx)
4	Frame synchronization ('1' = synchronized)
5	'1' timer T2 expired (NT mode only)
6	'1' receiving INFO0
7	'1' in NT mode: transition from G2 to G3 is allowed.

ST_WR_STA	(write only)	0x30

S/T interface state register

Bits	Description
3..0	Set new state xxxx (bit 4 must also be set to load the state).
4	'1' loads the prepared state (bit 3..0) and stops the state machine.This bit needs to be set for a minimum period of 5.21 μs and must be cleared by software (reset default). '0' enables the state machine. After writing an invalid state the state machine goes to deactivated state (G1, F2)
6..5	'00' no operation '01' no operation '10' start deactivation '11' start activation The bits are automatically cleared after activation/deactivation.
7	'0' no operation '1' in NT mode: allows transition from G2 to G3. This bit is automatically cleared after the transition.

☞ **Important !**

The S/T state machine is stuck to '0' after a reset.

In this state the HFC-S mini sends no signal on the S/T line and it is not possible to activate it by incoming INFOx.

Writing a '0' to bit 4 of the ST_WR_STA register restarts the state machine.

NT mode: The NT state machine does not change automatically from G2 to G3 if the TE side sends INFO3 frames. This transition must be activated each time by bit 7 of the ST_WR_STA register or by setting bit 0 of the SCTRL_E register.

SCTRL	(write only)	0x31

Bits	Description
0	'0' B1 send data disabled (permanent '1' sent in activated states, reset default) '1' B1 data enabled
1	'0' B2 send data disabled (permanent '1' sent in activated states, reset default) '1' B2 data enabled
2	S/T interface mode '0' TE mode (reset default) '1' NT mode
3	D-channel priority '0' high priority 8/9 (reset default) '1' low priority 10/11
4	S/Q bit transmission '0' S/Q bit disable (reset default) '1' S/Q bit and multiframe enable
5	'0' normal operation (reset default) '1' send 96 kHz transmit test signal (alternating zeros)
6	/TX1_LO and /TX2_LO line setup This bit must be configured depending on the used S/T module and circuitry to match the 400 ms pulse mask test. '0' capacitive line mode (reset default) '1' non capacitive line mode
7	Power down '0' normal operation, oscillator active (reset default) '1' power down, oscillator stopped Oscillator is restarted when AWAKE input becomes '1' or on any write access to the HFC-S mini.

SCTRL_E	(write only)	0x32

Bits	Description
0	force G2 to G3 automatic transition from G2 to G3 without setting bit 7 of ST_WR_STA register
1	must be '0'
2	D reset '0' normal operation (reset default) '1' D bits are forced to '1'
3	D_U enable '0' normal operation (reset default) '1' D-channel is always send enabled regardless of E receive bit
4	force E = '0' (NT mode) '0' normal operation (reset default) '1' E-bit send is forced to '0'
6..5	must be '0'
7	'1' swap B1- and B2-channels in the S/T interface

SCTRL_R	(write only)	0x33

Bits	Description
0	B1-channel receive enable
1	B2-channel receive enable '0' B receive bits are forced to '1' '1' normal operation
7..2	unused

SQ_REC	(read only)	0x34

Bits	Description
3..0	TE mode: S bits (bit 3 = S1, bit 2 = S2, bit 1 = S3, bit 0 = S4) NT mode: Q bits (bit 3 = Q1, bit 2 = Q2, bit 1 = Q3, bit 0 = Q4)
4	'1' a complete S or Q multiframe has been received Reading SQ_REC clears this bit.
6..5	not defined
7	'1' ready to send a new S or Q multiframe Writing to SQ_SEND clears this bit.

SQ_SEND	(write only)	0x34

Bits	Description
3..0	TE mode: Q bits (bit 3 = Q1, bit 2 = Q2, bit 1 = Q3, bit 0 = Q4) NT mode: S bits (bit 3 = S1, bit 2 = S2, bit 1 = S3, bit 0 = S4)
7..4	not defined

CLKDEL	(write only)	0x37

Bits	Description
3..0	TE: 4 bit delay value to adjust the 2 bit time delay between receive and transmit direction. The delay of the external S/T interface circuit can be compensated. The lower the value the smaller the delay between receive and transmit direction. NT: Data sample point. The lower the value the earlier the input data is sampled. The step size is 163 ns.
6..4	NT mode only early edge input data shaping Low pass characteristic of extended bus configurations can be compensated. The lower the value the earlier input data pulse is sampled. No compensation means a value of 6 ('110'). The step size is 163 ns.
7	unused

☞ **Please note !**

The register CLKDEL is not initialized with a '0' after reset. The register should be initialized as follows before activating the TE / NT state machine:

TE mode: 0x0D . . 0x0F (0x0F for S/T interface circuitry shown on page 75)

NT mode: 0x6C

4.3.1 S/T data registers

B1_REC	(read only)	0x3C

Bits	Description
7..0	B1-channel receive register

B1_SEND	(write only)	0x3C
Bits	**Description**	
7..0	B1-channel transmit register	

B2_REC	(read only)	0x3D
Bits	**Description**	
7..0	B2-channel receive register	

B2_SEND	(write only)	0x3D
Bits	**Description**	
7..0	B2-channel transmit register	

D_REC	(read only)	0x3E
Bits	**Description**	
7..0	D-channel receive register	

D_SEND	(write only)	0x3E

Bits	Description
7..0	D-channel transmit register

E_REC	(read only)	0x3F

Bits	Description
7..0	E-channel receive register

All S/T data registers are read / written automatically by the HDLC FIFO controller (HFC) or PCM controller and need not be accessed by the user. To read / write data the FIFO registers should be used.

5   Electrical characteristics

Absolute maximum ratings

Parameter	Symbol	Min.	Max.
Power supply	V_{DD}	$-0.3\,\text{V}$	$+7.0\,\text{V}$
Input voltage	V_I	$-0.3\,\text{V}$	$V_{CC}+0.3\,\text{V}$
Output voltage	V_O	$-0.3\,\text{V}$	$V_{CC}+0.3\,\text{V}$
Operating temperature	T_{opr}	$-10\,^\circ\text{C}$	$+85\,^\circ\text{C}$
Storage temperature	T_{stg}	$-40\,^\circ\text{C}$	$+125\,^\circ\text{C}$

Recommended operating conditions

Parameter	Symbol	Min.	Typ.	Max	Conditions
Power supply	V_{DD}	$3.0\,\text{V}$	$3.3\,\text{V}$	$3.6\,\text{V}$	$V_{DD}=3.3\,\text{V}$
		$4.75\,\text{V}$	$5\,\text{V}$	$5.25\,\text{V}$	$V_{DD}=5\,\text{V}$
Operating temperature	T_{opr}	$0\,^\circ\text{C}$		$+70\,^\circ\text{C}$	
Supply current					$f_{CLK}=24.576\,\text{MHz}$
Normal	I_{DD}		$12\,\text{mA}$		$V_{DD}=3.3\,\text{V}$, running oscillator
			$24\,\text{mA}$		$V_{DD}=5\,\text{V}$, running oscillator
Power down				$1\,\text{mA}$	$V_{DD}=3.3\,\text{V}$, oscillator stopped
				$2\,\text{mA}$	$V_{DD}=5\,\text{V}$, oscillator stopped

Electrical characteristics for 3.3 V power supply (TTL level)

$$V_{DD} = 3.0\,\text{V}\ to\ 3.6\,\text{V}, T_{opr} = 0\,°\text{C}\ to\ +70\,°\text{C}$$

Parameter	Symbol	Min.	Typ.	Max
Low input voltage	V_{IL}			0.5 V
High input voltage	V_{IH}	1.5 V		
Low output voltage	V_{OL}			0.4 V
High output voltage	V_{OH}	2.4 V		V_{DD}
Schmitt trigger, positive-going threshold	VT+			1.3 V
Schmitt trigger, negative-going threshold	VT-	0.5 V		

Electrical characteristics for 3.3 V power supply (CMOS level)

$$V_{DD} = 3.0\,\text{V}\ to\ 3.6\,\text{V}, T_{opr} = 0\,°\text{C}\ to\ +70\,°\text{C}$$

Parameter	Symbol	Min.	Typ.	Max
Low input voltage	V_{IL}			1.0 V
High input voltage	V_{IH}	2.0 V		
Low output voltage	V_{OL}			0.4 V
High output voltage	V_{OH}	2.4 V		V_{DD}
Schmitt trigger, positive-going threshold	VT+			2.0 V
Schmitt trigger, negative-going threshold	VT-	1.0 V		

Electrical characteristics for 5 V power supply (TTL level)

$$V_{DD} = 4.75\,\text{V}\ to\ 5.25\,\text{V}, T_{opr} = 0\,°\text{C}\ to\ +70\,°\text{C}$$

Parameter	Symbol	Min.	Typ.	Max
Low input voltage	V_{IL}			0.8 V
High input voltage	V_{IH}	2.0 V		
Low output voltage	V_{OL}			0.4 V
High output voltage	V_{OH}	2.4 V		
Schmitt trigger, positive-going threshold	VT+			2.0 V
Schmitt trigger, negative-going threshold	VT-	0.8 V		

Electrical characteristics for 5 V power supply (CMOS level)

$$V_{DD} = 4.75\,\text{V}\ to\ 5.25\,\text{V}, T_{opr} = 0\,°\text{C}\ to\ +70\,°\text{C}$$

Parameter	Symbol	Min.	Typ.	Max
Low input voltage	V_{IL}			1.5 V
High input voltage	V_{IH}	3.5 V		
Low output voltage	V_{OL}			0.4 V
High output voltage	V_{OH}	2.4 V		
Schmitt trigger, positive-going threshold	VT+			4.0 V
Schmitt trigger, negative-going threshold	VT-	1.0 V		

Table 7: *I/O characteristics*

Input	Interface level
/RD	CMOS
/WR	CMOS
/CS	CMOS, internal pull-up resistor
ALE	CMOS, internal pull-up resistor
A0	CMOS
D7 . . D0	CMOS
CLKI	CMOS
AWAKE	CMOS
C4IO	TTL Schmitt Trigger, internal pull-up resistor
F0IO	CMOS, internal pull-up resistor
STIO1, STIO2	CMOS, internal pull-up resistor
/RES	CMOS Schmitt Trigger, internal pull-up resistor

Table 8: *Driver Capability*

Output	Low 0.4 V	High $V_{DD} - 0.8$ V
D7 . . D0	4 mA	2 mA
C4IO	8 mA	4 mA
F0IO	8 mA	4 mA
STIO1, STIO2	8 mA	4 mA
F1_A, F1_B	4 mA	2 mA
/INT	4 mA	

6 Timing Characteristics

6.1 Microprocessor access

6.1.1 Register read access in mode 2 (Motorola) and mode 3 (Intel)
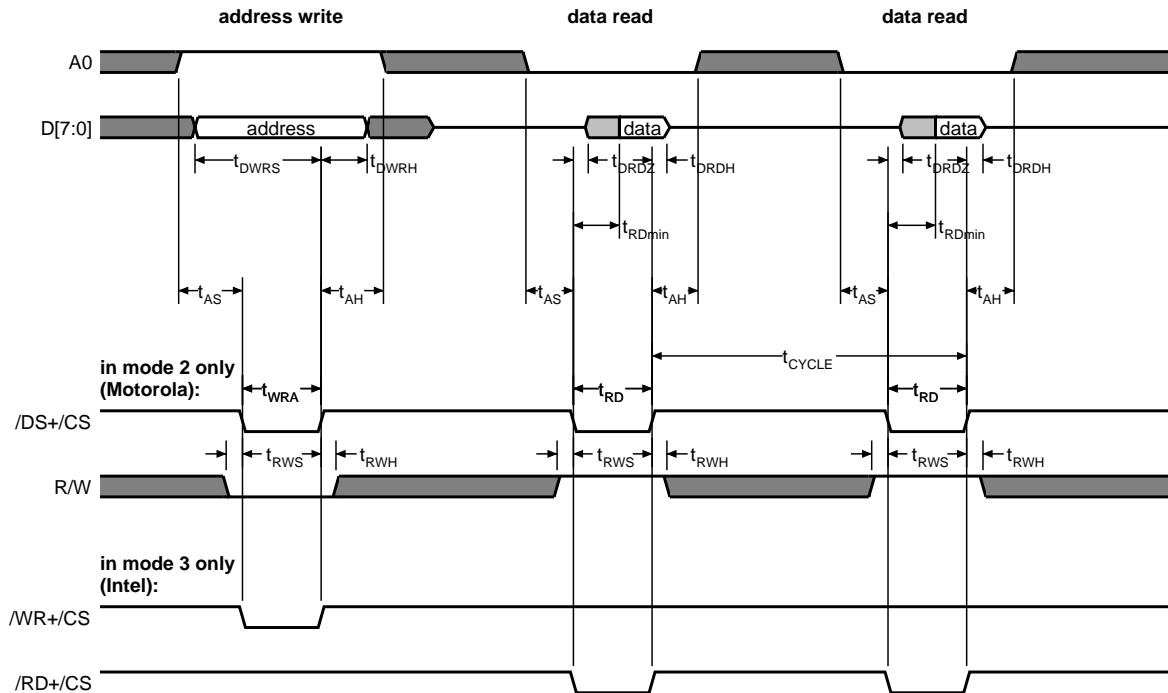
Figure 10: *Read access in mode 2 (Motorola) and mode 3 (Intel)*

t_{CLKI} is the CLKI clock period which is normally 40.69 ns (24.576 MHz system clock).

☞ **Important !**

All read accesses with register address bit D[7] = '1' (registers FIF_DATA, FIF_DATA_NOINC and RAM_DATA) have a cycle time

$$t_{CYCLE} \geq 6 \cdot t_{CLKI}$$

between two consecutive ⌐ of t_{RD}.

☞ **Hint !**

If the same register as in the last register read / write access is accessed the register address write is not required.

Table 9: *Symbols of read accesses in Figure 10*

Symbol	min / ns	max / ns	Characteristic
t_{AS}	10		A0 valid to /DS+/CS (/WR+/CS) ⌐ setup time
t_{AH}	10		Address hold time after /DS+/CS (/WR+/CS) ⌐
t_{WRA}	20		Write time for address write
t_{DWRS}	30		Write data setup time to /DS+/CS (/WR+/CS) ⌐
t_{DWRH}	10		Write data hold time from /DS+/CS (/WR+/CS) ⌐
t_{RD}			Read time:
	$2 \cdot t_{CLKI}$		D[7] = '0' (address range 0 … 0x7F: normal register access)
	20		D[7,6] = '10' (address range 0x80 … 0xBF: FIFO data access)
	$6 \cdot t_{CLKI}$		D[7,6] = '11' (address range 0xC0 … 0xFF: direct internal RAM access) *
t_{CYCLE}			/DS+/CS (/RD+/CS) ⌐ to next end of data access
			D[7] = '0' (address range 0 … 0x7F: normal register access)
	$6 \cdot t_{CLKI}$		D[7,6] = '10' (address range 0x80 … 0xBF: FIFO data access)
	$6 \cdot t_{CLKI}$		D[7,6] = '11' (address range 0xC0 … 0xFF: direct internal RAM access) *
t_{DRDZ}	3		/DS+/CS (/RD+/CS) ⌐ to data buffer turn on time
t_{DRDH}	2	15	/DS+/CS (/RD+/CS) ⌐ to data buffer turn off time
t_{RWS}	2		R/W setup time to /DS+/CS ⌐
t_{RWH}	2		R/W hold time after /DS+/CS ⌐

(*: Normally this time needs not to be matched because a direct RAM access is not needed.)

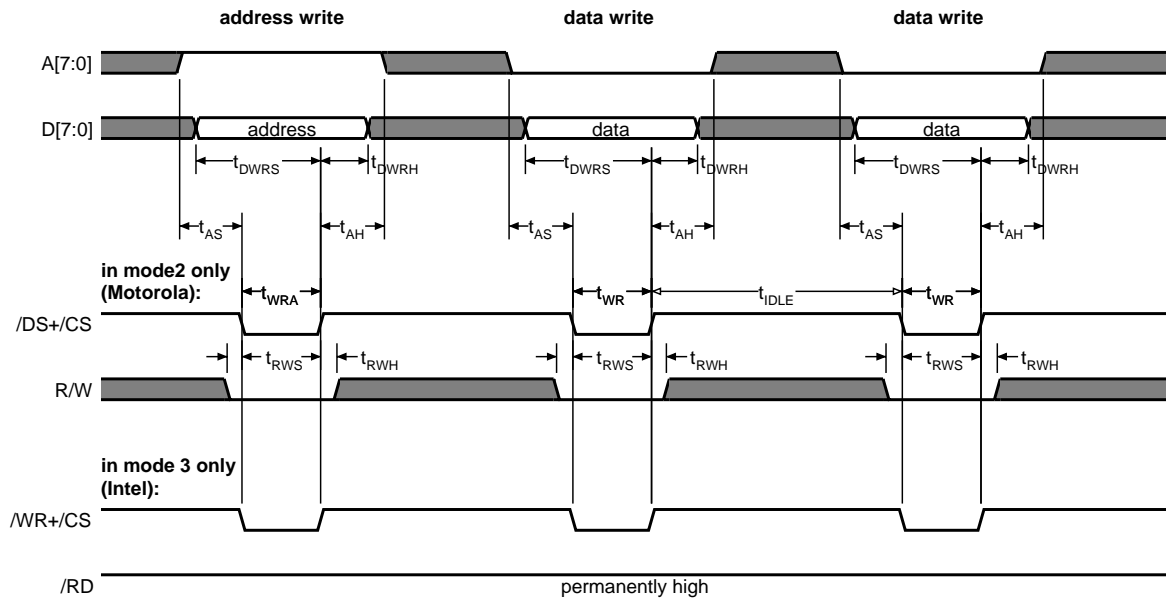## 6.1.2 Register write access in mode 2 (Motorola) and mode 3 (Intel)

Figure 11: *Write access in mode 2 (Motorola) and mode 3 (Intel)*

Table 10: *Symbols of write accesses in Figure 11*

Symbol	min / ns	max / ns	Characteristic
t_{AS}	10		A0 valid to /DS+/CS (/WR+/CS) $\_\Gamma$ setup time
t_{AH}	10		Address hold time after /DS+/CS (/WR+/CS) $\_\Gamma$
t_{WRA}	20		Write time for address write
t_{DWRS}	20		Write data setup time to /DS+/CS (/WR+/CS) $\_\Gamma$
t_{DWRH}	10		Write data hold time from /DS+/CS (/WR+/CS) $\_\Gamma$
t_{WR}	20		Write time
t_{IDLE}	$5 \cdot t_{CLKI}$		/DS+/CS (/WR+/CS) high time between two data accesses
t_{RWS}	2		R/W setup time to /DS+/CS $\_\_\_$
t_{RWH}	2		R/W hold time after /DS+/CS $\_\Gamma$

t_{CLKI} is the CLKI clock period which is normally 40.69 ns (24.576 MHz system clock).

☞ **Important !**

All write accesses with register address bit D[7] = '1' (registers FIF_DATA, FIF_DATA_NOINC, RAM_DATA, CH_MASK, CON_HDLC, HDLC_PAR and CHANNEL) have a idle time

$$t_{IDLE} \geq 5 \cdot t_{CLKI}$$

between ⌐ of t_{WR} and the next ⌐ of t_{WR}.

☞ **Hint !**

If the same register as in the last register read / write access is accessed, the register address write is not required.
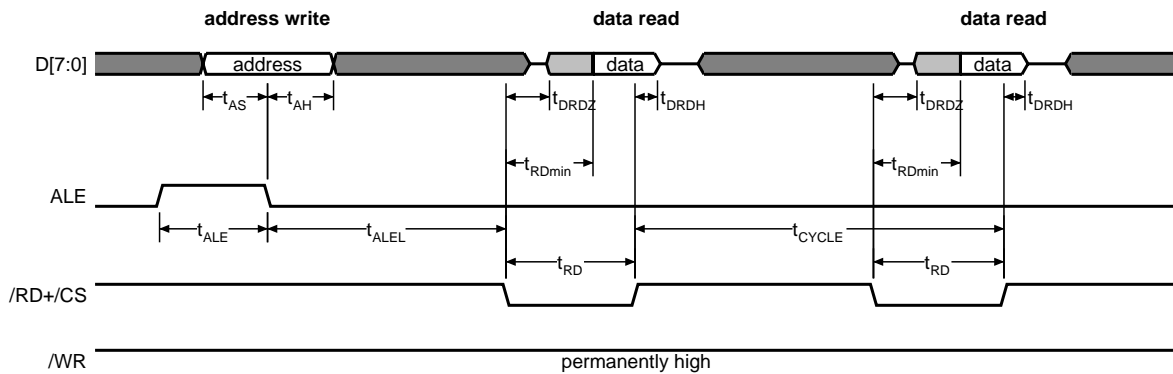
6.1.3 Register read access in mode 4 (Intel, multiplexed)

Figure 12: *Read access in mode 4 (Intel, multiplexed)*

Table 11: *Symbols of read accesses in Figure 12*

Symbol	min / ns	max / ns	Characteristic
t_{ALE}	10		Address latch time
t_{ALEL}	0		ALE ⌐ to /RD+/CS ⌐
t_{AS}	10		Address valid to ALE ⌐ setup time
t_{AH}	10		Address hold time after ALE ⌐
t_{DRDZ}	3		/RD+/CS ⌐ to data buffer turn on time
t_{DRDH}	2	15	/RD+/CS ⌐ to data buffer turn off time
t_{RD}			Read time:
	$2 \cdot t_{CLKI}$		D[7] = '0' (address range 0 ... 0x7F: normal register access)
	20		D[7,6] = '10' (address range 0x80 ... 0xBF: FIFO data access)
	$5 \cdot t_{CLKI}$		D[7,6] = '11' (address range 0xC0 ... 0xFF: direct internal RAM access) *
t_{CYCLE}			Cycle time between two consecutive /RD+/CS ⌐
			D[7] = '0' (address range 0 ... 0x7F: normal register access)
	$6 \cdot t_{CLKI}$		D[7,6] = '10' (address range 0x80 ... 0xBF: FIFO data access)
	$6 \cdot t_{CLKI}$		D[7,6] = '11' (address range 0xC0 ... 0xFF: direct internal RAM access) *

(*: Normally this time needs not to be matched because a direct RAM access is not needed.)

t_{CLKI} is the CLKI clock period which is normally 40.69 ns (24.576 MHz system clock).

> ☞ **Important !**
>
> A0 must be '0' during the whole register read cycle. It should be connected to GND.

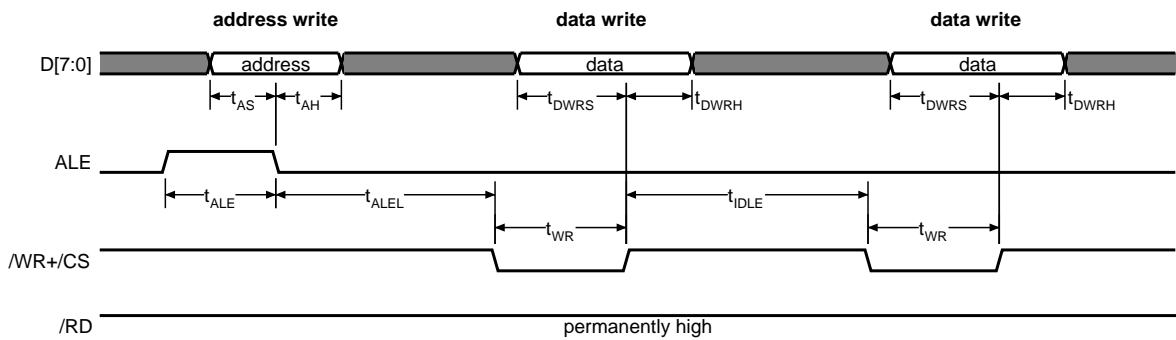### 6.1.4 Register write access in mode 4 (Intel, multiplexed)

Figure 13: *Write access in mode 4 (Intel, multiplexed)*

Table 12: *Symbols of write accesses in Figure 13*

Symbol	min / ns	max / ns	Characteristic
t_{ALE}	10		Address latch time
t_{ALEL}	0		ALE ⌐ to /WR+/CS ⌐
t_{AS}	10		Address valid to ALE ⌐ setup time
t_{AH}	10		Address hold time after /WR+/CS ⌐
t_{DWRS}	20		Write data setup time to /WR+/CS ⌐
t_{DWRH}	10		Write data hold time from /WR+/CS ⌐
t_{WR}	20		Write time
t_{IDLE}			/WR+/CS high time
			D[7] = '0' (address range 0 … 0x7F: normal register access)
	$5 \cdot t_{CLKI}$		D[7,6] = '10' (address range 0x80 … 0xBF: FIFO data access)
	$5 \cdot t_{CLKI}$		D[7,6] = '11' (address range 0xC0 … 0xFF: direct internal RAM access) *

(*: Normally this time needs not to be matched because a direct RAM access is not needed.)

t_{CLKI} is the CLKl clock period which is normally 40.69 ns (24.576 MHz system clock).

☞ **Important !**

A0 must be '0' during the whole register read cycle. It should be connected to GND.

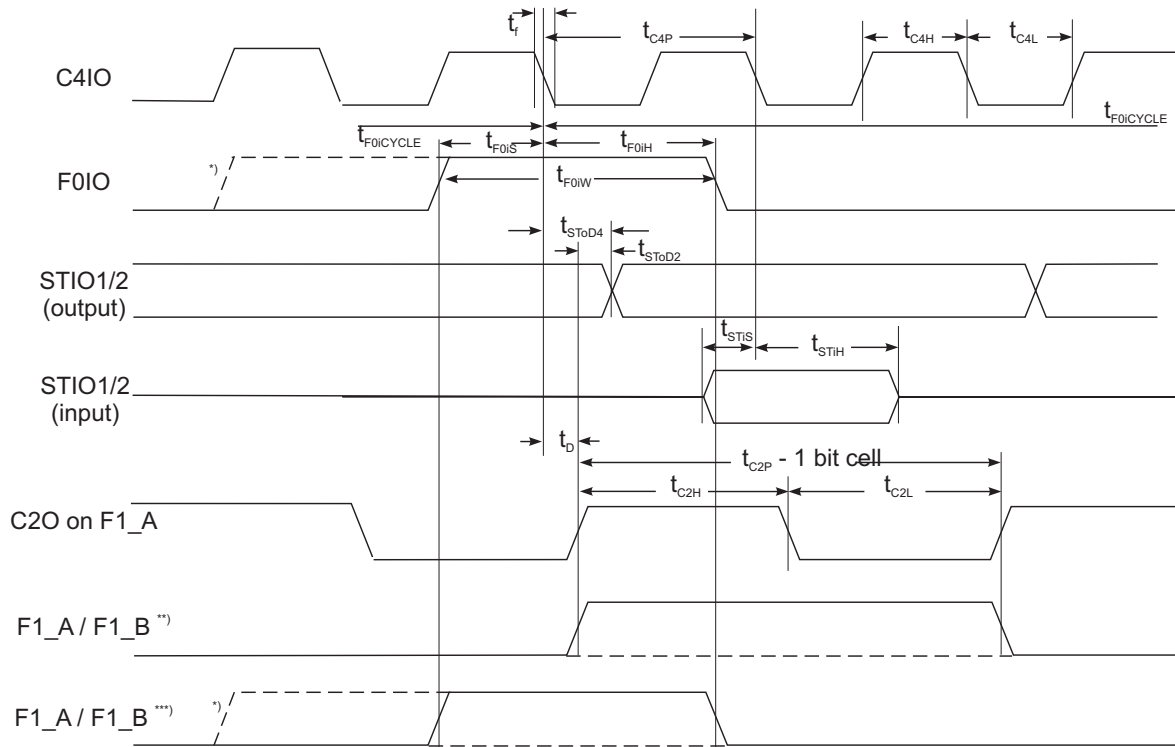## 6.2 PCM/GCI/IOM2 timing

Figure 14: *PCM / GCI / IOM2 timing*

*) F0IO starts one C4IO clock earlier if bit 3 in MST_MODE0 register is set. If this bit is set F0IO is also awaited one C4IO clock cycle earlier.

**) If bit 0 (or bit 1) of the MST_MODE2 register is set to '1' a frame signal for OKI^{TM} CODECs is generated on F1_A (or F1_B). The C2O clock on F1_A is not available if bit 0 of the MST_MODE2 register is set.

***) If bit 0 (or bit 1) of the MST_MODE2 register is cleared to '0' F1_A (or F1_B) is a CODEC enable signal with the same pulse shape and timing as the F0IO signal. If bits 5 . . 4 of MST_MODE0 are '11' F1_A is C2O clock.

6.2.1 Master mode

To configure the HFC-S mini as PCM / GCI / IOM2 bus master bit 0 of the MST_MODE0 register must be set. In this case C4IO and F0IO are outputs. The PCM bit rate is configured by bits 5..4 of the MST_MODE1 register.

Table 13: *PCM timing values in master mode*

Symbol	Characteristics		Min.	Typ.	Max.
t_C	for 2 Mb/s (PCM30)			122.07 ns	
	for 4 Mb/s (PCM64)			61.035 ns	
	for 8 Mb/s (PCM128)			30.518 ns	
t_{C4P}	Clock C4IO period [1] , [2]		$2t_C - 26\,\text{ns}$	$2t_C$	$2t_C + 26\,\text{ns}$
t_{C4H}	Clock C4IO High Width [1] , [2]		$t_C - 26\,\text{ns}$	t_C	$t_C + 26\,\text{ns}$
t_{C4L}	Clock C4IO Low Width [1] , [2]		$t_C - 26\,\text{ns}$	t_C	$t_C + 26\,\text{ns}$
t_{C2P}	Clock C2O Period		$4t_C - 52\,\text{ns}$	$4t_C$	$4t_C + 52\,\text{ns}$
t_{C2H}	Clock C2O High Width		$2t_C - 26\,\text{ns}$	$2t_C$	$2t_C + 26\,\text{ns}$
t_{C2L}	Clock C2O Low Width		$2t_C - 26\,\text{ns}$	$2t_C$	$2t_C + 26\,\text{ns}$
t_{F0iW}	F0IO Width	Short F0IO [3]	$2t_C - 26\,\text{ns}$	$2t_C$	$2t_C + 6\,\text{ns}$
		Long F0IO [3]	$4t_C - 26\,\text{ns}$	$4t_C$	$4t_C + 6\,\text{ns}$
t_{SToD2}	STIO1/2 output delay fom C2O ⌐			15 ns	30 ns
t_{SToD4}	STIO1/2 output delay fom C4IO ⌐			10 ns	25 ns
$t_{F0iCYCLE}$	F0IO Cycle Time 1 half clock adjust		$124.975\,\mu\text{s}$	$125.000\,\mu\text{s}$	$125.025\,\mu\text{s}$
	2 half clocks adjust		$124.950\,\mu\text{s}$	$125.000\,\mu\text{s}$	$125.050\,\mu\text{s}$
	3 half clocks adjust		$124.925\,\mu\text{s}$	$125.000\,\mu\text{s}$	$125.075\,\mu\text{s}$
	4 half clocks adjust		$124.900\,\mu\text{s}$	$125.000\,\mu\text{s}$	$125.100\,\mu\text{s}$

[1]: Time depends on accuracy of CLKI frequency. Because of clock adjustment in the 31st time slot these are the worst case timings when C4IO is adjusted.

[2]: In 8 MBit/s mode the duty cycle of C4IO is $\frac{1}{3}/\frac{2}{3}$.

[3]: 170 ns is the minimum value of F0IO for S/T data synchronization. Smaller values are only allowed if the S/T interface is not used.

All specifications are for $f_{CLK} = 24.576\,\text{MHz}$.

6.2.2 Slave mode

To configure the HFC-S mini as PCM / GCI / IOM2 bus slave bit 0 of the MST_MODE0 register must be cleared. In this case C4IO and F0IO are inputs.

Table 14: *PCM timing values in slave mode*

Symbol	Characteristics	Min.	Max.
t_C	for 2 Mb/s (PCM30)		122.07 ns
	for 4 Mb/s (PCM64)		61.035 ns
	for 8 Mb/s (PCM128)		30.518 ns
t_{C4P}	Clock C4IO period *		$2t_C$
t_{C4H}	Clock C4IO High Width	20 ns	
t_{C4L}	Clock C4IO Low Width	20 ns	
t_{C2P}	Clock C2O Period		$4t_C$
t_{C2H}	Clock C2O High Width		$2t_C$
t_{C2L}	Clock C2O Low Width		$2t_C$
t_{F0iS}	F0IO Setup Time to C4IO ⌐	20 ns	
t_{F0iH}	F0IO Hold Time after C4IO ⌐	20 ns	
t_{F0iW}	F0IO Width	170 ns	
t_{STiS}	STIO2 Setup Time	20 ns	
t_{STiH}	STIO2 Hold Time	20 ns	

*: If the S/T interface is activated, the frequency must be stable to $\pm 10^{-4}$.

All specifications are for $f_{CLK} = 24.576\,\text{MHz}$.

7 External circuitries

7.1 S/T interface circuitry

In order to comply to the physical requirements of ITU-T I.430 recommendation and considering the national requirements concerning overvoltage protection and electromagnetic compatibility (EMC), the HFC-S mini needs some additional circuitry, which are shown in this section.

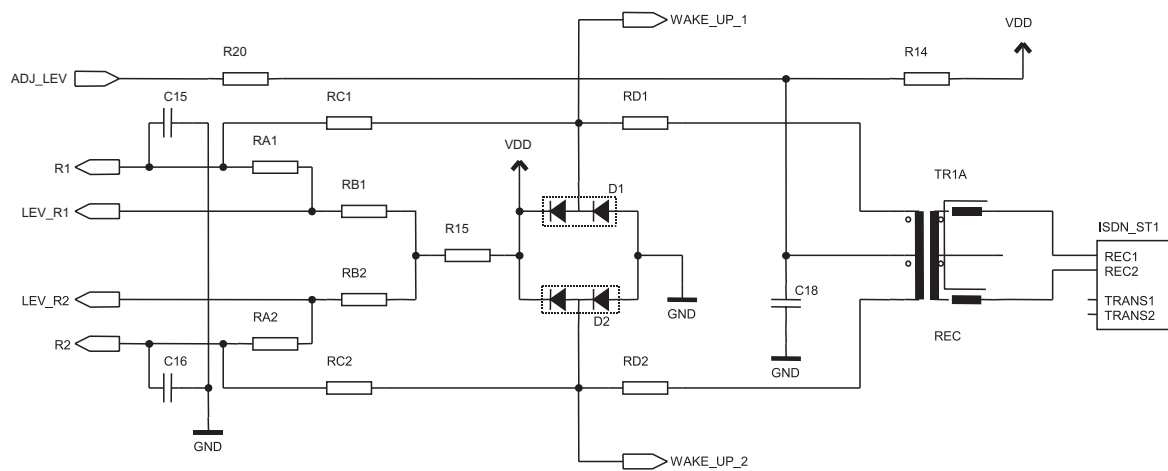### 7.1.1 External receiver circuitry

Figure 15: *External receiver circuitry*

WAKE_UP_1 and WAKE_UP_2 are for connection to the wake up circuitry (see section 7.1.2). C15 and C16 are for reduction of high frequency input noise and should be placed as close as possible to the HFC-S mini.

Part list

VDD	3.3 V	5 V	VDD	3.3 V	5 V
C15	22pF		RD1	4k7	
C16	22pF		RC1	4k7	
C18	47nF		RD2	4k7	
D2	BAV99		RC2	4k7	
D1	BAV99		R14	680k	1M
ISDN_ST1	ISDN Connector		R15	1M2	1M8
RA2	100k		R20	3k9	
RA1	100k		TR1A	S/T Module	
RB1	33k				
RB2	33k				

7.1.2 External wake-up circuitry

The wake-up circuitry is optional. It enables the HFC-S mini to wake up by incoming INFOx (non INFO0) signals on the S/T interface.
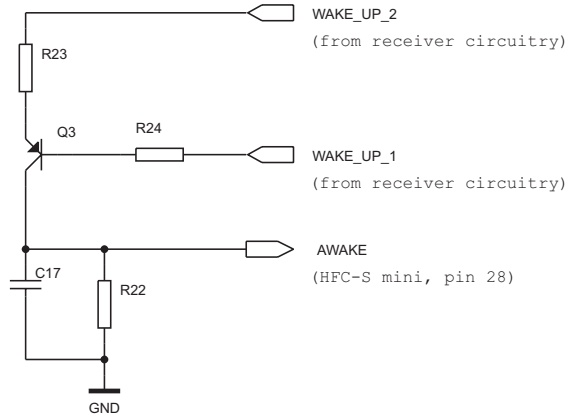

Figure 16: *External wake-up circuitry*

WAKE_UP_1 and WAKE_UP_2 are inputs from the receiver circuitry.

Part list

Part	Value
C17	100pF
Q3	BC860C
R22	4M7
R23	10k
R24	100k

7.1.3 External transmitter circuitry
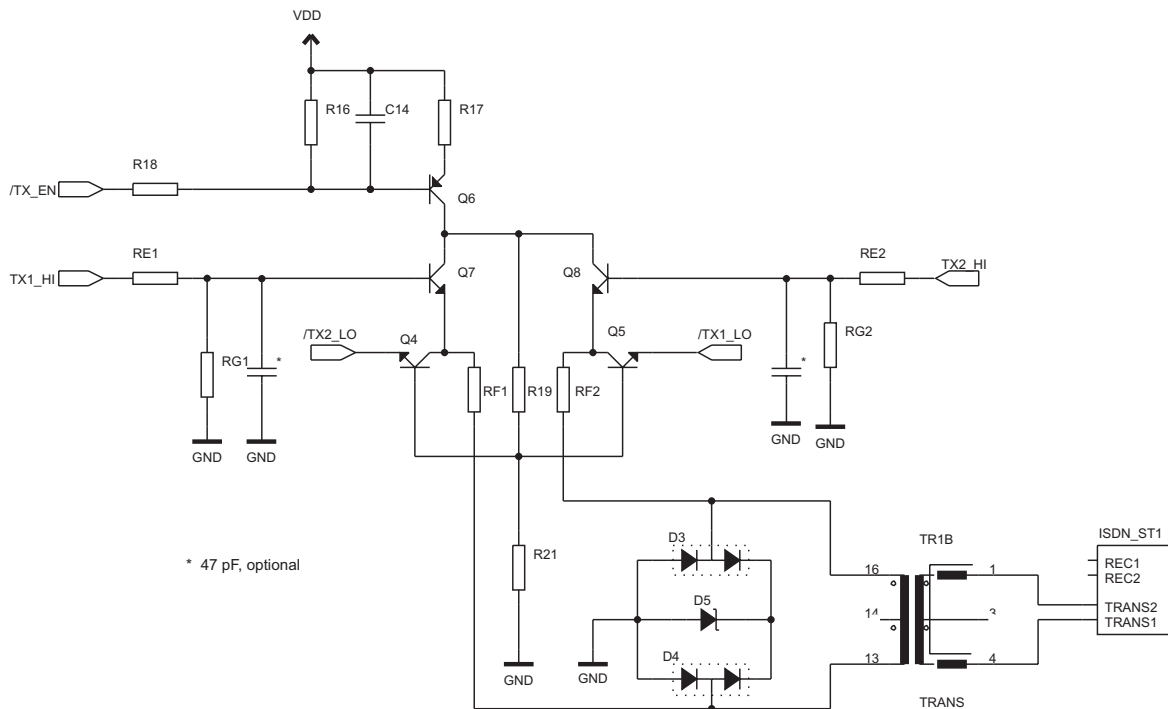
Figure 17: *External transmitter circuitry*

Part list

VDD	3.3 V	5 V	VDD	3.3 V	5 V
C14	470pF		RF1	18R *	
D3	BAV99		RF2	18R *	
D4	BAV99		RG1	3k9 1%	3k 1%
D5	2V7		RG2	3k9 1%	3k 1%
ISDN_ST1	ISDN Connector		R16	3k3	
Q4	BC850C		R21	2k2	
Q5	BC850C		R17	50	100
Q7	BC850C		R18	5k6	
Q8	BC850C		R19	1k8	3k3
Q6	BC860C		TR1B	S/T Module	
RE1	560 1%	2k2 1%			
RE2	560 1%	2k2 1%			

*: The optional capacitor value depends on the power supply voltage, the used S/T module and the line characteristics.

7.1.4 S/T modules and transformers

Customers of Cologne Chip can chose of a variety of S/T transformers for ISDN basic rate interface. All transformers are compatible to the S/T interface of Cologne Chip's "HFC-S" series of that fulfill two criteria:

- Turns Ratio of 1:2 (primary side : secondary side)
- Center Tap on the Secondary Side (required for Cologne Chip receiver circuitry)

Several companies provide transformers and modules that can be used with our ISDN basic rate interface controllers. Part numbers and manufacturer addresses are listed on Cologne Chip's website `http://www.colognechip.com`.

7.2 Oscillator circuitry for system clock
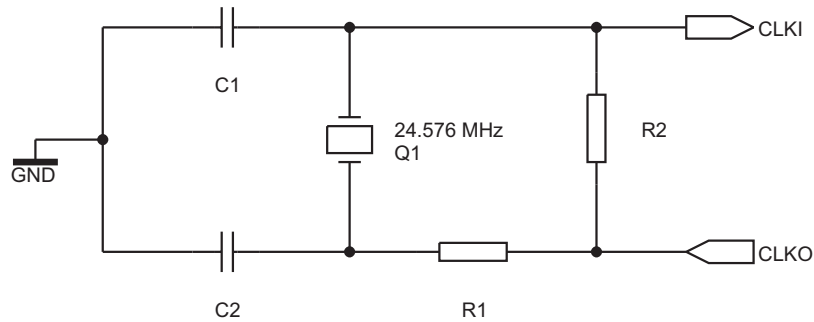
Figure 18: *Oscillator circuitry for S/T clock*

Part list

Part	Value
R1	330
R2	1M
C1	47pF
C2	47pF
Q1	24.576 MHz quartz

The values of C1, C2 and R1, R2 depend on the used quartz.

For a load-free check of the oscillator frequency the C4O clock of the PCM/GCI/IOM2 bus should be measured (HFC-S mini as master, S/T interface deactivated, 4.096 MHz frequency intented on the pin C4IO).

Figure 19 shows how to connect several HFC-S mini to only one quartz circuitry.
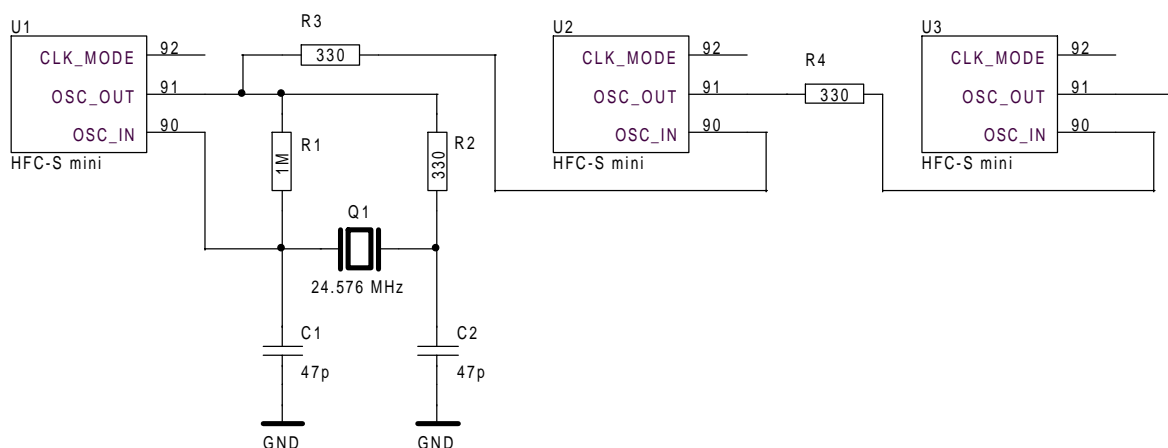
Figure 19: *Cascade-connected HFC-S mini with only one quartz circuitry*

8 State matrices for NT and TE

8.1 S/T interface activation / deactivation layer 1 state matrix for NT

State name:	Reset	Deactivate	Pending activation	Active	Pending deactivation
State number:	G 0	G 1	G 2	G 3	G 4
INFO sent:	INFO 0	INFO 0	INFO 2	INFO 4	INFO 0
Event:					
State machine release (Note 3)	G 1	|	|	|	|
Activate request	G 2 (Note 1)	G 2 (Note 1)	|	|	G 2 (Note 1)
Deactivate request	—	|	Start timer T2 G 4	Start timer T2 G 4	|
Expiry T2 (Note 2)	—	—	—	—	G1
Receiving INFO 0	—	—	—	G 2	G 1
Receiving INFO 1	—	G 2 (Note 1)	—	/	—
Receiving INFO 3	—	/	G 3 (Note 1, 4)	—	—
Lost framing	—	/	/	G2	—

Table 15: *Activation / deactivation layer 1 for finite state matrix for NT*

Legend:

— No state change

/ Impossible by the definition of peer-to-peer physical layer procedures or system internal reasons

| Impossible by the definition of the physical layer service

Notes:

Note 1: Timer 1 (T1) is not implemented in the HFC-S mini and must be implemented in software.

Note 2: Timer 2 (T2) prevents unintentional reactivation. Its value is 32 ms ($256 \cdot 125 \mu s$). This implies that a TE has to recognize INFO 0 and to react on it within this time.

Note 3: After reset the state machine is fixed to G0.

Note 4: Bit 7 of the ST_WR_STA register must be set every time to allow this transition. The transition is always allowed if bit 0 in SCTRL_E is set.

HFC-S mini

8.2 S/T interface activation / deactivation layer 1 state matrix for TE

State name:	Reset	Sensing	Deactivated	Awaiting signal	Identifying input	Synchronized	Activated	Lost framing
State number:	F 0	F 2	F 3	F 4	F 5	F 6	F 7	F 8
INFO sent:	INFO 0	INFO 0	INFO 0	INFO 1	INFO 0	INFO 3	INFO 3	INFO 0
Event:								
State machine release (Note 1)	F 2	/	/	/	/	/	/	/
Activate request, receiving any signal	—	|	F 5	|	|	—	|	—
receiving INFO 0	—	|	F 4	|	|	—	|	—
Expiry T3 (Note 5)	—	/	—	F 3	F 3	—	—	F 3
Receiving INFO 0	—	F 3	—	—	—	F 3	F 3	F 3
Receiving any signal (Note 2)	—	—	—	F 5	—	/	/	—
Receiving INFO 2 (Note 3)	—	F 6	F 6	F 6	F 6	—	F 6	F 6
Receiving INFO 4 (Note 3)	—	F 7	F 7	F 7	F 7	F 7	—	F 7
Lost framing (Note 4)	—	/	/	/	/	F 8	F 8	—

Table 16: *Activation / deactivation layer 1 for finite state matrix for TE*

Legend:

— No state change

/ Impossible situation

| Impossible by the definition of the layer 1 service

Notes:

Note 1: After reset the state machine is fixed to F 0.

Note 2: This event reflects the case where a signal is received and the TE has not (yet) determined wether it is INFO 2 or INFO 4.

Note 3: Bit- and frame-synchronization achieved.

Note 4: Loss of Bit- or frame-synchronization.

Note 5: Timer 3 (T3) is not implemented in the HFC-S mini and must be implemented in software.

9 Binary organization of the frames

9.1 S/T frame structure

The frame structures on the S/T interface are different for each direction of transmission. Both structures are illustrated in Figure 20.
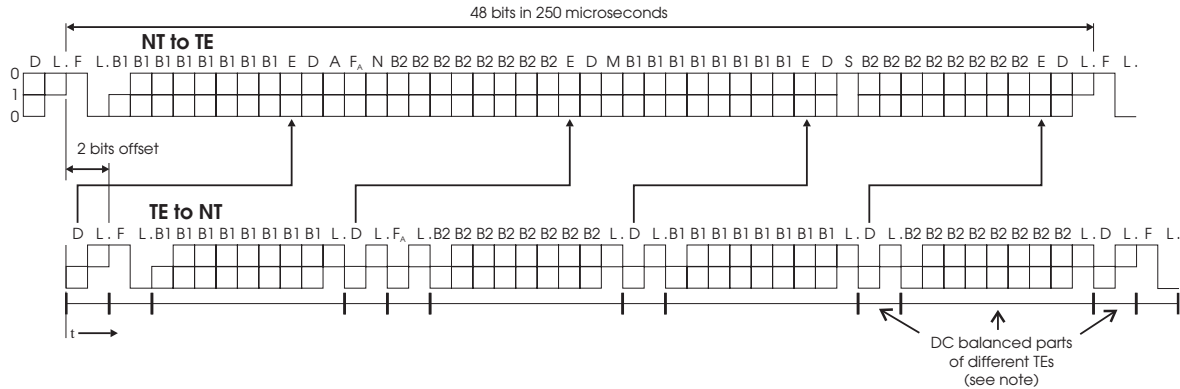

Figure 20: *Frame structure at reference point S and T*

Legend:

F	Framing Bit	N	Bit set to a binary value $N = \bar{F}_A$ (NT to TE)
L	DC balancing bit	B1	bit withion B-channel 1
D	D-channel bit	B2	bit withion B-channel 2
E	E-channel bit (echo of D-channel)	A	Bit used for activation
F_A	Auxiliary framing bit	S	S-channel bit
M	Multiframe bit		

👆 **Please note !**

Lines demarcate those parts of the S/T frame that are independently DC-balanced. The FA bit in the direction TE to NT is used as Q bit in every fifth frame if S/Q bit transmission is enabled (see SCTRL register).
The nominal 2-bit offset is as seen from the TE. The offset can be adjusted with the CLKDEL register in TE mode. The corresponding offset at the NT may be greater due to delay in the interface cable and varies by configuration.
HDLC B-channel data start with the LSB, PCM B-channel data start with the MSB.

9.2 GCI frame structure

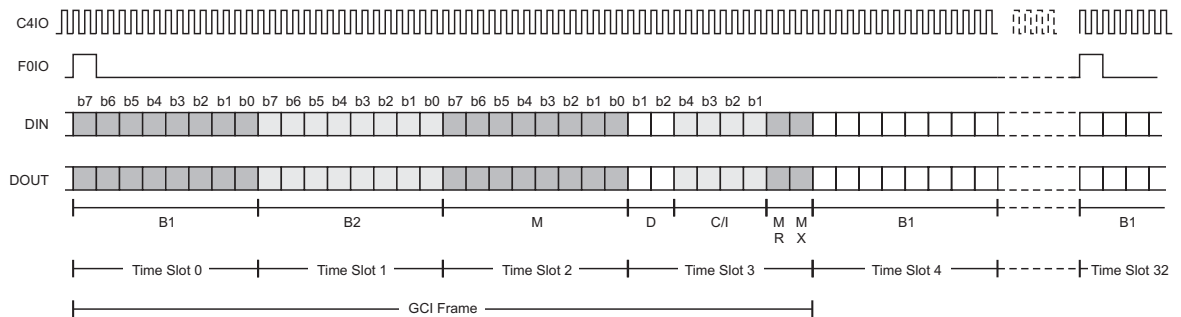The binary organization of a single GCI channel frame is described below. C4IO clock frequency is 4096 kHz.

Figure 21: *Single channel GCI format*

Legend:

B1   B-channel 1 data

B2   B-channel 2 data

M   Monitor channel data

D   D-channel data C/I Command/indication bits for controlling activation/deactivation and for additional control functions

MR   Handshake bit for monitor channel

MX   Handshake bit for monitor channel

10 Clock synchronization

10.1 Clock synchronization in NT-mode
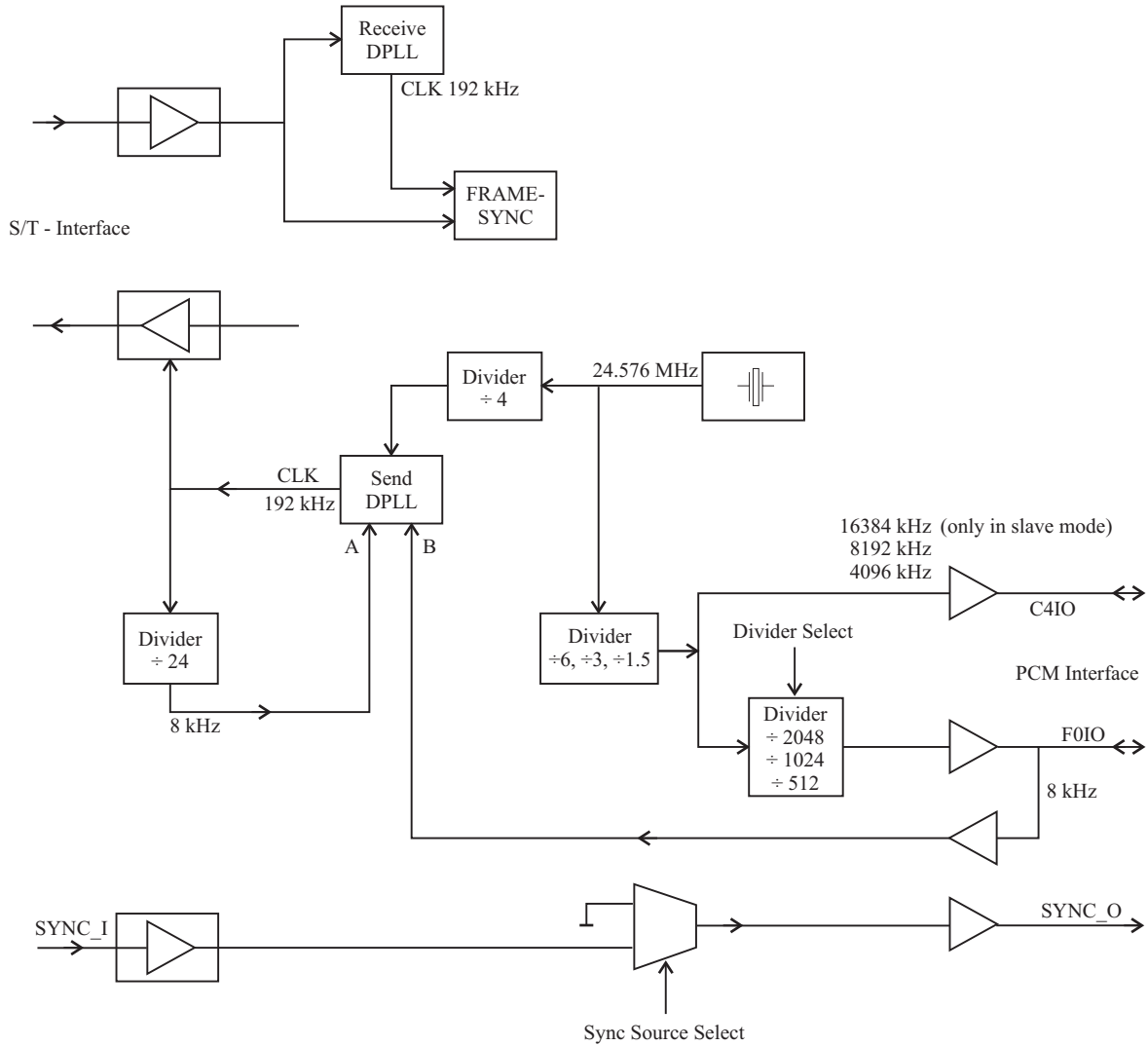
Figure 22: *Clock synchronization in NT-mode*

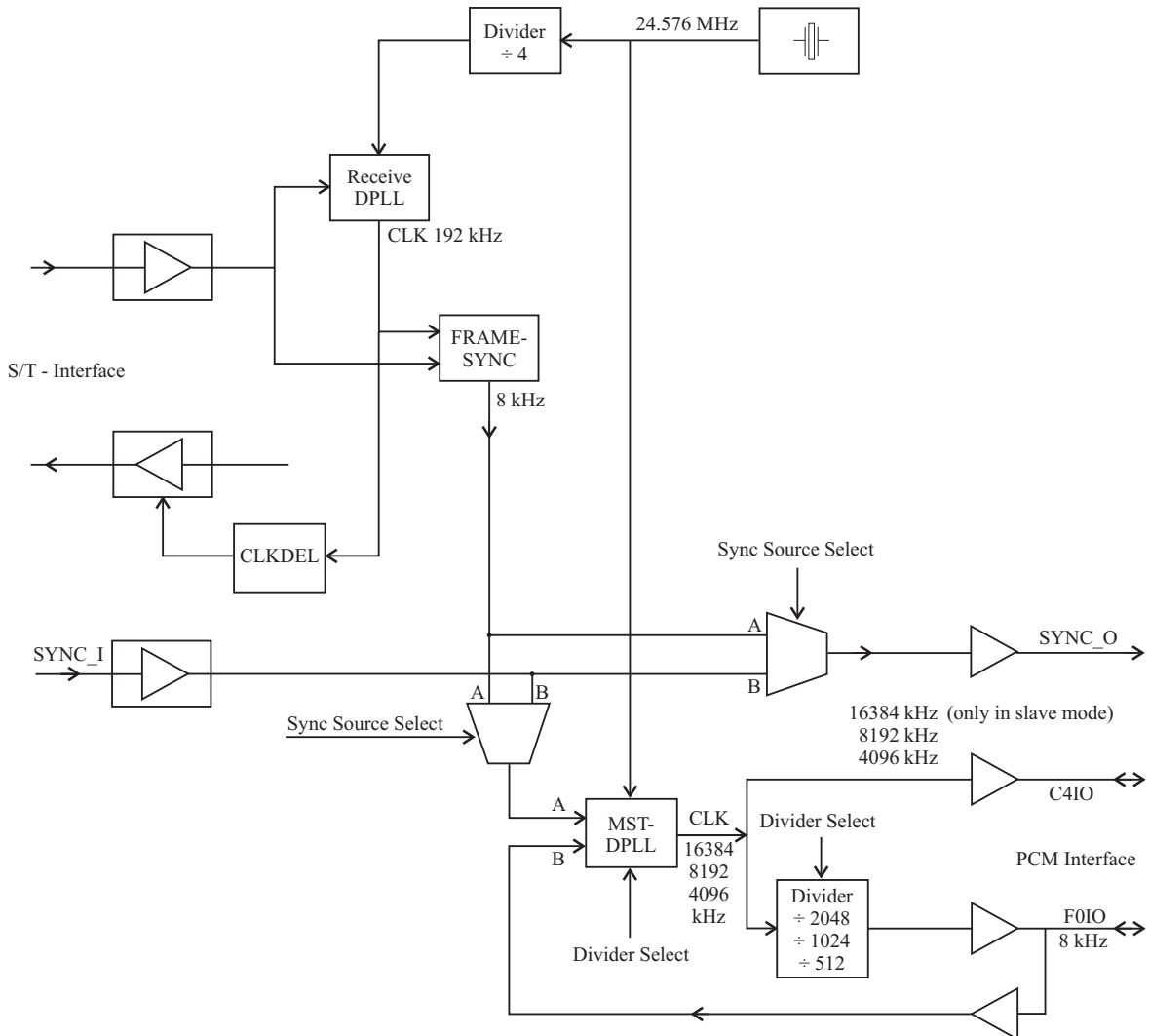## 10.2 Clock synchronization in TE-mode

Figure 23: *Clock synchronization in TE-mode*

The C4IO clock is adjusted in the 31th time slot at the GCI/IOM bus 1 . . 4 times for one half clock cycle. This can be reduced to one adjustment of a half clock cycle (see MST_MODE1 register). This is useful if another HFC series ISDN controller is connected as slave in NT mode to the PCM bus. The synchronization source can be selected by the MST_MODE2 register settings.

10.3 Multiple HFC-S mini synchronization scheme

The synchronization scheme for multiple HFC-S mini ISDN controllers is shown in Figure 24. The synchronization source of the whole system can be selected by software (see also MST_MODE2 register bit description).
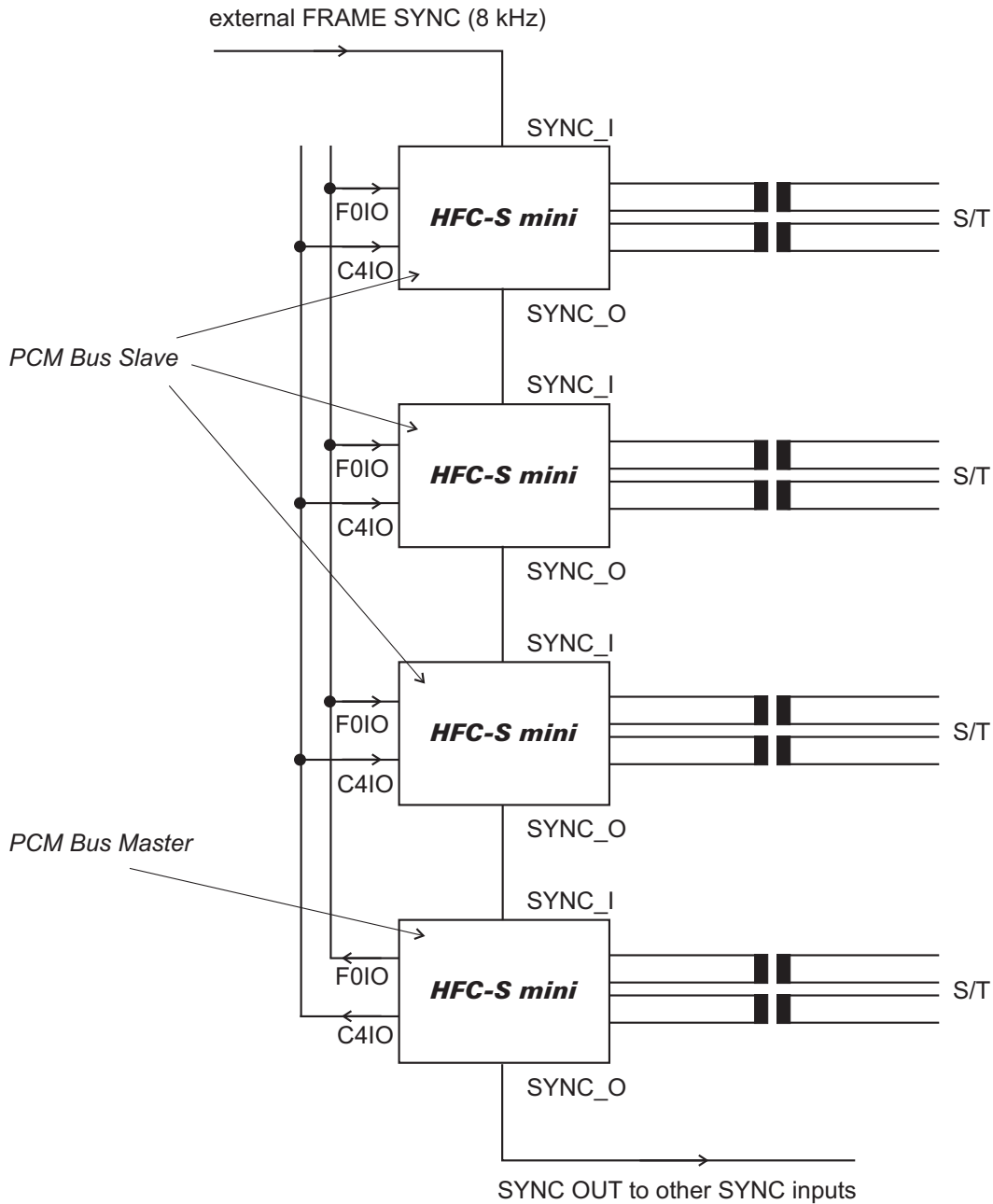

Figure 24: *Multiple HFC-S mini synchronization scheme*

Cologne Chip

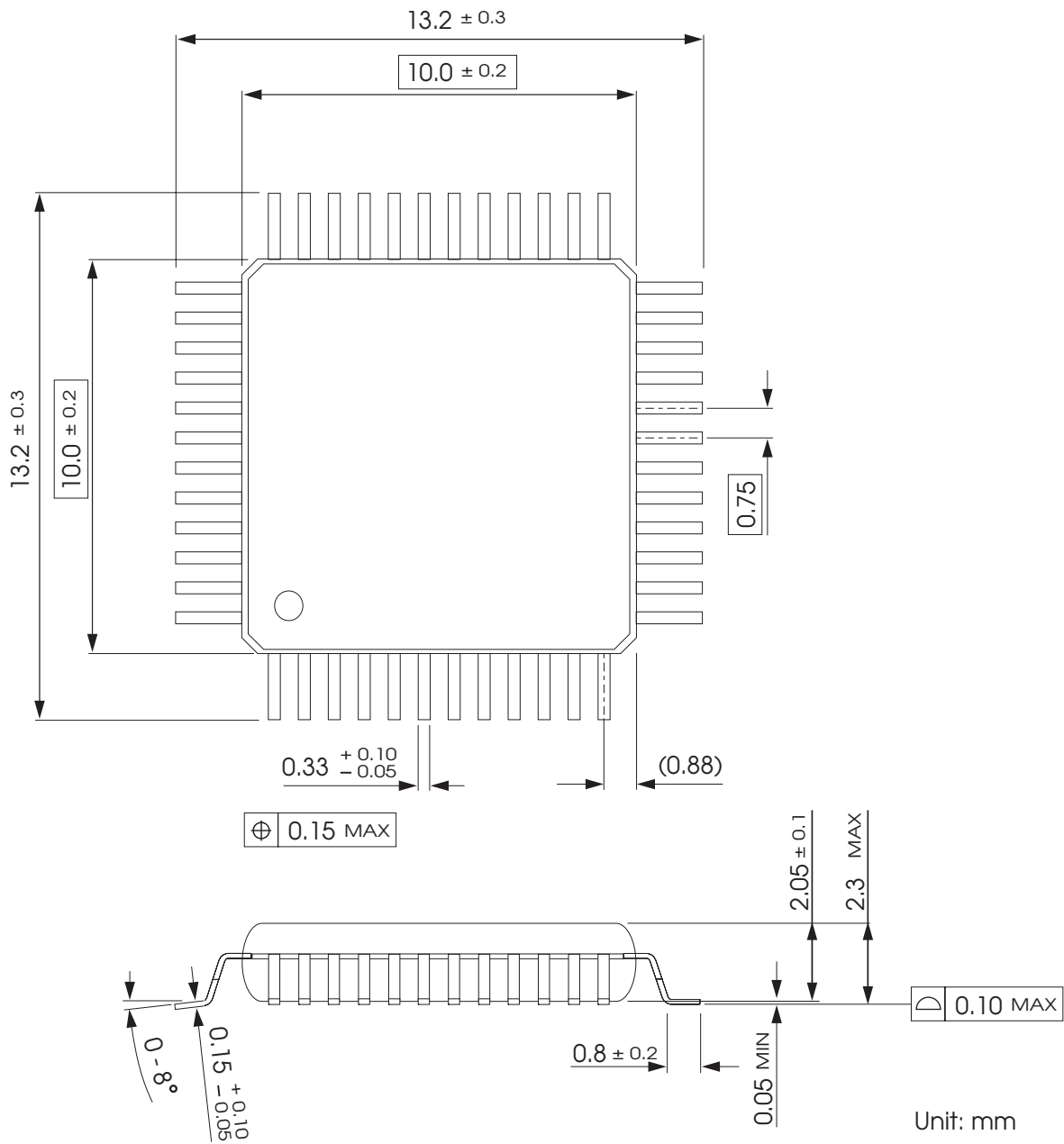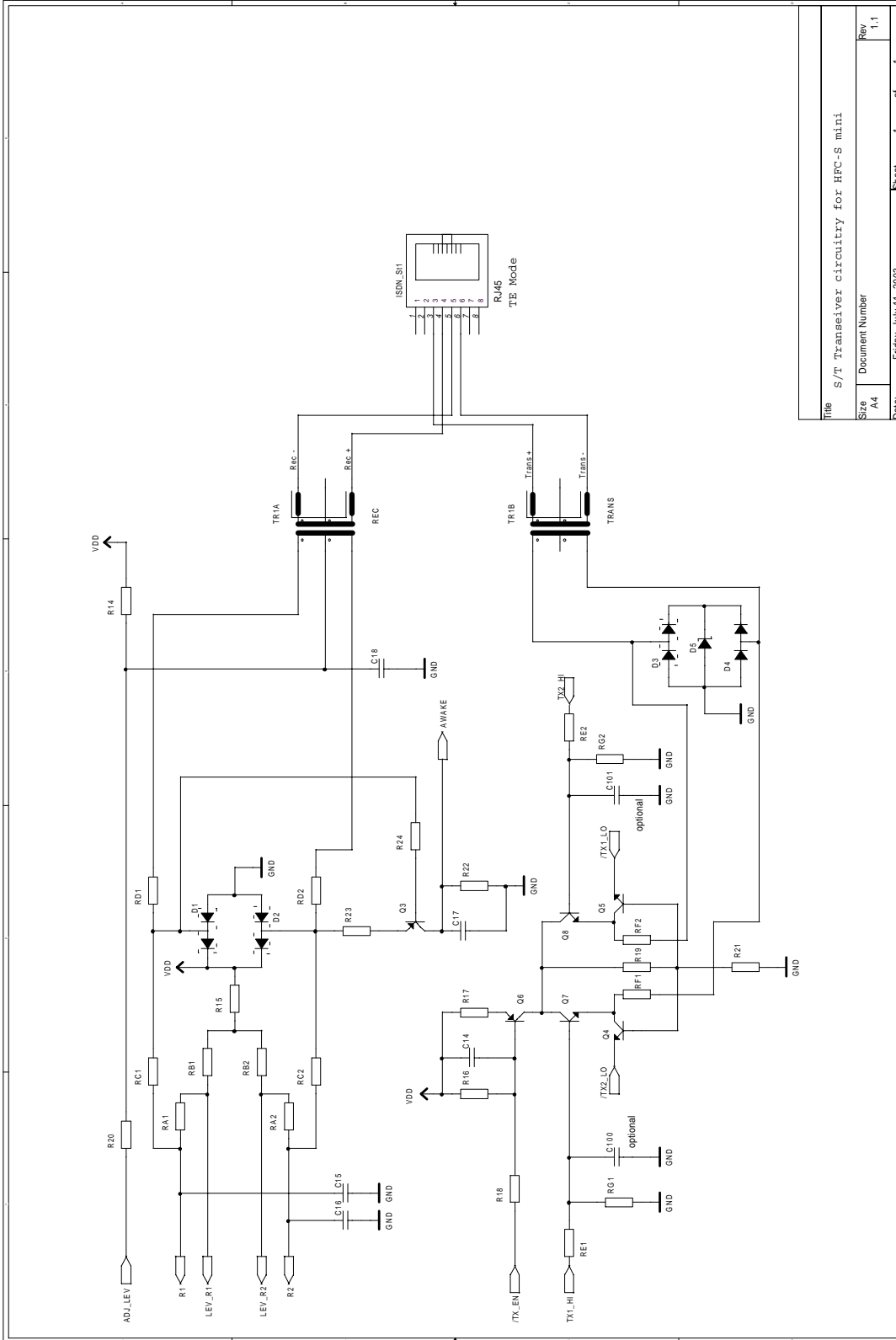## 11   HFC-S mini package dimensions

Figure 25: *HFC-S mini package dimensions*

12 Sample circuitries

12.1 S/T interface circuitry (valid in all modes)

Figure 26: *HFC-S mini sample circuitry*

The following *Bill of Materials* are related to Figure 26 both. They show the component values for 3.3 V or 5 V power supply respectively.

Bill of Materials: **S/T transceiver circuitry for 3.3 V power supply**

Revision: 1.1 generated on **Friday, July 11, 2003** by **Cologne Chip AG**

(n.b. = not used / not assembled)

Resistors (25 pcs.)

R14	680k
R15	1M2
R16	3k3
R17	51
R18	5k6
R19	1k8
R20	3k9
R21	2k2
R22	4M7
R23	10k
R24	100k
RA1	100k
RA2	100k
RB1	33k
RB2	33k
RC1	4k7
RC2	4k7
RD1	4k7
RD2	4k7
RE1	560
RE2	560
RF1	18
RF2	18
RG1	3k9
RG2	3k9

Capacitors (7 pcs.)

C14	470p
C15	22p
C16	22p
C17	100p
C18	47n
C100	optional
C101	optional

Diodes (5 pcs.)

D1	BAV99
D2	BAV99
D3	BAV99
D4	BAV99
D5	2V7

Transistors (6 pcs.)

Q3	BC858CL
Q4	BC848CL
Q5	BC848CL
Q6	BC858CL
Q7	BC848CL
Q8	BC848CL

Transformers (1 pc.)

TR1	S_TRANS

Misc (1 pc.)

ISDN_St1	RJ45

Total:

25 x Resistors
7 x Capacitors
5 x Diodes
6 x Transistors
1 x Transformers
1 x Misc

---

45   total
+ 0   not used / not assembled

Bill of Materials: **S/T transceiver circuitry for 5 V power supply**

Revision: 1.1 generated on **Friday, July 11, 2003** by **Cologne Chip AG**

(n.b. = not used / not assembled)

Resistors (25 pcs.)

R14	1M
R15	1M8
R16	3k3
R17	100
R18	5k6
R19	3k3
R20	3k9
R21	2k2
R22	4M7
R23	10k
R24	100k
RA1	100k
RA2	100k
RB1	33k
RB2	33k
RC1	4k7
RC2	4k7
RD1	4k7
RD2	4k7
RE1	2k2
RE2	2k2
RF1	18
RF2	18
RG1	3k
RG2	3k

Capacitors (7 pcs.)

C14	470p
C15	22p
C16	22p
C17	100p
C18	47n
C100	optional
C101	optional

Diodes (5 pcs.)

D1	BAV99
D2	BAV99
D3	BAV99
D4	BAV99
D5	2V7

Transistors (6 pcs.)

Q3	BC858CL
Q4	BC848CL
Q5	BC848CL
Q6	BC858CL
Q7	BC848CL
Q8	BC848CL

Transformers (1 pc.)

TR1   S_TRANS

Misc (1 pc.)

ISDN_St1   RJ45

Total:

25 x Resistors
 7 x Capacitors
 5 x Diodes
 6 x Transistors
 1 x Transformers
 1 x Misc

 45   total
+ 0   not used / not assembled

12.2 HFC-S mini in mode 2 (Motorola bus)

Figure 27 shows only the processor part of a HFC-S mini sample board in mode 2 (Motorola). The S/T interface circuitry shown in Figure 26 must be enclosed to complete the sample board.
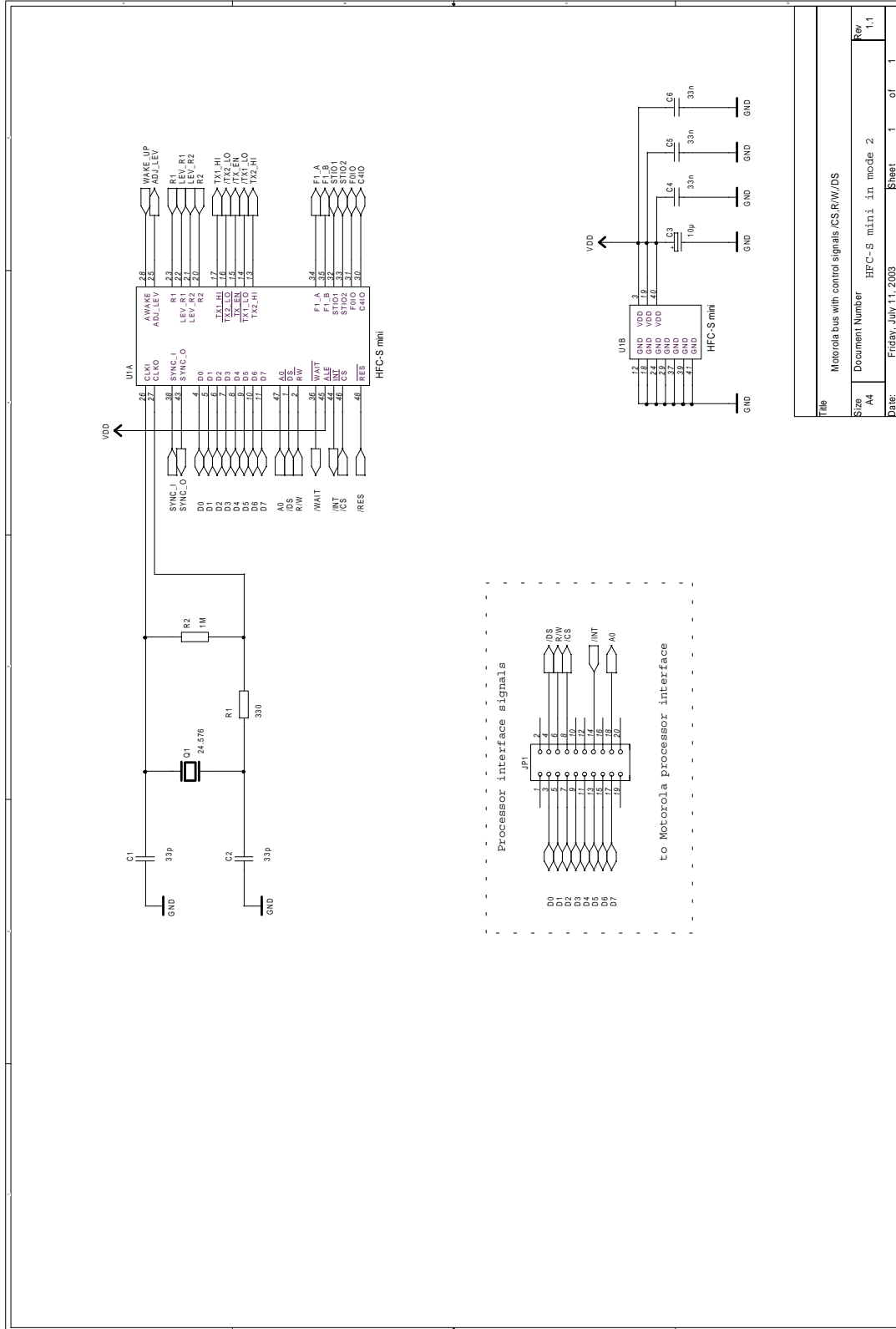

Figure 27: *HFC-S mini sample circuitry in processor mode 2 (Motorola)*

12.3 HFC-S mini in mode 3 (Intel bus with separate address bus/data bus)

Figure 28 shows only the processor part of a HFC-S mini sample board in mode 2 (Motorola). The S/T interface circuitry shown in Figure 26 must be enclosed to complete the sample board.
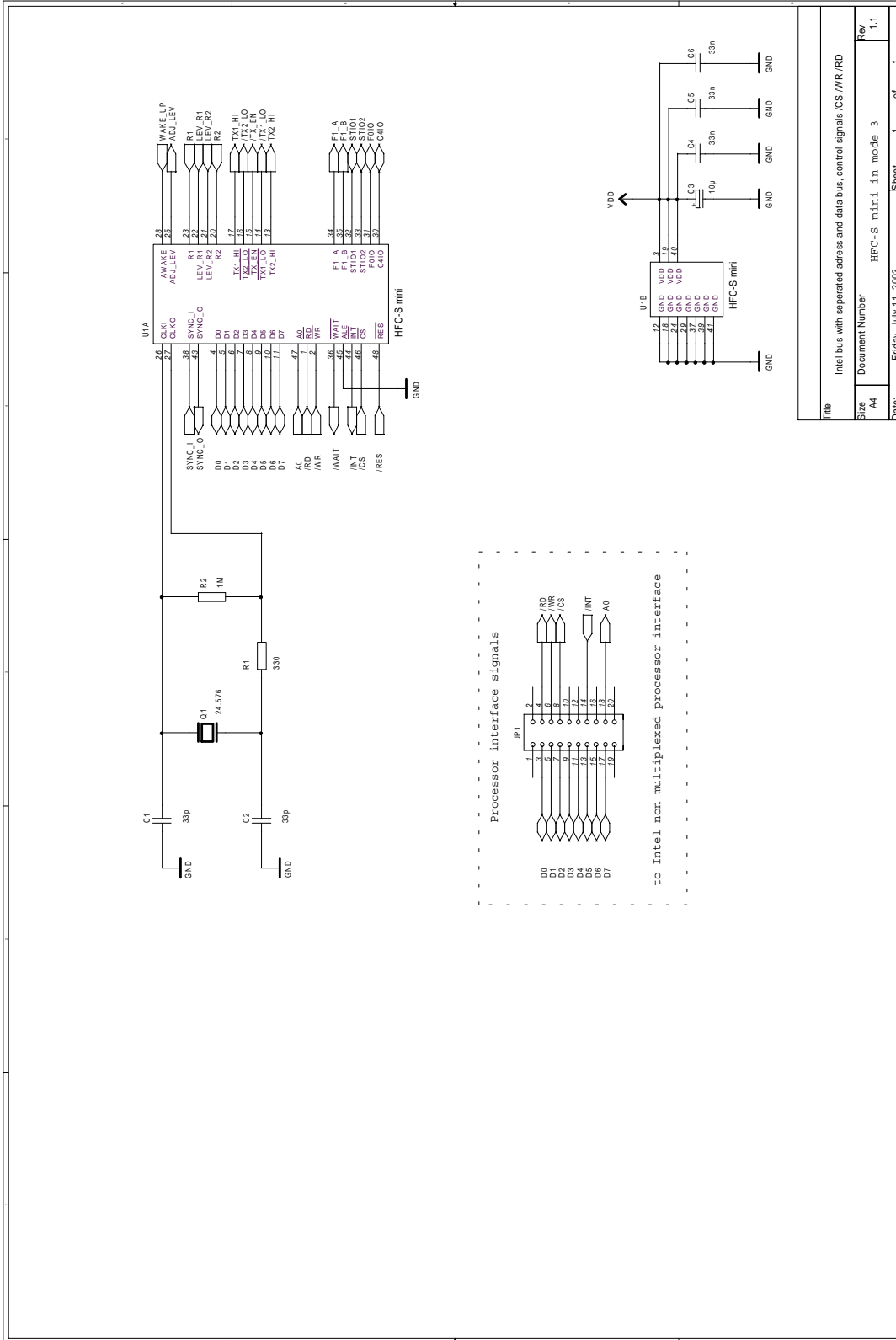

Figure 28: *HFC-S mini sample circuitry in processor mode 3 (Intel), 1st part*

12.4   HFC-S mini in mode 4 (Intel bus with multiplexed address bus/data bus)

Figure 29 shows only the processor part of a HFC-S mini sample board in mode 2 (Motorola). The
S/T interface circuitry shown in Figure 26 must be enclosed to complete the sample board.
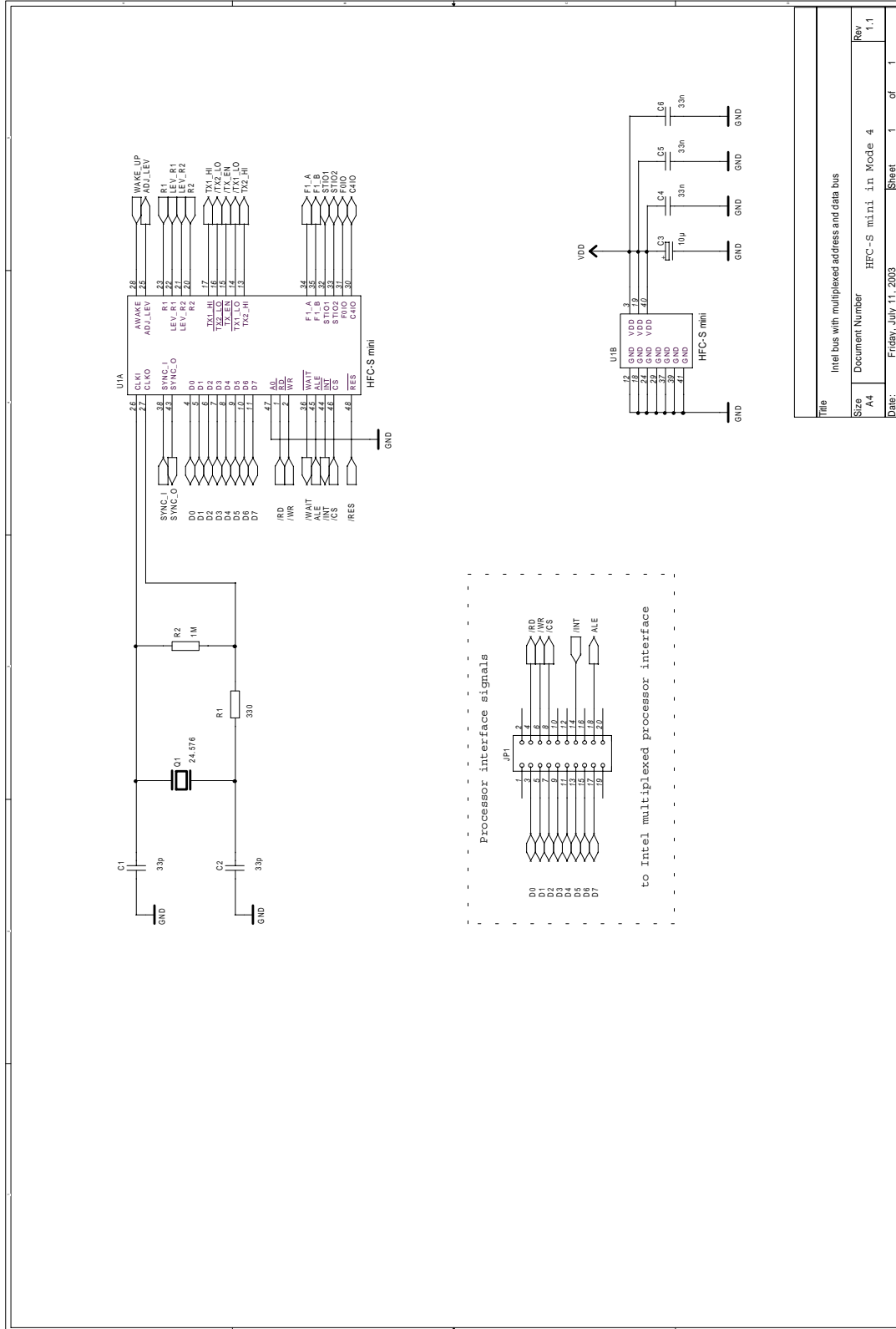

Figure 29: *HFC-S mini sample circuitry in processor mode 4 (Intel, multiplexed), 1st part*

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Data Sheet of HFC-S mini