64K x 1 Static RAM

L7C187

T-46-23-05

Features

- 64K by 1 Static RAM with separate I/O, Chip Select power down
- Auto-Powerdown™ design
- Advanced CMOS technology
- High speed — to 15 ns worst-case
- Low Power Operation
  Active: 225 mW typical at 45 ns
  Standby: 50 µW typical
- Data retention at 2 V for battery backup operation
- Plug-compatible with IDT 7187, Cypress CY7C187
- Package styles available:
  - 22-pin Plastic DIP
  - 22-pin Sidebraze, Hermetic DIP
  - 22-pin CerDIP
  - 22-pin Ceramic LCC
  - 24-pin Plastic SOIC (Gull-Wing)
  - 24-pin Plastic SOJ (J-Lead)

Description

The L7C187 is a high-performance, low-power CMOS static Random Access Memory. The storage circuitry is organized as 65,536 words by 1 bit per word. Parts are available in six speed categories with worst-case access times from 15 ns to 85 ns.

Operation is from a single +5 V power supply and all interface signals are TTL compatible. Power consumption is 225 mW (typical) at 45 ns. Dissipation drops to 25 mW (typical) when the memory is deselected ($\overline{CE}$ is high).

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write accesses which are longer than the minimum access time, or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The memory typically consumes only 3 µW at 2 V, allowing effective battery back-up operation.

The L7C187 provides asynchronous (unclocked) operation with matching access and cycle times. An active-low Chip Enable and a three-state output simplify the connection of several chips for increased capacity.

Memory locations are specified on address pins A0 through A15. Reading from a designated location is accomplished by presenting an address and then taking $\overline{CE}$ low while $\overline{WE}$ remains high. The data in the addressed memory location will then appear on the Data Out pin within one access time. The output pin stays in a high-impedance state when $\overline{CE}$ is high or $\overline{WE}$ is low.

Writing to an addressed location is accomplished when the active-low $\overline{CE}$ and $\overline{WE}$ inputs are both low. Either signal may be used to terminate the write operation. Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L7C187 can withstand an injection current of up to 200 mA on any pin without damage.

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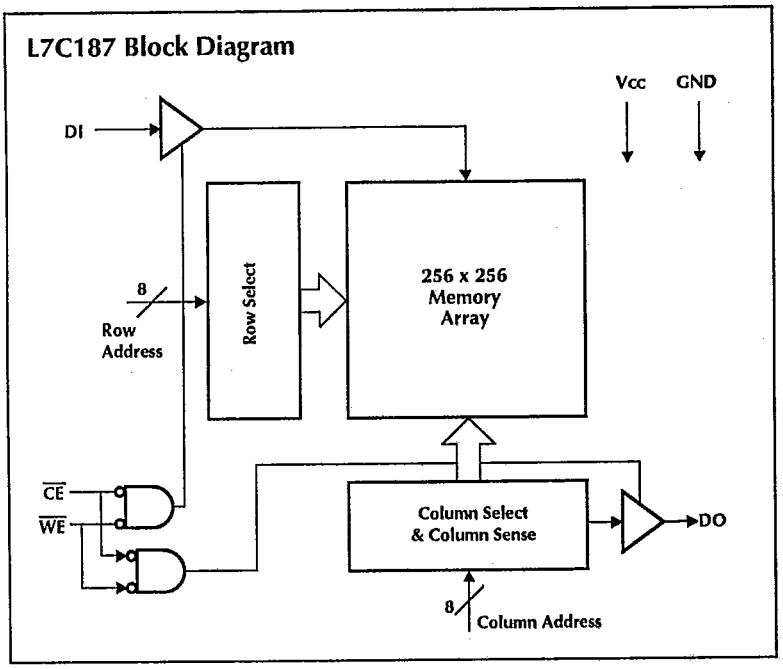
L7C187 Block Diagram



Maximum Ratings

Above which useful life may be impaired (Notes 1, 2)

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
Vcc supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

Operating Conditions

To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ Vcc ≤ 5.5 V
Active Operation, Military	–55°C to +125°C	4.5 V ≤ Vcc ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ Vcc ≤ 5.5 V
Data Retention, Military	–55°C to +125°C	2.0 V ≤ Vcc ≤ 5.5 V

Electrical Characteristics

Over Operating Conditions

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –4.0 mA, Vcc = 4.5 V	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		Vcc + 0.3	V
V_{IL}	Input Low Voltage	Note 3	–3.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_I ≤ Vcc	–10		+10	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_O ≤ Vcc, $\overline{CE}$ = Vcc	–50		+50	µA
I_{OS}	Output Short Current	V_O = Ground, Vcc = Max, Note 4			–350	mA
I_{CC2}	Vcc Current, Inactive	Notes 5, 7		5.0	20	mA
I_{CC3}	Vcc Current, Standby	Note 8		10	250	µA
I_{CC4}	Vcc Current, DR Mode	Vcc = 2.0 V, Note 9		1.5	50	µA
C_I	Input Capacitance	Ambient Temp = 25°C, Vcc = 5.0 V			5	pF
C_O	Output Capacitance	Test Frequency = 1 MHz, Note 10			7	pF

			L7C187-						
Symbol	Parameter	Test Condition	85	45	35	25	20	15	Unit
I_{CC1}	Vcc Current, Active	Notes 5, 6	35	60	70	100	120	150	mA

Switching Characteristics

Over Operating Range (ns)

Read Cycle *(Notes 11, 12, 22, 23, 24)*

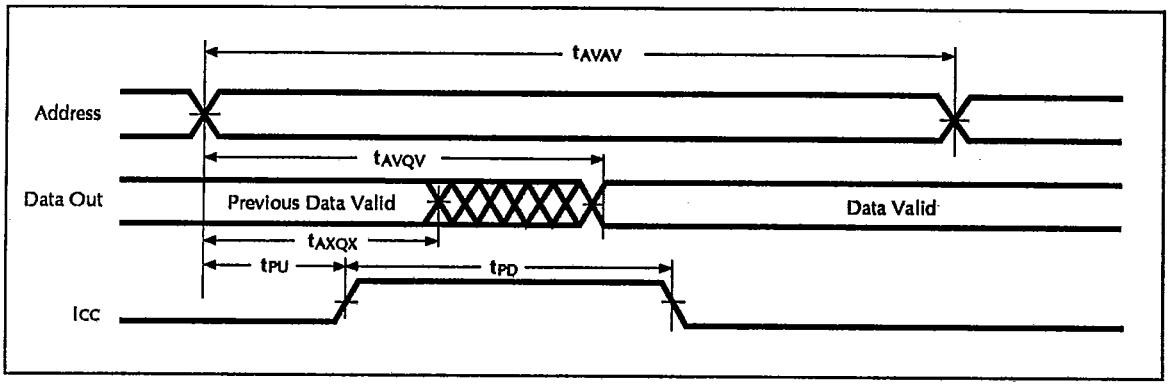
		L7C187-											
		85		45		35		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
tAVAV	Read Cycle Time	85		45		35		25		20		15	
tAVQV	Addr Valid to Output Valid (13, 14)		85		45		35		25		20		15
tAXQX	Addr Change to Output Change	5		5		5		5		5		3	
tCLQV	Chip Enable Low to Output Valid (13, 15)		85		45		35		25		20		15
tCLQZ	Chip Enable Low to Output Low Z (20, 21)	5		5		5		5		5		5	
tCHQZ	Chip Enable High to Output High Z (20, 21)		35		15		15		10		8		8
tPU	CE or WE Low to Power Up (10, 19)	0		0		0		0		0		0	
tPD	Power Up to Power Down (10, 19)		85		45		35		25		20		20

Write Cycle *(Notes 11, 12, 22, 23, 24)*

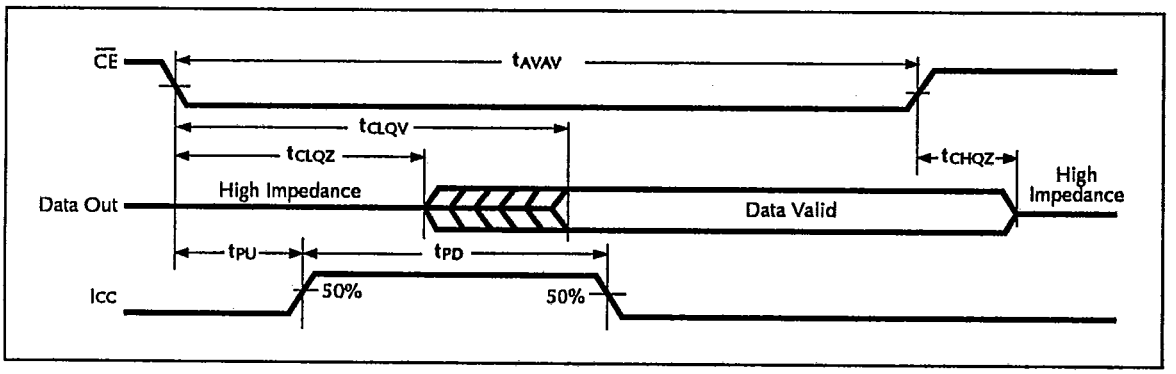
		L7C187-											
		85		45		35		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
tAVAV	Write Cycle Time	75		40		25		20		20		15	
tCLEW	Chip Enable Low to End of Write Cycle	65		30		25		20		12		12	
tAVBW	Address Valid to Beginning of Write Cycle	0		0		0		0		0		0	
tAVEW	Address Valid to End of Write Cycle	65		30		25		20		17		12	
tEWAX	End of Write Cycle to Address Change	0		0		0		0		0		0	
tWLEW	Write Enable Low to End of Write Cycle	45		20		20		20		17		12	
tDVEW	Data Valid to End of Write Cycle	35		15		15		15		13		10	
tEWDX	End of Write Cycle to Data Change	0		0		0		0		0		0	
tWHQZ	Write Enable High to Output Low Z (20, 21)	5		5		5		5		5		5	
tWLQZ	Write Enable Low to Output High Z (20, 21)		35		15		10		7		7		7
tCHVL	Chip Enable High to Data Retention (10)	0		0		0		0		0		0	

Switching Waveforms

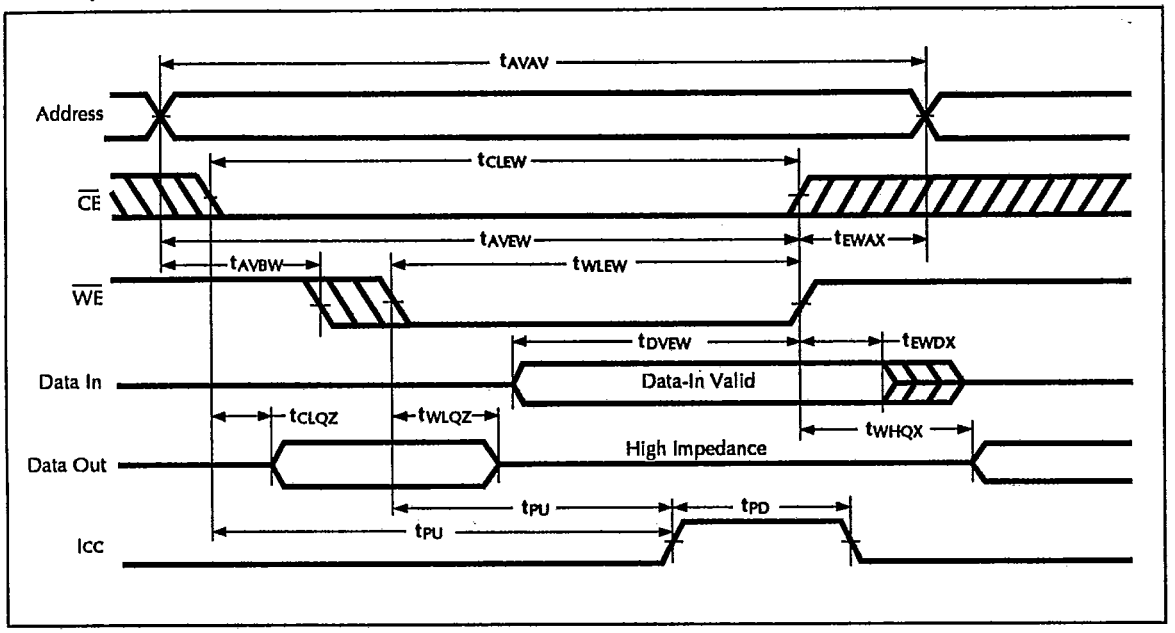
Read Cycle — Address Controlled *(Notes 13, 14)*



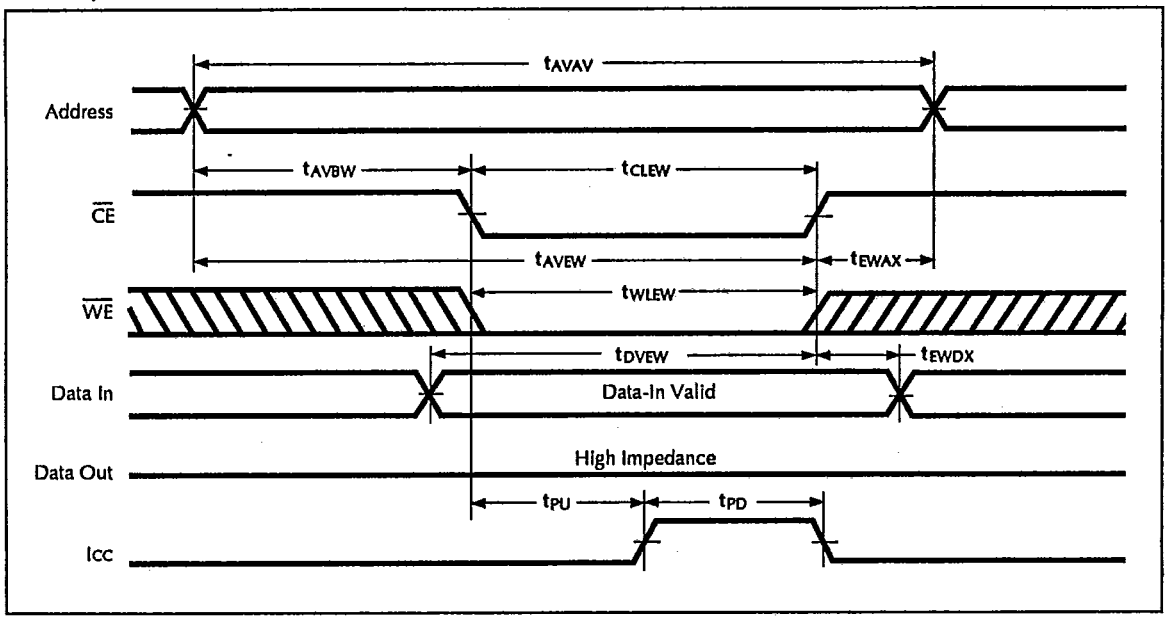
Read Cycle — $\overline{CE}$ Controlled *(Notes 13, 15)*



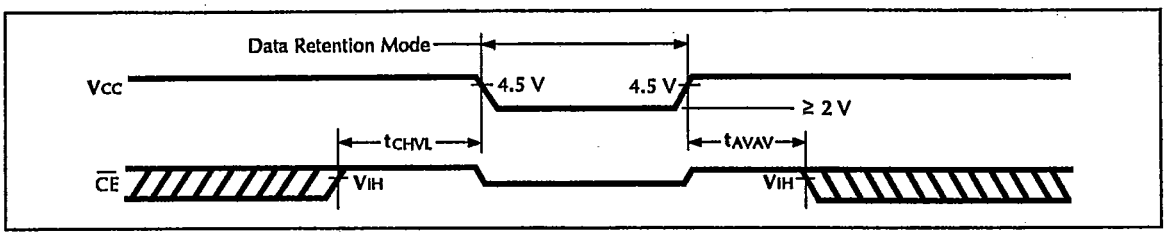
Write Cycle — $\overline{WE}$ Controlled (Notes 16, 17, 18, 19)



Write Cycle — $\overline{CE}$ Controlled (Notes 16, 17, 18, 19)



Data Retention



Test Loads and Transition Times

Figure 1a

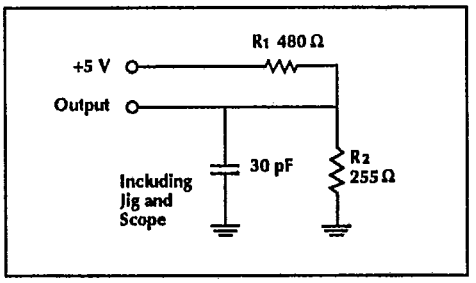


Figure 1b

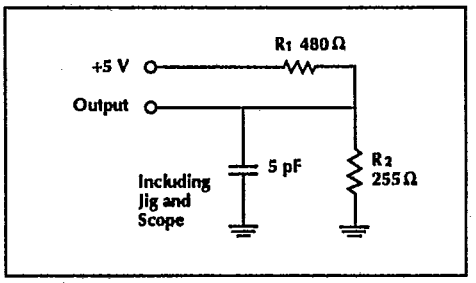
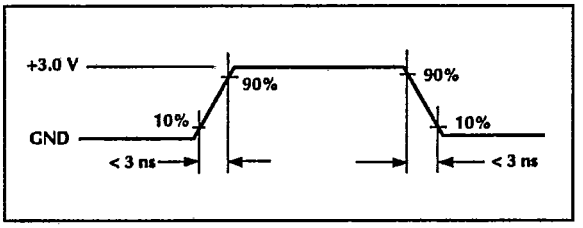


Figure 2



Notes

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. 'Typical' supply current values are not shown but may be approximated. At a V_{CC} of 5.0 V, an ambient temperature of +25°C and with nominal manufacturing parameters, the operating supply currents will be approximately 3/4 or less of the maximum values shown.

6. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously enabled for reading, i.e., $\overline{CE} \le V_{IL}$, $\overline{WE} \ge V_{IH}$.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE} \ge V_{IH}$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE} = V_{CC}$. Input levels are within 0.5 V of V_{CC} or ground.

9. Data retention operation requires that V_{CC} never drop below 2.0 V. $\overline{CE}$ must be $\ge V_{CC} - 0.3$ V. For all other inputs $V_{IN} \ge V_{CC} - 0.3$ or $V_{IN} \le 0.3$ V is required to ensure full power down.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading for specified I_{OL} and I_{OH} plus 30 pF.

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. t_{AVEW}, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}$ low).

15. All address lines are valid prior to or coincident with the $\overline{CE}$ transition to low.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write. Either signal can terminate a write by going high. The address, data, and control input setup and hold times should be referenced to the signal that falls last or rises first.

17. If $\overline{WE}$ goes low before or concurrent with $\overline{CE}$ going low, the output remains in a high impedance state.

18. If $\overline{CE}$ goes high before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE}$

b. Falling edge of $\overline{WE}$ ($\overline{CE}$ active)

c. Transition on any address line ($\overline{CE}$ active)

d. Transition on any data line ($\overline{CE}$ and $\overline{WE}$ active)

The device automatically powers down from I_{CC1} to I_{CC2} after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Figure 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper terminations must be used.

Ordering Information

Commercial Operating Range (0°C to +70°C)

Package Style	Performance					
	85 ns	45 ns	35 ns	25 ns	20 ns	15 ns
22-pin Plastic DIP (0.3") — P8	L7C187PC85	L7C187PC45	L7C187PC35	L7C187PC25	L7C187PC20	L7C187PC15
24-pin SOIC — U1	L7C187UC85	L7C187UC45	L7C187UC35	L7C187UC25	L7C187UC20	L7C187UC15
24-pin SOJ — W1	L7C187WC85	L7C187WC45	L7C187WC35	L7C187WC25	L7C187WC20	L7C187WC15
22-pin Sidebraze (0.3") Hermetic DIP — D8	L7C187DC85	L7C187DC45	L7C187DC35	L7C187DC25	L7C187DC20	L7C187DC15
22-pin CerDIP (0.3") — C3	L7C187CC85	L7C187CC45	L7C187CC35	L7C187CC25	L7C187CC20	L7C187CC15
22-pin Ceramic LCC — K4	L7C187KC85	L7C187KC45	L7C187KC35	L7C187KC25	L7C187KC20	L7C187KC15

Military Operating Range (–55°C to +125°C)

Package Style	Performance					
	85 ns	45 ns	35 ns	25 ns	20 ns	
22-pin Sidebraze (0.3") Hermetic DIP — D8	L7C187DM85 L7C187DME85 L7C187DMB85	L7C187DM45 L7C187DME45 L7C187DMB45	L7C187DM35 L7C187DME35 L7C187DMB35	L7C187DM25 L7C187DME25 L7C187DMB25	L7C187DM20 L7C187DME20 L7C187DMB20	
22-pin CerDIP (0.3") — C3	L7C187CM85 L7C187CME85 L7C187CMB85	L7C187CM45 L7C187CME45 L7C187CMB45	L7C187CM35 L7C187CME35 L7C187CMB35	L7C187CM25 L7C187CME25 L7C187CMB25	L7C187CM20 L7C187CME20 L7C187CMB20	
22-pin Ceramic LCC — K4	L7C187KM85 L7C187KME85 L7C187KMB85	L7C187KM45 L7C187KME45 L7C187KMB45	L7C187KM35 L7C187KME35 L7C187KMB35	L7C187KM25 L7C187KME25 L7C187KMB25	L7C187KM20 L7C187KME20 L7C187KMB20	

Pin Assignments *(P8, D8, C3, K4)*

Pin	Function	Pin	Function
1	A0	12	$\overline{CE}$
2	A1	13	DIN
3	A2	14	A8
4	A3	15	A9
5	A4	16	A10
6	A5	17	A11
7	A6	18	A12
8	A7	19	A13
9	DOUT	20	A14
10	$\overline{WE}$	21	A15
11	GND	22	VCC

Pin Assignments *(U1, W1)*

Pin	Function	Pin	Function
1	A0	13	$\overline{CE}$
2	A1	14	DIN
3	A2	15	A8
4	A3	16	A9
5	A4	17	A10
6	A5	18	A11
7	*NC*	19	*NC*
8	A6	20	A12
9	A7	21	A13
10	DOUT	22	A14
11	$\overline{WE}$	23	A15
12	GND	24	VCC

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