ROHM
SEMICONDUCTOR

Structure   Silicon Monolithic Integrated Circuit

Product Name   Audio Interface for Cellular Phone

Product No.   **BU7843AGU**

Features   Audio Interface
                         6x6 keyscan circuit

○Absolute Maximum Ratings(Ta=25°C)

Parameter	Symbol	Rating	Unit	Remarks
Analog supply voltage	AVDD	-0.3～4.5	V	
Digital supply voltage	DVDD	-0.3～4.5	V	
Power supply voltage	PVDD	-0.3～4.5	V	
Analog input voltage	V_{AIN}	AVSS-0.3～AVDD+0.3	V	
Digital input voltage	V_{DIN}	DVSS-0.3～DVDD+0.3	V	
Input current	I_{IN}	-10～+10	mA	
Allowable dissipation	P_d	310(*1)	mW	
Operating temperature range	T_{OPR}	-30～+85	^{o}C	
Storage temperature range	T_{STG}	-55～+125	^{o}C	

(*1) When Ta is above 25°C, reduce 3.1mW per 1°C.

○Recommended operating conditions（Ta=25°C）

Parameter	Symbol	Rating			Unit	Remarks
		Min.	Typ.	Max.		
Analog operation voltage	AVDD	2.7	2.8	3.1	V	(*2)
Digital operation voltage	DVDD	1.65	1.8	3.1	V	
Power operation voltage	PVDD	2.7	2.8	3.1	V	

(*2) AVDD and PVDD are internally connected in the IC and use the same potential.

This chip is not designed to protect itself against radioactive rays.

○Electrical Characteristics

(Unless otherwise noted, Ta = 25°C AVSS=DVSS=PVSS=0.0V   ATT is set at 0)

Parameter	Symbol	Rating			Unit	Condition
		Min.	Typ.	Max.		
Digital DC characteristics						
Digital high level input voltage 1	V_{IH1}	0.8 DVDD	-	-	V	DVDD=3.0V
Digital high level input voltage 2	V_{IH2}	DVDD -0.4	-	-	V	DVDD=1.8V
Digital low level input voltage 1	V_{IL1}	-	-	0.2 DVDD	V	DVDD=3.0V
Digital low level input voltage 2	V_{IL2}	-	-	0.4	V	DVDD=1.8V
Digital high level input current	I_{IH}	-	-	1	µA	VIH=DVDD
Digital low level input current	I_{IL}	-	-	1	µA	VIL=DVSS
Digital high level output voltage	V_{OH}	DVDD -0.5	-	-	V	IOH=-1mA
Digital low level output voltage	V_{OL}	-	-	0.5	V	IOL=1mA
Digital AC characteristics						
SCL clock frequency	f_{SCL}	-	-	400	kHz	
Bus free time	t_{BUF}	1.3	-	-	µs	
(Iterative) start condition setup time	$t_{SU;STA}$	0.6	-	-	µs	
(Iterative) start condition hold time	$t_{HD;STA}$	0.6	-	-	µs	
SCL low time	t_{LOW}	1.3	-	-	µs	
SCL high time	t_{HIGH}	0.6	-	-	µs	
Data setup time	$t_{SU;DAT}$	100	-	-	ns	
Data hold time	$t_{HD;DAT}$	0	-	-	ns	
Stop condition setup time	$t_{SU;STO}$	0.6	-	-	µs	
Current consumption AVDD=DVDD=PVDD=2.8V input signal = no signal.						
Standby current	I_{ST}	-	-	3	µA	After a reset
TX_OUT path current	I_{DD1}	-	1.3	2.2	mA	MIC1_IN→MIX6→TX_OUT
HF_OUT path current	I_{DD2}	-	1.4	2.4	mA	RX_IN→MIX2→HF_OUT
BT_OUT path current	I_{DD3}	-	1.3	2.2	mA	RX_IN→MIX2→BT_OUT
Reciever path current	I_{DD4}	-	2.5	4.2	mA	RX_IN→MIX2→RCVP_OUT、 RCVN_OUT
Headphone path current	I_{DD5}	-	3.5	5.9	mA	DACL_IN→MIX2→HPL_OUT DACR_IN→MIX3→HPR_OUT
Speaker path current	I_{DD6}	-	1.9	3.2	mA	DACL_IN→MIX4→SPL_OUT DACR_IN→MIX5→SPR_OUT
Full operation current	I_{DD9}	-	8.5	13.5	mA	All paths are ON
Microphone bias current	I_{DD8}	-	250	430	µA	BIAS_ON＝！

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○External measure and View
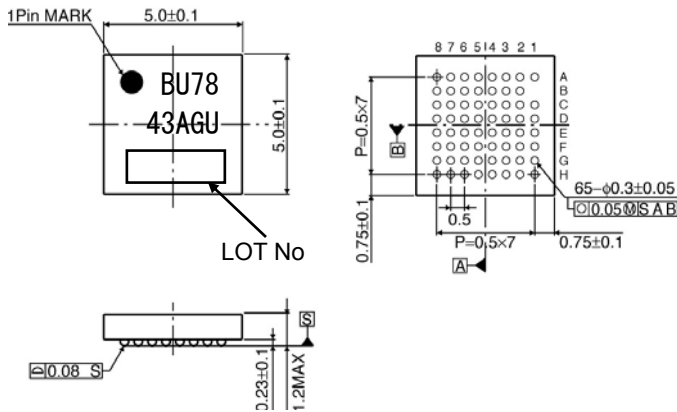
VBGA063T050　（Unit: mm）

○Pin layout diagram

Pin NO.	Pin name	Pin NO.	Pin name	Pin NO.	Pin name
A1	N. C.	F4	KB0	C8	RCVP_OUT
C3	MIC1_IN	H4	DVDD	C7	CPOP
C2	MIC2_IN	G5	DVSS	B8	N. C.
D2	MIC3_IN	F5	KB1	B7	N. C.
C1	AUX1_IN	H5	KB2	A8	N. C.
D3	DACR_IN	E5	KB3	A7	N. C.
D1	AUX2_IN	H6	KB4	C6	SPL_OUT
E2	DACL_IN	G6	KB5	B6	SPR_OUT
E3	RX_IN	H7	N. C.	B5	HF_OUT
E1	SDA	G7	N. C.	A6	BT_OUT
E4	SDL	H8	N. C.	C5	TX_OUT
F1	KBR0	G8	N. C.	A5	COMOUT
F2	KBR1	F6	IRQ	B4	COMIN
G1	N. C.	F7	RSTB	C4	AVDD
G2	N. C.	F8	HPR_OUT	A4	AVSS
H1	N. C.	E6	HPL_OUT	D4	CBIAS
H2	N. C.	E8	CHPL	A3	MIC1_OUT
F3	KBR2	D7	PVSS	B3	MICB
G3	KBR3	D6	PVDD	A2	N. C.
G4	KBR4	D8	RCVN_OUT	B3	N. C.
H3	KBR5	D5	CSTEP		

○Block diagram
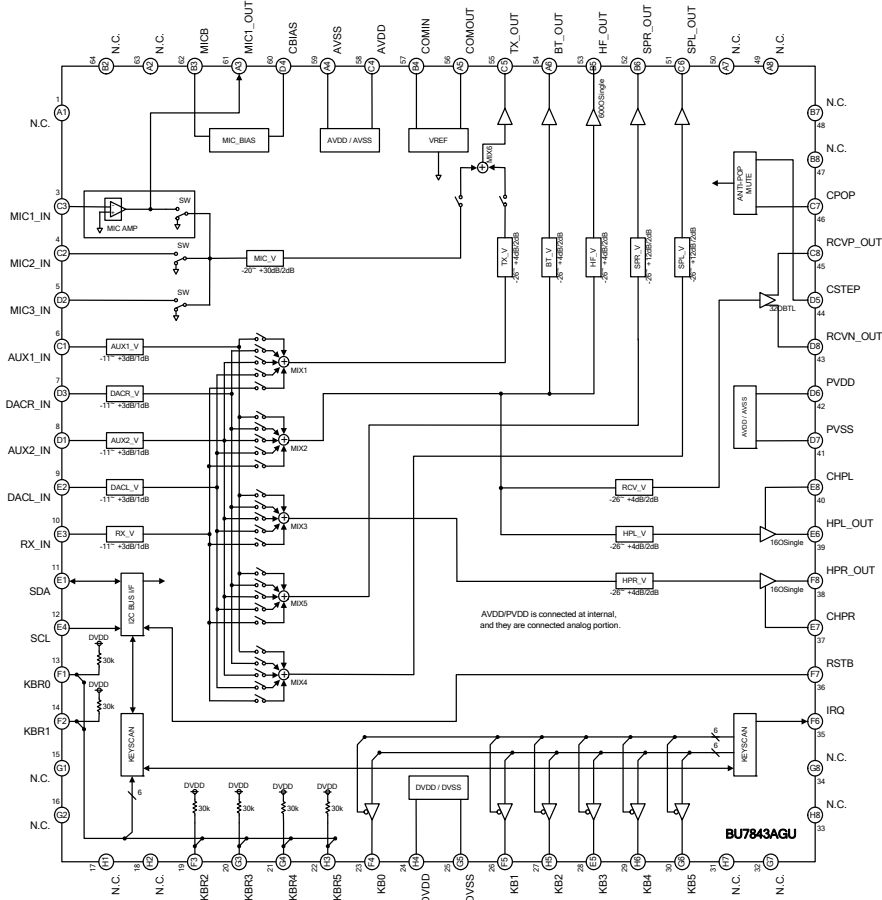
○Cautions on use

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions

These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranted under the conditions of each parameter.

(3) Reverse connection of power supply connector

The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines.In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.

Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern

If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(12) Others

In case of use this LSI, please peruse some other detail documents, we called ,Technical note, Functinal description, Application note.

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