



Display Specification

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DATE : June. 22. 2007

SAMSUNG TFT-LCD

MODEL NO : LMS250GF03-001

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AMLCD DIVISION

Samsung Electronics Co. , LTD.

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Revision History

Preliminary

Data	Rev. No.	Page	Summary
June. 22. 2007	000		Rev.000 was first issued.

General Description

* Description

LMS250GF03-001 is a TMR(Transmissive with Micro Reflective) type color active matrix TFT (Thin Film Transistor) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching devices. This model is composed of a TFT-LCD module, a driver circuit and a back-light unit. The resolution of a 2.5" contains 320 x 240 dots and can display up to 16,777,216 colors.

* Features

- Transmissive with Micro Reflective type and back-light with 3 LEDs.
- TN mode (Normally White).
- Wide Viewing Angle.
- Stripe Pixel structure.
- 8bit RGB parallel Interface + Serial Peripheral Interface (SPI)
- Gate Driver IC embeded on Panel
- Low Power consumption.

* Applications

- Display terminals for HHP, MP3, PMP application products.

* General information

Items	Specification	Unit	Note
Display Area	50.88(H) x 38.16(V)	mm	-
Driver Element	a-Si TFT active matrix	-	-
Display Colors	16.7 M	color	-
Number of Pixels	320(H) x 240(V)	pixel	-
Pixel Arrangement	Stripe Structure	-	-
Pixel Pitch	0.159(H) x 0.159(V)	mm	-
Display Mode	Normally White	-	-
Gray Inversion Angle	12	o'clock	-
Surface Treatment	2H	-	-

* Mechanical information

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)	55.73	55.88	56.03	mm	(1)
	Vertical(V)	47.81	47.96	48.11	mm	(1)
	Depth(D)	2.25	2.4	2.55	mm	(1)
Weight		-	10.4	-	g	(2)

Note (1) : Not include FPC

Note (2) : Included FPC

1. Absolute Maximum Ratings

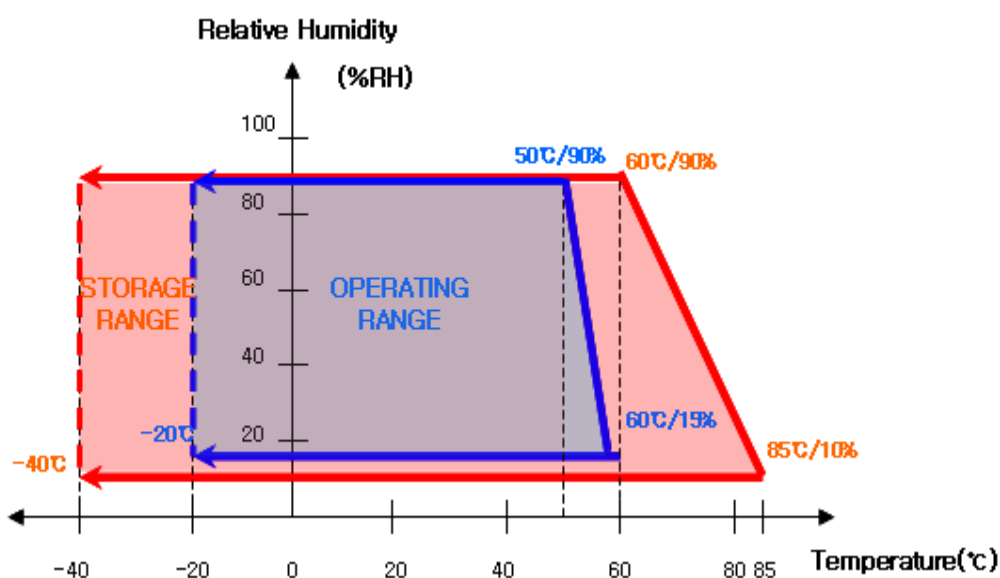
1.1 Absolute Ratings of Environment

Item	Symbol	Min.	Max.	Unit	Note
Storage temperature	T _{STG}	-40	85	°C	(1)
Operating temperature (Ambient temperature)	T _{OPR}	-20	60	°C	(1),(2)

Note (1) 90 % RH Max. (50°C ³ Ta)

Maximum wet-bulb temperature at 49°C or less. (Ta > 50°C)

No condensation.



(2) In case of below 0°, the response time of liquid crystal (LC) becomes slower and the color of panel becomes darker than normal one. Level of retardation depends on temperature, because of LC's characteristics.

(3) If any fixed pattern is displayed on LCD for minutes, image-sticking phenomenon may occur.

1.2 Electrical Absolute Ratings

(1) TFT-LCD Module

(Ta = 25°C ± 2°C, GND=0V)

Characteristics	Symbol	Min.	Max.	Unit	Note
Logic Input Voltage	VDD3	-0.3	5.0	V	(1)
Analog Input Voltage	VCI	-0.3	5.0	V	(1)

(2) Back-Light Unit

(Ta = 25 ± 2°C)

Item	Symbol	Min.	Max.	Unit.	Note
Current	I _B	-	30	mA	(1)

Note (1) Permanent damage to the device may occur if maximum values are exceeded or reverse voltage is loaded.

Functional operation should be restricted to the conditions described under normal operating conditions.

2. Optical Characteristics

The following items are measured under stable conditions. The optical characteristics should be measured in a dark room or equivalent state with the methods shown in Note (1). Measuring equipment: SR-3, BM-7, EZ-Contrast

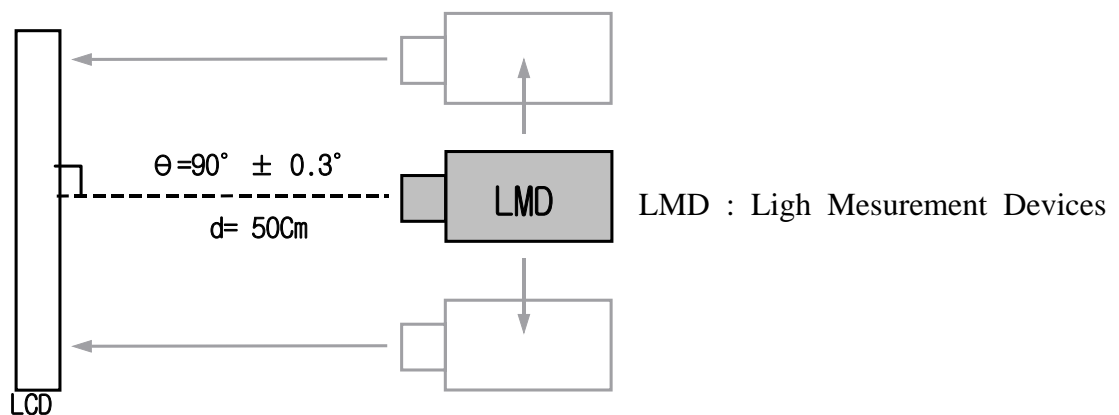
(Ta = 25 ± 2°C, VDD3 = VCI = 3.0V, Ib = 25mA)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast ratio (Center point)	C/R	Note (1), (6)	-	(300)	-	-	(2) SR-3
Luminance of white (Center point)	Y _L		-	(330)	-	cd/m ²	(3) SR-3
Response time	Rising: Tr	Tr+Tf	Φ = 0 Θ = 0	(27)	(35)	msec	(4) BM-7
	Falling: Tf						
Color chromaticity (CIE 1931)	White	W _x	Normal Viewing Angle B/L On	TBD	TBD	TBD	-
		W _y		TBD	TBD	TBD	
	Red	R _x		TBD	TBD	TBD	
		R _y		TBD	TBD	TBD	
	Green	G _x		TBD	TBD	TBD	
		G _y		TBD	TBD	TBD	
	Blue	B _x		TBD	TBD	TBD	
		B _y		TBD	TBD	TBD	
Viewing angle	Hor.	Θ _L	(60)	(70)	-	Degrees	(6) Ez - Contrast
		Θ _R	(60)	(70)	-		
	Ver.	Φ _H	(60)	(60)	-		
		Φ _L	(45)	(60)	-		

Note (1) Test Equipment Setup

After stabilizing and leaving the panel alone at a given temperature for 30 min, the measurement should be executed. Measurement should be executed in a stable, windless, and dark room. 30 min after lighting the back-light. This should be measured in the center of screen.

- Environment condition : $T_a = 25 \pm 2 \text{ }^\circ\text{C}$
- Back-Light On condition



Note (2) Definition of Contrast Ratio (C/R) : Ratio of gray max (Gmax) & gray min (Gmin) at the center point

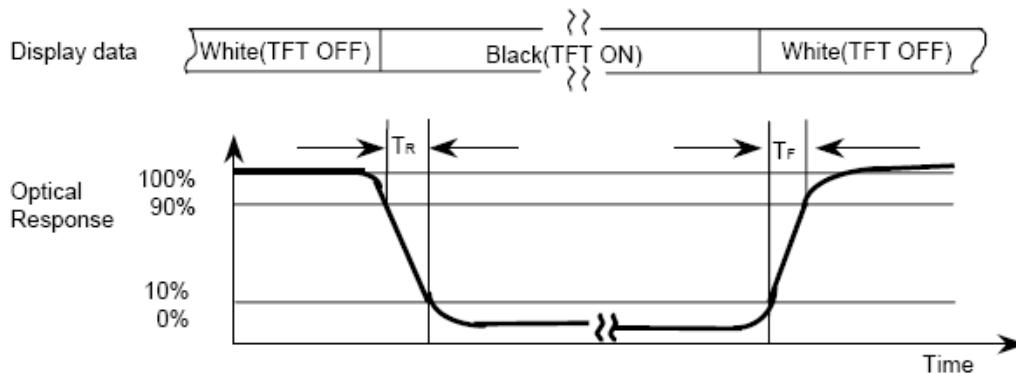
$$CR = \frac{G \text{ max}}{G \text{ min}}$$

- * Gmax : Luminance with all dots white
- * Gmin : Luminance with all dots black

Note (3) Definition of Luminance of White (YL)

: Luminance of white at the center point

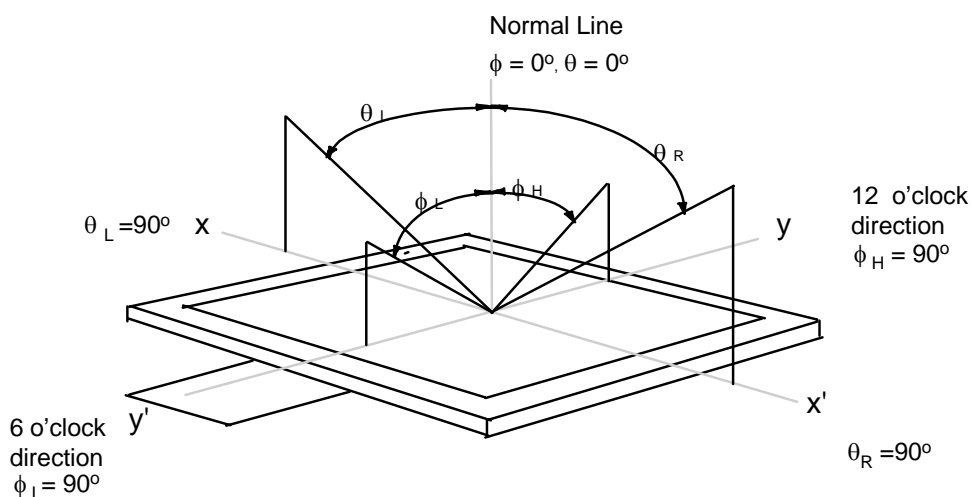
Note (4) Definition of Response time : Sum of T_r and T_f (Field : 1°)



Note (5) Definition of Color Chromaticity (CIE 1931)

Color coordinate of white & red, green, blue at center point.

Note (6) Definition of Viewing Angle : Viewing angle range ($CR \geq 10$)



3. Electrical Characteristics

3.1 TFT-LCD Module

$T_a = 25 \pm 2^\circ\text{C}$

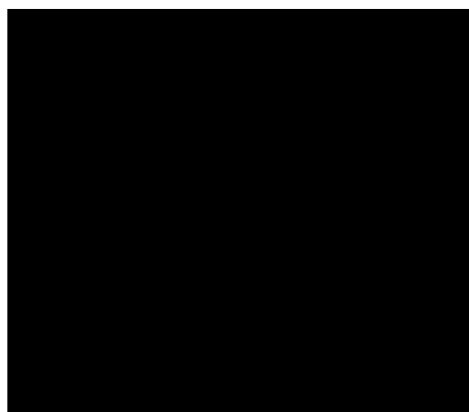
Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Logic Input Voltage	VDD	2.7	3.0	3.3	V	-
Analog Input Voltage	VCI	2.7	3.0	3.3	V	-
Power Dissipation	P _{FULL}	-	(30)	-	mW	(1),(2)
Frame frequency	f _{Frame}	-	90	-	Hz	-
Dot Clock	DCK	-	-	27	MHz	-
Serial Clock	XSCK	-	-	10	MHz	-

* To prevent a latch-up or DC operation of the LCD module, the power on/off sequence should be as the Chapter 10. Power On/Off Sequence.

Note (1) VDD3 = VCI = 3.0V f_{Frame} = 90 Hz

(2) Dissipation current check pattern

▶ Black pattern



3.2 Back-Light unit

The back-light system is an edge-lighting type with three white LED (Light Emitting Diode)s.

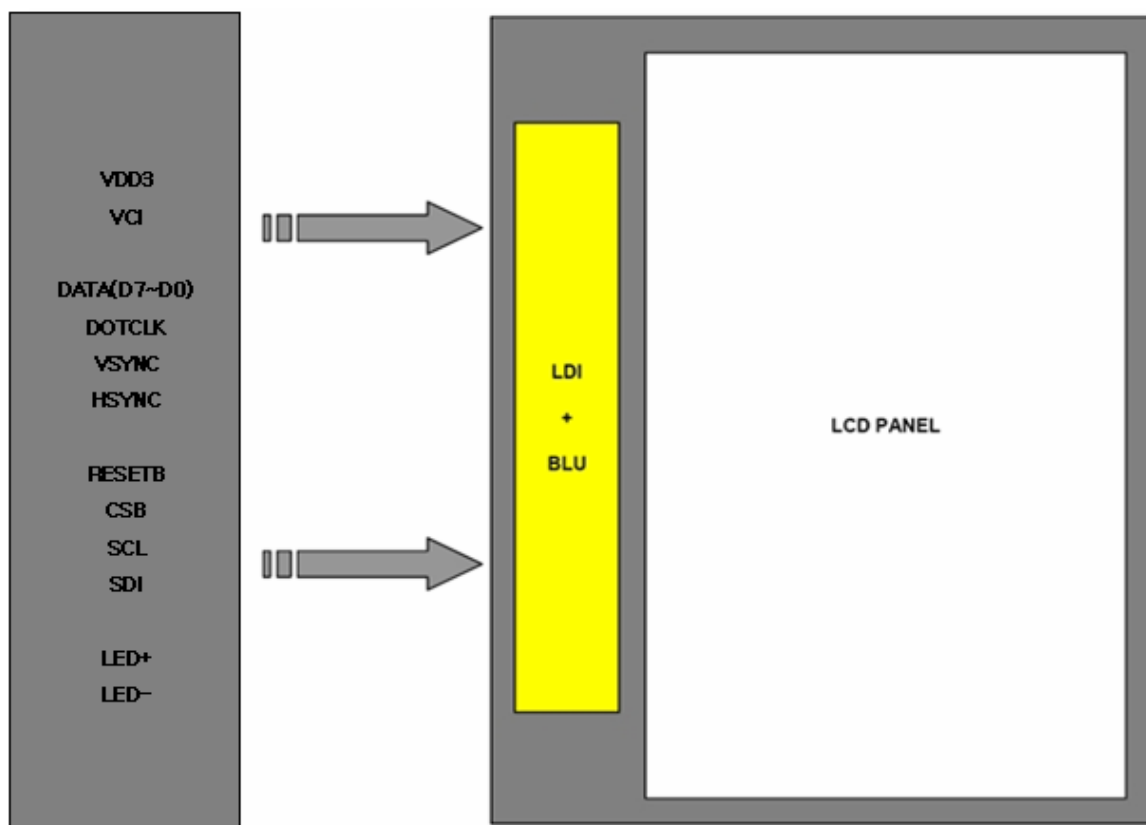
(Ta=25 ± 2°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Current	I _B	-	25	-	mA	(1)
Power Consumption	P _{BL}	-	(264)	-	mW	-

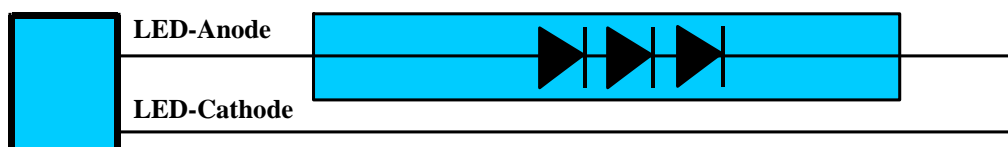
Note (1) Three LEDs serial type.

4. Block Diagram

4.1 TFT-LCD Module (Interface System Structure)



4.2 Back Light Unit



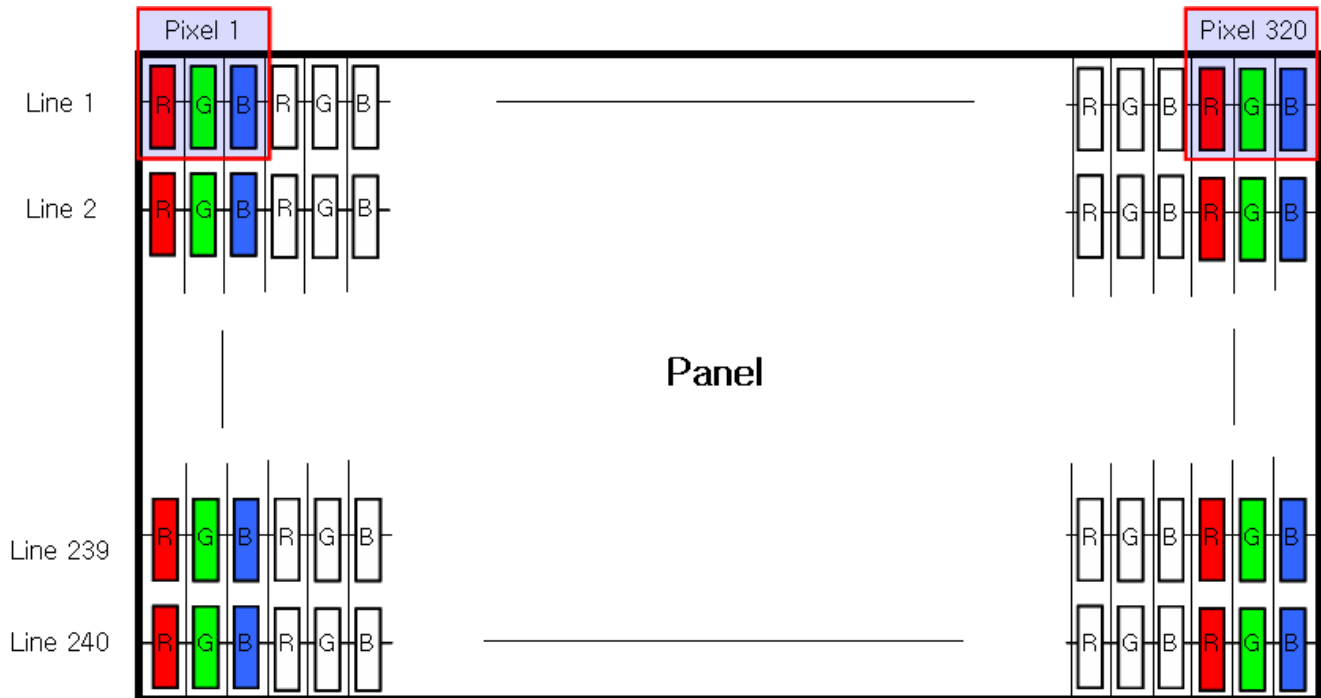
5. Input Terminal Pin Assignment

5.1 Input Signal & Power (Connector : DDK FF12A-51A-R11B, 51Pin, 0.3mm Pitch)

Pin No	Symbol	Description	I/O	Pin No	Symbol	Description	I/O
1	LED-	LED Cathode	I	27	VCOMH	VCOM High Level	O
2	NC	Not Connection	-	28	VOCML	VCOM Low Level	O
3	LED+	LED Anode	I	29	GVDD	Gamma Voltage Generator	O
4	NC	Not Connection	-	30	RVDD	Regulated VDD output	O
5	VGOFFL	Power Output for ASG driver	O	31	GND	Ground	I
6	GND	Ground	I	32			
7	VGL	Gate off Voltage	O	33	VDD3	Logic Input Voltage (typ 3.0V)	I
8	GND	Ground	I	34			
9	VGH	Gate on Voltage	O	35	VSYNC	Vsync signal	I
10	C22P	Charge pumping capacitor	O	36	HSYNC	Hsync signal	I
11	C22M	Charge pumping capacitor	O	37	GND	Ground	I
12	C21P	Charge pumping capacitor	O	38	DOTCLK	Dot clock signal	I
13	C21M	Charge pumping capacitor	O	39	GND	Ground	I
14	AVDD	Power output for Source Driver	O	40	DATA7	Data 7 (MSB)	I
15	C11Pb	Charge pumping capacitor	O	41	DATA6	Data 6	I
16	C11Mb	Charge pumping capacitor	O	42	DATA5	Data 5	I
17	C11P	Charge pumping capacitor	O	43	DATA4	Data 4	I
18	C11M	Charge pumping capacitor	O	44	DATA3	Data 3	I
19	GND	Ground	I	45	DATA2	Data 2	I
20	VCI1	Reference Voltage in step-up circuit 1	I	46	DATA1	Data 1	I
21	VCI	Analog Input Voltage (typ 3.0V)	I	47	DATA0	Data 0 (LSB)	I
22				48	SCL	Serial Clock	I
23	C23M	Charge pumping capacitor	O	49	CSB	Chip Select	I
24	C23P	Charge pumping capacitor	O	50	SDI	Serial Data Input	I
25	VCL	Power Supply for Generating VCOML	O	51	RESETB	RESETB	I
26	GND	Ground	I				

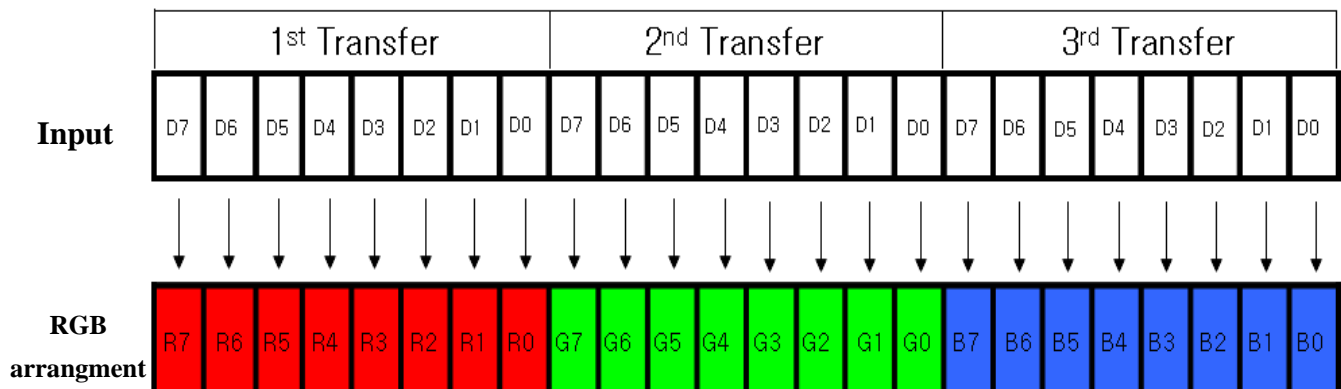
6. Operation Specifications

6.1 Pixel Formation (Stripe Pixel Structure)



6.2 Data Format for 8bit RGB Interface

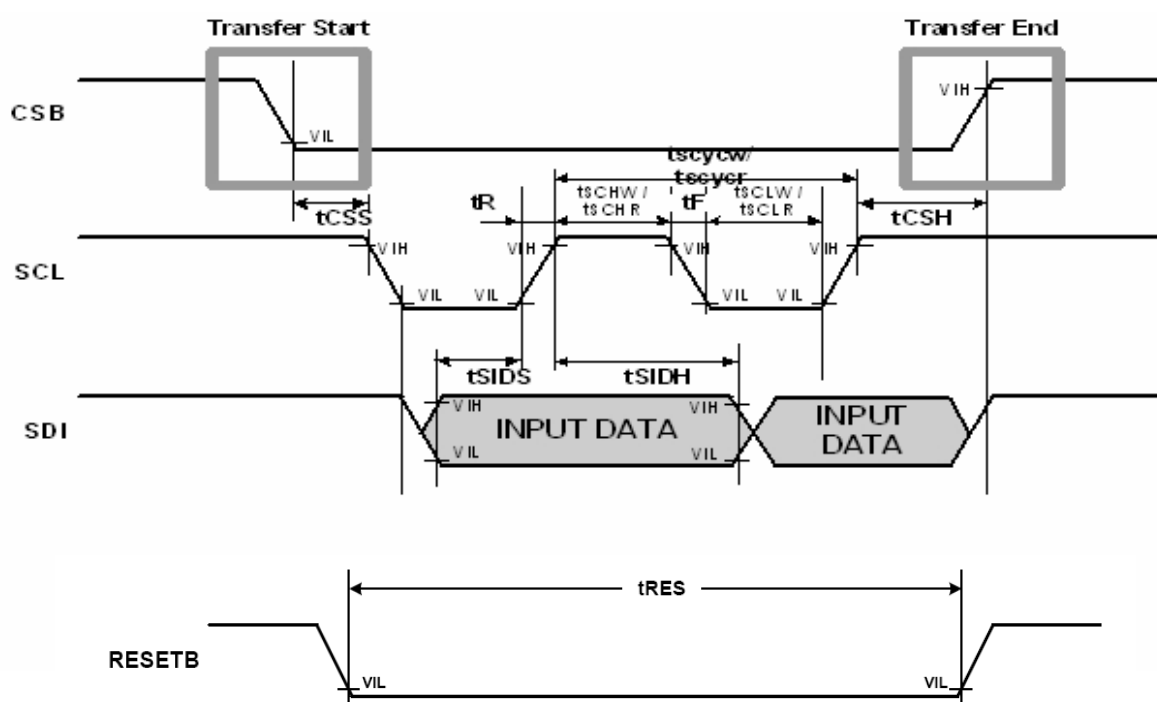
8bit 3times Transfer



8. Electrical Specifications

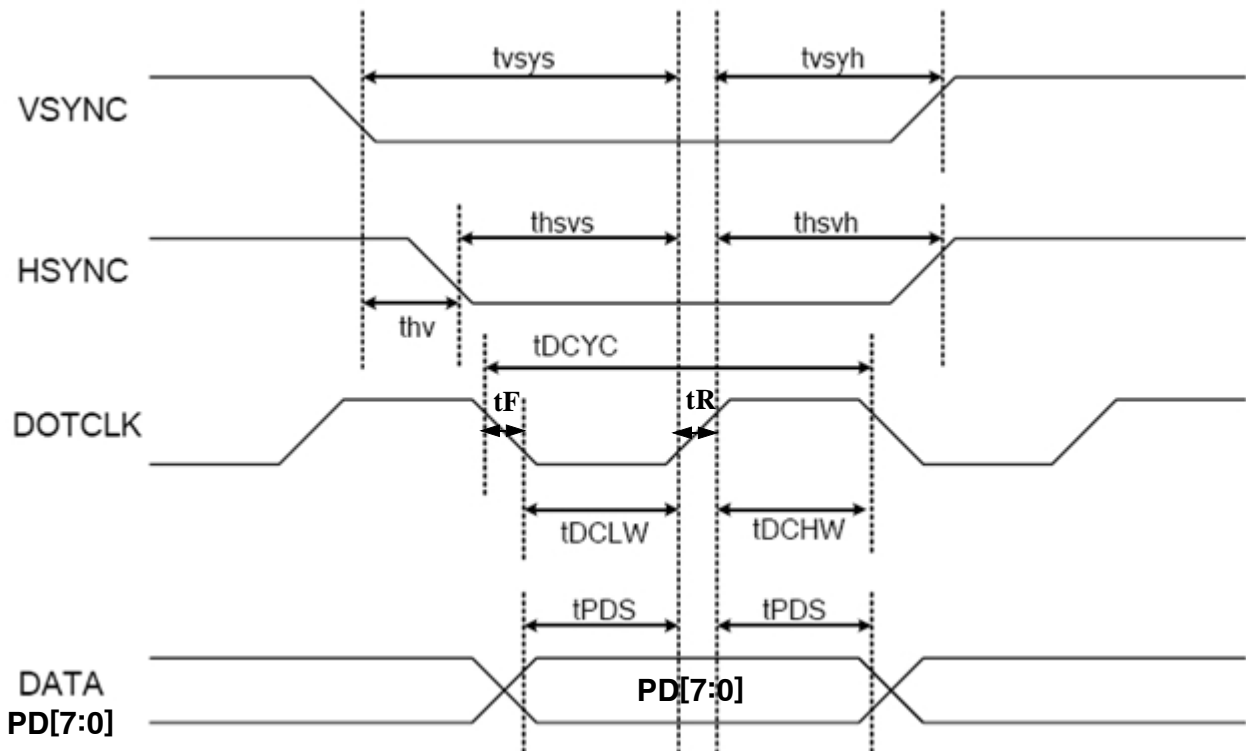
VDD3 = 3.0V, Ta = 25°C ± 2°C

Item	Symbol	Min.	Max.	Unit
Serial Clock Cycle Time	tSCYCW	100	-	ns
Serial Clock rise/fall time	tR,tF	-	10	
Pulse width high for write	tSCHW	30	-	
Pulse width low for write	tSCLW	50	-	
Chip Select Setup Time	tCSS	20	-	
Chip Select Hold Time	tCSH	90	-	
Serial Input Data Setup Time	tSIDS	30	-	
Serial Input Data Hold Time	tSIDH	30	-	
Serial Output Data delay Time	tSODD	-	200	
Serial Output Data Hold Time	tSODH	5	-	
Reset Low Pulse Width	tRES	30	-	
CSB Low Pulse Width for Wake up	tCSBR	12	-	



VDD3 = 3.0V, Ta = 25°C ± 2°C

Item	Symbol	Min.	Typ.	Max.	Unit
Vsync/Hsync Setup Time	Tvsys Thsvs	20	-	-	ns
Vsync/Hsync Hold Time	Tvsyh Thsyh	20	-	-	
Dotclk Low Level Pulse Width	tDCLW	17	-	-	
Dotclk High Level Pulse Width	tDCHW	17	-	-	
Dotclk Cycle Time	tDCYC	35	-	-	
PD(Data) Setup Time	tPDS	12	-	-	
PD(Data) Hold Time	tPDH	12	-	-	
Dotclk Rise/Fall Time	tR, tF	-	-	5	
Phase difference of Sync signal Falling Edge	thv	-	0	-	t _{dotclk}



9. Power On/Off Sequence (*Can be changed for better quality)

9.1 Power On Sequence

System Power On	System Power On wait 1ms Reset
Power Setting Sequence	R07h=0000 wait 10ms R12h=1618 R11h=2227 R13h=XXD1 (Note 5) R10h=550C wait 5frame or more R12h=0C58
Initializing Sequence	R01h= (note 1) R02h=0300 R03h=(note 2) R08h= (note 3) R09h= (note 4) R76h=2213 R0Bh=33E1 R0Ch=0023 R76h=0000 R0Dh=0007 R0Eh=0000 R15h=0803 R14h=0000 R16h=0000 R30h=0706 R31h=0406 R32h=0C09 R33h=0606 R34h=0706 R35h=0406 R36h=0C06 R37h=0601 R38h=0504 R39h=0504
Display On Sequence	R07h=0001 wait 1frame or more R07h=0101 wait 2frame or more R76h=2213 R1Ch=6650 R0Bh=33E1 R76h=0000 R07h=0103

9.2 Power Off Sequence

Display Off Sequence	R0Bh=30E1h R07h=0102h wait 2frame or more R07h=0000h R12h=0000h R10h=0100h
-----------------------------	--

9.3 Standby In / Out Sequence

Standby In Sequence	Display On Status Display off Sequence R10h=0001h
----------------------------	--

Standby Out Sequence	Standby In Status R10h=0000h Power Setting Sequence Display On Sequence
-----------------------------	--

Note 1) Inversion Setting

DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	BGR	0	TB	SS	0	0	0	1	1	1	0	1

- * **BGR** : Color Inversion (0 : R ↔ B, 1 : bypass)
- * **TB** : Vertical Inversion (0 : Bottom → Top, 1 : Top → Bottom)
- * **SS** : Horizontal Inversion (0 : Right → Left, 1 : Left → Right)

Note 2) Polarity Setting

DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
VPL	HPL	DPL	1	0	0	0	0	0	1	0	0	0	0	0	0

- * **VPL** : Vsync Polarity (0 : High Active, 1 : Low Active)
- * **HPL** : Hsync Polarity (0 : High Active, 1 : Low Active)
- * **DPL** : Dotclk Polarity (0 : Data fetched at falling edge, 1 : at rising edge)

Note 3) VBP (Vsync Back Porch)

DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0

VBP 7	VBP 6	VBP 5	VBP 4	VBP 3	VBP 2	VBP 1	VBP 0	Number of Raster Periods In the Back Porch
0	0	0	0	0	0	0	0	3
0	0	0	0	0	0	0	1	3
0	0	0	0	0	0	1	0	4
0	0	0	0	0	0	1	1	5
0	0	0	0	0	1	0	0	6
⋮								⋮
1	1	1	1	1	1	0	0	254
1	1	1	1	1	1	0	1	255
1	1	1	1	1	1	1	0	256
1	1	1	1	1	1	1	1	257

* The porch period should meet the following condition.

$$257H \geq VBP \geq 3H, VBP > VLW$$

Note 4) HBP (Hsync Back Porch)

DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	HBP8	HBP7	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0

HBP 8	HBP 7	HBP 6	HBP 5	HBP 4	HBP 3	HBP 2	HBP 1	HBP 0	Number of MCLKs In the Back Porch 24 bit (8 bit)
0	0	0	0	0	0	0	0	0	8 (24)
0	0	0	0	0	0	0	0	1	8 (24)
0	0	0	0	0	0	0	1	0	8 (24)
0	0	0	0	0	0	0	1	1	8 (24)
0	0	0	0	0	0	1	0	0	8 (24)
0	0	0	0	0	0	1	0	1	8 (24)
0	0	0	0	0	0	1	1	0	8 (24)
0	0	0	0	0	0	1	1	1	8 (24)
0	0	0	0	0	1	0	0	0	8 (24)
0	0	0	0	0	1	0	0	1	9 (27)
0	0	0	0	0	1	0	1	0	10 (30)
0	0	0	0	0	1	0	1	1	11 (33)
⋮									⋮
1	1	1	1	1	1	1	0	1	509 (1527)
1	1	1	1	1	1	1	1	0	510 (1530)
1	1	1	1	1	1	1	1	1	511 (1533)

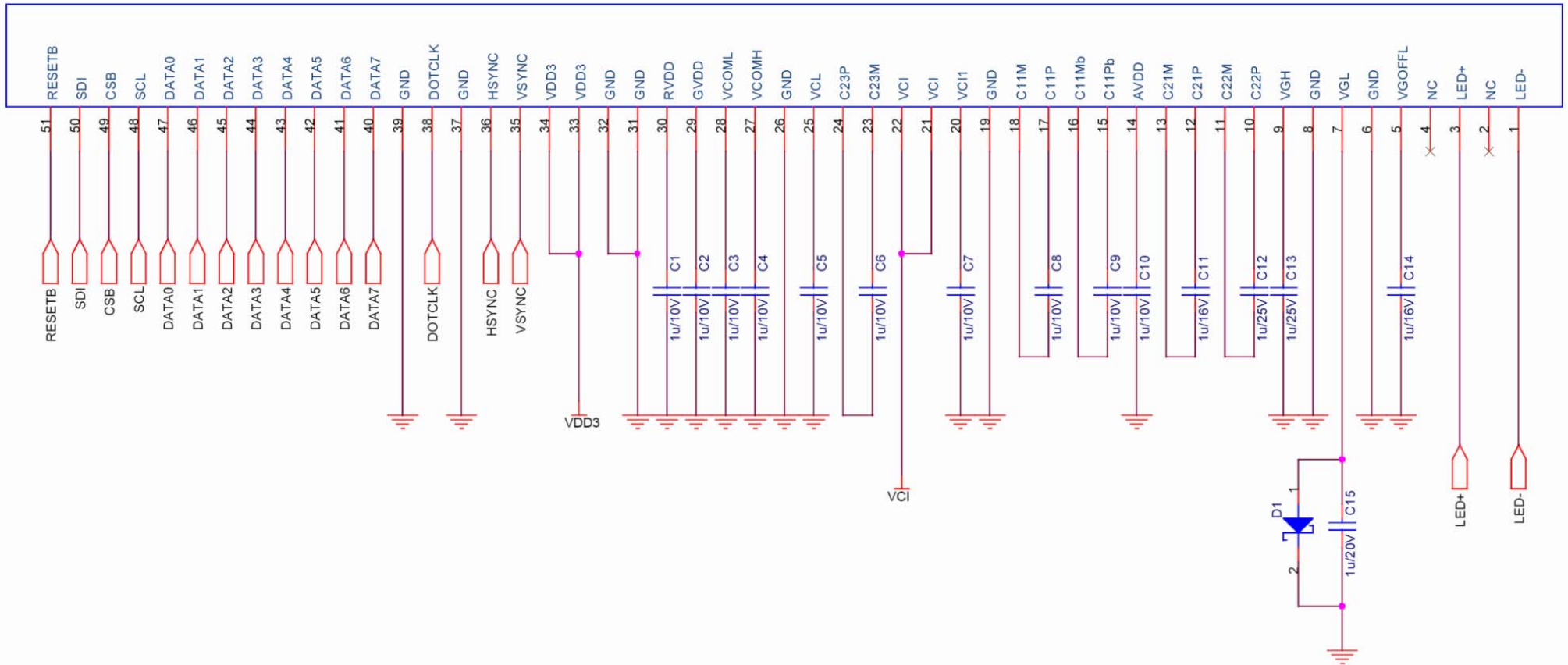
* The porch period should meet the following condition.

$$1533dck \geq HBP \geq 24dck, HBP > HLW$$

Note 5) Brightness Control Setting

XX	Brightness
10	Max
11	↓
12	
...	
61	Recommended
...	
7D	↓
7E	
7F	Min

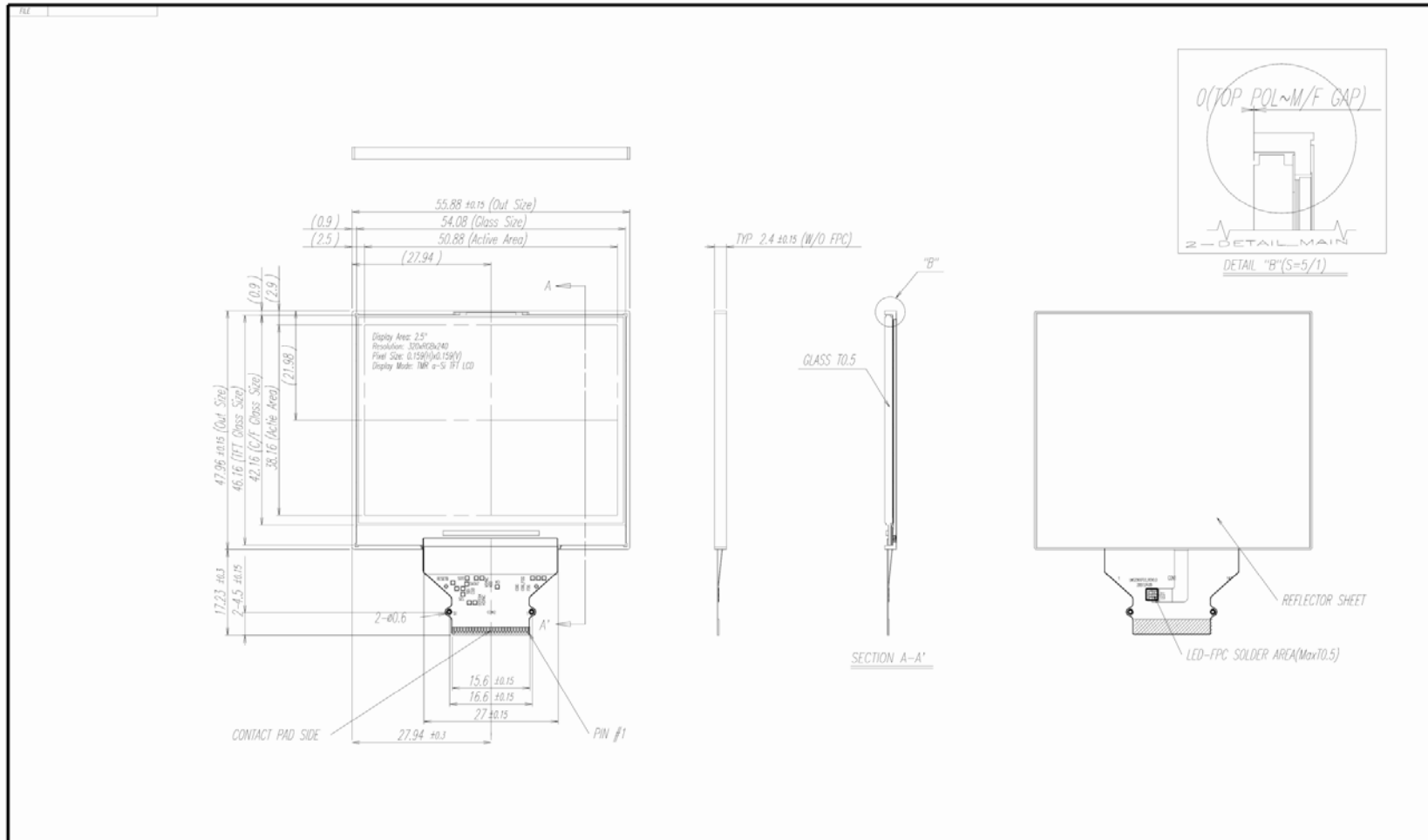
10. Application Circuit



✧ recommends

1. All components would better be close to FPC connector as possible.
2. Schottky diode's low F/V(forward voltage) makes internal circuit more stable.

11. Module outline Dimension

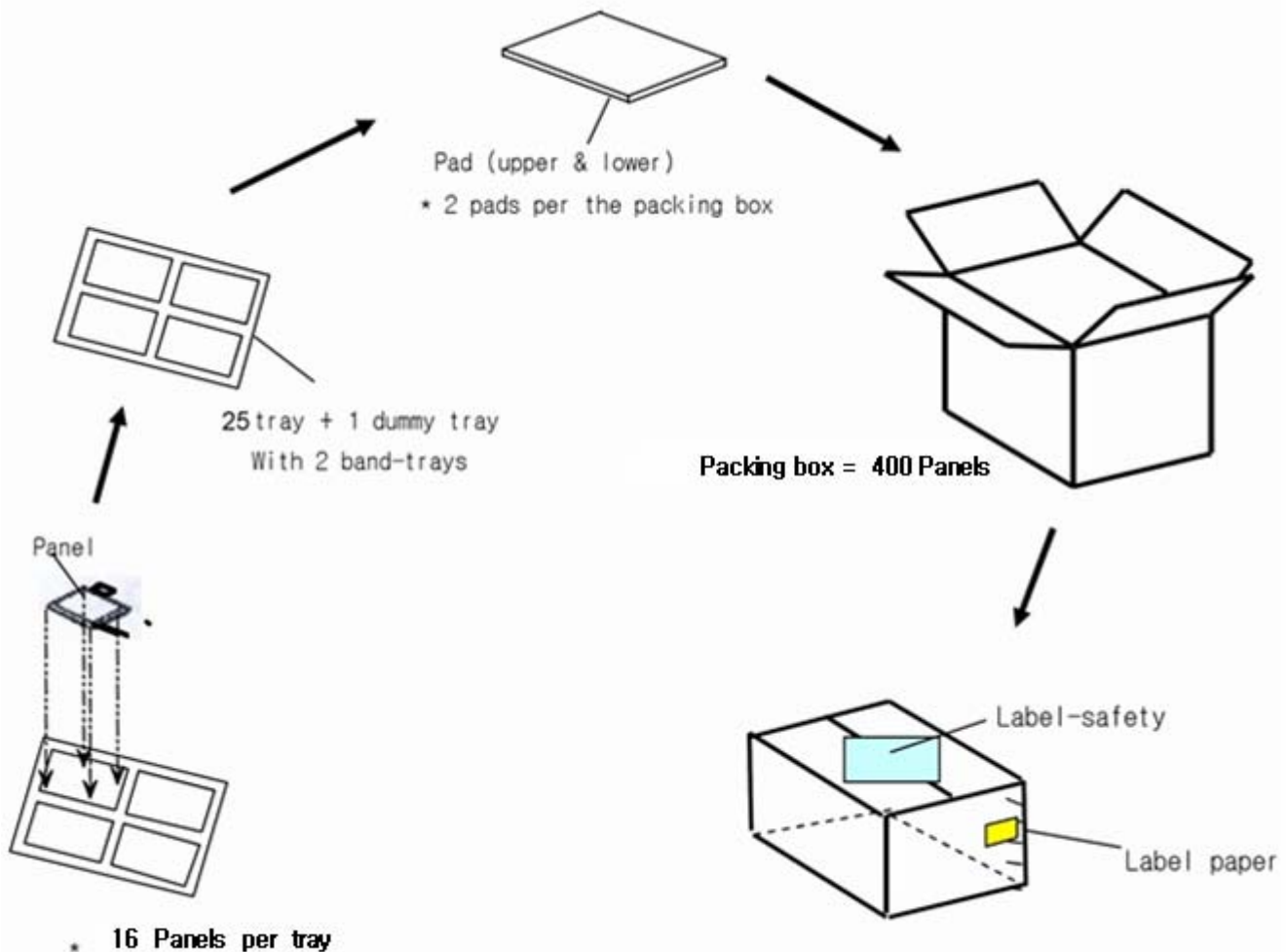


Preliminary

GENERAL TOLERANCE				REV	DATE	DISCRPTION OF REVISION				REASON	CHK'D BY		
STEP	LEVEL 1	LEVEL 2	LEVEL 3	UNIT	mm	DRA'N BY	DES'D BY	CHK'D BY	APP'D BY	MODEL NAME	LMS250GF03		
0 < X ≤ 4	±0.05	±0.1	±0.2	SCALE	1/1	J.J.LEE				PART/SHEET NAME	Outline Dimension	SHEET 1/1	
4 < X ≤ 16	±0.08	±0.15	±0.3	TOLERANCE	LEVEL 3	07.06.15				CODE NO.			
16 < X ≤ 64	±0.12	±0.25	±0.5	SAMSUNG ELECTRONICS									
64 < X ≤ 256	±0.25	±0.4	±0.8										

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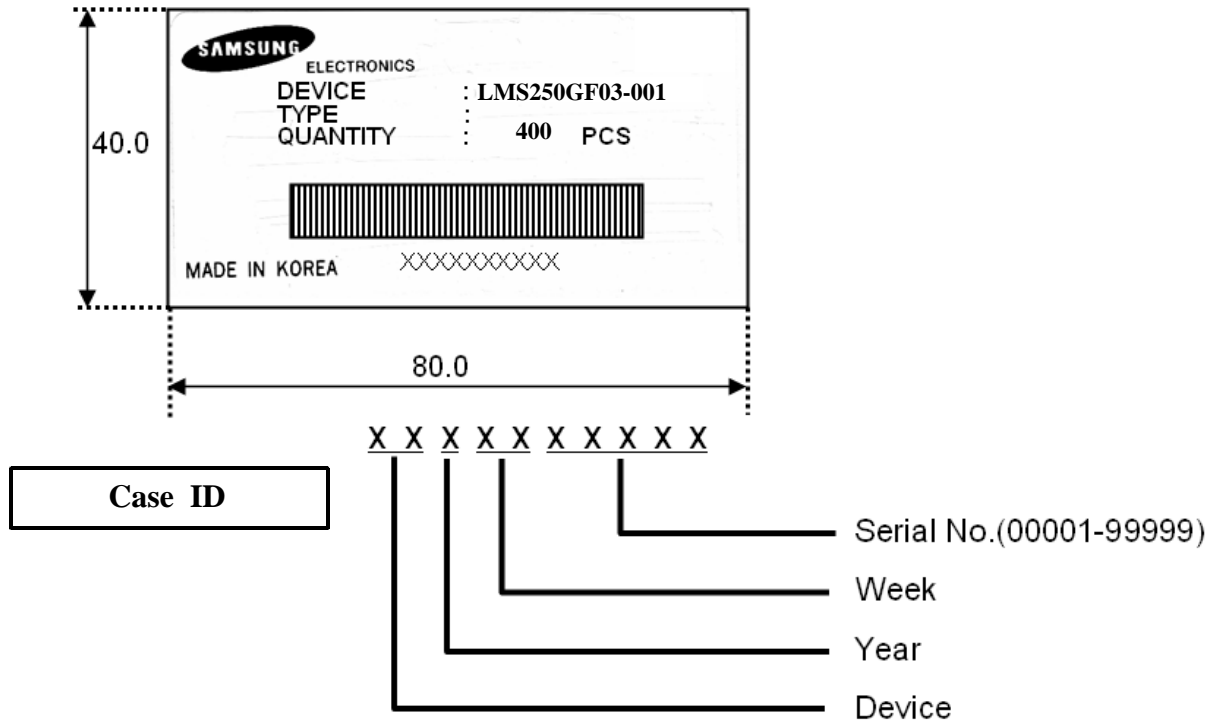
12. Packing



- Note**
- (1) Packing Box Weight : Approx. TBD Kg
 - (2) Packing Box Size : 505(W) x 355(D) x 319(H)
 - (3) Place the panels in the tray facing the direction shown in the figure.
 - (4) Place 25 tray and 1 cover tray and 2 pads inside the packing-box
 - (5) Affix the label-safety, label-paper.

13. Marking & Others

(1) Packing case attach



14. General Precautions

14.1 Handling

- (a) When the module is assembled, it should be attached to the system firmly. Be careful not to twist and bend the module.
- (b) Refrain from strong mechanical shock and / or any force to the module. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
- (c) Note that polarizers are very fragile and could be easily damaged. Do not press or scratch the surface harder than a HB pencil lead.
- (d) Wipe off water droplets or oil immediately. If you leave the droplets for a long time, Staining and discoloration may occur.
- (e) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
- (f) The desirable cleaners are water, IPA(Isopropyl Alcohol) or Hexane. Do not use Ketone type materials(ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
- (g) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs or clothes, it must be washed away thoroughly with soap.
- (h) Protect the module from static, it may cause damage to the Integrated Gate Circuit.
- (i) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (j) Do not disassemble the module.
- (k) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
- (l) Pins of I/F connector shall not be touched directly with bare hands

14.2 Storage

- (a) Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35°C and relative humidity of less than 70%.
- (b) Do not store the TFT-LCD module in direct sunlight.
- (c) The module shall be stored in a dark place. It is prohibited to apply sunlight or fluorescent light during the store.

14.3 Operation

- (a) Do not connect, disconnect the module in the "Power On" condition.
- (b) Power supply should always be turned on/off by the "Power on/off sequence"

14.4 Others

- (a) The Liquid crystal is deteriorated by ultraviolet, do not leave it in direct sunlight and strong ultraviolet ray for many hours.
- (b) Avoid condensation of water. It may result in improper operation or disconnection of electrode.
- (c) Do not exceed the absolute maximum rating value. (the supply voltage variation, input voltage variation, variation in part contents and environmental temperature, and so on) Otherwise the panel may be damaged.
- (d) If the panel displays the same pattern continuously for a long period of time, it can be the situation when the image "Sticks" to the screen.
- (e) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.