

# MC14067B

## Analog Multiplexers / Demultiplexers

The MC14067 multiplexer/demultiplexer is a digitally controlled analog switch featuring low ON resistance and very low leakage current. This device can be used in either digital or analog applications.

The MC14067 is a 16-channel multiplexer/demultiplexer with an inhibit and four binary control inputs A, B, C, and D. These control inputs select 1-of-16 channels by turning ON the appropriate analog switch (see MC14067 truth table.)

- Low OFF Leakage Current
- Matched Channel Resistance
- Low Quiescent Power Consumption
- Low Crosstalk Between Channels
- Wide Operating Voltage Range: 3 to 18 V
- Low Noise
- Pin for Pin Replacement for CD4067B

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 1.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	- 0.5 to + 18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	- 0.5 to $V_{DD} + 0.5$	V
$I_{in}$	Input Current (DC or Transient), per Control Pin	$\pm 10$	mA
$I_{sw}$	Switch Through Current	$\pm 25$	mA
$P_D$	Power Dissipation, per Package (Note 2.)	500	mW
$T_A$	Ambient Temperature Range	- 55 to + 125	$^{\circ}C$
$T_{stg}$	Storage Temperature Range	- 65 to + 150	$^{\circ}C$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}C$

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}C$  From 65 $^{\circ}C$  To 125 $^{\circ}C$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

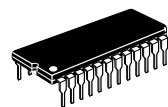
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



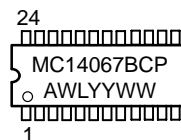
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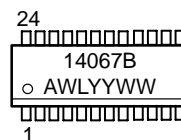
### MARKING DIAGRAMS



PDIP-24  
P SUFFIX  
CASE 709



SOIC-24  
DW SUFFIX  
CASE 751E



A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week

### ORDERING INFORMATION

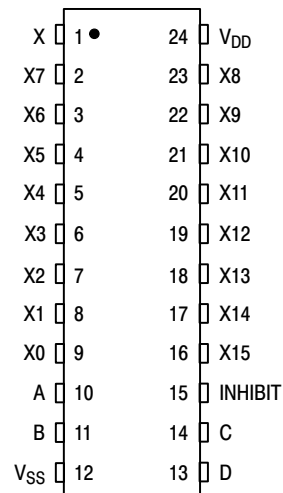
Device	Package	Shipping
MC14067BCP	PDIP-24	15/Rail
MC14067BDW	SOIC-24	30/Rail
MC14067BDWR2	SOIC-24	1000/Tape & Reel

# MC14067B

MC14067 TRUTH TABLE

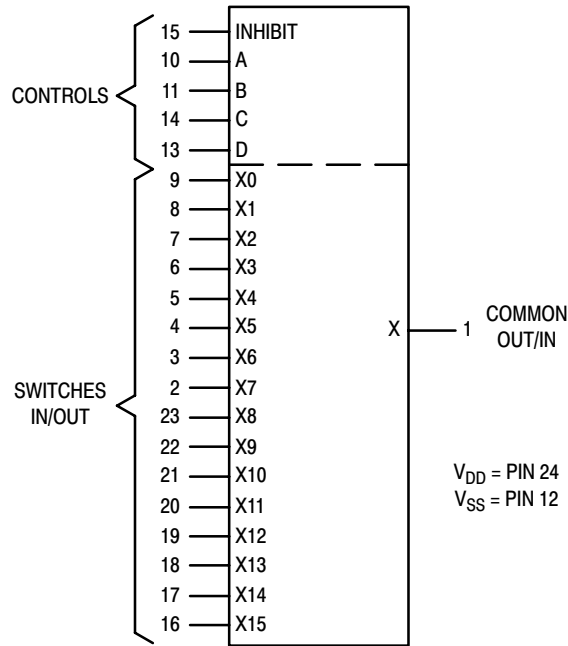
Control Inputs					Selected Channel
A	B	C	D	Inh	
X	X	X	X	1	None
0	0	0	0	0	X0
1	0	0	0	0	X1
0	1	0	0	0	X2
1	1	0	0	0	X3
0	0	1	0	0	X4
1	0	1	0	0	X5
0	1	1	0	0	X6
1	1	1	0	0	X7
0	0	0	1	0	X8
1	0	0	1	0	X9
0	1	0	1	0	X10
1	1	0	1	0	X11
0	0	1	1	0	X12
1	0	1	1	0	X13
0	1	1	1	0	X14
1	1	1	1	0	X15

## MC14067B PIN ASSIGNMENT

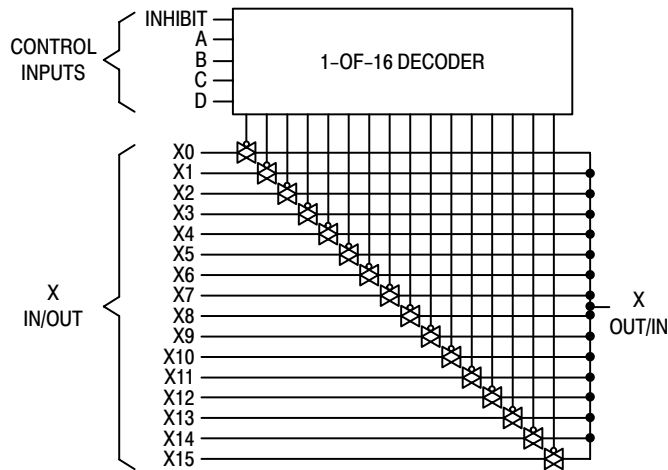


# MC14067B

## MC14067B 16-Channel Analog Multiplexer/Demultiplexer



### MC14067 FUNCTIONAL DIAGRAM



# MC14067B

## ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V <sub>DD</sub>	Test Conditions	- 55°C		25°C			125°C		Unit
				Min	Max	Min	Typ <sup>(3.)</sup>	Max	Min	Max	

### SUPPLY REQUIREMENTS (Voltages Referenced to V<sub>SS</sub>)

Power Supply Voltage Range	V <sub>DD</sub>	—		3.0	18	3.0	—	18	3.0	18	V
Quiescent Current Per Package	I <sub>DD</sub>	5.0 10 15	Control Inputs: V <sub>in</sub> = V <sub>SS</sub> or V <sub>DD</sub> , Switch I/O: V <sub>SS</sub> ≤ V <sub>I/O</sub> ≤ V <sub>DD</sub> , and ΔV <sub>switch</sub> ≤ 500 mV <sup>(4.)</sup>	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	μA
Total Supply Current (Dynamic Plus Quiescent, Per Package)	I <sub>D(AV)</sub>	5.0 10 15	T <sub>A</sub> = 25°C only (The channel component, (V <sub>in</sub> - V <sub>out</sub> )/R <sub>on</sub> , is not included.)	Typical (0.07 μA/kHz) f + I <sub>DD</sub> (0.20 μA/kHz) f + I <sub>DD</sub> (0.36 μA/kHz) f + I <sub>DD</sub>						μA	

### CONTROL INPUTS — INHIBIT, A, B, C, D (Voltages Referenced to V<sub>SS</sub>)

Low-Level Input Voltage	V <sub>IL</sub>	5.0 10 15	R <sub>on</sub> = per spec, I <sub>off</sub> = per spec	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	V
High-Level Input Voltage	V <sub>IH</sub>	5.0 10 15	R <sub>on</sub> = per spec, I <sub>off</sub> = per spec	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	V
Input Leakage Current	I <sub>in</sub>	15	V <sub>in</sub> = 0 or V <sub>DD</sub>	—	±0.1	—	±0.00001	±0.1	—	1.0	μA
Input Capacitance	C <sub>in</sub>	—		—	—	—	5.0	7.5	—	—	pF

### SWITCHES IN/OUT AND COMMONS OUT/IN — X, Y (Voltages Referenced to V<sub>SS</sub>)

Recommended Peak-to-Peak Voltage Into or Out of the Switch	V <sub>I/O</sub>	—	Channel On or Off	0	V <sub>DD</sub>	0	—	V <sub>DD</sub>	0	V <sub>DD</sub>	V <sub>p-p</sub>
Recommended Static or Dynamic Voltage Across the Switch <sup>(4.)</sup> (Figure 1)	ΔV <sub>switch</sub>	—	Channel On	0	600	0	—	600	0	300	mV
Output Offset Voltage	V <sub>OO</sub>	—	V <sub>in</sub> = 0 V, No Load	—	—	—	10	—	—	—	μV
ON Resistance	R <sub>on</sub>	5.0 10 15	ΔV <sub>switch</sub> ≤ 500 mV <sup>(4.)</sup> , V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> (Control), and V <sub>in</sub> 0 to V <sub>DD</sub> (Switch)	— — —	800 400 220	— — —	250 120 80	1050 500 280	— — —	1300 550 320	Ω
ΔON Resistance Between Any Two Channels in the Same Package	ΔR <sub>on</sub>	5.0 10 15		— — —	70 50 45	— — —	25 10 10	70 50 45	— — —	135 95 65	Ω
Off-Channel Leakage Current (Figure 2)	I <sub>off</sub>	15	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> (Control) Channel to Channel or Any One Channel	—	±100	—	±0.05	±100	—	±1000	nA
Capacitance, Switch I/O	C <sub>I/O</sub>	—	Inhibit = V <sub>DD</sub>	—	—	—	10	—	—	—	pF
Capacitance, Common O/I	C <sub>O/I</sub>	—	Inhibit = V <sub>DD</sub> (MC14067B) (MC14097B)	— —	— —	— —	100 60	— —	— —	— —	pF
Capacitance, Feedthrough (Channel Off)	C <sub>I/O</sub>	— —	Pins Not Adjacent Pins Adjacent	—	—	—	0.47	—	—	—	pF

3. Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

4. For voltage drops across the switch (ΔV<sub>switch</sub>) > 600 mV (> 300 mV at high temperature), excessive V<sub>DD</sub> current may be drawn; i.e. the current out of the switch may contain both V<sub>DD</sub> and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

# MC14067B

## ELECTRICAL CHARACTERISTICS ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD} - V_{SS}$ V <sub>dc</sub>	Typ <sup>(5.)</sup>	Max	Unit		
Propagation Delay Times Channel Input-to-Channel Output ( $R_L = 200 \text{ k}\Omega$ ) MC14067B	$t_{PLH}, t_{PHL}$ (Figure 3)	5.0 10 15	35 15 12	90 40 30	ns		
	Control Input-to-Channel Output Channel Turn-On Time ( $R_L = 10 \text{ k}\Omega$ ) MC14067B	$t_{PZH}, t_{PZL}$ (Figure 4)	5.0 10 15	240 115 75	600 290 190	ns	
		Channel Turn-Off Time ( $R_L = 300 \text{ k}\Omega$ ) MC14067B	$t_{PHZ}, t_{PLZ}$ (Figure 4)	5.0 10 15	250 120 75	625 300 190	ns
			Any Pair of Address Inputs to Output MC14067B	$t_{PLH}, t_{PHL}$	5.0 10 15	280 115 85	700 290 215
Second Harmonic Distortion ( $R_L = 10 \text{ k}\Omega$ , $f = 1 \text{ kHz}$ , $V_{in} = 5 V_{p-p}$ )	—			10	0.3	—	%
ON Channel Bandwidth [ $R_L = 1 \text{ k}\Omega$ , $V_{in} = 1/2 (V_{DD} - V_{SS})$ p-p (sine-wave)] $20 \text{ Log}_{10} (V_{out}/V_{in}) = -3 \text{ dB}$ MC14067B	BW (Figure 5)	10		15	—	MHz	
Off Channel Feedthrough Attenuation [ $R_L = 1 \text{ k}\Omega$ , $V_{in} = 1/2 (V_{DD} - V_{SS})$ p-p (sine-wave)] $f_{in} = 20 \text{ MHz}$ – MC14067B	— (Figure 5)	10	-40	—	dB		
Channel Separation [ $R_L = 1 \text{ k}\Omega$ , $V_{in} = 1/2 (V_{DD} - V_{SS})$ p-p (sine-wave)] $f_{in} = 20 \text{ MHz}$	— (Figure 6)	10	-40	—	dB		
Crosstalk, Control Inputs-to-Common O/I ( $R_1 = 1 \text{ k}\Omega$ , $R_L = 10 \text{ k}\Omega$ , Control $t_r = t_f = 20 \text{ ns}$ , Inhibit = $V_{SS}$ )	— (Figure 7)	10	30	—	mV		

5. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

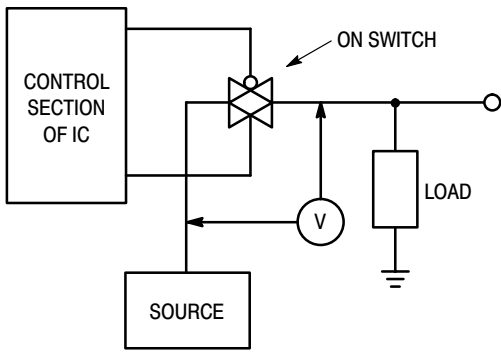


Figure 1.  $\Delta V$  Across Switch

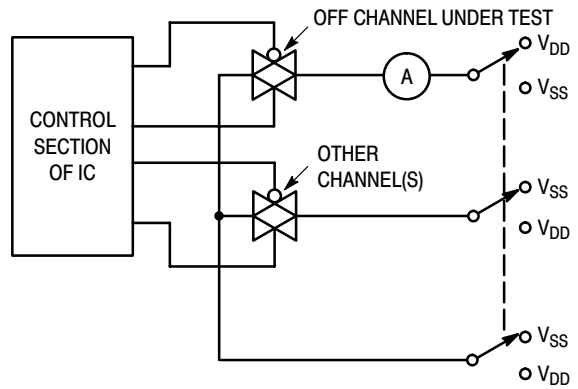


Figure 2. Off Channel Leakage

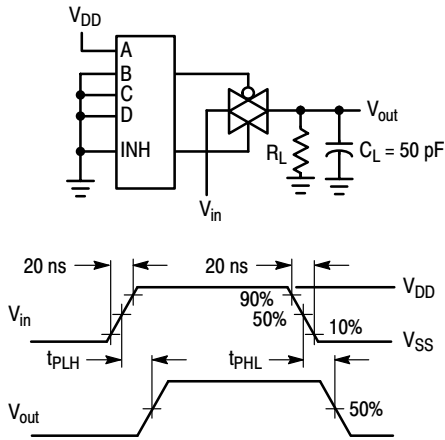


Figure 3. Propagation Delay Test Circuit and Waveforms  $V_{in}$  to  $V_{out}$

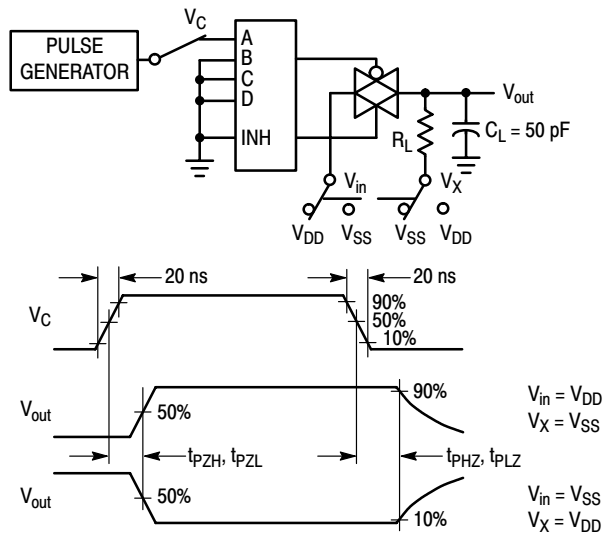
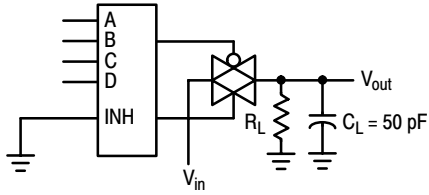


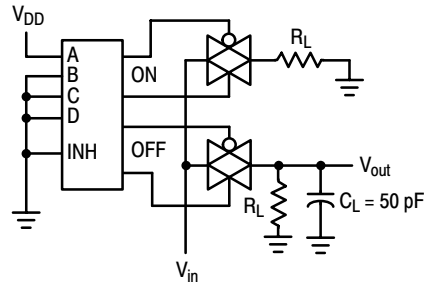
Figure 4. Turn-On and Delay Turn-Off Test Circuit and Waveforms

# MC14067B

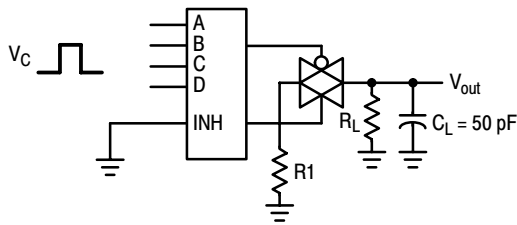
A, B, and C inputs used to turn ON or OFF the switch under test.



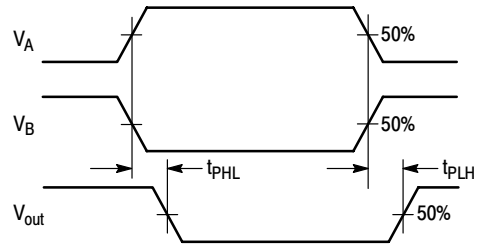
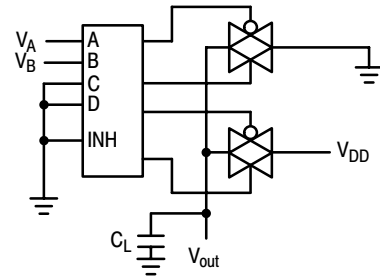
**Figure 5. Bandwidth and Off-Channel Feedthrough Attenuation**



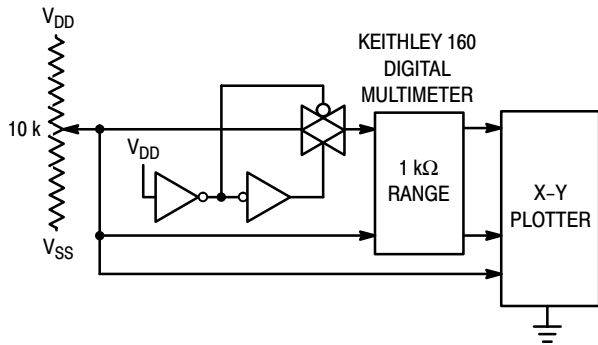
**Figure 6. Channel Separation (Adjacent Channels Used for Setup)**



**Figure 7. Crosstalk, Control to Common O/I**



**Figure 9. Propagation Delay, Any Pair of Address Inputs to Output**



**Figure 8. Channel Resistance ( $R_{ON}$ ) Test Circuit**

TYPICAL RESISTANCE CHARACTERISTICS

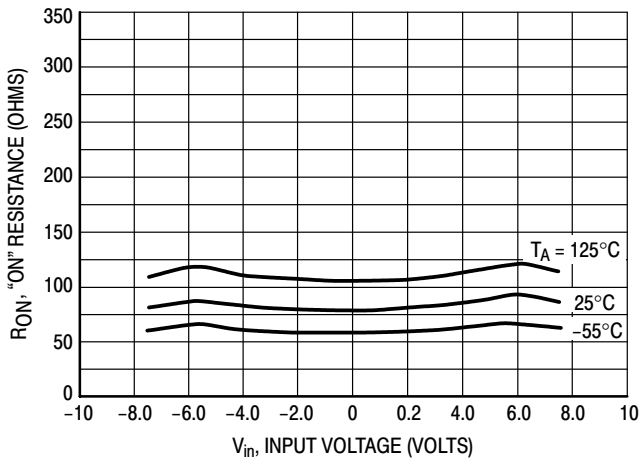


Figure 10.  $V_{DD} = 7.5\text{ V}$ ,  $V_{SS} = -7.5\text{ V}$

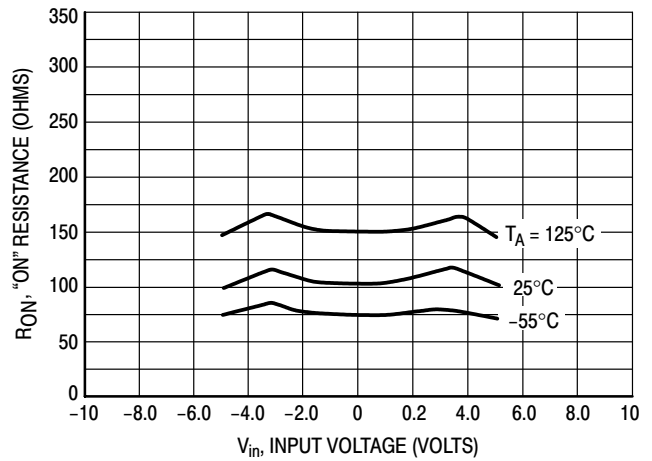


Figure 11.  $V_{DD} = 5.0\text{ V}$ ,  $V_{SS} = -5.0\text{ V}$

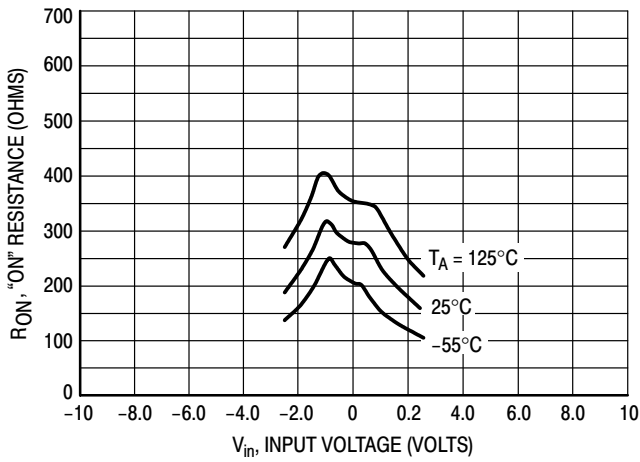


Figure 12.  $V_{DD} = 2.5\text{ V}$ ,  $V_{SS} = -2.5\text{ V}$

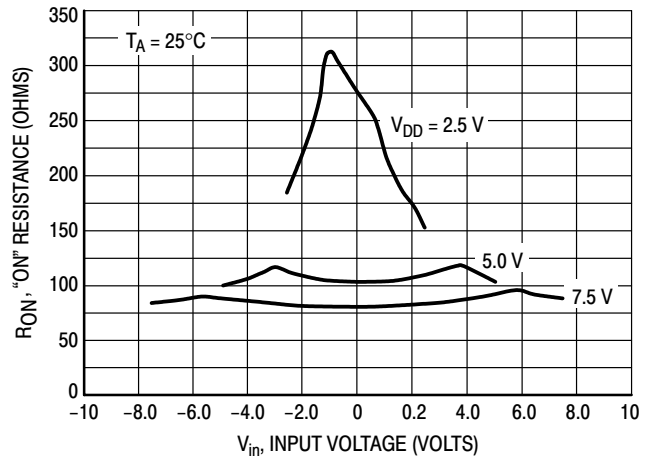


Figure 13. Comparison at 25°C,  $V_{DD} = -V_{SS}$



APPLICATIONS INFORMATION

Figure A illustrates use of the Analog Multiplexer/Demultiplexer. The 0-to-5 volt Digital Control signal is used to directly control a 5 V<sub>p-p</sub> analog signal.

The digital control logic levels are determined by V<sub>DD</sub> and V<sub>SS</sub>. The V<sub>DD</sub> voltage is the logic high voltage; the V<sub>SS</sub> voltage is logic low. For the example, V<sub>DD</sub> = + 5 V = logic high at the control inputs; V<sub>SS</sub> = GND = 0 V = logic low.

The maximum analog signal level is determined by V<sub>DD</sub> and V<sub>SS</sub>. The analog voltage must swing neither higher than V<sub>DD</sub> nor lower than V<sub>SS</sub>. The example shows a 5 V<sub>p-p</sub>

signal which allows no margin at either peak. If voltage transients above V<sub>DD</sub> and/or below V<sub>SS</sub> are anticipated on the analog channels, external diodes (D<sub>x</sub>) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The absolute maximum potential difference between V<sub>DD</sub> and V<sub>SS</sub> is 18.0 volts. Most parameters are specified up to 15 V which is the recommended maximum difference between V<sub>DD</sub> and V<sub>SS</sub>.

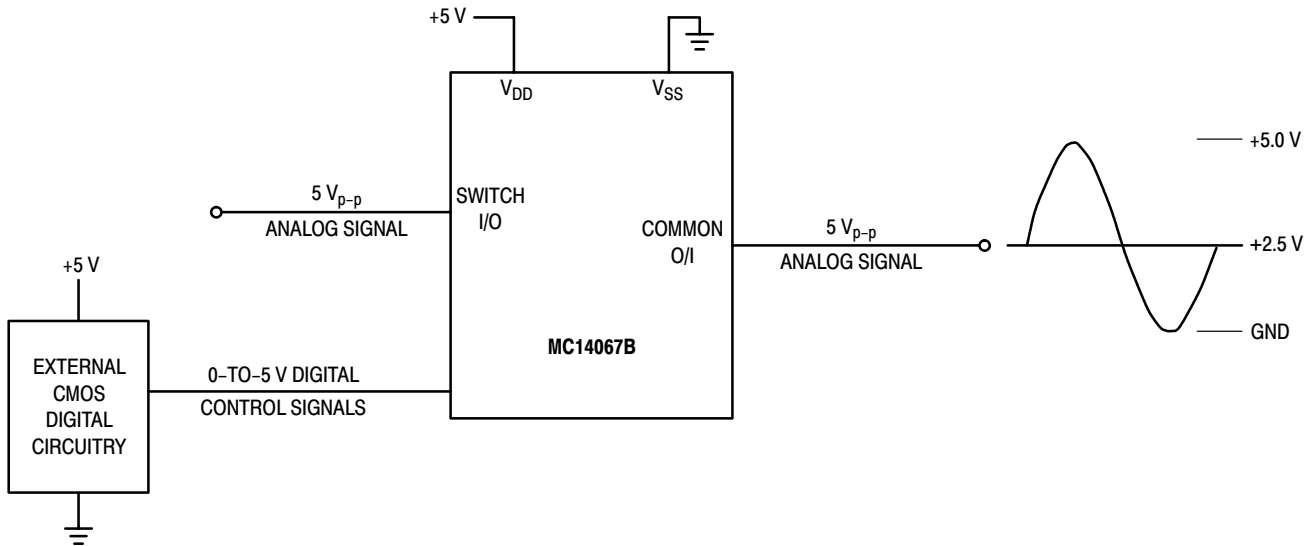


Figure A. Application Example

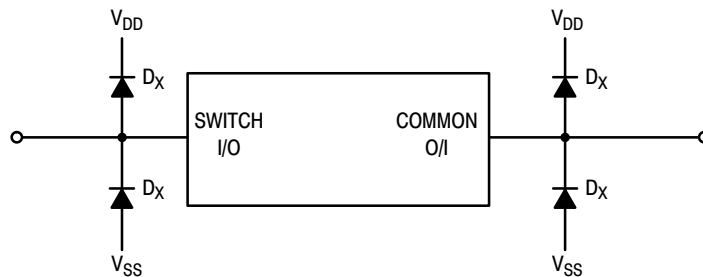
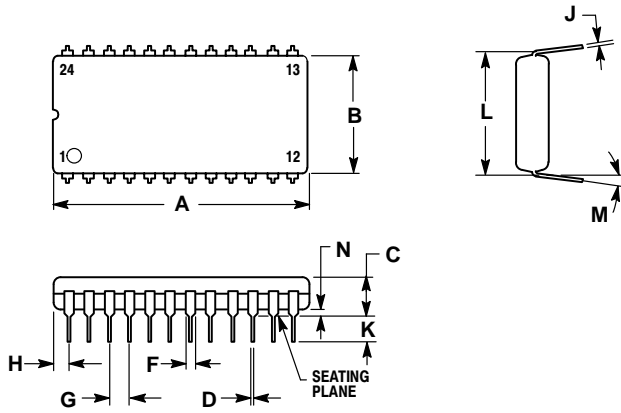


Figure B. External Germanium or Schottky Clipping Diodes

# MC14067B

## PACKAGE DIMENSIONS

PDIP-24  
P SUFFIX  
CASE 709-02  
ISSUE C



NOTES:

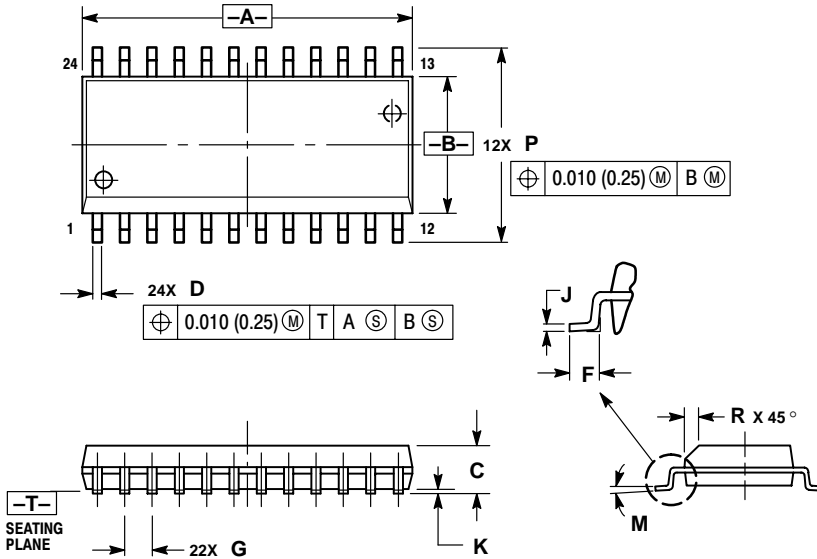
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.235	1.265	31.37	32.13
B	0.540	0.560	13.72	14.22
C	0.155	0.200	3.94	5.08
D	0.014	0.022	0.36	0.56
F	0.040	0.060	1.02	1.52
G	0.100 BSC		2.54 BSC	
H	0.065	0.080	1.65	2.03
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.600 BSC		15.24 BSC	
M	0° 15°		0° 15°	
N	0.020	0.040	0.51	1.02

# MC14067B

## PACKAGE DIMENSIONS


SOIC-24  
DW SUFFIX  
CASE 751E-04  
ISSUE E



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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