PCtel

The Leader in Host Signal Processing (HSP) Modem Technology

PCT1789W Chip Set

PCI HSP56 World MicroModem Data/Fax/Voice Modem Solution

PCT789T-A Features

- 3.3 V PCI HSP Controller
- 56K ITU upgradable/data 14.4K Fax/ADPCM Voice/V.80
- Low power consumption (35 mW operating @ 3.3 V) and auto power management
- Supports Win 95, Win 98, Win NT 4.0 and NT 5.0 operating systems
- Support for D3 cold, VAUX, Wake-on-Ring
- Minimum system configuration: Pentium MMX 166 MHz +, AMD K6 MMX 200 MHz +, or Cyrix 6x86MX PR200 +; 256K Cache; 16 MB RAM
- HSP speakerphone via software upgrade with full-duplex sound chip
- V.80 for Point to Point H.324 video conferencing

PCT789T-A Hardware Features

- PCI interface
  - comply with PCI V2.2 specification
  - comply with PCI Bus Power Management Interface Specification V1.1
- Programmable circular buffer
  - for effectively supporting different sampling rates and protocols
- EEPROM required for storing user defined subsystem ID, subsystem vendor ID, anddevice ID
- Low power consumption
  - power supply range for digital circuit: 3.3 V ± 5%.
  - the lowest power consumptive solution in the modem industry today
  - support power-down mode for CODEC and/or core logic

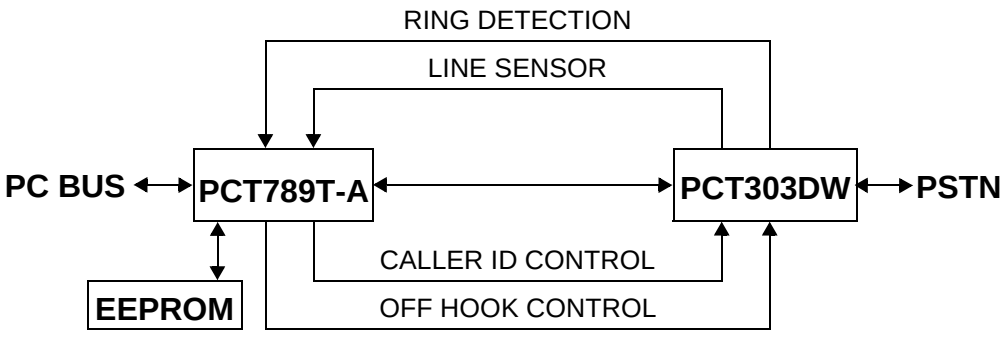
PCT789T-A Functional Description

The PCT789T-A device provides the interface and buffering between PCI bus and CODEC serial interface, input/output port, interrupt control, and auto power-down management. This device works with CODEC, DAA, and PC-TEL's advanced host signal processing software to perform data/fax/voice functions. The figure below shows the hardware block diagram of an internal modem using the PCT789T-A device.

PCT789T-A is a single-chip modem controller which supports PC-TEL Host Signal Processing 56Kbps modem solution. The PCT789T-A provides the most compact, power-saving, and cost-effective solution for 56Kbps internal modems. It can also be used with other hardware such as audio chip and video-conferencing chip sets for combo board applications.

PCT789T-A

PCT1789W Functional Block Diagram



PCT303DW FEATURES

Complete DAA includes:

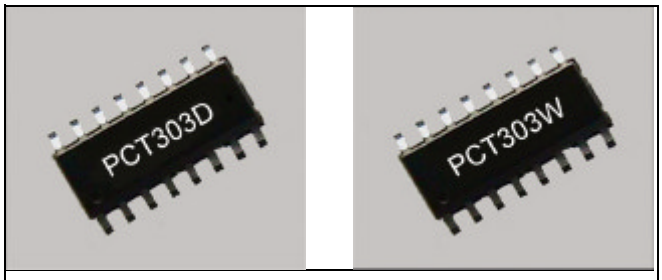
- Programmable line interface
  - AC termination
  - DC termination
  - Ringer impedance
  - Ringer threshold
- 86 dB dynamic range TX/RX paths
- Integrated ring detector
- Up to 4000 V isolation
- Support for Caller ID
- Low-profile SOIC packages
- Low power consumption (15mW operating @3.3V)
- 3.3 or 5 V analog/digital power supply
- Direct interface to DSPs
- Integrated analog front end (AFE)
- 2–4-wire hybrid
- Daisy-chaining for up to eight devices

PCT303DW APPLICATIONS

- Modems
- Phone line interface systems

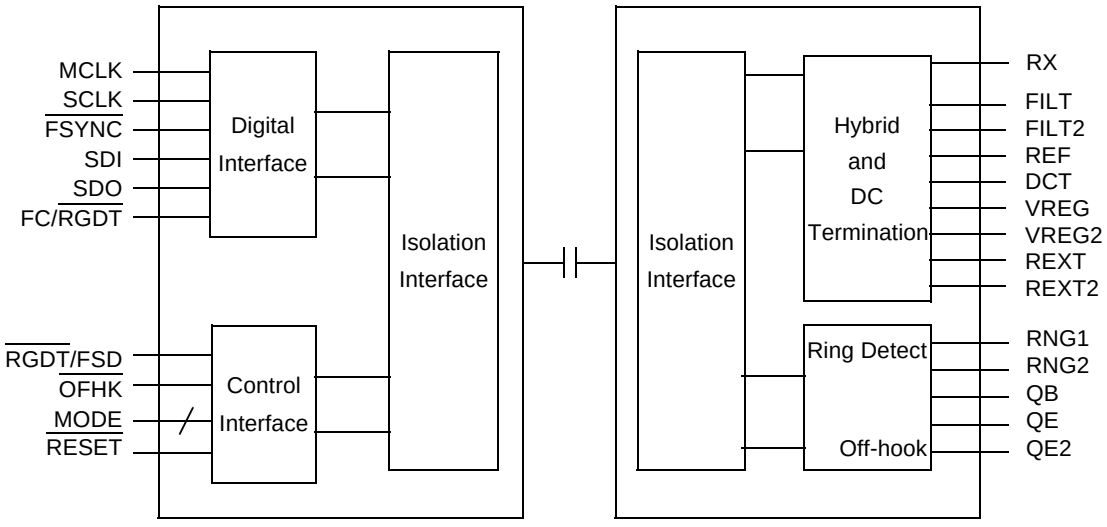
PCT303DW FUNCTIONAL DESCRIPTION

The PCT303DW is an integrated direct access arrangement (DAA) that provides a programmable line interface to meet international telephone line requirements. Available in two 16-pin small outline packages, it eliminates the need for an analog front end (AFE), an isolation transformer, relays, opto-isolators, and 2- to 4-wire hybrid. The PCT303DW dramatically reduces the number of discrete components and cost required to achieve compliance with international regulatory requirements. The PCT303DW interfaces directly to standard modem DSPs.



PCT303DW Chip Set

PCT303DW FUNCTIONAL BLOCK DIAGRAM



PCT303D **PCT303W**

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BLOCK DIAGRAM

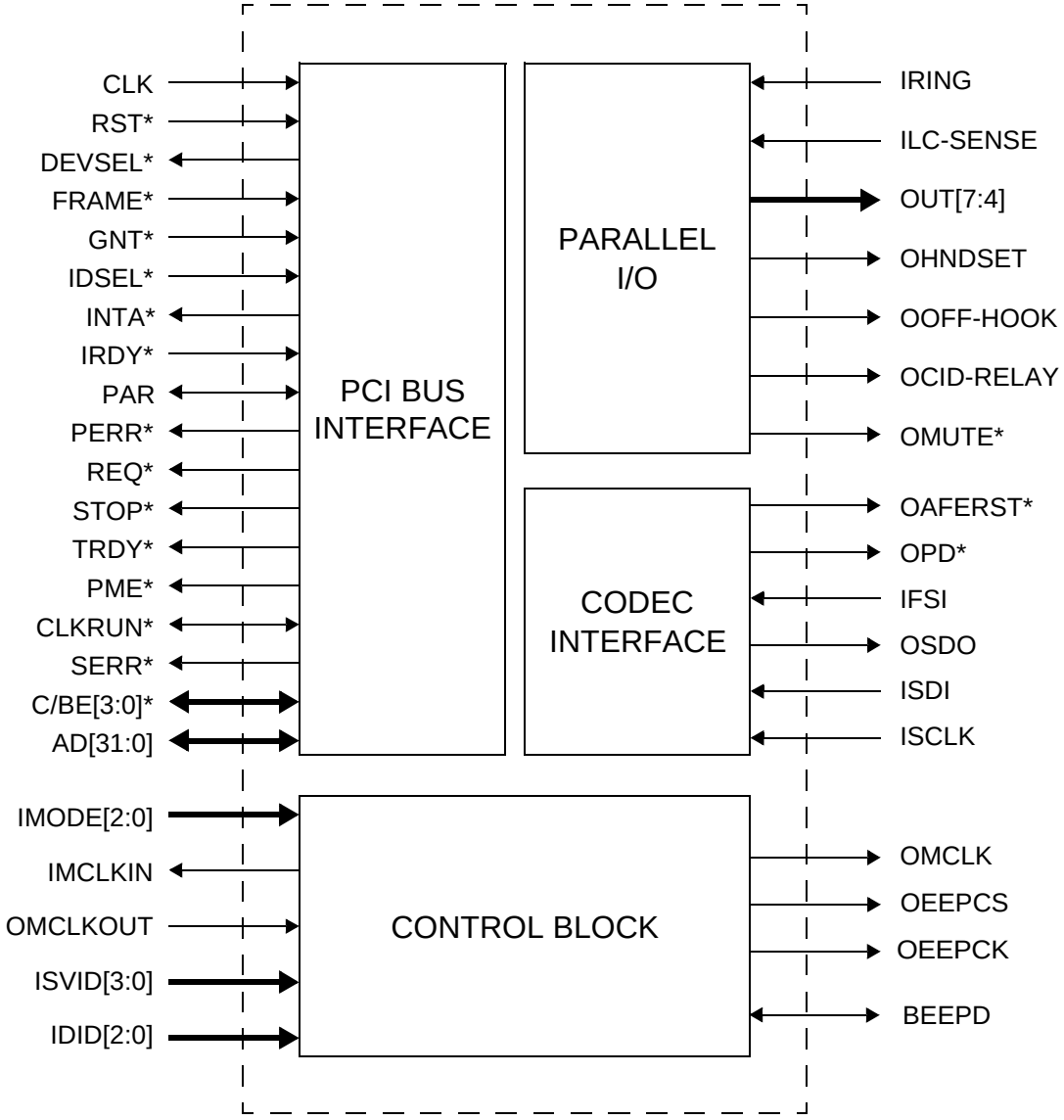


Figure 1 PCT789T-A Block Diagram

PCT303DW APPLICATION CIRCUITS

Typical Application (CTR21 International Design)

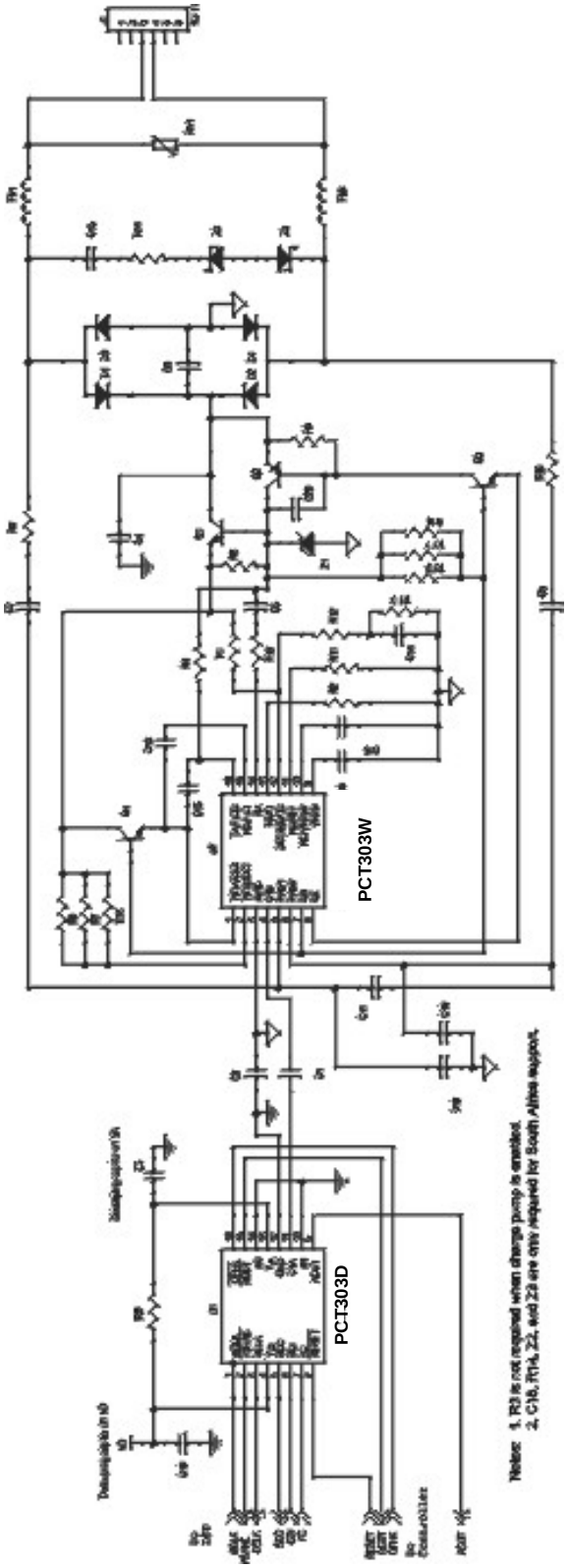


Figure 2 PCT303DW Typical Applications Circuit (CRT21 International Design)

Typical Application Component Values

Table 1 PCT303DW Typical Application Component Values (CTR21 International Design)

Symbol	North American Value	International Value
C1	150pF, 2kV, X7R,±20%	150pF, 3kV, X7R, ±20%
C2,C4	1000pF, 2kV, X7R, ±20%	1000pF, 3kV, X7R, ±20%
C3,C10	0.1µF, 16V, X7R, ±20%	Same as North American
C5	0.47µF, 16V, X7R, ±20%	0.1µF, 50V, X7R, ±20%
C6	0.047µF, 16V, X7R, ±20%	0.1µF, 16V, X7R, ±20%
C7,C8	2200pF, 250V, X7R, ±20%	680pF, 250V, X7R, ±20%
C9	15nF, 250V, X7R, ±20%	22nF, 250V, X7R, ±10%
C11	5600pF, 16V, X7R, ±20%	Not Installed
C12	Not Installed	0.22µF, 16V, X7R, ±20%
C13,C16	Not Installed	0.1µF, 16V, X7R, ±20%
C14	Not Installed	560nF,16V, X7R, ±20%
C15 [a]	Not Installed	0.47µF, 250V, ±20%
C18,C19	Not Installed	3900pF,16V, X7R, ±20%
C20	Not Installed	47pF, 250V, X7R, ±20%
R1	51Ω, 1/2W ±5%	Not Installed
R2	15Ω, 1/4W ±5%	402 Ω, 1/10 W, ±1%
R3 [b]	10Ω, 1/10W, ±5%	Same as North American
R4	604Ω, 1/4W, ±1%	Not Installed
R5	36kΩ, 1/10W ±5%	Same as North American
R6	36kΩ, 1/10W ±5%	121kΩ, 1/10W, ±5%
R7,R8,R15,R16,R17,R19	Not Installed	4.87kΩ, 1/4W, ±1%
R9,R10	10kΩ, 1/4W ±5%	30kΩ, 1/4W, ±5%
R11	Not Installed	10kΩ, 1/10W, ±1%
R12	Not Installed	140Ω, 1/10W, ±1%
R13	Not Installed	442Ω, 1/10W, ±1%
R14 [a]	Not Installed	18.7kΩ, 1/4W, ±1%
R18	0Ω	2.2kΩ, 1/10W, ±5%
Z1	Zener Diode, 18V	Not Installed
Z2,Z3 [a]	Not Installed	Zener Diode, 3V
Q1,Q3	Motorola MMBTA42LT1	Same as North American
Q2	Motorola MMBTA92LT1	Same as North American
Q4	Not Installed	Motorola PZT2222AT1, 1/2W
D1–D4	1N4004	Same as North American
FB1,FB2	Ferrite Bead	Same as North American
RV1	Sidactor 275V, 100A	Same as North American

a. C14, R15, Z2, and Z3 required only for South Africa support.
b. R3 not required when charge pump is enabled.

Analog Output

Figure 3 illustrates an optional application circuit to support the analog output capability of the PCT303DW for call progress monitoring purposes.

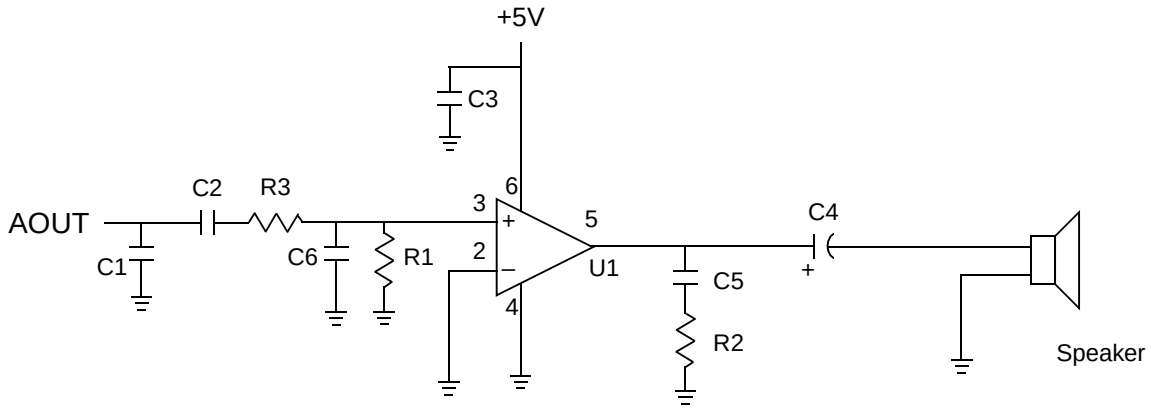


Figure 3 Optional Connection to AOUT For a Call Progress Speaker

Table 2 Optional Connection Component Values

Symbol	Value
C1	2200pF, 16V, ±20%
C2, C3, C5	0.1µF, 16V, ±20%
C4	100µF, 16V, Elec. ±20%
C6	820pF, 16V, ±20%
R1	10kΩ, 1/10W, ±5%
R2	10Ω, 1/10W, ±5%
R3	47kΩ, 1/10W, ±5%
U1	LM386

PCT789T-A PINOUT

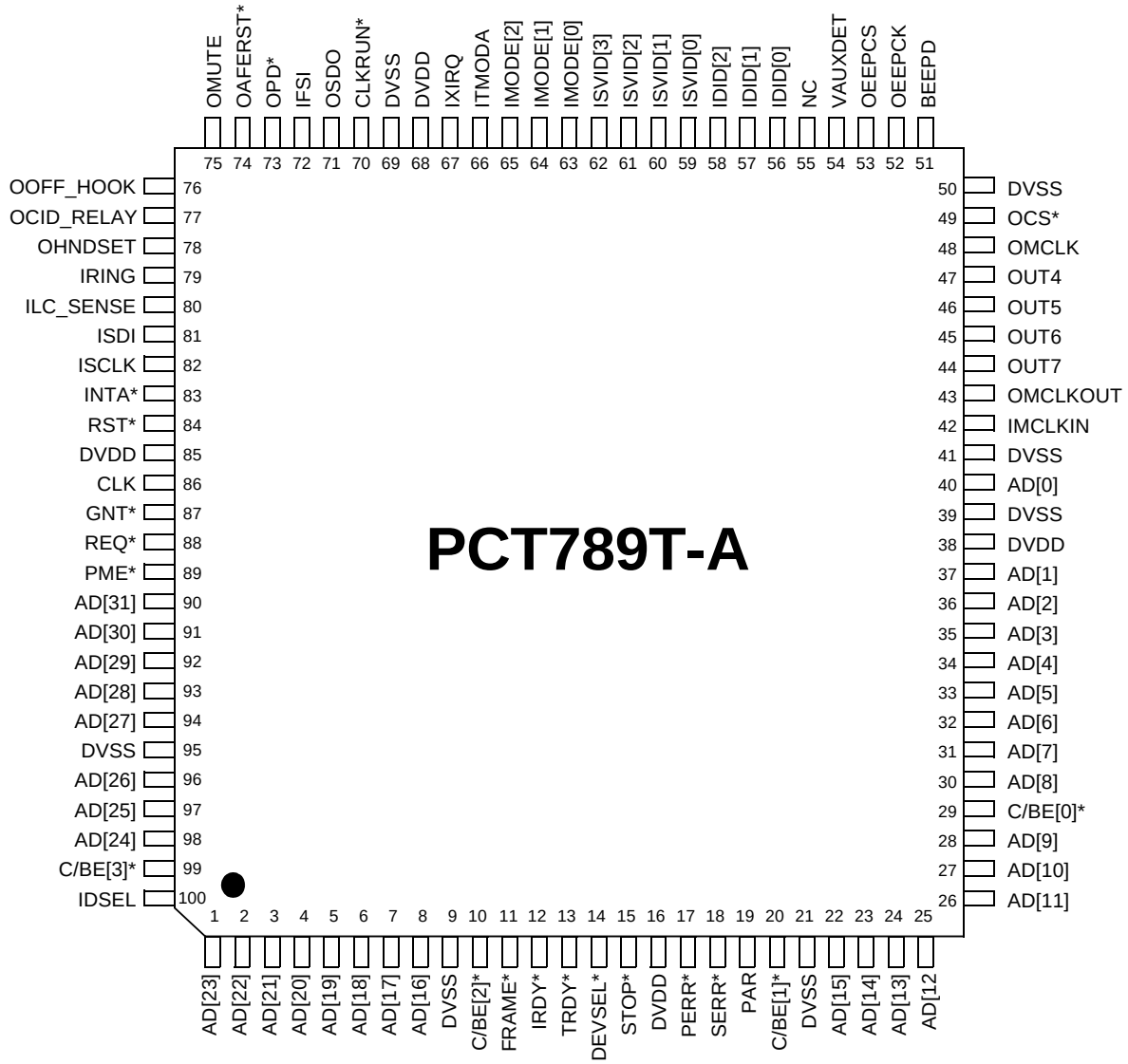


Figure 4 PCT789T-A 100-Pin TQFP/LQFP

PCT789T-A PIN DESCRIPTION

Table 3 PCT789T-A Pin Description

Name	Numbers	I/O	Type	Description
System Bus Interface Signals				
AD[31:16]	90-94, 96-98, 1-8	t/s	PCI	Dual-purpose pins. Address/data bus bits [31:16]. Address and data are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases.
AD[15:0]	22-25, 26-28, 30-37, 40	t/s	PCI	Address/data bus bits [15:0]. Address and data are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases.
C/BE[3:0]*	99,10, 20,29	t/s	PCI	Bus command/byte enables pins. During the address phase of a transaction, C/BE[3:0]* define the bus command. During the data phase C/BE[3:0]* are used as byte enables.
CLK	86	I	PCI	Clock. This is a input clock signal which provides timing for all transactions on PCI.
DEVSEL*	14	s/t/s	PCI	Device select. When actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, DEVDEL* indicates whether any device on the bus has been selected.
FRAME*	11	s/t/s	PCI	Frame. This signal is driven by the current master to indicate the beginning and duration of an access. While FRAME* is asserted, data transfer continues. When FRAME* is deasserted, the transaction is in the final data phase.
GNT*	87	t/s	PCI	Grant. This signal indicates that PCT789T-A access request to the PCI bus has been granted. NOTE: The PCI master mode is not supported in this version, but the pin is reserved for future expansion.
IDSEL	100	t/s	PCI	Initialization device select. This signal is active when the host wants to do configuration read and write transactions.
INTA*	83	OD	PCI	Interrupt A. This is a level sensitive output which is used to request an interrupt by PCT789T-A.
IRDY*	12	s/t/s	PCI	Initiator ready. This signal indicates the initiating agent's ability to complete the current data phase of the transaction.
PAR	19	t/s	PCI	Parity. This signal should be even parity across AD[31:00] and C/BE[3:0]*. PAR is stable and valid one clock after the address phase.
PERR*	17	s/t/s	PCI	Parity error. This signal is driven active when a data parity error is detected.
REQ*	88	t/s	PCI	Request. This signal is driven when the PCT789T-A desires use of the PCI bus. NOTE: The PCI master mode is not supported in this version, but the pin is reserved for future expansion.
RST*	84	I	ST	Reset. This signal brings PCI-specific registers, sequencers, and signals to a consistent state. When active, the chip is returned to its initial state with all the internal registers set at their default value.
STOP*	15	s/t/s	PCI	Stop. This signal indicates the current target is requesting the master to stop the current transaction.

Table 3 PCT789T-A Pin Description (Continued)

Name	Numbers	I/O	Type	Description
TRDY*	13	s/t/s	PCI	Target ready. This signal indicates the target agent's ability to complete the current data phase of the transaction.
PME*	89	t/s	PCI	Power management event. A power management event is requested via the assertion of this signal.
CLKRUN*	70	in, o/d	PCI	Clock running. This signal is used as an input for a device to determine the status of CLK and an open drain output used by the device to request starting or speeding up CLK.
SERR*	18	o/d	PCI	System error. This signal is used to report address parity errors, data parity errors on the special cycle command, or any other catastrophic system error.
Multi-Purpose Input/Output and Other Control Signals				
OOFF-HOOK	76	O	8mA	Off-hook relay control output. This pin is used as the active-high control for the OFFHOOK Relay. It is driven by bit 0 of the external output register.
OCID-RELAY	77	O	8mA	Caller-ID relay control output. This pin is used for controlling the Caller ID relay. It is driven by bit 1 of the external output register.
OHNDSET	78	O	8mA PU	Voice relay control output. For systems that support voice playback and recording, this pin is used for controlling the handset relay. It is driven by bit 2 of the external output register.
OMUTE*	75	O	4mA	Mute speaker. When active, this pin is used to mute the on-board speaker so no signal monitoring on the telephone line can be heard. It is driven by bit 3 of the external output register.
IRING	79	I	PU	Ring detection input. It is used to indicate that the telephone ring is detected. The IRING signal can be read by the host through bit 0 of external input register.
ILC-SENSE	80	I	PU	Loop current sense input or handset detection input. It is used to indicate the state of Loop current sensing or the handset being on- or off-hooked while in the voice playback and recording mode. The ILC-SENSE signal can be read by the host through bit 1 of external input register.
OAFERST*	74	O	4mA PU	AFE reset output for external CODEC. This pin is used as the AFE reset signal for external CODEC.
OPD	73	O	4mA PU	Power-down output for external CODEC. This pin is used as the AFE power-down signal for external CODEC.
IFSI	72	I	4mA PU	Receive frame synchronization input. This signal is driven by external CODEC to inform the PCT789T-A that a new frame of serial data is to be received from ISDI line.
OSDO	71	O	4mA PU	Serial data output to external CODEC. The serial data output for the DAC is driven through this pin to the external CODEC.
ISDI	81	I	PU	Serial data input from external CODEC. The serial data from ADC is driven through this pin from external CODEC to the internal PCT core logic.
ISCLK	82	I	4mA PU	Serial clock input. The serial clock is driven by external CODEC as the reference clock for serial data communication between external CODEC and PCT789T-A.

Table 3 PCT789T-A Pin Description (Continued)

Name	Numbers	I/O	Type	Description
OCS*	49	O	4mA	Chip select for companion chip. Any base I/O access to the PCT789T-A is direct to the companion chip also, if any, through this pin.
IXIRQ	67	I	PU	External IRQ input. The interrupt request from the companion chip can be routed through this input to the host bus.
IMCLKIN, OMCLKOUT	42, 43	I O		Terminals to connect to external crystal. These pins are the two terminals of the on-chip oscillator circuit to which a quartz crystal should be attached to provide the fundamental clock for generating oversampling clock for the AFE. The recommended frequency of the quartz crystal is 18.432MHz with ± 50ppm frequency tolerance at room temperature.
OMCLK	48	O	4mA	Master clock. This pin provides the master clock to drive external AFE.
OUT[4]	47	O	4mA PU	General-purpose output bit 4. In normal operating mode, this pin reflects bit 4 of the external output register.
OUT[5]	46	O	4mA PU	General-purpose output bit 5. In normal operating mode, this pin reflects bit 5 of the external output register.
OUT[6]	45	O	4mA PU	General-purpose output bit 6. In normal operating mode, this pin reflects bit 6 of the external output register.
OUT[7]	44	O	4mA PU	General-purpose output bit 7. In normal operating mode, this pin reflects bit 7 of the external output register.
VAUXDET	54	I	PD	Auxiliary power detection. Detects the presence of 3.3Vaux.
IMODE[2:0]	65-63	I	PU	Operating mode selection. These input pins are used for setting the operation mode of the PCT789T-A.
ISVID[3:0]	62-59	I	PD	Subsystem vendor ID selection. These input pins are used for selecting one of the 16 preselected subsystem vendor IDs to be initialized into PCI Configuration register 2Ch at power-up. Refer to the PCI configuration register definition section for a detailed list.
IDID[2:0]	58-56	I	PD	Device ID selection. The logic state of these input pins is latched into bits [2:0] of the PCI device ID field in PCI Configuration register 00h during the power-on reset period. It is used for product differentiation.
Serial EEPROM Interface Signals				
OEEPCK	52	O	4mA	EEPROM Clock. For providing clock signal for accessing off-chip serial EEPROM which stored the resource information of a PCI card.
OEEPCS	53	O	4mA	EEPROM Chip Select. Provides the chip enable signal for the external serial EEPROM.
BEEPD	51	I/O	4mA	EEPROM Data I/O. Provides the serial data gateway for the external serial EEPROM.
Power and Ground Pins				
DVDD	16, 38, 68, 85	P		Positive digital power supply (3.3V ± 5%)
DVSS	9, 21, 41, 39, 50, 69, 95	G		Digital ground (0V)

PCT789T-A OPERATING MODES

PCT789T-A supports operating modes in PCI mode. These options are selected through strap options (pull-up or pull-down on the input pins) over three mode selection input pins, IMODE[2:0]. A detailed mode configuration table is shown in Table 4 below.

Table 4 PCT789T-A Operating Mode Configuration

IMODE			Mode Description	I/O Address	Data Bus Width
2	1	0			
1	1	1	Reserved		
1	1	0	PCI 32-bit Data Mode (with external CODEC)	32	32
1	0	1	Reserved		
1	0	0	Reserved		
0	1	1	Reserved		
0	1	0	Reserved		
0	0	1	Reserved		
0	0	0	Reserved		

PCT303DW PINOUTS

PCT303D Pinout

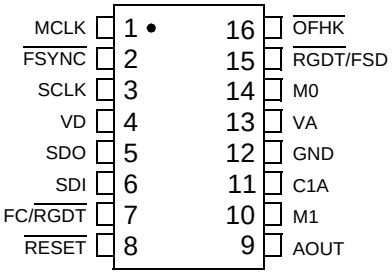


Figure 5 PCT303D 16-Pin SOIC

PCT303W Pinout

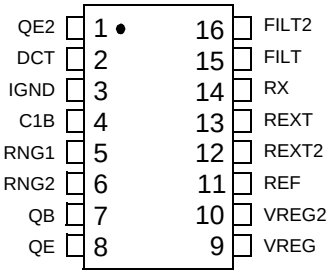


Figure 6 PCT303W 16-Pin SOIC

PCT303DW PIN DESCRIPTIONS

PCT303D Pin Description

Table 5 PCT303D Pin Description

Name	Number	I/O	Description
Serial Interface			
MCLK	1		Master clock input. High speed master clock input. Generally supplied by the system crystal clock or modem/DSP.
SCLK	3		Serial port bit clock output. Controls the serial data on SDOUT and latches the data on SDIN.
SDI	6		Serial port data in. Serial communication and control data that is generated by the modem/DSP and presented as an input to the PCT303D.
SDO	5		Serial port data out. Serial communication data that is provided by the PCT303D to the Modem/DSP.
$\overline{\text{FSYNC}}$	2		Frame sync output. Data framing signal that is used to indicate the start and stop of a communication data frame.
FC/ $\overline{\text{RGDT}}$	7		Secondary transfer request input/Ring detect. As FC, this pin is an optional signal to instruct the PCT303D that control data is being requested in a secondary frame. When daisy-chain is enabled, this pin becomes the ring detect output, $\overline{\text{RGDT}}$, which produces an active-low, half-wave rectified version of the ring signal.
Control Interface			
$\overline{\text{RGDT}}$/ FSD	15		Ring detect/Delayed frame sync. As $\overline{\text{RGDT}}$, this pin is an output signal that indicates the status of a ring signal, which produces an active-low, half-wave rectified version of the ring signal. When daisy-chain is enabled, this signal becomes a delayed frame sync, FSD, to drive a slave device.
$\overline{\text{OFHK}}$	16		Off hook. Input control signal that provides a termination across tip and ring for line seizing and pulse dialing, active-low.
$\overline{\text{RESET}}$	8		Reset input. An active-low input that is used to reset all control registers to a defined, initialized state. Also used to bring the PCT303DW out of sleep mode.
M0	14		Mode select 0. One of two mode select pins that is used to select the operation of the serial port/DSP interface.
M1	10		Mode select 1. The second of two mode select pins that is used to select the operation of the serial port/DSP interface.
Miscellaneous Signals			
AOUT	9		Analog speaker output. Provides an analog output signal for driving a call progress speaker.
C1A	11		Isolation capacitor 1A. Connects to one side of the isolation capacitor C1.
Power Signals			
VD	4		Digital supply voltage. Provides the digital supply voltage to the PCT303D. Nominally either 5V or 3.3V.
VA	13		Analog supply voltage. Provides the analog supply voltage for the PCT303D. Nominally either 5V or 3.3V. The 3.3V supply is internally generated with an on-chip charge pump set through a control register.
GND	12		Ground. Connects to the system digital ground.

PCT303W Pin Descriptions

Table 6 PCT303W Pin Descriptions

Name	Number	I/O	Description
Line Interface			
FILT	15		Filter. Sets the time constant for the DC termination circuit.
FILT2	16		Filter 2. Sets the time constant for the DC termination circuit.
RX	14		Receive input. Serves as the receive side input from the telephone network.
DCT	2		DC termination. Provides DC termination to the telephone network.
REXT	13		External resistor. Sets the real AC termination impedance.
REXT2	12		External resistor 2. Sets the complex AC termination impedance.
RNG1	5		Ring 1. Connects through a 680pF capacitor to the “Tip” lead of the telephone line. Provides the ring and caller ID signals to the PCT303DW.
RNG2	6		Ring 2. Connects through a 680pF capacitor to the “Ring” lead of the telephone line. Provides the ring and caller ID signals to the PCT303DW.
QB	7		Transistor base. Connects to the base of transistor Q3.
QE	8		Transistor emitter. Connects to the emitter of transistor Q3.
QE2	1		Transistor emitter 2. Connects to the emitter of transistor Q4.
REF	11		Reference. Connects to an external resistor to provide a high-accuracy reference current.
Isolation			
C1B	4		Isolation capacitor 1B. Connects to one side of isolation capacitor C1.
IGND	3		Isolated ground. Connects to ground on the line-side interface. Also connects to capacitor C2.
Miscellaneous Signals			
VREG	9		Voltage regulator. Connects to an external capacitor to provide bypassing for an internal power supply.
VREG2	10		Voltage regulator 2. Connects to an external capacitor to provide bypassing for an internal power supply.

PIN COMPARISON OF PCT301L AND PCT303W

Table 7 PCT301L/PCT303W Pin Comparison

Pin Number	Pin Name	
	PCT301L	PCT303W
1	TSTA	QE2
2	TSTB	DCT
3	IGND	IGND
4	C1B	C1B
5	RNG1	RNG1
6	RNG2	RNG2
7	QB	QB
8	QE	QE

Pin Number	Pin Name	
	PCT301L	PCT303W
9	VREG	VREG
10	NC	VREG2
11	NC	REF
12	DCT	REXT2
13	REXT	REXT
14	RX	RX
15	NC	FILT
16	TX	FILT2

PCT303DW FUNCTIONAL DESCRIPTION

The PCT303DW is an integrated direct access arrangement (DAA) that provides a programmable line interface to meet international telephone-line requirements. The device implements Silicon Laboratories' proprietary ISOLink™ technology which offers the highest level of integration by replacing an analog front end (AFE), an isolation transformer, relays, opto-isolators, and a 2–4-wire hybrid with two 16-pin small outline packages (SOIC). The chipset can be fully programmed to meet international requirements, and the device is compliant with FCC, NET4, CTR21, JATE, and country-specific PTT specifications. In addition, the PCT303DW has been designed to meet the most stringent world-wide requirements for out-of-band energy, billing-tone immunity, lightning surges, and safety requirements.

The PCT303DW solution needs only a few low-cost discrete components to achieve global compliance. See Figure 2 on page 6 for a typical application circuit.

Isolation Barrier

The PCT303DW achieves an isolation barrier through a low-cost, high-voltage capacitor in conjunction with ISOLink signal processing techniques. These techniques eliminate any signal degradation due to capacitor mismatches, common mode interference, or noise coupling. As shown in Figure 2, the C1, C2, and C4 capacitors isolate the PCT303D (DSP side) from the PCT303W (line side). All transmit, receive, control, and caller ID data are communicated through this barrier.

The Isolation Pass is disabled by default. To enable it, the PDL bit in register 6 must be cleared. No communication between the PCT303D and PCT303W can occur until this bit is cleared. The clock generator must be programmed to an acceptable sample rate prior to clearing the PDL bit.

AC Termination

The PCT303DW supports international AC Termination requirements with two selectable impedances, one real and one complex. Mode 0 is a nominal 600-ohm termination that supports the FCC 68 requirement in addition to the requirement of many European countries. Mode 1 is a complex impedance as dictated by countries such as the UK and Germany, and also specified by CTR21. This complex impedance is set by circuitry internal to the PCT303DW as well as the external components connected to REXT2.

DC Termination

The PCT303DW has four programmable modes related to DC termination. Two bits in register 16 (DCT1, DCT0) set the DC characteristics. While the modes are designed to support the extreme conditions in various countries, the user can determine if a line in a given country can support a mode with a higher transmit power level and switch to the appropriate mode. This decision will depend on the amount of loop current available on the line.

Mode 1 (0,1) is a low-voltage mode with no current limiting; it supports transmit signals up to –2.71 dBm. The low voltage requirement is dictated by countries such as Japan and Australia. See Figure 7.

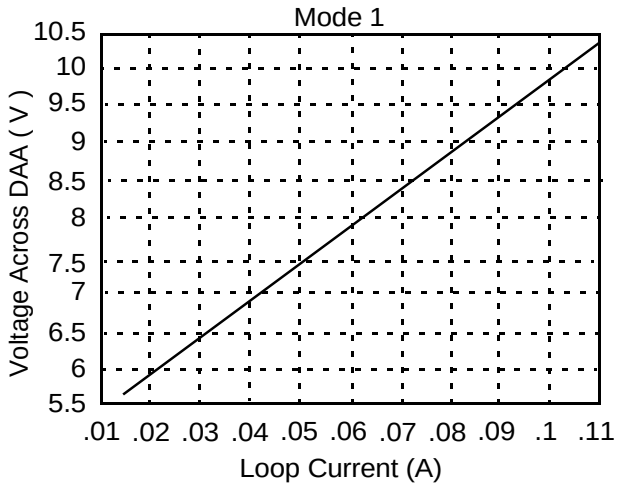


Figure 7 Mode 1 I/V Characteristics (0,1)

Mode 2 (1,0) is the default DC termination mode, with no current limiting, providing a maximum transmit level of –1 dBm at Tip and Ring. This mode meets FCC requirements in addition to the requirements of many European countries. Figure 8 shows the I/V characteristics of mode 2.

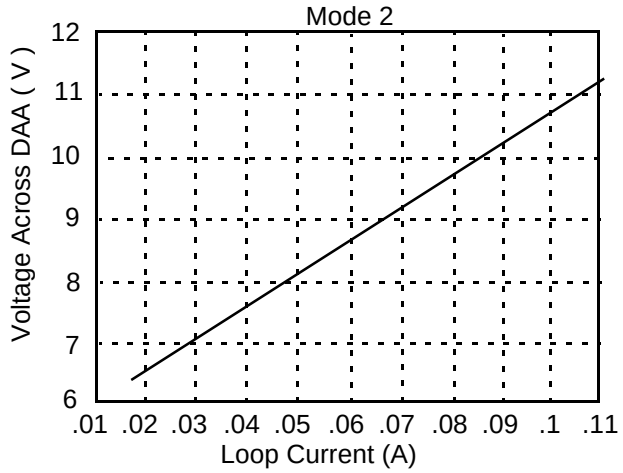


Figure 8 Mode 2 I/V Characteristics (1,0)

Mode 3 (1,1) provides current limiting, while maintaining a transmit level of –1 dBm at Tip and Ring. Figure 9 shows the I/V characteristics of mode 3. In mode 3, the DC termination will current limit before reaching 60 mA.

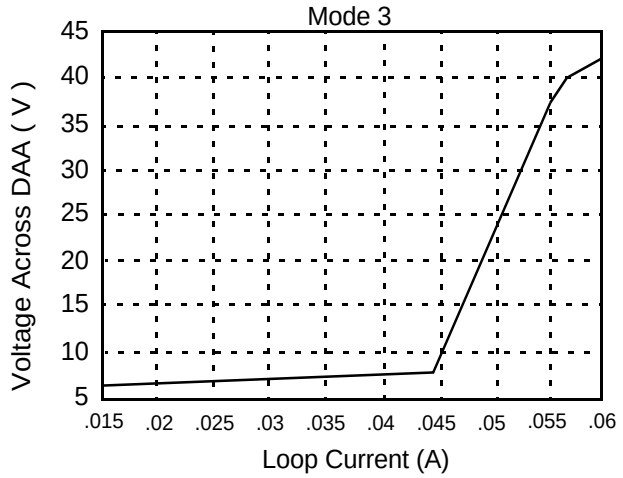


Figure 9 Mode 3 I/V Characteristics (1,1)

The PCT303DW can be fully programmed to meet international requirements, and the device is compliant with FCC, NET4, CTR21, JATE, and country-specific PTT specifications. Figure 2 outlines a limited set of line interface configurations required to support CTR21 and other key countries by setting different AC and DC termination modes. See “Appendix: NET4 Country Support” on page 65 for a more complete set of the line interface configurations required to support NET4 countries.

Table 8 Line Interface Configurations (Register 16)

Country	AC Termination	DC Termination	
	Bit 5	Bit 4	Bit 3
1. FCC	0	1	0
2. Australia	1	0	1
3. Japan	0	0	1
4. New Zealand	1	1	0
5. Singapore [a]	0	0	1
6. South Africa	1	1	0
7. CTR21 [b,c]	1	1	1

a. Support for loop currents greater than or equal to 20 mA.

b. The PCT303DW can also be configured to meet the individual specifications for these countries. (See “Appendix: NET4 Country Support” on page 65.)

c. CTR21 includes Austria, Belgium, Denmark, Finland, France, Germany, Greece, Hungary, Iceland, Ireland, Italy, Liechtenstein, Luxembourg, Netherlands, Norway, Portugal, Spain, Sweden, Switzerland, and the UK.

Ring Detection

The ring signal is capacitively coupled from Tip and Ring to the RNG1 and RNG2 pins. The PCT303DW supports either full- or half-wave ring detection. With full-wave ring detection, the designer can detect a polarity reversal as well as the ring signal.

The ring detector output can be monitored in one of three ways. The first method uses the $\overline{\text{RGDT}}$ pin. The second method uses the register bits RDTP, RDTN, and RDT of register 5. The final method uses the SDO output.

The DSP must detect the frequency of the ring signal in order to distinguish a ring from pulse dialing by telephone equipment connected in parallel. If necessary, the DSP can estimate the amplitude of the ring signal based on the ring detect threshold and the duty cycle of the ring detector output.

The PCT303DW can be programmed for both ringer impedance and ringer threshold as described in the “Appendix: NET4 Country Support” on page 65.

Billing Tone Immunity

In some countries, billing tones generated by the central office can cause modem connection difficulties. The PCT303DW enables the modem developer to provide feedback to the user for problems associated with billing tones on the line.

Billing tone detection is enabled by setting the BTE bit of register 16. Depending on line conditions, the billing tone can be large enough to cause major errors related to the modem data. If this situation occurs, the BTD bit of register 17 is set. This bit remains set until the user sets it to zero or a reset of the device is executed.

The billing tone may only be large enough to overdrive the receive input. In this case, the ROV bit of register 17 is set, indicating an overdrive situation. This bit remains set until set to zero or a reset is executed.

Lightning Test

The PCT303DW meets the lightning test requirements of EN6100-4-5 and FCC part 68.

Safety and Isolation

The PCT303DW meets the requirements of the European safety specification EN60950 as well as the requirements of FCC part 68 and UL.

Off-Hook

The communication system generates an off-hook command by applying logic 0 to the $\overline{\text{OFHK}}$ pin or writing a logic 1 to bit 0 of control register 5. The $\overline{\text{OFHK}}$ pin must be enabled by setting bit 1 (OHE) of register 5. With $\overline{\text{OFHK}}$ at logic 0, the system is in an off-hook state. This state is used to seize the line for incoming/outgoing calls and can also be used for pulse dialing. With $\overline{\text{OFHK}}$ at logic 1, negligible DC current flows through the hookswitch. When a logic 0 is applied to the $\overline{\text{OFHK}}$ pin, the hookswitch transistor pair, Q1 & Q2, turn on. The net effect of the off-hook signal is the application of a termination impedance across tip and ring and the flow of DC loop current. The termination impedance has both an AC and DC component.

When executing an off-hook sequence, the PCT303DW requires 4620/Fs clock cycles to complete the off-hook and provide phone-line data on the serial link. This includes the 12/Fs filter group delay. If necessary, for the shortest delay, a higher Fs may be established prior to executing the off-hook, such as an Fs of 10.286 kHz.

Digital Interface

The PCT303DW has two serial interface modes that support most standard modem DSPs. The M0 and M1 mode pins select the interface mode. The key difference between these two serial modes is the operation of the FSYNC signal. Table 9 summarizes the serial mode definitions.

Table 9 Serial Modes

Mode	M1	M0	Description
0	0	0	$\overline{\text{FSYNC}}$ frames data
1	0	1	$\overline{\text{FSYNC}}$ pulse starts data frame
2	1	0	Slave mode
3	1	1	Reserved

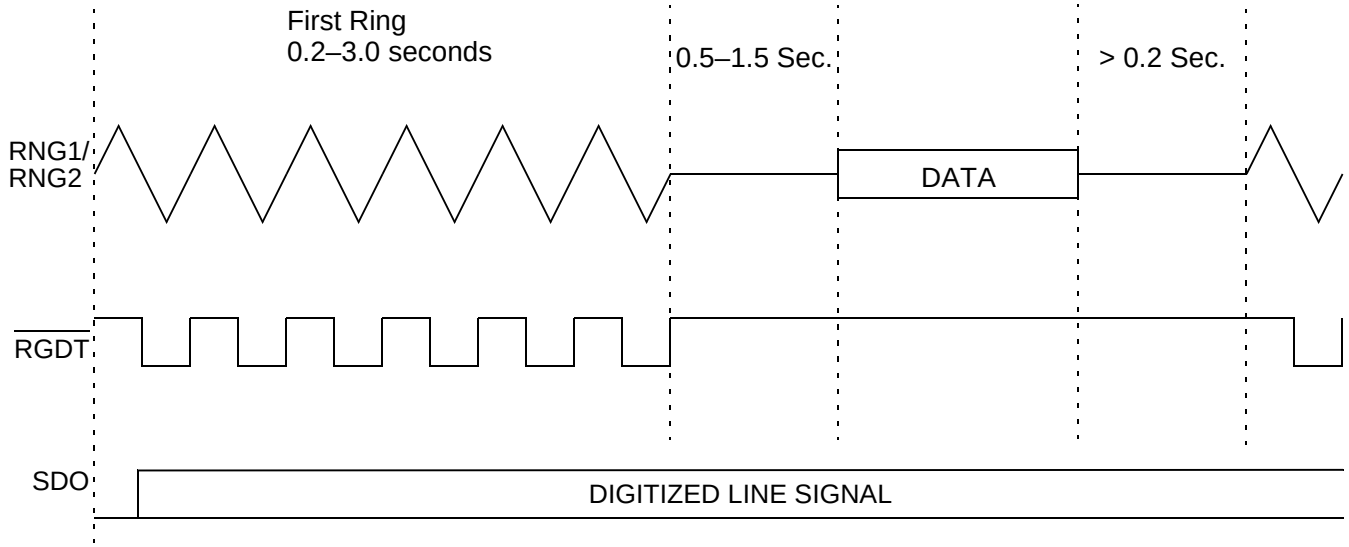


Figure 10 Ring Detect Timing

The digital interface consists of a single, synchronous serial link which communicates both telephony and control data.

In Serial mode 0 or 1, the PCT303D operates as a master, where the master clock (MCLK) is an input, the serial data clock (SCLK) is an output, and the frame sync signal (FSYNC) is an output. The MCLK frequency and the value of the sample rate control registers 7, 8, 9 and 10 determine the sample rate (Fs). The serial port clock, SCLK, runs at 256 bits per frame, where the frame rate is equivalent to the sample rate. Refer to “Clock Generation Subsystem” on page 23 for more details on programming sample rates.

The PCT303DW transfers 16-bit or 15-bit telephony data in the primary timeslot and 16-bit control data in the secondary timeslot. Figure 11 and Figure 12 show the relative timing of the serial frames. Primary frames occur at the frame rate and are always present. To minimize overhead in the external DSP, secondary frames are present only when requested.

Two methods exist for transferring control information in the secondary frame. The default power-up mode uses the LSB of the 16-bit transmit (TX) data word as a flag to request a secondary transfer. In this mode, only 15-bit TX data is transferred, resulting in a loss of SNR but allowing software control of the secondary frames. As an alternative method, the FC pin can serve as a hardware flag for requesting a secondary frame. The external DSP can turn on the 16-bit TX mode by setting the SB bit of register 1. In the 16-bit TX mode, the hardware FC pin must be used to request secondary transfers.

Figure 13 and Figure 14 illustrate the secondary frame read cycle and write cycle, respectively. During a read cycle, the R/W bit is high and the 5-bit address field contains the address of the register to be read. The contents of the 8-bit control register are placed on the SDO signal. During a write cycle, the R/W bit is low and the 5-bit address field contains the address of the register to be written. The 8-bit data to be written immediately follows the address on SDI. Only one register can be read or written during each secondary frame. See “PCT303DW Control Registers” on page 41 for the register addresses and functions.

In serial mode 2, the PCT303D operates as a slave device, where the MCLK is an input, the SCLK is a no connect, and the FSYNC is an input. In addition, the RGDT/FSD pin operates as a delayed frame sync (FSD) and the FC/RGDT pin operates as ring detect (RGDT). Note that in this mode, FC operation is not supported.

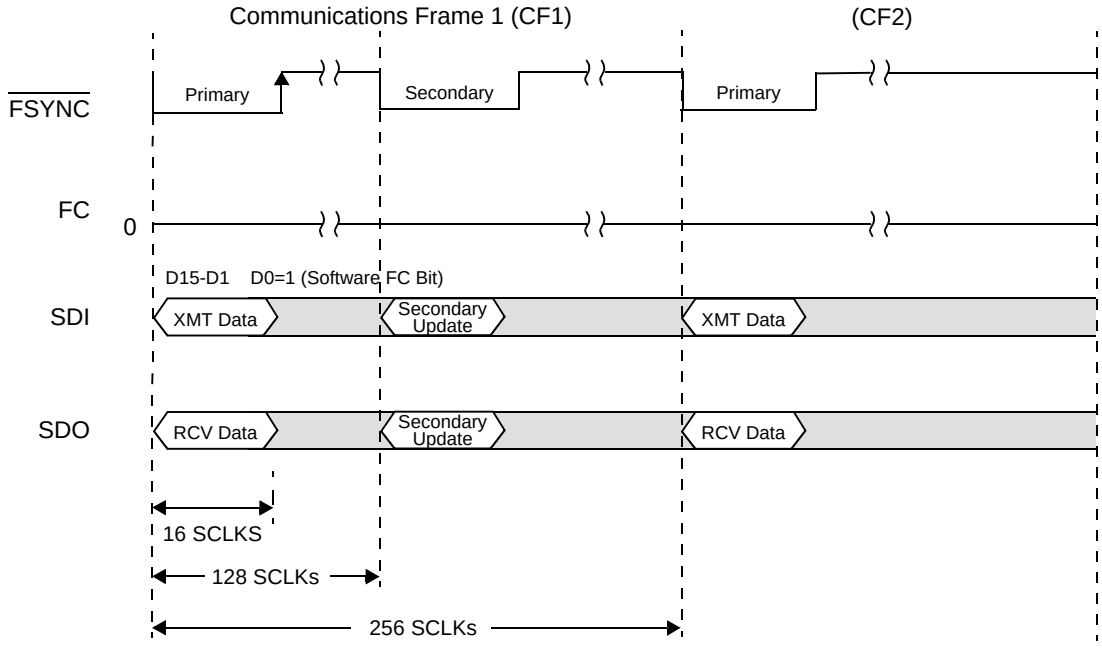


Figure 11 Software FC/RGDT Secondary Request

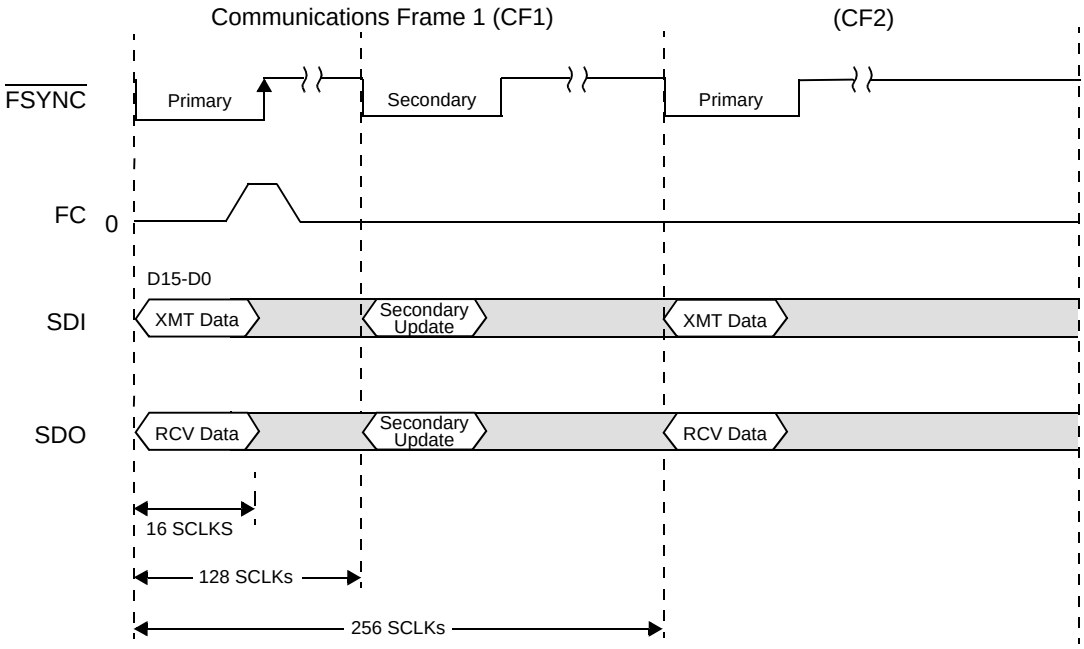


Figure 12 Hardware FC/$\overline{\text{RGDT}}$ Secondary Request

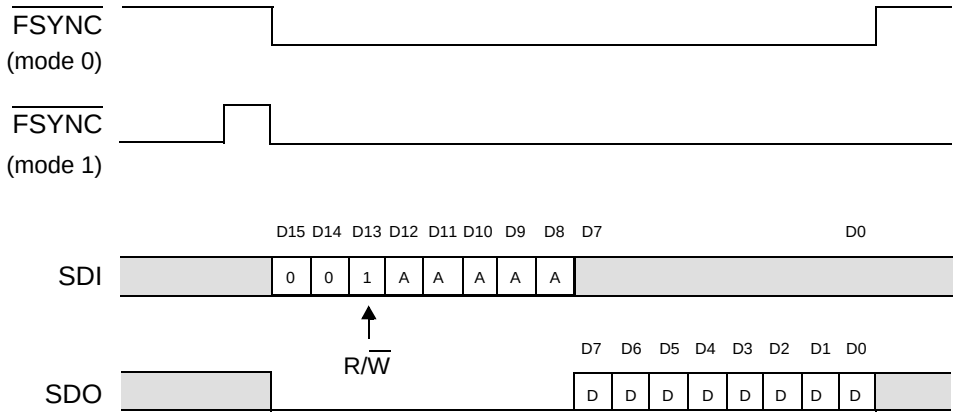


Figure 13 Secondary Communication Data Format - Read Cycle

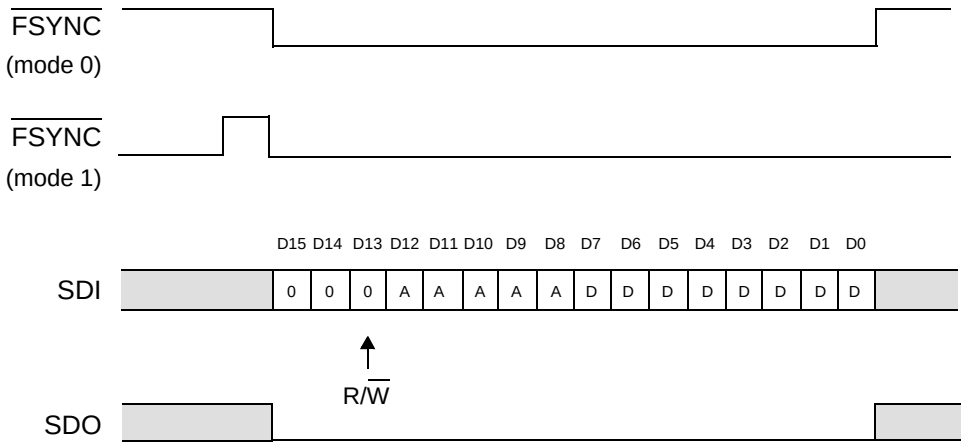


Figure 14 Secondary Communication Data Format - Write Cycle

Clock Generation Subsystem

The PCT303DW contains an on-chip clock generator. Using a single MCLK input frequency, the PCT303DW can generate all the desired standard modem sample rates, as well as the common 11.025 kHz rate for audio playback.

The clock generator consists of two phase-locked loops (PLL1 and PLL2) that achieve the desired sample frequencies. Figure 15 illustrates the clock generator. The architecture of the dual PLL scheme allows for fast lock time on initial start-up, fast lock time when changing modem sample rates, high noise immunity, and the ability to change modem sample rates with a single register write. A large number of MCLK frequencies between 1 MHz and 60 MHz are supported.

In serial mode 2, the PCT303D operates as a slave device. The clock generator is configured (by default) to set the SCLK output equal to the MCLK input. The net effect is the clock generator multiplies the MCLK input by 20.

Programming the Clock Generator

As noted in Figure 15, the clock generator must output a clock equal to 1024*Fs, where Fs is the desired sample rate. The 1024*Fs clock is determined through programming of the following registers:

Register 7—N1 divider, 8 bits.

Register 8—M1 divider, 8 bits.

Register 9—N2/M2 dividers, 4 bits/4 bits.

Register 10—CGM, 1 bit.

When using the PCT303DW for modem applications, the clock generator can be programmed to allow for a single register write to change the modem sampling rate. These standard sample rates are shown in Table 10. The programming method is described below.

Table 10 N2, M2 Values (CGM = 0, 1)

Fs (Hz)	N2	M2
7200	2	2
8000	9	10
8229	7	8
8400	6	7
9000	4	5
9600	3	4
10286	7	10

The main design consideration is the generation of a base frequency, defined as the following:

$$F_{Base} = \frac{F_{MCLK} \cdot M1}{N1} = 36.864MHz, CGM = 0$$

$$F_{Base} = \frac{F_{MCLK} \cdot M1 \cdot 16}{N1 \cdot 25} = 36.864MHz, CGM = 1$$

N1 (register 7) and M1 (register 8) are 8-bit unsigned values. F_{MCLK} is the clock provided to the MCLK pin. Table 11 lists several standard crystal oscillator rates that could be supplied to MCLK. This list simply represents a sample of MCLK frequency choices. Many more are possible.

After the first PLL has been setup, the second PLL can be programmed easily. The values for N2 and M2 (register 9) are shown in Table 10. N2 and M2 are 4-bit unsigned values.

When programming the registers of the clock generator, the order of register writes is important. For PLL1 updates, N1 (register 7) must always be written first, immediately followed by a write to M1 (register 8). For PLL2, the CGM bit must set as desired prior to writing N2/M2 (register 9). Changes to CGM only take effect when N2/M2 are written.

NOTE: The values shown in Table 10 and Table 11 satisfy the equations above. However, when programming the registers for N1, M1, N2, and M2, the value placed in these registers must be one less than the value calculated from the equations. For example, for CGM = 0 with a MCLK of 48.0 MHz, the values placed in the N1 and M1 registers would be 7Ch and 5Fh, respectively. If CGM = 1, a non-zero value must be programmed to register 9 in order for the 16/25 ratio to take effect.

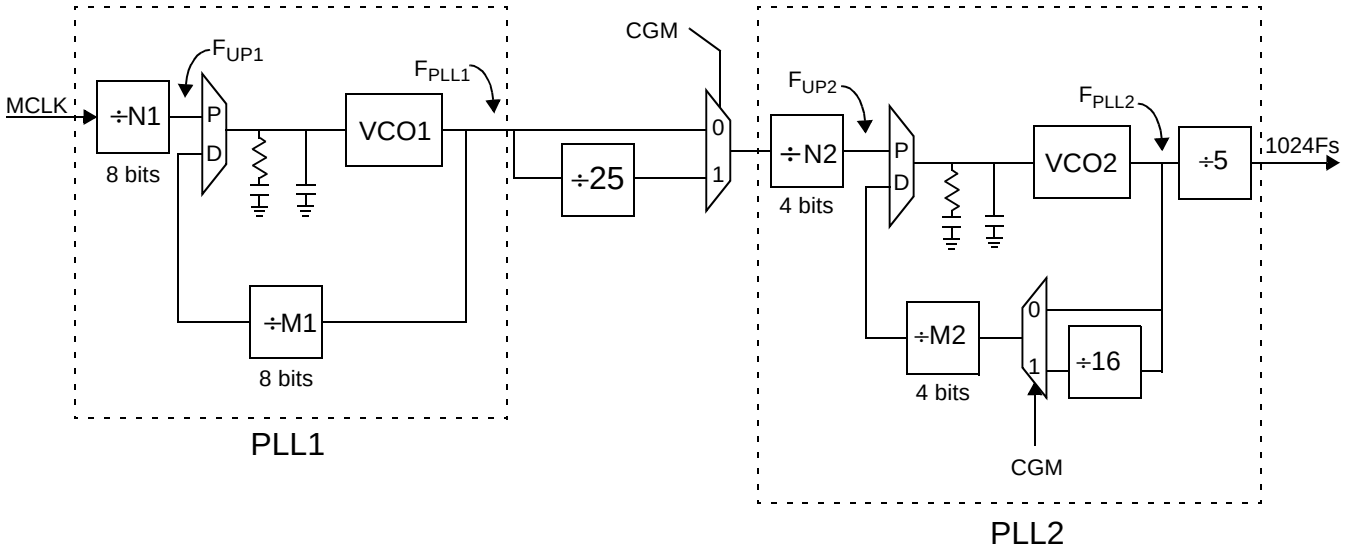


Figure 15 Clock Generation Subsystem

PLL Lock Times

The PCT303DW changes sample rates very quickly. However, lock time varies based on the programming of the clock generator. The major factor contributing to PLL lock time is the CGM bit. When the CGM bit is used (set to one), PLL2 locks slower than when CGM is zero. The following relationships describe the boundaries on PLL locking time:

PLL1 lock time < 1 ms (CGM = 0,1)

PLL2 lock time <100 us (CGM = 0)

PLL2 lock time <1 ms (CGM = 1)

For modem designs, it is recommended that PLL1 be programmed during initialization. No further programming of PLL1 is necessary. The CGM bit and PLL2 can be programmed for the desired initial sample rate, typically 7200 Hz. All further sample rate changes are made by simply writing to register 9 to update PLL2.

The final design consideration for the clock generator is the update rate of PLL1. The following criteria must be satisfied in order for the PLLs to remain stable:

$$F_{UP1} = F_{MCLK} / (N1) \geq 144kHz$$

Where F_{UP1} is shown in Figure 15.

Setting Generic Sample Rates

The above clock generation description focuses on the common modem sample rates. An application may require a sample rate not listed in Table 10, such as the common audio rate of 11.025 kHz. The restrictions and equations above still apply; however, a more generic relationship between MCLK and Fs (the desired sample rate) is needed. The following equation describes this relationship:

$$\frac{?M1? \cdot ?M2?}{?N1? \cdot ?N2?} = ratio \bullet \frac{5 \cdot 1024 \cdot Fs}{?MCLK?}$$

where *Fs* is the sample frequency, *ratio* is 1 for CGM=0 and 25/16 for CGM = 1, and all other symbols are shown in Figure 15.

Table 11 MCLK Examples

MCLK (MHz)	N1	M1	CGM
1.8432	1	20	0
4.0000	5	72	1
4.0960	1	9	0
5.0688	11	80	0
6.0000	5	48	1
6.1440	1	6	0
8.1920	32	225	1
9.2160	1	4	0
10.0000	25	144	1
10.3680	9	32	0
11.0592	3	10	0
12.288	1	3	0
14.7456	2	5	0
16.0000	5	18	1
18.4320	1	2	0
24.5760	2	3	0
25.8048	7	10	0
33.8688	147	160	0
44.2368	96	125	1
46.0800	5	4	0
47.9232	13	10	0
48.0000	125	96	0
56.0000	35	36	1
60.0000	25	24	1

Knowing the MCLK frequency and desired sample rate the values for the M1, N1, M2, N2 registers can be determined. When determining these values, remember to consider the range for each register as well as the minimum update rate for the first PLL.

The values determined for M1, N1, M2, and N2 must be adjusted by minus one when determining the value written to the respective registers. This is due to internal logic, which adds one to the value stored in the register. This addition allows the user to write a zero value in any of the registers and the effective divide by is one. A special case occurs when both M1 and N1 and/or M2 and N2 are programmed with a zero value. When Mx and Nx are both zero, the corresponding PLLx is bypassed. Note that if M2 and N2 are set to zero, the ratio of 25/16 is eliminated and cannot be used in the above equation. In this condition the CGM bit has no effect.

Power Management

The PCT303DW supports four basic power management operation modes. The modes are normal operation, reset operation, sleep mode, and full power down mode. The power management modes are controlled by the PDN and PDL bits of register 6.

On power up, or following a reset, the PCT303DW is in reset operation. In this mode, the PDL bit is set, while the PDN bit is cleared. The PCT303D is fully operational, except for the ISOLink. No communication between the PCT303D and PCT303W can occur during reset operation. Note, any bits associated with the PCT303W are not valid in this mode.

The most common mode of operation is the normal operation. In this mode, the PDL and PDN bits are cleared. The PCT303D is fully operational and the ISOLink is communicating information between the PCT303D and the PCT303W. Note that the clock generator must be programmed to a valid sample rate prior to entering this mode.

The PCT303DW supports a low-power sleep mode. This mode supports the popular wake-up-on-ring feature of many modems. The clock generator registers 7, 8, and 9 must be programmed with valid non-zero values prior to enabling sleep mode. Then, the PDN bit must be set and the PDL bit cleared. When the PCT303DW is in sleep mode, the MCLK signal may be stopped or remain active, but it *must* be active before waking up the PCT303DW. The PCT303D is non-functional except for the ISOLink and RGDT signal. To take the PCT303DW out of sleep mode, pulse the reset pin ($\overline{\text{RESET}}$) low.

In summary, the power down/up sequence for sleep mode is as follows:

1. Registers 7, 8, and 9 must have valid non-zero values.
2. Set the PDN bit (register 6, bit 3) and clear the PDL bit (register 6, bit 4).
3. MCLK may stay active or stop.
4. Restore MCLK before initiating the power-up sequence.
5. Reset the PCT303DW using $\overline{\text{RESET}}$ pin (after MCLK is present).
6. Program registers to desired settings.

The PCT303DW also supports an additional power-down mode. When both the PDN (register 6, bit 3) and PDL (register 6, bit 4) are set, the chip-set enters a complete power-down mode and draws negligible current. Set the PDL bit either before setting the PDN bit or at the same time. In this mode, the RGDT pin does not function. Normal operation may be restored using the same process for taking the chip-set out of sleep mode.

Analog Output

The PCT303DW supports an analog output (AOUT) for driving the call progress speaker found with most of today's modems. AOUT is an analog signal that is comprised of a mix of the transmit and receive signals. The receive portion of this mixed signal has a 0 dB gain, while the transmit signal has a gain of –20 dB.

The transmit and receive signals of the AOUT signal have independent mute controls. The ATM bit (register 6, bit 6) mutes the transmit portion, while the ARM (register 6, bit 5) mutes the receive portion. Figure 3 on page 8 illustrates a recommended application circuit. Note that in the configuration shown, the LM386 provides a gain of 26 dB. Additional gain adjustments may be made by varying the voltage divider created by R1 and R3 of Figure 3.

On-Hook Line Monitor

The PCT303DW allows the user to detect line activity when the device is in an on-hook state. When the system is on-hook, the line data can be passed to the DSP across the serial port while drawing a small amount of DC current from the line. This feature is similar to the passing of line information (such as caller ID), while on-hook, following a ring signal detection. To activate this feature, set the ONHM bit in register 5.

The on-hook line monitor can also be used to detect whether a phone line is physically connected to the PCT303W and associated circuitry. When the on-hook line monitor is activated (if no line is connected), the output of SDO will move towards a negative full scale value (–32768). The value is guaranteed to be at least 89% of negative full scale.

If a line is present while in on-hook line monitor mode, SDO will have a near zero value. The designer must allow for the group delay of the receive filter before making a decision.

The on-hook line monitor may be used in conjunction with the loop current sense bits to determine if a phone line is physically connected to the PCT303W and associated circuitry. When on-hook line monitor is active (if a phone line is present), the LCS value will be a 1111b value.

If a phone line is not present, the LCS value will be a zero value. The designer must allow for a 5/Fs delay before making a decision. Refer to "Loop Current Monitor" for more details on the LCS bits.

Loop Current Monitor

When the system is in an off-hook state, the LCS bits of register 12 indicate the approximate amount of DC loop current that is flowing in the loop. The LCS is a 4-bit value ranging from zero to fifteen. Each unit represents approximately 6 mA of loop current. An LCS value of zero means the loop current is less than required for normal operation and the system should be on-hook. An LCS value of 15 means the loop current is greater than 120 mA. To determine a rough approximation of the current (mA) flowing in the loop the following equation may be used:

$$LoopCurrent \approx 6 \cdot LCS + 12$$

The LCS detector has a built-in hysteresis of 2 mA of current. This allows for a stable LCS value when the loop current is near a transition level. The LCS value is a rough approximation of the loop current, and the designer is advised to use this value in a relative means rather than an absolute value.

This feature enables the modem to determine if an additional line has "picked up" while the modem is transferring information. In the case of a second phone going off-hook, the loop current falls approximately 50% and is reflected in the value of the LCS bits.

Gain Control

The PCT303DW supports multiple gain and attenuation settings for the receive and transmit paths, respectively. When the ARX bit is set, 6 dB of gain is applied to the receive path. When the ATX bit is set, –3 dB of gain is applied to the transmit path.

Register 15 can be used to provide additional gain control. For register 15 to have an effect on the receive and transmit paths, the ATX and ARX bits of register 13 must be zero.

The receive path can support gains of 0, 3, 6, 9, and 12 dB. The gain is selected by bits 2:0 (ARX2:ARX0). The receive path can also be muted by setting bit 3 (RXM). The transmit path can support attenuations of 0, 3, 6, 9, and 12 dB. The attenuation is selected by bits 6:4 (ATX2:ATX0). The transmit path can also be muted by setting bit 7 (TXM).

Filter Selection

The PCT303D supports additional filter selections for the receive and transmit signals. The IIR bit of register 16, when set, enables the IIR filters defined in Table 29 on page 59. This filter provides a much lower, however non-linear, group delay than the default FIR filters.

Revision Identification

The PCT303DW provides the system designer the ability to determine the revision of the PCT303D and/or the PCT303W. Register 11 identifies the revision of the PCT303D with 4 bits named REVA. Register 13 identifies the revision of the PCT303W with 4 bits named REVB. Table 12 shows the values for the various revisions.

Table 12 Revision Values

Revision	PCT303D	PCT303W
A	0100	0001

In-Circuit Testing

The PCT303DW's advanced design provides the modem manufacturer with increased ability to determine system functionality during production line tests, as well as support for end-user diagnostics. Four loopback modes exist allowing increased coverage of system components. For three of the test modes, a line-side power source is needed. While a standard phone line can be used, the test circuit in Figure 20 on page 60 is adequate. In addition, an off-hook sequence must be performed to connect the power source to the line-side chip.

For the start-up test mode, no line-side power is necessary and no off-hook sequence is required. The start-up test mode is enabled by default. When the PDL bit (register 6, bit 4) is set (the default case), the line side is in a power-down mode and the DSP side is in a digital loop-back mode. In this mode, data received on SDI is passed through the internal filters and transmitted on SDO. This path will introduce approximately 0.9 dB of attenuation on the SDI signal received. The group delay of both transmit and receive filters will exist between SDI and SDO. Clearing the PDL bit disables this mode and the SDO data is switched to the receive data from the line side. Note, when PDL is cleared the FDT bit (register 12, bit 6) will become active, indicating the successful communication between the line side and DSP side. This can be used to verify that the ISOLink is operational.

The remaining test modes require an off-hook sequence to operate. The following sequence defines the off-hook requirement:

1. Power up or reset.
2. Program clock generator to desired sample rate.
3. Enable line side by clearing PDL bit.
4. Issue off-hook
5. Delay 4608/Fs to allow calibration to occur.
6. Set desired test mode.

The ISOLink digital loopback mode allows the data pump to provide a digital input test pattern on SDI and receive that digital test pattern back on SDO. To enable this mode, set the DL bit of register 1. In this mode, the isolation barrier is actually being tested. The digital stream is delivered across the isolation capacitor, C1 of Figure 2 on page 6, to the line side device and returned across the same barrier. Note in this mode, the 0.9 dB attenuation and filter group delays also exist.

The analog loopback mode allows an external device to drive the RX pin of the line-side chip and receive the signal from the TX pin. This mode allows testing of external components connecting the RJ-11 jack (tip and ring) to the line side of the PCT303DW. To enable this mode, set the AL bit of register 2.

The final testing mode, internal analog loopback, allows the system to test the basic operation of the transmit/ receive path of the line side and the external components R4 and C5 of Figure 2 on page 6. In this test mode, the data pump provides a digital test waveform on SDI. This data is passed across the isolation barrier, looped from the TX to RX pin, passed back across the isolation barrier, and presented to the data pump on SDO. To enable this mode, clear the HBE bit of register 2.

When the HBE bit is cleared, this will cause a DC offset which affects the signal swing of the transmit signal. In this test mode, it is recommended that the transmit signal be 12 dB lower than normal transmit levels. This lower level will eliminate clipping caused by the DC offset which results from disabling the hybrid. It is assumed in this test that the line AC impedance is nominally 600 Ω.

NOTE: All test modes are mutually exclusive. If more than one test mode is enabled concurrently, the results are unpredictable.

Exception Handling

The PCT303DW provides several mechanisms to determine if an error occurs during operation. Through the secondary frames of the serial link, the controlling DSP can read several status bits. The bit of highest importance is the frame detect bit (FDT, register 12 bit 6). This bit indicates that the DSP side (PCT303D) and line side (PCT303W) devices are communicating. During normal operation, the FDT bit can be checked before reading any bits that indicate information about the line side. If FDT is not set, the following bits related to the line side are invalid—RDT, LCS, CBID, REVB; the RGDT operation will also be non-functional.

Following power-up and reset, the FDT bit is not set because the PDL bit (register 6 bit 4) defaults to 1. In this state, the ISOLink is not operating and no information about the line side can be determined. The user must program the clock generator to a valid configuration for the system and clear the PDL bit to activate the ISOLink. While the DSP and line side are establishing communication, the DSP side does not generate FSYNC signals. Therefore, if the controlling DSP serial interface is interrupt driven, based on the FSYNC signal, the controlling DSP does not require a special delay loop to wait for this event to complete.

The FDT bit can also indicate if the line side executes an off-hook request successfully. If the line side is not connected to a phone line (that is, the user fails to connect a phone line to the modem), the FDT bit remains cleared. The controlling DSP must allow sufficient time for the line side to execute the off-hook request. The maximum time for FDT to be valid following an off-hook request is 10 ms. If the FDT is high, the LCS bits indicate the amount of loop current flowing. If the FDT fails to be set following an off-hook request, the PDL bit in register 6 must be set high for at least 1 ms to reset the line side. For more information, see “Loop Current Monitor” on page 25.

Another useful bit is the communication link error (CLE) bit (register 12 bit 7). The CLE bit indicates a time-out error for the ISOLink following a change to either PLL1 or PLL2. For more information, see “Clock Generation Subsystem” on page 22. When the CLE bit is set, the DSP side chip has failed to receive verification from the line side that the clock change has been accepted in an expected period of time. This condition indicates a severe error in programming the clock generator or possibly a defective line-side chip.

PCT789T-A BASE I/O LOCATIONS

PCT789T-A Base I/O Definition

For compatibility reasons, the base I/O address space is limited to 8 bytes, which is less than enough to support the rich features provided by the PCT789T-A modem chip. An index addressing method has been adopted to extend the on-chip register space beyond what can be provided.

All internal registers are in 16-bit word format. Each one is accessed by writing to INDEX register first with the appropriate index address then read or write to the addressed register through the DATA port. The index range allocated for on-chip registers is from index 0 through 15.

Table 13 PCT789T-A Base I/O Definition

Address	Write	Read
BASE+0	DATA[7:0]	DATA[7:0]
BASE+1	DATA[15:8]	DATA[15:8]
BASE+2	Reserved	Reserved
BASE+3	Reserved	Reserved
BASE+4	INDEX[7:0]	Reserved
BASE+5	Reserved	Reserved
BASE+6	Reserved	Reserved
BASE+7	Reserved	Reserved

DATA[15:0] – *Data Register*. This base I/O location is the 16-bit data port for the host CPU to communicate with the PCT789T-A on-chip FIFO buffers and the control/status registers.

INDEX[15:0] – *Index Register*. This base I/O location is write-only; it is the address register for all on-chip FIFO buffers and registers.

PCT789T-A PCI CONFIGURATION REGISTERS

PCI Configuration Register Summary

Table 14 PCI Configuration Registers

Index	PCI Configuration Register			
00h	Device ID		Vendor ID	
04h	Status		Command	
08h	Class code			Revision ID
0Ch	Reserved [a]			
10h	Base address 0 (Control registers)			
14h	Reserved [a]			
18h	Reserved [a]			
1Ch	Reserved [a]			
20h	Reserved [a]			
24h	Reserved [a]			
28h	Reserved [a]			
2Ch	Subsystem ID		Subsystem vendor ID	
30h	Reserved [a]			
34h	Reserved [a]		Capability pointer	
38h	Reserved [a]			
3Ch	Reserved [a]		Interrupt pin	Interrupt line
40h	Power management capabilities	Next-item pointer	Capability identifier	
44h	Reserved [a]		Power management control/status	
48h-FFh	Reserved [a]			

a. All reserved registers return 0 when read.

PCI Configuration Register Detailed Description

Configuration ID (00h, R)

DID[15:0]															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**

VID[15:0]															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Bit Definitions:

Bits	Name	Description
31:16	DID[15:0]	Device ID (R: default 789xh). Unique PCT789T-A ID number. The last three bits of the ID are loaded into this register through three strapped input pins, IDID[2:0], during the power-on reset period.
15:0	VID[15:0]	Vendor ID (R: default 134Dh). Specifies the manufacturer of the PCT789T-A: PC-TEL Inc.

Command and Status Configuration (04h, R/W)

PERR	SSERR	0	0	0	DEVSEL[1:0]		0	0	0	0	CAP	0	0	0	0
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**

0	0	0	0	0	0	0	SERREN	1	RSPPE	0	0	0	0	0	IOACS
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Bit Definitions:

Bits	Name	Description
31	PERR	Detected parity error (R/W: default 0b). Set when the PCT789T-A detects a parity error.
30	SSERR	Signaled system error (R/W: default 0b). Set when the PCT789T-A asserts SERR#.
29:27	Reserved	Reserved. Read returns zero.
26:25	DEVSEL[1:0]	DEVSEL timing (R: default 01b). Indicates the timing of the assertion of the DEVSEL* pin. The PCT789T-A is set for median speed PCI device.
24:21	Reserved	Reserved. Read returns zero.
20	CAP	Capabilities (R: default 1b). When set, indicates that the PCT789T-A is capable of handling PCI power management.
19:9	Reserved	Reserved. Read returns zero.
8	SERREN	System error enable (R/W: default 0b). When set, enables the SERR# driver on the PCT789T-A to report a system error.
7	Reserved	Reserved. Read returns one.
6	RSPPE	Parity error response (R/W: default 0b). When set, signals the PCT789T-A to assert PERR* after a parity error detection. Otherwise, any parity error detection is ignored. Parity checking is disabled after reset.
5:1	Reserved	Reserved. Read returns zero.
0	IOACS	I/O space access (W). Set to allow the PCT789T-A to respond to I/O space accesses.

Configuration Revision (08h, R)

BCLS[7:0]								SCLS[7:0]							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

PGIF[7:0]								REV[7:0]							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
31:24	BCLS[7:0]	Base class (R: default 07h). Indicates that the PCT789T-A modem controller is a simple communication device class.
23:26	SCLS[7:0]	Subclass (R: default 80h). Indicates the sub-class code for the PCT789T-A modem controller (as other communication device).
15:8	PGIF[7:0]	Step number (R: default 00h). Indicates the PCT789T-A program interface.
7:0	REV[7:0]	Revision number (R: default 01h). Indicates the PCT789T-A revision number.

Configuration Base Address (10h, R/W)

BIOA[31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

BIOA[15:5]											Reserved			0	MIO
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
31:5	BIOA[31:5]	Configuration base I/O address (R/W: default 00003Exxh). Defines the address assignment for on-chip registers.
4:2	Reserved	Reserved.
1	Reserved	Reserved. Read returns zero.
0	MIO	I/O space indicators (R: default 1b). Indicates the register maps into the I/O space. This bit always returns 1 upon reading.

Subsystem ID / Subsystem Vendor ID (2Ch, R)

SSYID[15:0]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

SSVID[15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
31:16	SSYID[15:0]	Subsystem ID (R: default 0001h). Allows add-in card or subsystem vendors to put their product ID in this field. During normal operation, this register is read-only. However, a new value can be downloaded into this field during power-up through external serial EEPROM if it is available and valid. In addition, a write-enable bit for this register is defined in bit 11 of local control register 6 which can be used by the BIOS to overwrite this register for the desired subsystem ID before the OS being loaded.
15:0	SSVID[15:0]	Subsystem vendor ID (R: default 134Dh). Allows add-in card or subsystem vendors to put their unique ID in this field. During normal operation, this register is read-only. However, the content of this register can be changed in several ways: • The PCT789T-A checks the availability of the external serial EEPROM during the power-up reset period and if the data is valid, loads the configuration information into the corresponding registers. • A write-enable bit for this register is defined in bit 1 of local control register 6, which can be used by the BIOS to overwrite this register for the desired subsystem vendor ID before the OS being loaded. * Contact your PC-TEL representative for more information on subsystem vendor ID codes.

Power Management Capability Register Pointer (34h, R/W)

0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**

0	0	0	0	0	0	0	0	CAPRP[7:0]							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Bit Definitions:

Bits	Name	Description
31:8	Reserved	Reserved. Read returns zero.
7:0	CAPRP[7:0]	Capability register pointer (R: default 40h). Indicates the offset location of the Power Management Capability register of the PC-TEL HSP modem module in the PCI configuration register space. The PC-TEL power management registers are mapped to 40h–47h in the PCI configuration register space.

Configuration Interrupt (3Ch, R/W)

0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**

IPIN[7:0]								ILIN[7:0]							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Bit Definitions:

Bits	Name	Description
31:16	Reserved	Reserved. Read returns zero.
15:8	IPIN[7:0]	Interrupt pin (R: default 01h). Indicates the PCT789T-A uses INTA* as its interrupt pin.
7:0	ILIN[7:0]	Interrupt line (R/W: default 00h). Provides interrupt line routing information, POST software writes the routing information into this register as it initializes and configures the system.

Power Management Capability (40h, R)

PMED3C	PMED3H	PMED2	0	PMED0	D2PMS	0	AUXC[2:0]			0	0	0	PMEV[2:0]		
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**

0	0	0	0	0	0	0	0	CAPID[7:0]							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Bit Definitions:

Bits	Name	Description
31	PMED3C	Assert PME# from D3cold (R: 1b or 0b). Indicates that PME# can be asserted from D3cold state when VAUXDET input is high (Vaux power is present). When Vaux power is not present, this bit returns 0.
30	PMED3H	Assert PME# from D3hot (R: 1b). Indicates that PME# can be asserted from D3hot state.
29	PMED2	Assert PME# from D2 (R: 1b). Indicates that PME# can be asserted from D2 state.
28	Reserved	Reserved. Read returns zero.
27	PMED0	Assert PME# from D0 (R: 1b). Indicates that PME# can be asserted from D0 state.
26	D2PMS	D2 state support (R: 1b). Indicates that the HSP modem function supports the D2 power management state.
25	Reserved	Reserved. Read returns zero.
24:22	AUXC[2:0]	Auxiliary current (R: 001b). Indicates the 3.3Vaux auxiliary current requirement for the PC-TEL HSP modem module. For 3.3Vaux current requirement reporting from the Data register, use a value of 000b.
21:19	Reserved	Reserved. Read returns zero.
18:16	PMEV[2:0]	Version (R: 010b). Indicates which revision of the PCI Power Management Interface Specification that the PC-TEL HSP modem module complies with.
15:8	Reserved	Reserved. Read returns zero.
7:0	CAPID[7:0]	Capability ID (R: 01h). Indicates that the linked list item is the PCI Power Management registers.

Power Management Control/Status (44h, R, R/W)

0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**

PMESTS	0	0	0	0	0	0	PMEEN	0	0	0	0	0	0	PMST[1:0]	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Bit Definitions:

Bits	Name	Description
31:16	Reserved	Reserved. Read returns zero.
15	PMESTS	PME# status (R/W-clear: default 0b). Set when an event causes PME# to be asserted independent of the state of PMEEN bit. Writing a 1 to this bit clears it and deasserts the PME# signal if enabled. Writing a 0 has no effect. Since the PC-TEL HSP modem module supports PME# from D3cold, this bit must be explicitly cleared by the OS each time it is initially loaded.
14:9	Reserved	Reserved. Read returns zero.
8	PMEEN	PME# enable (R/W: default 0b). When set, enables PME# to be asserted. Otherwise PME# assertion is disabled. Since the PC-TEL HSP modem module supports PME# from D3cold, this bit must be explicitly cleared by the OS each time it is initially loaded.
7:2	Reserved	Reserved. Read returns zero.
1:0	PMST[1:0]	Power state (R/W: default 11b). Used to determine the current power state of the PC-TEL HSP modem module and to set it into a new power state. Supported field values are shown below. Software attempts to write an unsupported state to this field have no effect.

PMST[1:0]	Power State
00	D0
01	D1 (not defined)
10	D2
11	D3hot

PCT789T-A CONTROL REGISTERS

PCT789T-A Control Register Summary

Table 15 PCT789T-A Control Registers

Index	Write			Read	
	Hi Byte		Lo Byte	Hi Byte	Lo Byte
0	TxData[15:8]		TxData[7:0]	RxData[15:8]	RxData[7:0]
1	CNTL[15:8]		CNTL[7:0]	STS[15:8]	STS[7:0]
2	Reserved		EXTOUT[7:0]	Reserved	EXTIN[3:0]
3	Reserved	TOC[3:0]	FFSZ[7:0]	ERRCNT[11:8]	ERRCNT[7:0]
4	Reserved				
5	Reserved		CLK1D[7:0]	Reserved	
6-15	Reserved			Reserved	
16-255	Not Accessible			Not Accessible	

PCT789T-A Control Register Detailed Description

Transmit Data (Register 0, W)

TxData[15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	TxData[15:0]	Transmit data register. Input port to the transmit FIFO.

Receive Data (Register 0, R)

RxData[15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	RxData[15:0]	Receive data. Output port for the receive FIFO.

Control (Register 1, W)

SLEEP	AFEPDN	XIRQEN	XIRQ POL	AFERST	XIRQTYP	Reserved		NTORST	ENIRQ	START	Reserved	ENTX	Reserved		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

The default value for this register is 0000h.

Bit Definitions:

Bits	Name	Description
15	SLEEP	Power-down ASIC (sleep mode, stop clocks).
14	AFEPDN	Power-down AFE (active-low).
13	XIRQEN	External IRQ enable.
12	XIRQPOL	External IRQ polarity. 1 = positive-edge; 0 = trailing-edge
11	AFERST	AFE reset (active-low).
10	XIRQTYP	External IRQ type. 1 = pass-thru; 0 = re-sync.
9:8	Reserved	Reserved.
7	NTORST	Disable time-out reset (level).
6	ENIRQ	IRQ enable (level).
5	START	Start (positive-edge).
4	Reserved	Reserved.
3	ENTX	Transmit enable (positive-edge).
2:0	Reserved	Reserved.

Status (Register 1, R)

Reserved	IMODE[2:0]			Reserved			RIRQS	Reserved				XIRQS	IRQS	Rx OVRUN	Tx UDRUN
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Bit Definitions:

Bits	Name	Description
15	Reserved	Reserved.
14:12	IMODE[2:0]	IMODE[2:0].
11:9	Reserved	Reserved.
8	RIRQS	Ring IRQ status.
7:4	Reserved	Reserved.
3	XIRQS	XIRQS (reset after read).
2	IRQS	IRQS (reset after read).
1	RxOVRUN	Receive buffer overrun (reset after read).
0	TxUDRUN	Transmit buffer underrun (reset after read).

External Output (Register 2, W)

Reserved								EXTOUT[7:0]							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:8	Reserved	Reserved.
7:0	EXTOUT[7:0]	External output register (default 00h). Directly drives four programmable output pins. EXTOUT[7:4]: OUT[7:4]. EXTOUT[3]: mute speaker. EXTOUT[2]: handset relay control. EXTOUT[1]: Caller ID relay control. EXTOUT[0]: OFF-Hook relay control.

External Input (Register 2, R)

Reserved												EXTIN[3:0]			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:4	Reserved	Reserved.
3:0	EXTIN[3:0]	External input register allows system to monitor four programmable input pins. EXTIN[3:2]: IN[1:0] EXTIN[1]: ILC-Sense (or handset detect) input. EXTIN[0]: ring detect input.

Miscellaneous Control (Register 3, W)

Reserved				TOC[3:0]				FFSZ[7:0]							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:12	Reserved	Reserved.
11:8	TOC[3:0]	Time-out count register (default 00h). Allows PCT789T-A to generate internal time-out if errors detected for (N+1)*256*FFSZ*1/Sampling Frequency, where N=0–15.
7:0	FFSZ[7:0]	FIFO size control register (default 20h). Allows Tx and Rx buffer size to be chosen up to 128 words deep (the legal number accepted is between 16 and 128). Whenever the Rx buffer is full, INTA is generated, if enabled.

Error Count (Register 3, R)

Reserved				ERRCNT[11:0]											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:12	Reserved	Reserved.

Bits	Name	Description
11:0	ERRCNT[11:0]	Error count records the number of overrun and underrun errors occurred.

CLK1 Divider (Register 5, W)

CLK1D[7:0]							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	CLK1D[7:0]	CLK1 divider register provides a programmable divider for generating CLK1 output for various CODEC from the crystal oscillator input.

CLK1D[7]	CLK1D[6]	Function
0	0	*2 invert
0	1	*2
1	0	/1
1	1	/2

CLK1D[5]	CLK1D[4]	CLK1D[3]	Function
0	0	0	DIVA =1
0	0	1	DIVA = 2
0	1	0	DIVA = 3
0	1	1	DIVA =4
1	0	0	DIVA = 5
1	0	1	DIVA = 6
1	1	0	Reserved
1	1	1	DIVA = 8

CLK1D[2]	CLK1D[1]	CLK1D[0]	Function
0	0	0	DIVB=1
0	0	1	DIVB=2.5
0	1	0	DIVB=3
0	1	1	DIVB=3.5
1	0	0	DIVB=4
1	0	1	DIVB=4.5
1	1	0	DIVB=5
1	1	1	DIVB=5.5

PCT303DW CONTROL REGISTERS

Any register not listed here is reserved and should not be written.

Control 1 (Register 1, R/W)

7	6	5	4	3	2	1	0
SR	Reserved					DL	SB

Reset settings: 00h

Bit Definitions:

Bits	Name	Description
7	SR	Software reset. 1 = Sets all registers to their reset value. 0 = Enables chip for normal operation. Bit automatically clears after being set.
6:2	Reserved	Reserved. Read returns zero.
1	DL	Isolation digital loopback. 1 = Enables digital loopback mode across isolation barrier. Line side must be enabled prior to setting this mode.
0	SB	Serial digital interface mode. 1 = The serial port is operating in 16-bit mode and requires use of the secondary frame sync signal, FC, to initiate control data reads/writes. 0 = Operation is in 15-bit mode and the LSB of the data field indicates whether a secondary frame is required.

Control 2 (Register 2, R/W)

7	6	5	4	3	2	1	0
Reserved				AL	Reserved	HBE	RXE

Reset settings: 03h

Bit Definitions:

Bits	Name	Description
7:4	Reserved	Reserved. Read returns zero.
3	AL	Analog loopback. 1 = Enables analog loopback mode.
2	Reserved	Reserved. Read returns zero.
1	HBE	Hybrid enable. 1 = Connects transmit path in hybrid.
0	RXE	Receive enable. 1 = Enables receive path.

Control 3 (Register 3, R)

7	6	5	4	3	2	1	0
Reserved							

Reset settings: 00h

Bit Definitions:

Bits	Name	Description
7:0	Reserved	Reserved. Read returns zero.

Control 4 (Register 4, R)

Reserved							
7	6	5	4	3	2	1	0

Reset settings: 00h

Bit Definitions:

Bits	Name	Description
7:0	Reserved	Reserved. Read returns zero.

DAA Control 1 (Register 5, R/W)

Reserved	RDTN	RDTP	OPOL	ONHM	RDT	OHE	OH
7	6	5	4	3	2	1	0

Reset settings: 00h

Bit Definitions:

Bits	Name	Description
7	Reserved	Reserved. Read returns zero.
6	RDTN	Ring detect signal negative. Read-only. When set, a negative ring signal is occurring.
5	RDTP	Ring detect signal positive. Read-only. When set, a positive ring signal is occurring.
4	OPOL	Off-hook polarity. 1 = Off-hook pin is active-high. 0 = Off-hook pin is active-low.
3	ONHM	On-hook line monitor. 1 = Enables low-power monitoring mode allowing the DSP to receive line activity without going off-hook.
2	RDT	Ring detect. Read-only. 1 = Indicates a ring is occurring. 0 = Reset either 4.5–9 seconds after last positive ring is detected or when the system executes an off-hook.
1	OHE	Off-hook pin enable. 1 = Enables the operation of the off-hook pin. 0 = Off-hook pin is ignored.
0	OH	Off-hook. 1 = Causes the line-side chip to go off-hook. This bit operates independently of OHE and is a logic OR with the off-hook pin when enabled.

DAA Control 2 (Register 6, R/W)

CPE	ATM1	ARM1	PDL	PDN	Reserved	ATM0	ARM0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Reset settings: 70h

Bit Definitions:

Bits	Name	Description
7	CPE	Charge pump enable. 1 = Charge pump on. 0 = Charge pump off.
6,1	ATM[1:0]	AOUT transmit path level control.

ATM[1:0]	Description
00	–20dB transmit path attenuation for call progress AOUT pin only.
01	–32dB transmit path attenuation for call progress AOUT pin only.
10	Mutes transmit path for call progress AOUT pin only.
11	–26dB transmit path attenuation for call progress AOUT pin only.

5,0	ARM[1:0]	AOUT receive path level control.

ARM[1:0]	Description
00	0dB receive path attenuation for call progress AOUT pin only.
01	–12dB receive path attenuation for call progress AOUT pin only.
10	Mutes receive path for call progress AOUT pin only.
11	–6dB receive path attenuation for call progress AOUT pin only.

4	PDL	Power down line-side chip. 1 = Places the PCT303W in lower power mode. 0 = Normal operation. Program the clock generator before clearing this bit.
3	PDN	Power down. 1 = Powers down the PCT303DW. A reset pulse on $\overline{\text{RESET}}$ is required to restore normal operation.
2	Reserved	Reserved. Read returns zero.

PLL1 Divide N1 (Register 7, R/W)

Divider N1							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Reset settings: 00h (serial mode 0, 1, 2)

Bit Definitions:

Bits	Name	Description
7:0	Divider N1	Contains the (value – 1) for determining the output frequency on PLL1.

PLL1 Multiply M1 (Register 8, R/W)

Multiplier M1							
7	6	5	4	3	2	1	0

Reset settings: 00h (serial mode 0,1)

Reset settings: 13h (serial mode 2)

Bit Definitions:

Bits	Name	Description
7:0	Multiplier M1	Contains the (value – 1) for determining the output frequency on PLL1.

PLL2 Divide/Multiply N2/M2 (Register 9, R/W)

Divider N2				Multiplier M2			
7	6	5	4	3	2	1	0

Reset settings: 00h (serial mode 0, 1, 2)

Bit Definitions:

Bits	Name	Description
7:4	Divider N2	Contains the (value – 1) for determining the output frequency on PLL2.
3:0	Multiplier M2	Contains the (value – 1) for determining the output frequency on PLL2.

PLL Control (Register 10, R/W)

Reserved							CGM
7	6	5	4	3	2	1	0

Reset settings: 00h

Bit Definitions:

Bits	Name	Description
7:1	Reserved	Reserved. Read returns zero.
0	CGM	Clock Generation Mode. 1 = A 25/16 ratio is applied to the PLL allowing for a more flexible choice of MCLK frequencies while slowing down the PLL lock time. 0 = No additional ratio is applied to the PLL and faster lock times are possible.

DSP-Side Chip Revision (Register 11, R)

Reserved				REVA			
7	6	5	4	3	2	1	0

Reset settings: N/A

Bit Definitions:

Bits	Name	Description
7:4	Reserved	Reserved. Read returns zero.
3:0	REVA	Chip revision. Read-only. Four-bit value indicating the revision of the PCT303D (DSP-side) silicon.

Line-Side Status (Register 12, R/W)

CLE	FDT	Reserved		LCS			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Reset settings: N/A

Bit Definitions:

Bits	Name	Description
7	CLE	Communications (ISOlink) error. 1 = Indicates a communication problem between the PCT303D and the PCT303W. When it goes high, it remains high until a logic 0 is written to it.
6	FDT	Frame detect. Read-only. 1 = Indicates ISOLink frame lock has been established. 0 = Indicates ISOLink has not established frame lock.
5:4	Reserved	Reserved. Read returns zero.
3:0	LCS	Loop current sense. Read-only. Four-bit value returning the loop current in 6mA increments. 0 = Loop current < 6mA. 1111 = Loop current > 120mA. See “Loop Current Monitor” on page 25.

Transmit and Receive Gain (Register 13, R/W)

Reserved	CBID	REVB				ARX	ATX
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Reset settings: 00h

Bit Definitions:

Bits	Name	Description
7	Reserved	Reserved. Read returns zero.
6	CBID	Chip B ID. Read-only. 1 = Indicates the line-side has international support. 0 = Indicates the line-side is domestic only.
5:2	REVB	Chip revision. Read-only. Four-bit value indicating the revision of the PCT303W (line-side) silicon.
1	ARX	Receive gain.[a] 1 = A +6dB gain is applied to the receive path. 0 = 0dB gain is applied.
0	ATX	Transmit gain.[a] 1 = A –3dB gain (attenuation) is applied to the transmit path. 0 = 0dB gain is applied.

a. See register 15 for additional transmit/receive gain and attenuation steps.

Daisy-Chain Control (Register 14, R/W)

NSLV[2:0]			SSEL[1:0]		FSD	RPOL	DCE
7	6	5	4	3	2	1	0

Reset settings: 02h (serial mode 0,1)

Reset settings: 3Fh (serial mode 2)

Bit Definitions:

Bits Name Description

7:5 NSLV[2:0] Number of slave devices.

NSLV[2:0]	Description
000	0 slave devices. Simply redefines the FC/RGDT and RGDT/FSD pins.
001	1 slave device.
010	2 slave devices.
011	3 slave devices.
100	4 slave devices. For four or more slave devices, the FSD bit MUST be set.
101	5 slave devices.
110	6 slave devices.
111	7 slave devices.

4:3 SSEL[1:0] Slave device select.

SSEL[1:0]	Description
00	16-bit SDO receive data.
01	Reserved.
10	15-bit SDO receive data. LSB = 1 for the PCT303DW device.
11	15-bit SDO receive data. LSB = 0 for the PCT303DW device.

2 FSD Delayed frame sync control.
1 = Sets the number of SCLK periods between frame syncs to 16.
0 = Sets the number of SCLK periods between frame syncs to 32.
This bit MUST be set when PCT303DW devices are used as slaves. For the master PCT303DW, only serial mode 1 is allowed in this case.

1 RPOL Ring detect polarity.
1 = The FC/RGDT pin (operating as ring detect) is active-high.
0 = The FC/RGDT pin (operating as ring detect) is active-low.

0 DCE Daisy-chain enable.
1 = Enables the PCT303DW to operate with slave devices on the same serial bus. The FC/RGDT signal (pin 7) becomes the ring detect output and the RGDT/FSD signal (pin 15) becomes the delayed frame sync signal. Note that ALL other bits in this register are ignored if DCE = 0.

TX/RX Gain Control (Register 15, R/W)

TXM	ATX[2:0]			RXM	ARX[2:0]		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Reset settings: 00h

Bit Definitions:

Bits	Name	Description
7	TXM	Transmit mute. 1 = Mutes the transmit signal.
6:4	ATX[2:0]	Analog transmit attenuation.

ATX[2:0]	Description
000	0dB attenuation.
001	3dB attenuation.
010	6dB attenuation.
011	9dB attenuation.
1xx	12dB attenuation.

NOTE: Register 13 bit 0 (ATX) must be 0 for these bits to work as expected. Unpredictable results can occur if ATX is 1 and these bits are non-zero.

3	RXM	Receive mute. 1 = Mutes the receive signal.
2:0	ARX[2:0]	Analog receive gain.

ATX[2:0]	Description
000	0dB gain.
001	3dB gain.
010	6dB gain.
011	9dB gain.
1xx	12dB gain.

NOTE: Register 13 bit 1 (ARX) must be 0 for these bits to work as expected. Unpredictable results can occur if ARX is 1 and these bits are non-zero.

International Control 1 (Register 16, R/W)

ONS[1:0]		ACT	IIRE	DCT[1:0]		RZ	RT
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Reset settings: 08h

Bit Definitions:

Bits Name Description

7:6 ONS[1:0] On-hook speed.

ONS[1:0]	Description
00	The PCT303DW will execute a slow controlled on-hook.
11	The PCT303DW will execute a fast on-hook.

5 ACT AC termination select.
1 = Selects the complex impedance.
0 = Selects the real impedance.

4 IIRE IIR filter enable.
1 = IIR filter enabled for transmit and receive filters. (See Figures 25–28 on page 61.)
0 = FIR filter enabled for transmit and receive filters. (See Figures 21–24 on page 60.)

3:2 DCT[1:0] DC termination select.

DCT[1:0]	Mode	Description
00	0	Low voltage mode. See “Appendix: NET4 Country Support” on page 65. (Transmit level = –2dBm).
01	1	Low voltage mode. Provides different I/V characteristics than mode 0. (Transmit level = –5dBm).
10	2	Standard voltage mode. (Transmit level = –1dBm).
11	3	Current limiting mode. (Transmit level = –1dBm).

1 RZ Ringer impedance select.
When set, ringer impedance is decreased to satisfy some countries’ ringer requirements.

0 RT Ringer threshold select.
Used to satisfy country requirements on ring detection. Signals below the lower level will not generate a ring detection; signals above the upper level are guaranteed to generate a ring detection.
1 = 15 ±5 Vrms
0 = 21.5 ±4.5 Vrms

International Control 2 (Register 17, R/W)

Reserved					BTE	ROV	BTD
7	6	5	4	3	2	1	0

Reset settings: 00h

Bit Definitions:

Bits	Name	Description
7:3	Reserved	Reserved. Read returns zero.
2	BTE	Billing tone detector enable. When set, the PCT303DW can detect a billing tone signal on the line and maintain off-hook through the billing tone. If a billing tone is detected, bit 0 (BTD) is set to indicate the event.
1	ROV	Receive overload. Read-only. This bit is set when the receive input detects an excessive input level. This bit is cleared by writing a zero to this location.
0	BTD	Billing tone detected. Read-only. This bit is set if bit 2 (BTE) is enabled and a billing tone is detected. This bit is cleared by writing a zero to this location.

International Control 3 (Register 18, R/W)

Reserved						RFWE	SQLCH
7	6	5	4	3	2	1	0

Reset settings: 00h

Bit Definitions:

Bits	Name	Description
7:2	Reserved	Reserved. Read returns zero.
1	RFWE	Ring detector full-wave rectifier enable. Read-only. When set, the ring-detection circuitry provides full-wave rectification. This effects the data stream presented on SDO during ring detection.
0	SQLCH	Ring detect network squelch. This bit must be set, then cleared, following a polarity reversal detection.

ELECTRICAL CHARACTERISTICS

PCT789T-A Electrical Characteristics

Unless otherwise noted, electrical characteristics are specified over the operating range. Typical values are: VDD = +3.3 V; T_{AMB} = 25 °C.

PCT789T-A Absolute Maximum Ratings

These absolute maximum ratings are referenced to GND.

Table 16 PCT789T-A Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
DC supply voltage	V_{DD}	–0.3, 7.0	V
Digital input voltage	V_I, V_{IN}	–0.3, V_{DD}+0.3	V
Digital input current	I_I, I_{IN}	±1	mA
Operating temperature	T_{OPER}	0, 70	°C
Storage temperature	T_{STG}	–40, 125	°C
Maximum power dissipation	P_{DMAX}	200	mW
Electrostatic discharge	ESD	2000	V

PCT789T-A DC Characteristics

Unless otherwise specified, given values are: V_D = +3.3 V ± 5%; GND = 0 V; T_A = 0 °C to 70 °C.

Table 17 PCT789T-A DC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply And Common Mode Voltage					
Supply voltage	V_{DD}	3.14	3.3	3.47	V
Digital supply current	I_{DDD}		TBD		mA
Digital Interface (T_A = 25ºC, D_{VDD} = +3.3V)					
Low-level input voltage	V_{IL}	-0.3		0.8	V
High-level input voltage	V_{IH}	2.2		Vcc+0.3	V
Input current V_I = V_{DD} or V_I = GND	I_I	-10	±1	10	µA
High-level output voltage (I_{LOAD} = -600µA)	V_{OH}	2.4			V
Low-level output voltage (I_{LOAD} = 800µA)	V_{OL}			0.4	V

PCT303DW Electrical Characteristics

PCT303DW Recommended Operating Conditions

Table 18 PCT303DW Recommended Operating Conditions

Parameter [a]	Symbol	Test Condition	Min [b]	Typ	Max [a]	Unit
Ambient temperature	T_A	K-grade	0	25	70	°C
Ambient temperature	T_A	B-grade	–40	25	85	°C
PCT303D supply voltage, analog	V_A		3.0	3.3/5.0	5.25	V
PCT303D supply voltage, digital [c]	V_D		3.0	3.3/5.0	5.25	V

a. The PCT303DW specifications are guaranteed when the typical application circuit (including component tolerance) and any PCT303D and PCT303W are used. See Figure 2 for typical application circuit.
b. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25°C unless otherwise stated.
c. The digital supply, V_D, can operate from either 3.3V or 5.0V. The PCT303D supports interface to 3.3V logic when operating from 3.3V. The 3.3V operation applies to both the serial port and the digital signals RGDT/FSD, OFHK, $\overline{\text{RESET}}$, M0, and M1.

PCT303DW Absolute Maximum Ratings

Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 19 PCT303DW Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
DC supply voltage	V_D, V_A	–0.5 to +6.0	V
Input current, PCT303D digital input pins	I_{IN}	±10	mA
Digital input voltage	V_{IND}	–0.3 to (V_D+0.3)	V
Operating temperature range	T_A	–10 to +100	°C
Storage temperature range	T_{STG}	–40 to +150	°C

PCT303DW Loop Characteristics

Given values are: V_A = charge pump, V_D = +3.3 V ± 5%; T_A = 0 °C to 70 °C for K-grade, –40 °C to +85 °C for B-grade; refer to Figure 20 on page 60.

Table 20 PCT303DW Loop Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC termination voltage	V_{DCT}	I_L = 20mA			7.7	V
DC termination voltage	V_{DCT}	I_L = 120mA	12			V
DC ring current (with Caller ID)	I_{RDC}				500	µA
DC ring current (w/o Caller ID)	I_{RDC}				20	µA
AC termination impedance	Z_{ACT}			600		Ω
Operating loop current	I_{LP}		20		100	mA
Ring voltage detect	V_{RD}		13	18	26	V_{RMS}
Ring frequency	F_R		15		68	Hz
On-hook leakage current	I_{LK}	V_{BAT} = –48V			1	µA
Ringer equivalence num. (with Caller ID)	REN				1.2	
Ringer equivalence num. (w/o Caller ID)	REN				0.2	

PCT303DW DC Characteristics

V_D = 5V

Given values are: V_A = +5 V ±5%; V_D = +5 V ± 5%; T_A = 0 °C to 70 °C for K-grade, –40 °C to +85 °C for B-grade.

Table 21 PCT303DW DC Characteristics, V_D = +5V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High-level input voltage	V_{IH}		3.5			V
Low-level input voltage	V_{IL}				0.8	V
High-level output voltage	V_{OH}	I_O = –2mA	2.4			V
Low-level output voltage	V_{OL}	I_O = +2mA			0.4	V
Input leakage current	I_L				±10	µA
Power supply current, analog	I_A	V_A pin		1	6	mA
Power supply current, digital	I_D	V_D pin		13	17	mA
Total supply current, sleep mode					1.5	mA

V_D = 3.3V

Given values are: V_A = charge pump; V_D = +3.3 V ± 10%; T_A = 0 °C to 70 °C for K-grade, –40 °C to +85 °C for B-grade.

Table 22 PCT303DW DC Characteristics, V_D = +3.3V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High-level input voltage	V_{IH}		2.0			V
Low-level input voltage	V_{IL}				0.8	V
High-level output voltage	V_{OH}	I_O = –2mA	2.4			V
Low-level output voltage	V_{OL}	I_O = +2mA			0.35	V
Input leakage current	I_L				±10	µA
Power supply current, analog	I_A	V_A pin		1	6	mA
Power supply current, digital	I_D	V_D pin		8	11	mA
Total supply current, sleep mode					1.5	mA

PCT303DW AC Characteristics

Given values are: V_A = charge pump, V_D = +3.3 V ± 5%; T_A = 0 °C to 70 °C for K-grade, –40 °C to +85 °C for B-grade.

Table 23 PCT303DW AC Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Freq response, transmit [a,b]	F_{RT}	Low –3dB corner		33		Hz
Freq response, transmit [a,b]	F_{RT}	300Hz	–0.2		0	dB
Freq response, transmit [b]	F_{RT}	3400Hz	–0.2		0	dB
Transmit full scale level [c] (0dB gain)	V_{TX}			0.98		V_{peak}
Freq response, receive [a,b]	F_{RR}	Low –3dB corner		33		Hz
Freq response, receive [a,b]	F_{RR}	300Hz	–0.01		0	dB
Freq response, receive [b]	F_{RR}	3400Hz	–0.2		0	dB
Receive full scale level [c,d] (0dB gain)	V_{RX}			0.98		V_{peak}
Dynamic range [e]	DR	VIN = 1kHz, –60dB		84		dB
Total harmonic distortion [f]	THD	VIN = 1kHz, –3dB			–84	dB
Gain drift	A_T	VIN = 1kHz		0.002		dB/°C
Dynamic range (call progress AOUT)	DR_{AO}	VIN = 1kHz	60			dB
THD (call progress AOUT)	THD_{AO}	VIN = 1kHz			1.0	%
AOUT full scale level				$0.75V_A$		V_{p-p}
AOUT output impedance				10		kΩ
Mute level (call progress AOUT)			–90			dB
Dynamic range (Caller ID mode)	DR_{CID}	VIN = 1kHz, –60dB		60		dB
Caller ID full scale level (0dB gain) [c]	V_{CID}			0.8		V_{peak}

a. These characteristics are determined by external components. See Figure 2 on page 6.
b. Sample rate = 8 kHz
c. Parameter measured at Tip and Ring of Figure 2 on page 6.
d. Full scale receive level produces –0.9dBFS at SDO.
e. DR = 60dB + 20 log (RMS signal/RMS noise). Applies to both the transmit and receive paths. Measurement bandwidth is 10Hz to 3400Hz. Valid sample rate ranges between 7200Hz and 11025Hz.
f. THD = 20 log (RMS distortion/RMS signal). Applies to both the transmit and receive paths. Valid sample rate ranges between 7200Hz and 11025Hz.

SWITCHING CHARACTERISTICS

General Inputs

Given values are: V_A = charge pump, V_D = +3.3 V ± 5%; T_A = 70 °C for K-grade, 85 °C for B-grade; C_L = 20 pF.

All timing is referenced to the 50% level of the waveform. Input test levels are: $V_{IH} = V_D – 0.4V$, $V_{IL} = 0.4V$.

Table 24 Switching Characteristics—General Inputs

Parameter	Symbol	Min	Typ	Max	Unit
Cycle time, MCLK	t_{mc}	16.67			ns
MCLK duty cycle	t_{dty}	40	50	60	%
Rise time, MCLK	t_r			5	ns
Fall time, MCLK	t_f			5	ns
MCLK before $\overline{\text{RESET}}$ ↑	t_{mr}	10			cycles
$\overline{\text{RESET}}$ pulse width [a]	t_{rl}	250			ns
M0, M1 before $\overline{\text{RESET}}$ ↑ [b]	t_{mxr}	20			ns

a. The minimum $\overline{\text{RESET}}$ pulse width is the greater of 250ns or 10 MCLK cycle times.
b. M0 and M1 are typically connected to V_D or GND and should not be changed during normal operation.

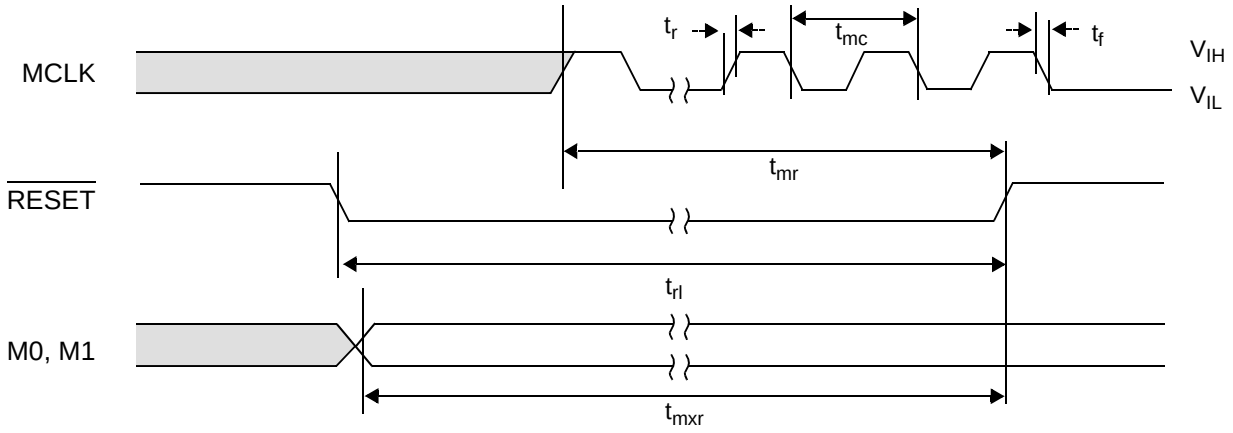


Figure 16 General Inputs Timing Diagram

Serial Interface (DCE = 0)

Given values are: V_A = charge pump, V_D = +3.3 V ± 5%; T_A = 70 °C for K-grade, 85 °C for B-grade; C_L = 20 pF.

All timing is referenced to the 50% level of the waveform. Input test levels are: $V_{IH} = V_D - 0.4V$, $V_{IL} = 0.4V$.

Table 25 Switching Characteristics—Serial Interface (DCE = 0)

Parameter	Symbol	Min	Typ	Max	Unit
Cycle time, SCLK	t_c	354	1/256 Fs		ns
SCLK duty cycle	t_{dty}		50		%
Delay time, SCLK ↑ to $\overline{\text{FSYNC}}$ ↓	t_{d1}			10	ns
Delay time, SCLK ↑ to SDO valid	t_{d2}			20	ns
Delay time, SCLK ↑ to $\overline{\text{FSYNC}}$ ↑	t_{d3}			10	ns
Setup time, SDI before SCLK ↓	t_{su}	25			ns
Hold time, SDI after SCLK ↓	t_h	20			ns
Setup time, FC ↑ before SCLK ↑	t_{sfc}	40			ns
Hold time, FC ↑ after SCLK ↑	t_{hfc}	40			ns

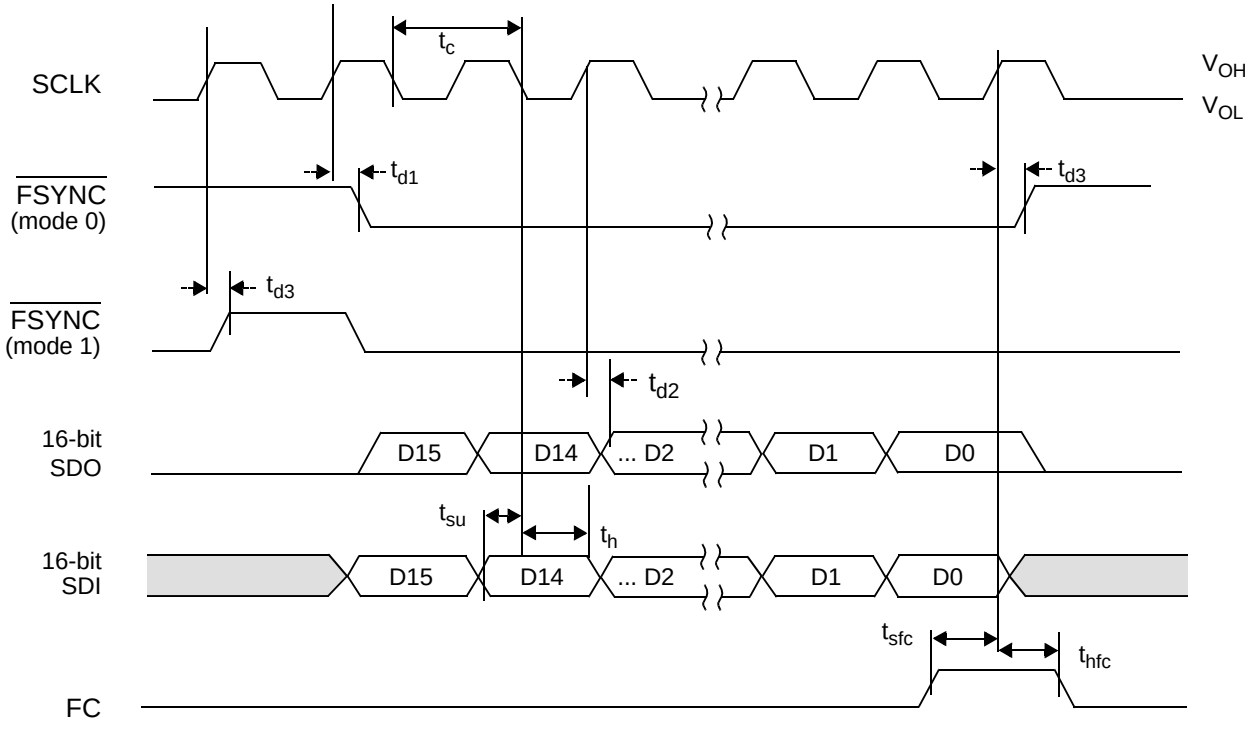


Figure 17 Serial Interface Timing Diagram (DCE = 0)

Serial Interface (DCE = 1, FSD = 0)

Given values are: V_A = charge pump, V_D = +3.3 V ± 5%; T_A = 70 °C for K-grade, 85 °C for B-grade; C_L = 20 pF.

All timing is referenced to the 50% level of the waveform. Input test levels are: $V_{IH} = V_D - 0.4V$, $V_{IL} = 0.4V$.

Table 26 Switching Characteristics—Serial Interface (DCE = 1, FSD = 0)

Parameter	Symbol	Min	Typ	Max	Unit
SCLK duty cycle	t_{dty}		50		%
Delay time, SCLK ↑ to $\overline{\text{FSYNC}}$ ↑	t_{d1}			10	ns
Delay time, SCLK ↑ to $\overline{\text{FSYNC}}$ ↓	t_{d2}			10	ns
Delay time, SCLK ↑ to SDO valid	t_{d3}			20	ns
Delay time, SCLK ↑ to SDO Hi-Z	t_{d4}			20	ns
Setup time, SDO before SCLK ↓	t_{su}	25			ns
Hold time, SDO after SCLK ↓	t_h	20			ns
Setup time, SDI before SCLK ↓	t_{su2}	25			ns
Hold time, SDI after SCLK ↓	t_{h2}	20			ns

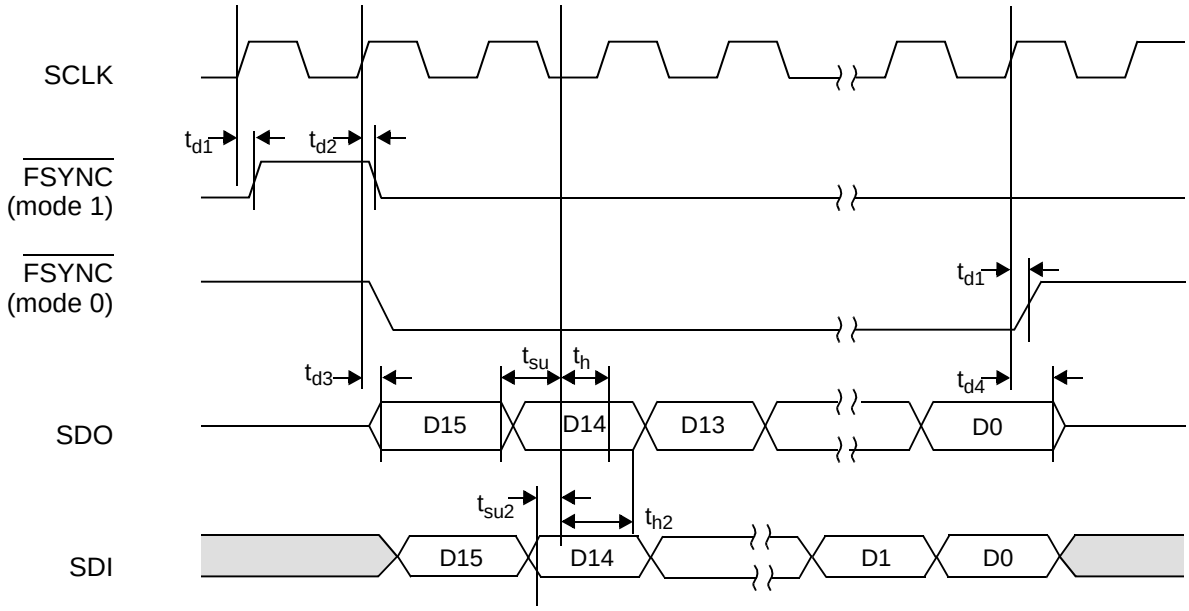


Figure 18 Serial Interface Timing Diagram (DCE = 1, FSD = 0)

Serial Interface (DCE = 1, FSD = 1)

Given values are: V_A = charge pump, V_D = +3.3 V ± 5%; T_A = 70 °C for K-grade, 85 °C for B-grade; C_L = 20 pF.

All timing is referenced to the 50% level of the waveform. Input test levels are: $V_{IH} = V_D - 0.4V$, $V_{IL} = 0.4V$.

Table 27 Switching Characteristics—Serial Interface (DCE = 1, FSD = 0)

Parameter	Symbol	Min	Typ	Max	Unit
Cycle time, SCLK	t_c	354	1/256 Fs		ns
SCLK duty cycle	t_{dty}		50		%
Delay time, SCLK ↑ to $\overline{\text{FSYNC}}$ ↑	t_{d1}			10	ns
Delay time, SCLK ↑ to $\overline{\text{FSYNC}}$ ↓	t_{d2}			10	ns
Delay time, SCLK ↑ to SDO valid	t_{d3}	$0.25t_c$–20		$0.25t_c$+20	ns
Delay time, SCLK ↑ to SDO Hi-Z	t_{d4}			20	ns
Delay time, SDO before $\overline{\text{RGDT}}$ ↓	t_{d5}			20	ns
Setup time, SDO before SCLK ↓	t_{su}	25			ns
Hold time, SDO after SCLK ↓	t_h	20			ns
Setup time, SDI before SCLK	t_{su2}	25			ns
Hold time, SDI after SCLK	t_{h2}	20			ns

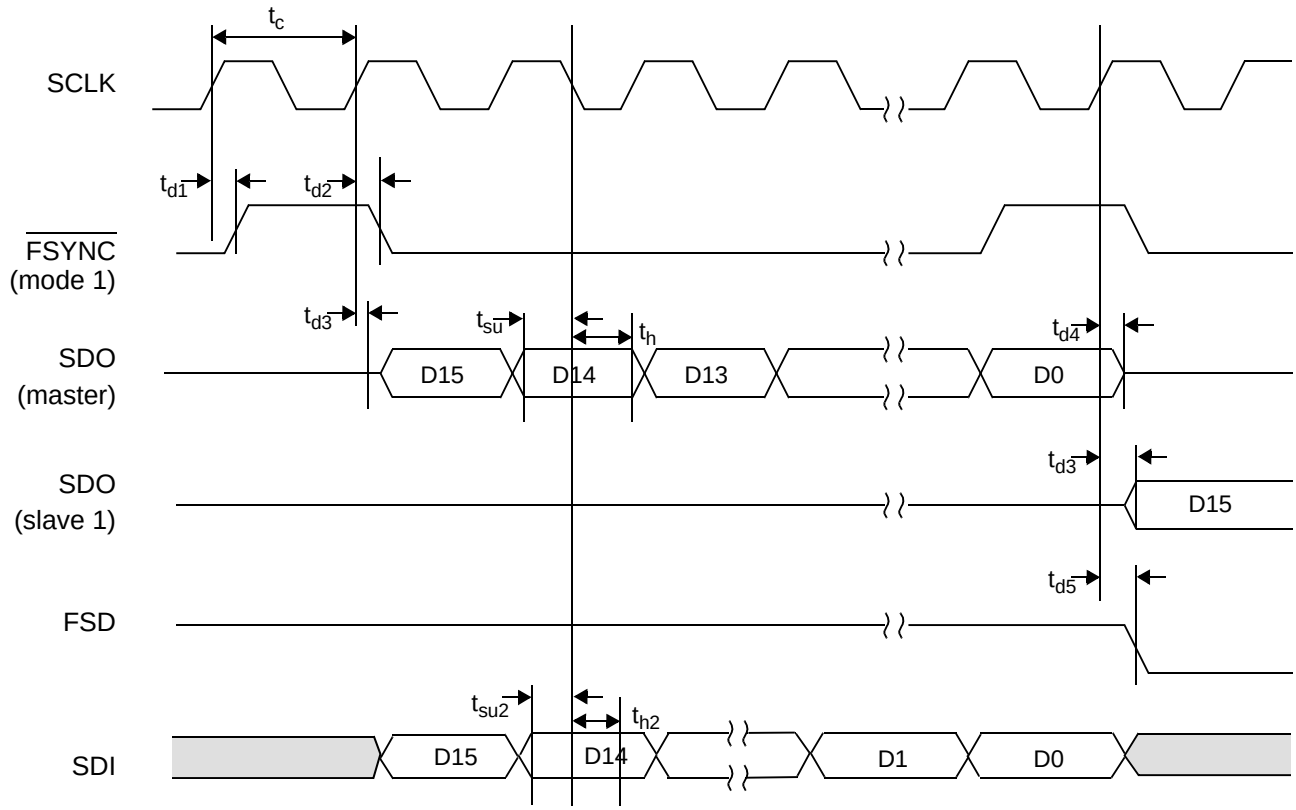


Figure 19 Serial Interface Timing Diagram (DCE = 1, FSD = 1)

DIGITAL FILTER CHARACTERISTICS

Digital FIR Filter Characteristics

Given values are: V_A = charge pump, V_D = +3.3 V ± 5%; sample rate = 8 kHz; T_A = 70 °C for K-grade, 85 °C for B-grade.

Typical FIR filter characteristics for Fs = 8000Hz are shown in Figures 21, 22, 23, and 24.

Table 28 Digital FIR Filter Characteristics—Transmit and Receive

Parameter	Symbol	Min	Typ	Max	Unit
Passband (0.1dB)	$F_{(0.1dB)}$	0		3.3	kHz
Passband (3dB)	$F_{(3dB)}$	0		3.6	kHz
Passband ripple peak-to-peak		–0.1		0.1	dB
Stopband			4.4		kHz
Stopband attenuation		–74			dB
Group delay	t_{gd}		12/Fs		sec

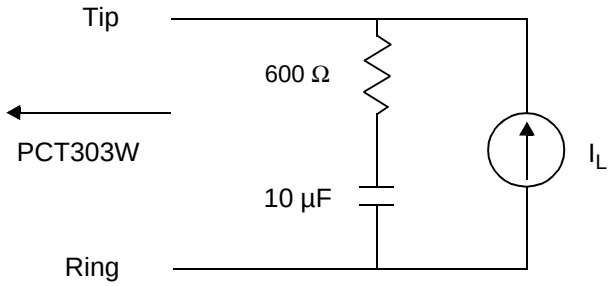
Digital IIR Filter Characteristics

Given values are: V_A = charge pump, V_D = +3.3 V ± 5%; sample rate = 8 kHz; T_A = 70 °C for K-grade, 85 °C for B-grade.

Typical IIR filter characteristics for Fs = 800 Hz are shown in Figures 25, 26, 27, and 28. Figures 29 and 30 show group delay versus input frequency.

Table 29 Digital IIR Filter Characteristics—Transmit and Receive

Parameter	Symbol	Min	Typ	Max	Unit
Passband (3dB)	$F_{(3dB)}$	0		3.6	kHz
Passband ripple peak-to-peak		–0.2		0.2	dB
Stopband			4.4		kHz
Stopband attenuation		–40			dB
Group delay	t_{gd}		1.6/Fs		sec



Note: The remainder of the circuit is identical to the one shown in the Application Diagram.

Figure 20 Test Circuit For Loop Characteristics

Filter Plot Diagrams

For Figures 21, 22, 23, and 24, all filter plots apply to a sample rate of Fs = 8 kHz. The filters scale with the sample rate as follows:

$F_{(0.1\ dB)} = 0.4125\ Fs$

$F_{(-3\ dB)} = 0.45\ Fs$

where Fs is the sample frequency.

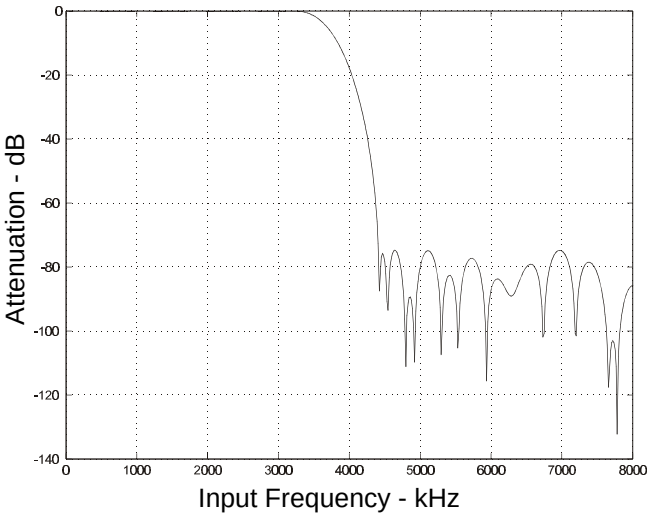


Figure 21 FIR Receive Filter Response

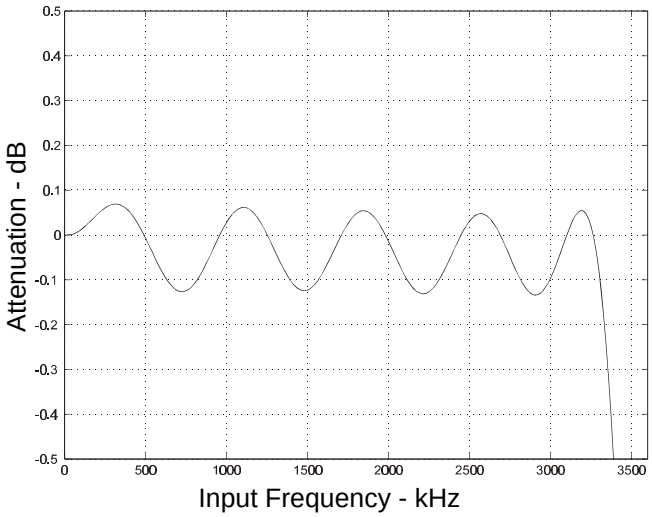


Figure 22 FIR Receive Filter Passband Ripple

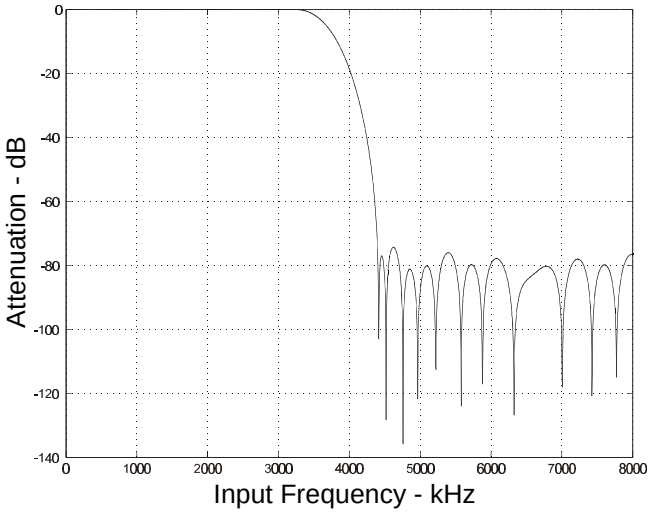


Figure 23 FIR Transmit Filter Response

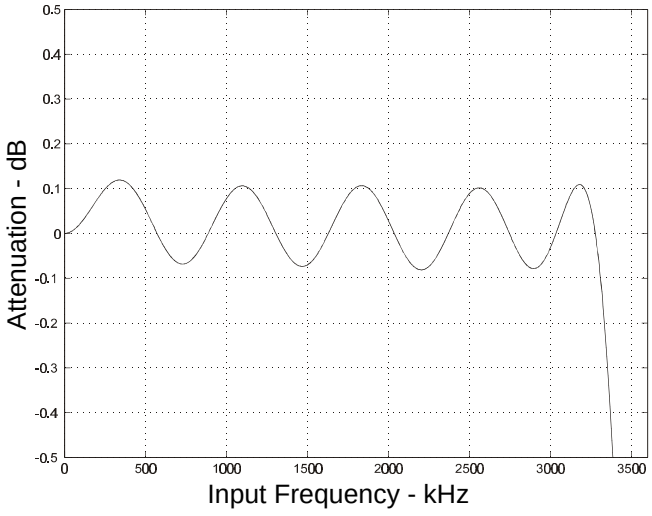


Figure 24 FIR Transmit Filter Passband Ripple

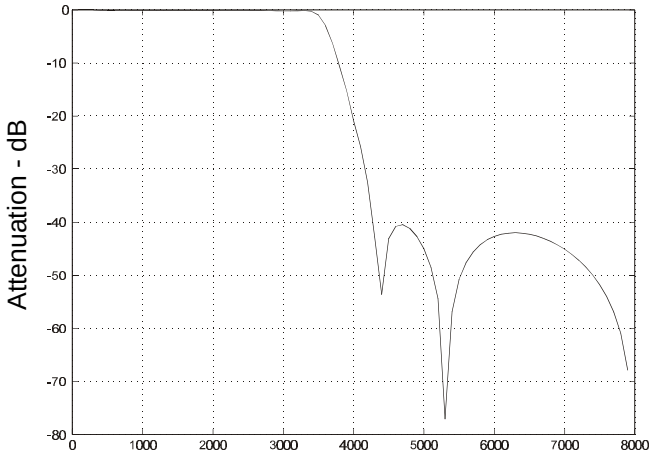


Figure 25 IIR Receive Filter Response

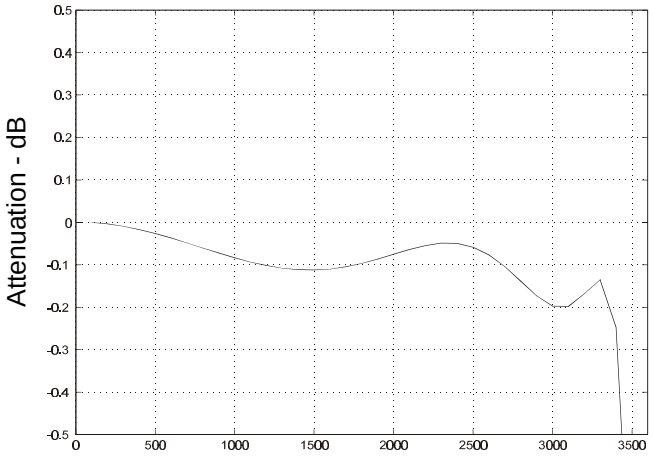


Figure 26 IIR Receive Filter Passband Ripple

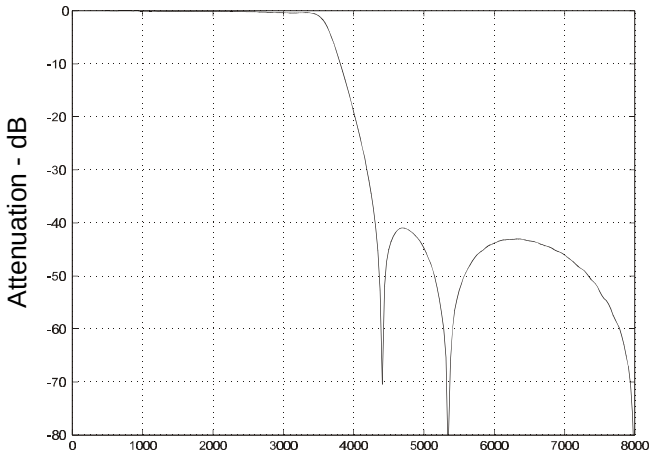


Figure 27 IIR Transmit Filter Response

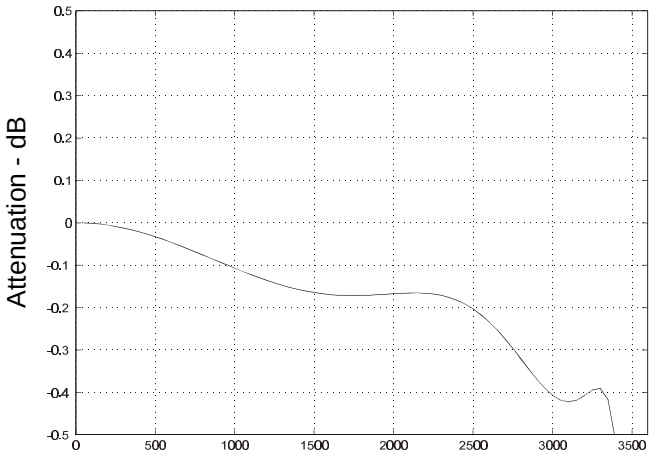


Figure 28 IIR Transmit Filter Passband Ripple

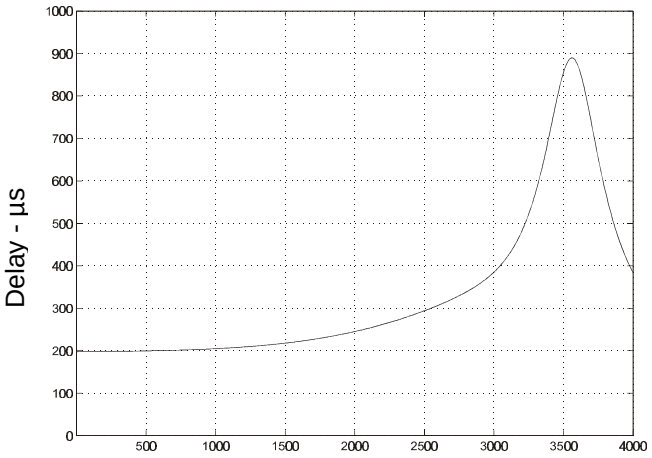


Figure 29 IIR Receive Group Delay

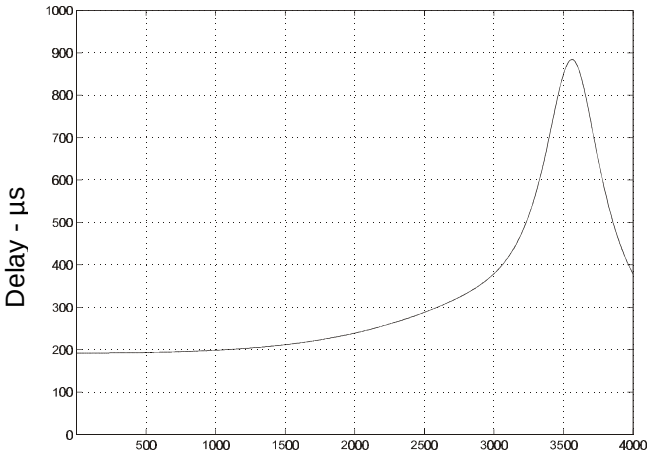


Figure 30 IIR Transmit Group Delay

MECHANICAL DIMENSIONS

PCT789T-A Mechanical Dimensions

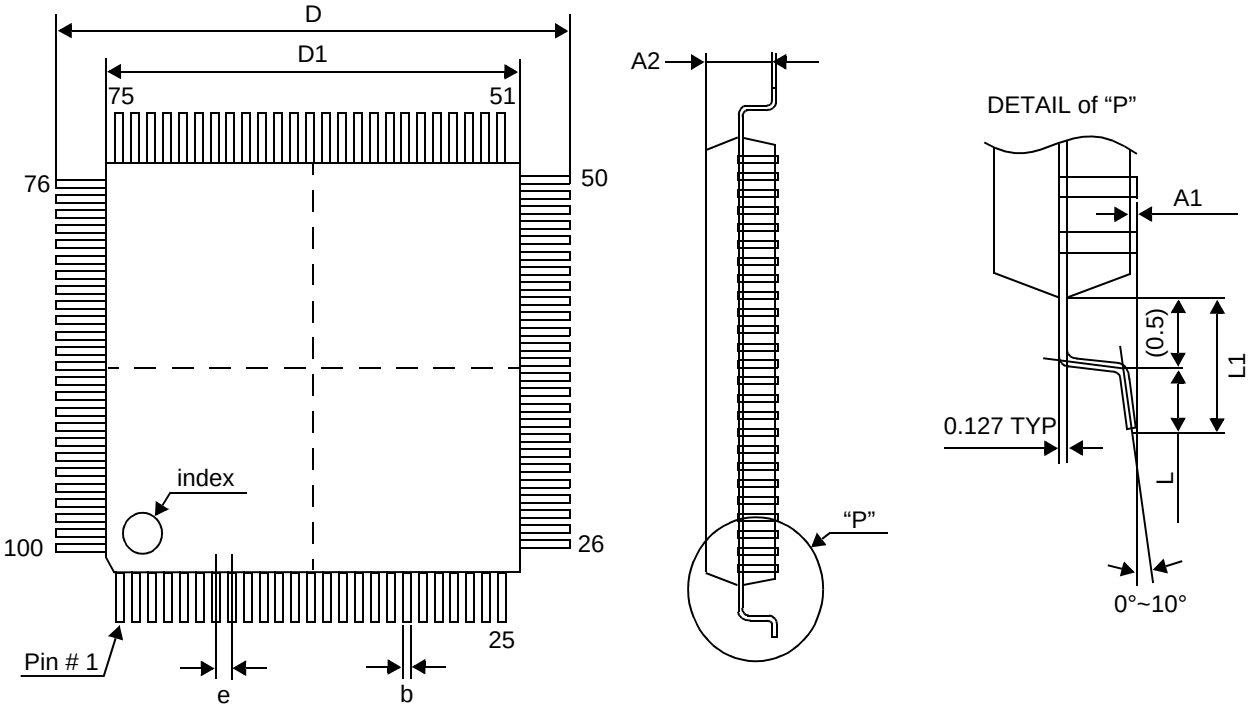


Figure 31 100-Pin TQFP Package

Table 30 TQFP Mechanical Dimensions

Symbol	Description	Millimeters		
		Min	Nom	Max
D	Lead to lead, X-/Y-axis	15.60	16.00	16.40
D1	Package's outside, X-/Y-axis	13.90	14.00	14.10
A1	Board standoff	-	0.10	-
A2	Package thickness	-	1.41	1.70
b	Lead width	-	0.18	-
e	Lead pitch	-	0.50	-
L	Foot length	0.30	0.50	0.70
L1	Lead length	-	1.00	-
-	Foot angle	0°		10°
-	Coplanarity	-	-	0.102
-	Leads in X-axis	-	25	-
-	Leads in Y-axis	-	25	-
-	Total leads	-	100	-
-	Package type	-	TQFP	-

PCT303DW Mechanical Dimensions

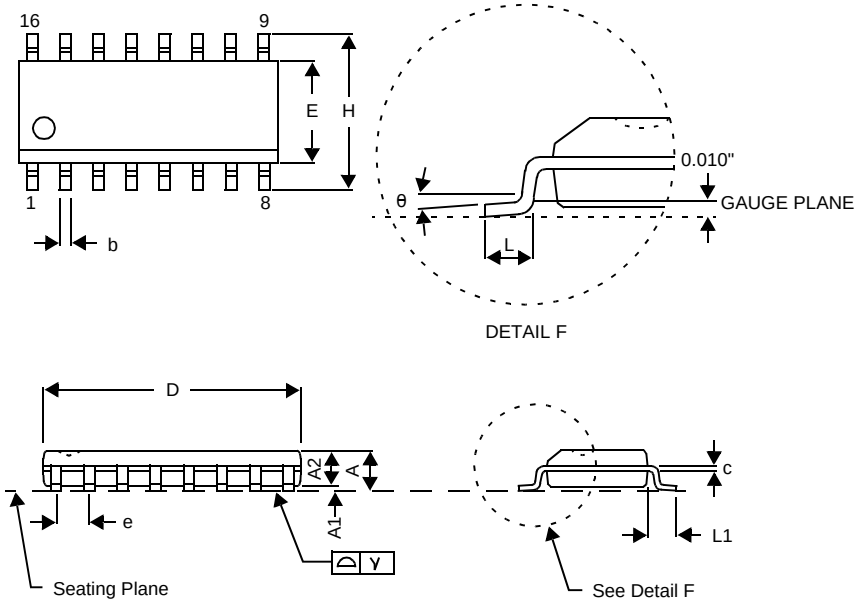


Figure 32 16-pin SOIC Package

Table 31 SOIC Mechanical Dimensions
(Controlling dimension: millimeters)

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.30	1.50	0.051	0.059
b	0.330	0.51	0.013	0.020
c	0.19	0.25	0.007	0.010
D	9.80	10.01	0.386	0.394
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
L1	1.07 BSC		0.042 BSC	
g		0.10		0.004
q	0°	8°	0°	8°

APPENDIX: NET4 COUNTRY SUPPORT

Introduction

The international design for the PCT303DW can be implemented to support global requirements targeting compliance with CTR21 or compliance with NET4. This appendix outlines the component changes and control registers required for NET4 support. NET4 support requires different DC termination (mode 0) and programmable ringer impedance and ringer threshold in order to meet country-specific requirements. Some component changes (vs. CTR21 only support) are necessary and are outlined in the notes of Table 32 on page 67.

Mode 0

Mode 0 (0,0) is a low-voltage mode which supports a maximum transmit signal of –5.22 dBm. This mode meets the very low voltage requirements for countries such as Norway. See Figure 33.

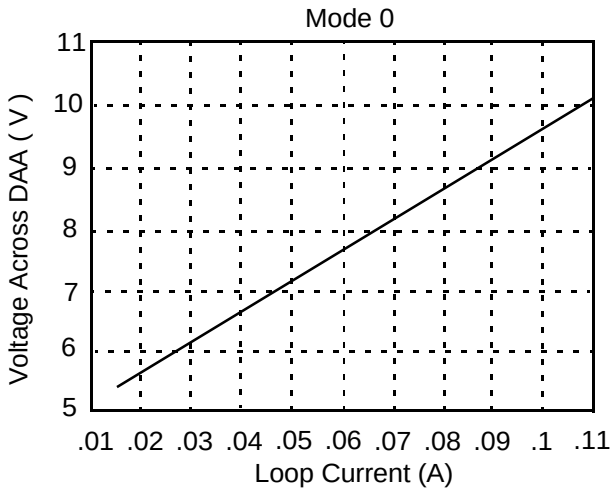


Figure 33 Mode 0 I/V Characteristics (0,0)

Ringer Impedance

The PCT303DW has a very high impedance ring detector that satisfies the requirements of most countries. In order to meet the maximum impedances of Germany (20 kΩ) and South Africa (60 kΩ), while not violating the minimum 20 kΩ requirement of Austria, a selectable ringer impedance has been included. The default (mode 0) is 24 kΩ and satisfies most countries. Mode 1 selects a 16 kΩ impedance, primarily to support Germany. The mode is selected by the RZ bit of register 16.

Ringer Threshold

The PCT303DW has a programmable ringer threshold. Mode 1 sets a ring threshold of 21.5 ± 5 Vrms. The mode is selected by bit 0 (RT) of register 16. Most countries will be programmed as mode 1 except Switzerland, Austria, and Belgium which require mode 0. Many countries can operate in either mode, such as those complying to FCC regulations.

Typical Application (NET4 Specifications)

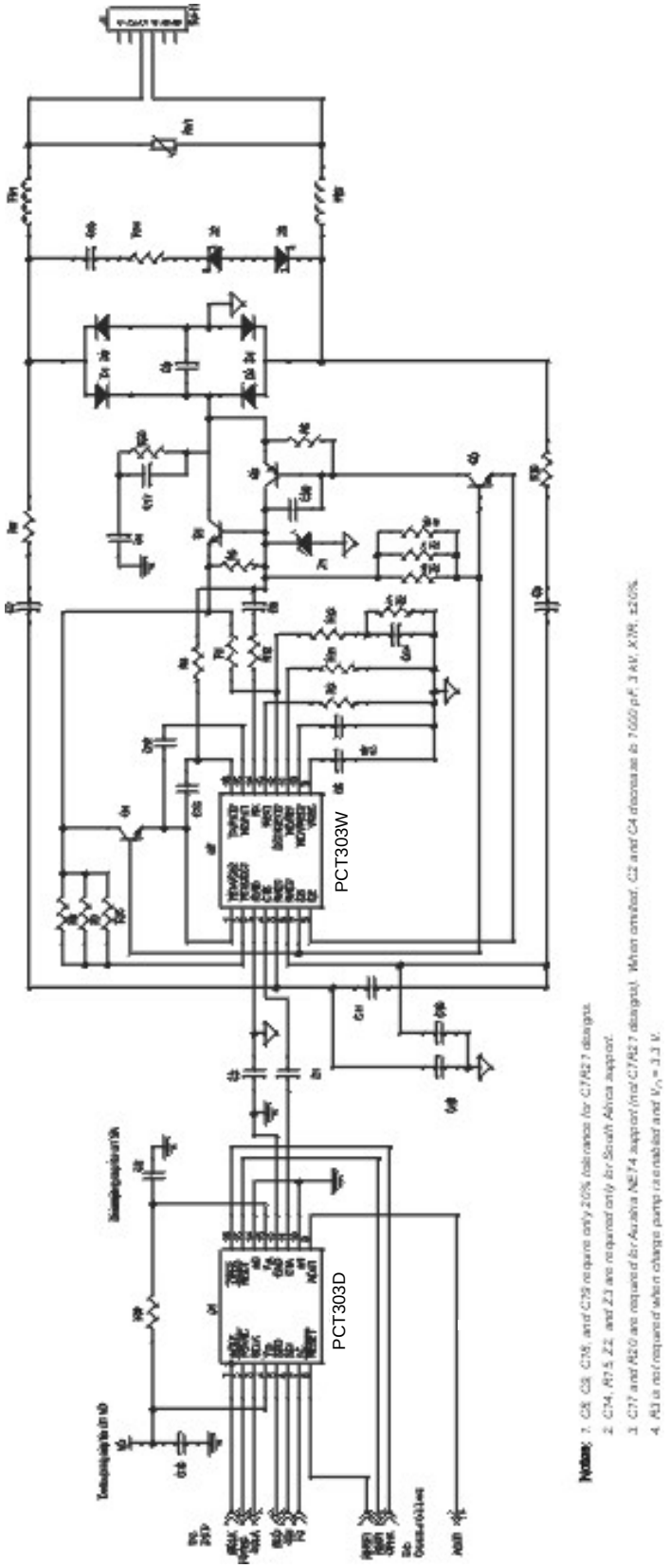


Figure 34 Typical Applications Circuit (NET4 Specifications)

Typical Application Component Values

Table 32 Component Values (NET4 Specifications)

Symbol	North American Value	International Value
C1	150pF, 2kV, X7R,±20%	150pF, 3kV, X7R, ±20%
C2,C4	1000pF, 2kV, X7R, ±20%	2200pF, 3kV, X7R, ±20%
C3,C10	0.1µF, 16V, X7R, ±20%	Same as North American
C5	0.47µF, 16V, X7R, ±20%	0.1µF, 50V, X7R, ±20%
C6	0.047µF, 16V, X7R, ±20%	0.1µF, 16V, X7R, ±20%
C7	2200pF, 250V, X7R, ±20%	680pF, 250V, X7R, ±20%
C8 [a]	2200pF, 250V, X7R, ±20%	680pF, 250V, X7R, ±10%
C9 [a]	15nF, 250V, X7R, ±20%	22nF, 250V, X7R, ±10%
C11	5600pF, 16V, X7R, ±20%	Not Installed
C12	Not Installed	0.22µF, 16V, X7R, ±20%
C13,C16	Not Installed	0.1µF, 16V, X7R, ±20%
C14	Not Installed	560nF,16V, X7R, ±20%
C15 [b]	Not Installed	0.47µF, 250V, ±20%
C17 [c]	Not Installed	Not Installed
C18,C19 [a]	Not Installed	3900pF,16V, X7R, ±10%
C20	Not Installed	47pF, 250V, X7R, ±20%
R1	51Ω, 1/2W ±5%	Not Installed
R2	15Ω, 1/4W ±5%	402Ω, 1/10W ±1%
R3 [d]	10Ω, 1/10W, ±5%	Same as North American
R4	604Ω, 1/4W, ±1%	Not Installed
R5	36kΩ, 1/10W ±5%	Same as North American
R6	36kΩ, 1/10W ±5%	121kΩ, 1/10W ±5%
R7,R8,R15,R16,R17,R19	Not Installed	4.87kΩ, 1/4W ±1%
R9,R10	10kΩ, 1/4W ±5%	30kΩ, 1/4W ±5%
R11	Not Installed	10kΩ, 1/10W ±1%
R12	Not Installed	140Ω, 1/10W ±1%
R13	Not Installed	442Ω, 1/10W ±1%
R14 [b]	Not Installed	18.7kΩ, 1/4W ±1%
R18	0Ω	2.2kΩ, 1/10W ±5%
R20 [c]	0Ω	0Ω
Z1	Zener Diode, 18V	Not Installed
Z2,Z3 [c]	Not Installed	Zener Diode, 3V
Q1,Q3	Motorola MMBTA42LT1	Same as North American
Q2	Motorola MMBTA92LT1	Same as North American
Q4	Not Installed	Motorola PZT2222AT1, 1/2W

Table 32 Component Values (NET4 Specifications) (Continued)

Symbol	North American Value	International Value
D1–D4	1N4004	Same as North American
FB1,FB2	Ferrite Bead	Same as North American
RV1	Sidactor 275V, 100A	Same as North American

a. C8, C9, C18, and C19 require only 20% tolerance for CTR21 designs.
b. C14, R15, Z2, and Z3 required only for South Africa support.
c. C17 and R20 required for Austria Net 4 support (not CTR21 designs). When omitted, C2 and C4 decrease to 1000 pF, 3kV, X7R, ±20%.
d. R3 not required when charge pump is enabled and V_D = 3.3 V.

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http://www.pctel.com

NET4 Line Interface Configurations

Table 33 NET4 Country Line Interface Configurations (Register 16)

Country	AC Termination	DC Termination		Ringer Impedance	Ringer Threshold
	Bit 5	Bit 4	Bit 3	Bit 2	Bit 0
1. FCC	0	1	0	0	0
2. Australia	1	0	1	0	0
3. Austria [a]	0	1	0	0	1
4. Belgium [a]	0	1	0	0	1
5. Denmark [a]	1	1	1	0	0
6. Finland [a]	0	1	0	0	0
7. France [a]	0	1	1	0	0
8. Germany [a]	1	1	0	1	0
9. Greece [a]	1	1	1	0	0
10. Hungary [a]	1	1	1	0	0
11. Iceland [a]	1	1	1	0	0
12. Ireland [a]	1	1	0	0	0
13. Italy [a]	0	0	1	0	0
14. Japan	0	0	1	0	0
15. Liechtenstein [a]	1	1	1	0	0
16. Luxembourg [a]	1	1	1	0	0
17. Netherlands [a]	1	1	1	0	0
18. New Zealand	1	1	0	0	0
19. Norway [a]	1	0	0	0	0
20. Portugal [a]	0	1	0	0	0
21. Singapore [b]	0	0	1	0	0
22. South Africa	1	1	0	0	0
23. Spain [a]	0	1	0	0	0
24. Sweden [a]	1	1	1	0	0
25. Switzerland [a]	1	0	1	0	1
26. CTR21	1	1	1	0	0
27. UK [a]	1	1	0	0	1

a. These countries are now accepting CTR21.
b. Support for loop currents greater than or equal to 20 mA.

PATENTS

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