LOW POWER, DUAL SIM CARD HYBRID SWITCH

IDTHS421V16

Description

The IDTHS421V16 is a bi-directional, low power, Quad single-pole, double-throw (SPDT) hybrid switch targeted at dual SIM card multiplexing. It is optimized for switching the WLAN-SIM data and control signals and dedicates one channel as a supply-source switch.

This device is compatible with the requirements of SIM cards and features a low on capacitance (C_{ON}) of 10 pF to ensure high-speed data transfer. The V_{SIM} switch path has a low R_{ON} characteristic to insure minimal voltage drop in the dual SIM card supply paths.

The IDTHS421P16 contains special circuitry that minimizes current consumption when the control voltage applied to the SEL pin is lower than the supply voltage (VCC). This feature is especially valuable in ultra-portable applications, such as cell phones; allowing direct interface with the general purpose I/Os of the baseband processor. Other applications include switching and connector sharing in portable cell phones, PDAs, digital cameras, printers, and notebook computers.

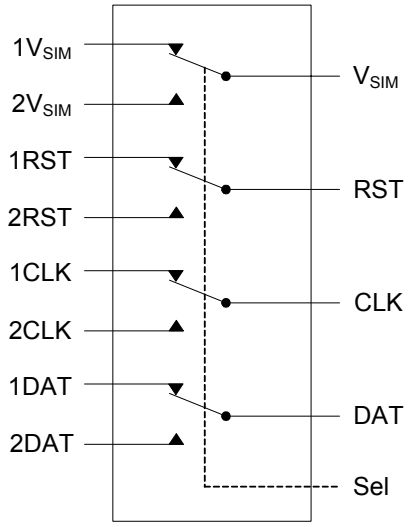
Features

- Low On Capacitance for data path: 10 pF typical
- Low On Resistance for data path: 10Ω typical
- Low On Resistance for supply path: 0.4Ω typical
- Low power consumption: 1 µA maximum
  - 15 µA maximum I_{CCT} over expanded voltage range (V_{IN} = 1.8 V, VCC = 4.3 V)
- Wide -3dB bandwidth: >160 MHz
- Available in 16-pin QFN package – RoHS compliant
- 8 kV ESD rating, >16kV power/ground ESD rating

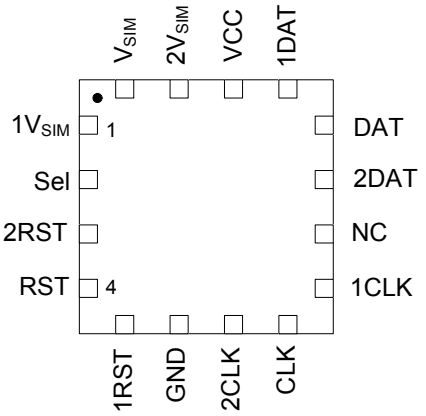
Applications

- Cell phones, PDAs, Digital cameras, and Notebooks
- LCD monitors, TV, and Set-top boxes

Analog Symbol



Pin Assignment (16-pin QFN)



16-pin QFN

Truth Table

Sel	Function
Logic LOW	1DAT=DAT, 1RST=RST, 1CLK=CLK, $1V_{SIM}=V_{SIM}$
Logic HIGH	2DAT=DAT, 2RST=RST, 2CLK=CLK, $2V_{SIM}=V_{SIM}$

Pin Descriptions

Pin Name	Pin Description
nDAT, nRST, nCLK	Multiplexed data source inputs.
nV_{SIM}	Multiplexed SIM supply inputs.
V_{SIM}, DAT, RST, CLK	Common SIM ports.
Sel	Switch select.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the IDTHS421P16. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Symbol	Parameter		Min.	Max.	Units
VCC	Supply Voltage		-0.5	+5.5	V
V_{CNTRL}	DC Input Voltage, Sel (note 1)		-0.5	VCC	V
V_{SW}	DC Switch I/O Voltage (note 1)		-0.5	VCC+0.3	V
I_{IK}	DC Input Diode Current		-50		mA
I_{SIM}	DC Output Current, V_{SIM}			350	mA
I_{OUT}	DC Output Current, DAT, CLK, RST			35	mA
T_{STG}	Storage Temperature		-65	+150	°C
ESD	Human Body Model, JEDEC: JESD22-A114	All pins		8	kV
		I/O to GND		8	
	Charged Device Model, JEDEC: JESD22-C101			2	

Note 1 : The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

Recommended Operation Conditions

Symbol	Parameter	Min.	Max.	Units
VCC	Supply Voltage	2.7	4.3	V
V_{CNTRL}	Control Input Voltage, Sel (note 2)	0	VCC	V
V_{SW}	Switch I/O Voltage	-0.5	VCC	V
I_{SIM}	DC Output Current, V_{SIM}		150	mA
I_{OUT}	DC Output Current, DAT, CLK, RST		25	mA
T_A	Operating Temperature	-40	+85	°C

Note 2 : The control pin must be held HIGH or LOW; it must not float.

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		69.4		°C/W
	θ_{JA}	1 m/s air flow		60.7		°C/W
	θ_{JA}	2.5 m/s air flow		54.4		°C/W
Thermal Resistance Junction to Case	θ_{JC}			9.7		°C/W

DC Electrical Characteristics

Unless stated otherwise, **VCC = 3.3 V @ 25°C**

Parameter	Symbol	Conditions	VCC (V)	T_A = -40°C to +85°C			Units
				Min.	Typ.	Max.	
Clamp Diode Voltage	V_{IK}	I_{IN} = 18 mA	2.7			-1.2	V
Input Voltage High	V_{IH}		2.7 to 3.6	1.3			V
			4.3	1.7			
Input Voltage Low	V_{IL}		2.7 to 3.6			0.5	V
			4.3			0.7	
Control Input Leakage	I_{IN}	V_{SW} = 0 to VCC	4.3	-1		1	µA
OFF State Leakage	$I_{nc(OFF)}$, $I_{no(OFF)}$	nRST, nDAT, nCLK, nV_{SIM} = 0.3 V or 3.6 V (Fig. 2)	4.3	-60		60	nA
Data Path Switch On Resistance (note 3)	R_{OND}	V_{SW} = 0, 2.3 V, I_{ON} = -20 mA (Fig. 1)	2.7		6.0	10.0	Ω
V_{SIM} Switch On Resistance (note 3)	R_{ONV}	V_{SW} = 0, 2.3 V, I_{ON} = -100 mA (Fig. 1)	2.7		0.4	0.6	Ω
Data Path Delta On Resistance (note 4)	$\triangle R_{OND}$	V_{SW} = 0V, I_{ON} = -20 mA	2.7		0.65		Ω
Quiescent Supply Current	I_{CC}	V_{CNTRL} = 0 or VCC, I_{OUT} = 0	4.3			1.0	µA
Increase in I_{CC} Current per Control Voltage and VCC	I_{CCT}	V_{CNTRL} = 2.6 V, VCC = 4.3 V	4.3			10.0	µA
		V_{CNTRL} = 1.8 V, VCC = 4.3 V	4.3			15.0	

Notes:

3. Measured by the voltage drop between nDAT, nRST, nCLK and relative common port pins at the indicated current through the switch. On resistance is determined by the lower of the voltage on the relative ports.

4. Guaranteed by characterization.

AC Electrical Characteristics

Unless stated otherwise, **VCC = 3.3 V @ 25°C**

Parameter	Symbol	Conditions	VCC (V)	T_A = -40°C to +85°C			Units
				Min.	Typ.	Max.	
Turn-on Time Sel to Output (DAT, CLK, RST)	t_{OND}	R_L = 50Ω, C_L = 35 pF, V_{SW} = 1.5 V (Fig. 3, Fig. 4)	2.7 to 3.6			60	ns
Turn-off Time Sel to Output (DAT, CLK, RST)	t_{OFFD}	R_L = 50Ω, C_L = 35 pF, V_{SW} = 1.5 V (Fig. 3, Fig. 4)	2.7 to 3.6			40	ns
Turn-on Time Sel to Output (V_{SIM})	t_{ONV}	R_L = 50Ω, C_L = 35 pF, V_{SW} = 1.5 V (Fig. 3, Fig. 4)	2.7 to 3.6			50	ns
Turn-off Time Sel to Output (V_{SIM})	t_{OFFV}	R_L = 50Ω, C_L = 35 pF, V_{SW} = 1.5 V (Fig. 3, Fig. 4)	2.7 to 3.6			40	ns
Propagation Delay (DAT, CLK, RST)	t_{PD}	R_L = 50Ω, C_L = 35 pF, (Fig. 3, Fig. 5), Note 5	3.3		0.25		ns
Break-Before-Make (V_{SIM})	t_{BBMV}	R_L = 50Ω, C_L = 35 pF, V_{SW1} = V_{SW2} = 1.5 V (Fig. 7), Note 5	2.7 to 3.6	3	12		ns
Break-Before-Make (DAT, CLK, RST)	t_{BBMD}	R_L = 50Ω, C_L = 35 pF, V_{SW1} = V_{SW2} = 1.5 V (Fig. 7), Note 5	2.7 to 3.6	3	18		ns
Charge Injection (DAT, CLK, RST)	Q	R_{GEN} = 0Ω, C_L = 50 pF, V_{GEN} = 0V	2.7 to 3.6		10		pC
Off Isolation (DAT, CLK, RST)	O_{IRR}	R_L = 50Ω, f = 10 MHz (Fig. 9)	2.7 to 3.6		-80		dB
Non-Adjacent Channel Crosstalk (DAT, CLK, RST)	Xtalk	R_L = 50Ω, f = 10 MHz (Fig. 10)	2.7 to 3.6		-80		dB
-3 dB Bandwidth (DAT, CLK, RST)	BW	R_L = 50Ω, C_L = 5 pF (Fig. 8)	2.7 to 3.6		>160		MHz

Note:

5. Guaranteed by characterization.

Capacitance

Parameter	Symbol	Conditions	T_A = -40°C to +85°C			Units
			Min.	Typ.	Max.	
Control Pin Input Capacitance	C_{IN}	VCC = 0V		1.5		pF
RST, CLK, DAT On Capacitance	C_{OND}	VCC = 3.3 V, f = 1 MHz (Fig. 12)		10	12	
V_{SIM} On Capacitance	C_{ONV}	VCC = 3.3 V, f = 1 MHz (Fig. 12)		130	150	
RST, CLK, DAT Off Capacitance	C_{OFFD}	VCC = 3.3 V(Fig. 11)		3		
V_{SIM} Off Capacitance	C_{OFFV}	VCC = 3.3 V(Fig. 11)		40		

Test Diagrams

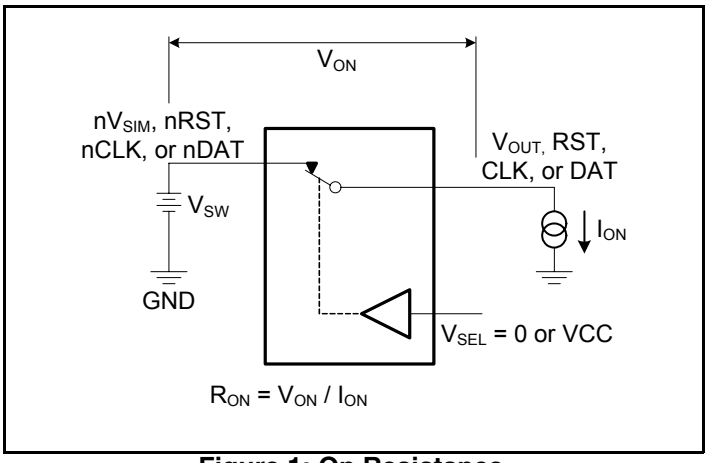


Figure 1: On Resistance

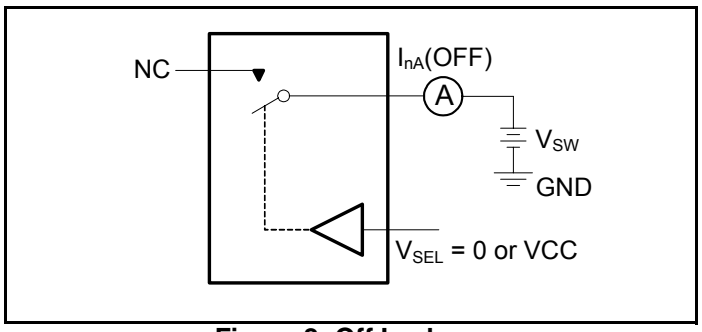


Figure 2: Off Leakage

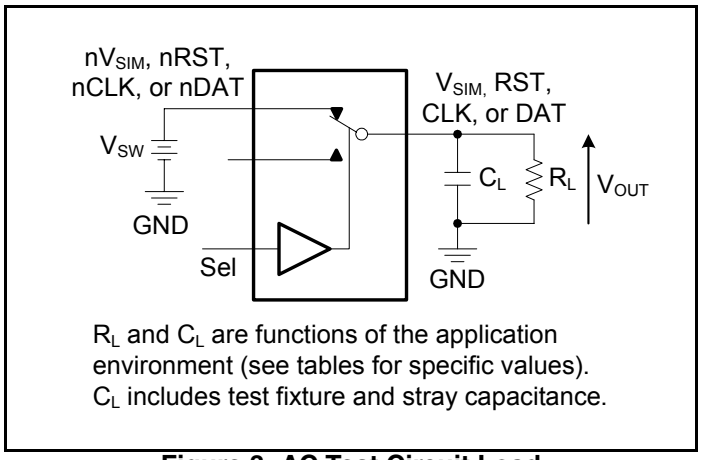


Figure 3: AC Test Circuit Load

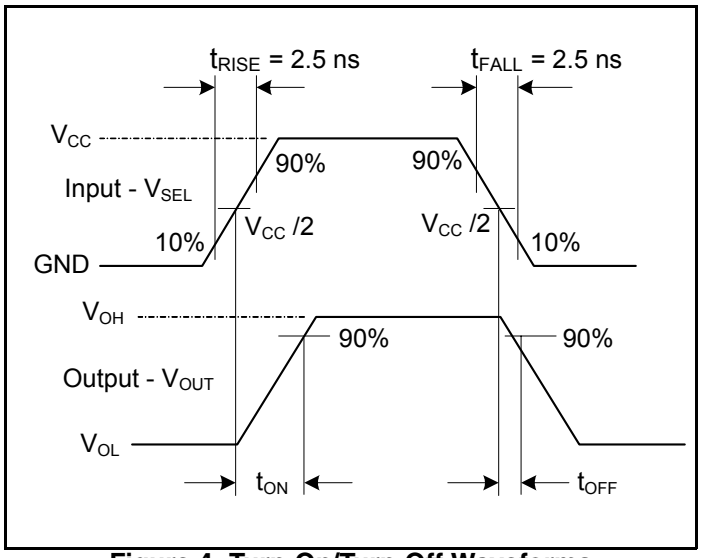


Figure 4: Turn-On/Turn-Off Waveforms

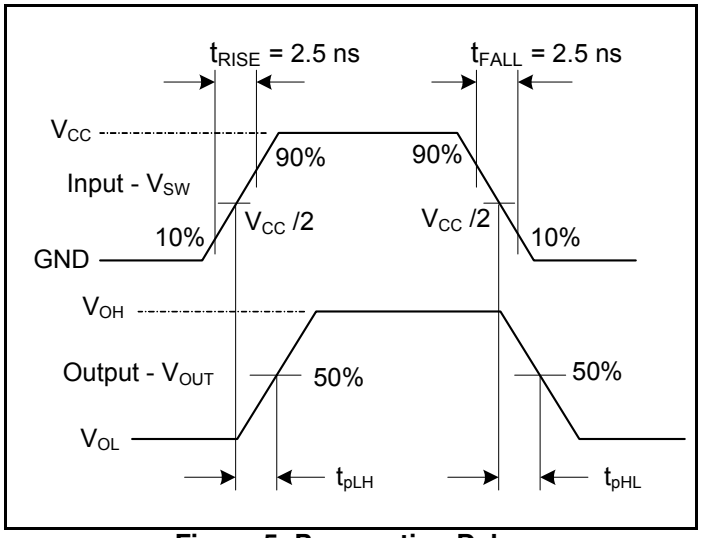


Figure 5: Propagation Delay

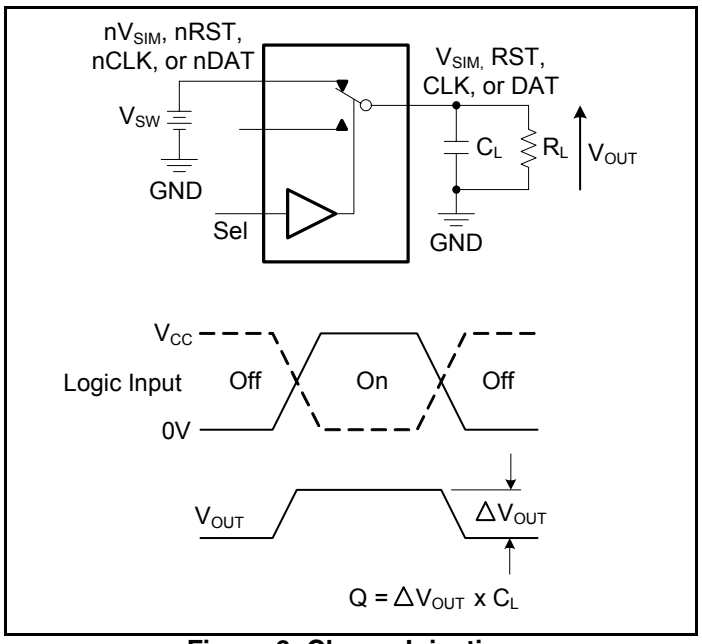


Figure 6: Charge Injection

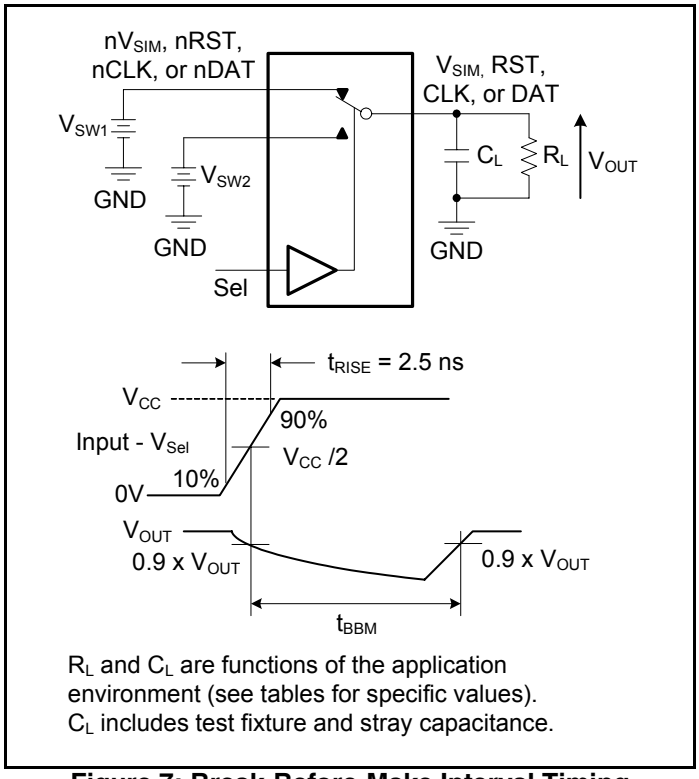


Figure 7: Break-Before-Make Interval Timing

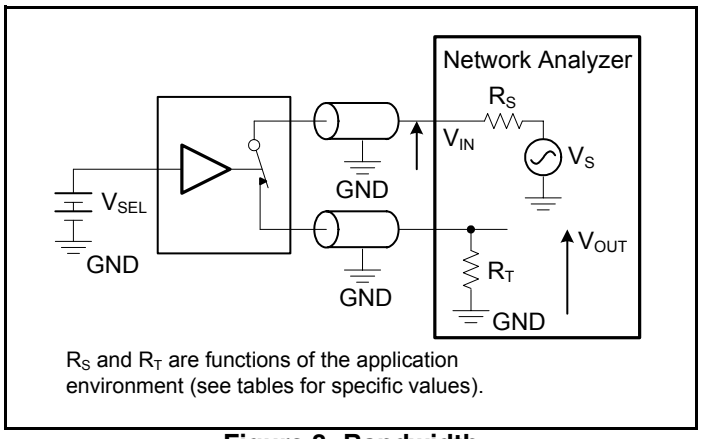


Figure 8: Bandwidth

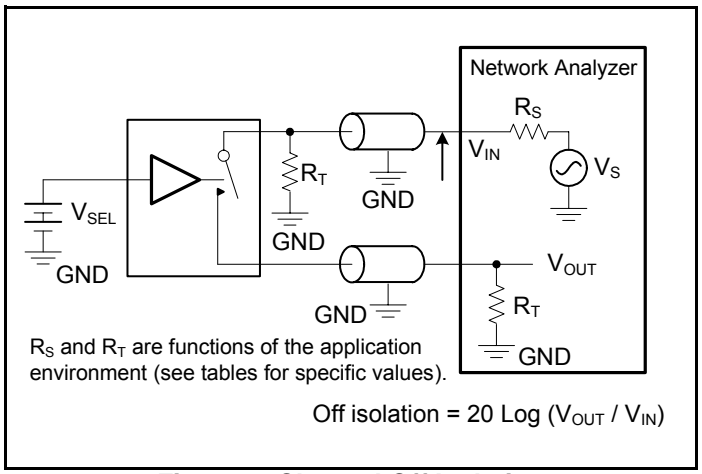


Figure 9: Channel Off Isolation

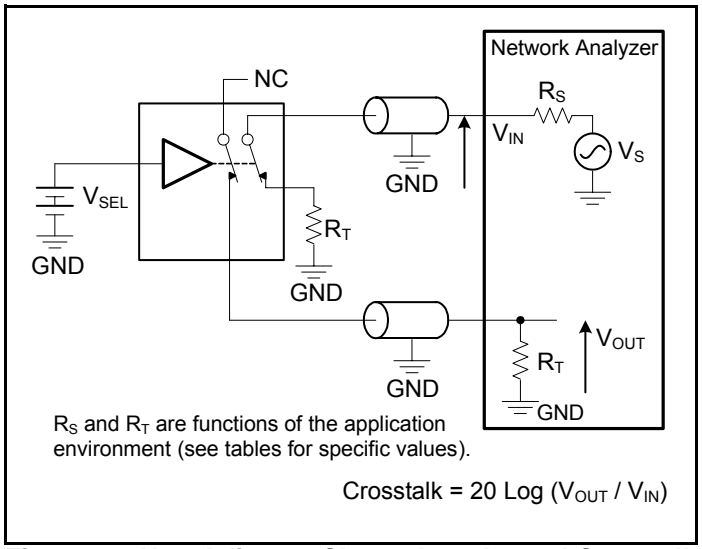


Figure 10: Non-Adjacent Channel-to-channel Crosstalk

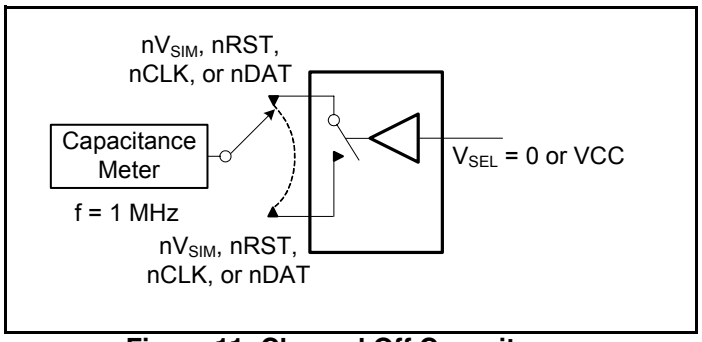


Figure 11: Channel Off Capacitance

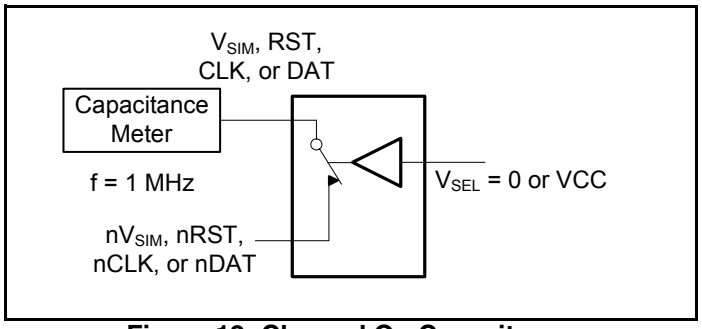
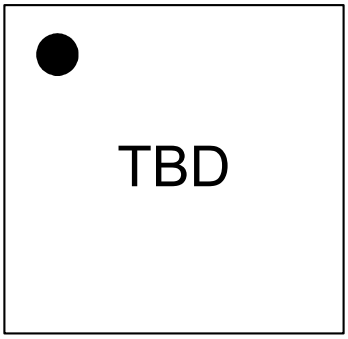


Figure 12: Channel On Capacitance

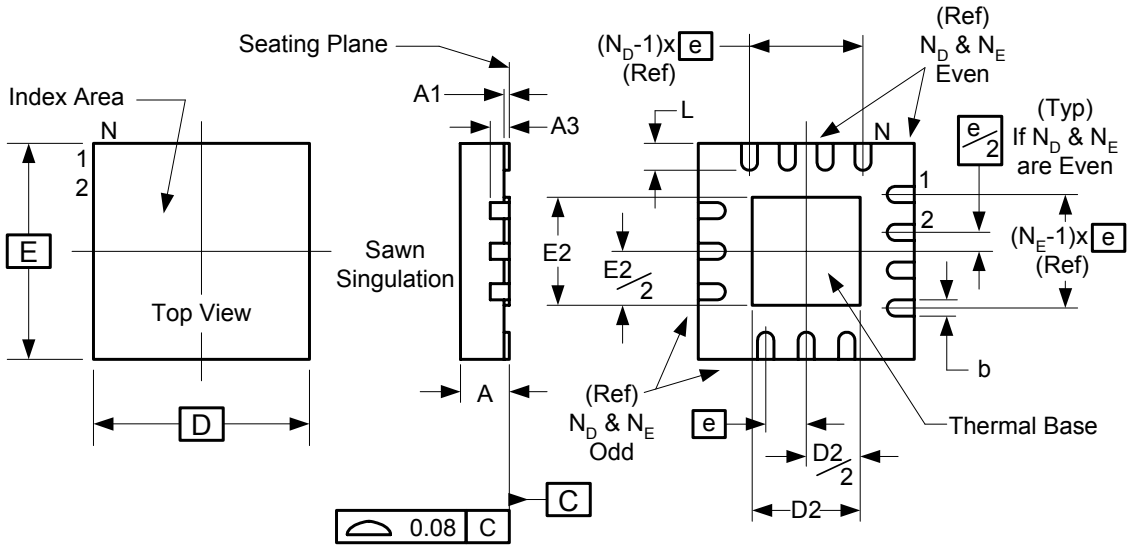
Marking Diagram (QFN)



Notes:
1. “Z” is the device step (1 to 2 characters).
2. YYWW is the last two digits of the year and week that the part was assembled.
3. “$” is the assembly mark code.
4. “G” after the two-letter package code designates RoHS compliant package.
5. “I” at the end of part number indicates industrial temperature range.
6. Bottom marking: country of origin if not USA.

Package Outline and Package Dimensions (16-pin 3x3mm QFN)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters	
Symbol	**Min**	**Max**
A	0.80	1.00
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 BASIC	
N	16	
N_D	4	
N_E	4	
D x E BASIC	3.00 x 3.00	
D2	1.55	1.80
E2	1.55	1.80
L	0.30	0.50

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
IDTHS421V16NLGI	TBD	Tubes	16-pin QFN	-40 to +85° C
IDTHS421V16NLGI8		Tape and Reel	16-pin QFN	-40 to +85° C

Parts that are ordered with a "G" after the two-letter package code are the Pb-Free configuration and are RoHS compliant.

Revision History

Rev.	Originator	Date	Description of Change
A	JS	01/15/08	Preliminary datasheet. Initial release.
B	JS	02/12/08	Change the part number to IDTHS421V16.

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