

To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.)

Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

Description

Description

The M30221 group of single-chip microcomputers are built using the high-performance silicon gate CMOS process using a M16C/60 Series CPU core. The M30221 group has LCD controller/driver. M30221 group is packaged in a 120-pin plastic molded QFP. These single-chip microcomputers operate using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, they are capable of executing instructions at high speed.

Features

- Basic machine instructions Compatible with the M16C/60 series
- Memory capacity See Figure 1.1.3 Memory Expansion
- Shortest instruction execution time 100ns ($f(X_{IN})=10\text{MHz}$)
- Supply voltage 4.0 to 5.5V ($f(X_{IN})=10\text{MHz}$)
2.7 to 5.5V ($f(X_{IN})=7\text{MHz}$ with software one-wait)
- Interrupts 24 internal and 8 external interrupt sources, 4 software interrupt sources; 7 levels(including key input interrupt)
- Multifunction 16-bit timer Timer A (output) x 8, timer B (input) x 6
- Real time port outputs 8 bits X 3 lines, 6 bits X 1 lines
- Serial I/O 2 channels for UART or clock synchronous
- DMAC 2 channels (trigger: 24 sources)
- A-D converter 10 bits X 7 channels
- D-A converter 8 bits X 2 channels
- Watchdog timer 1 line
- Programmable I/O 83 lines (26 lines are shared with LCD outputs)
- Output port 14 lines (14 lines are shared with LCD output)
- Input port 1 line (P77, shared with NMI pin)
- LCD drive control circuit 1/2, 1/3 bias
2, 3 and 4 duty
4 common outputs
40 segment outputs
built-in charge pump
- Key input interrupt 20 lines
- Clock generating circuit 2 built-in clock generation circuits
(built-in feedback resistor, and external ceramic or quartz oscillator)

Specifications written in this manual are believed to be accurate, but are not guaranteed to be entirely free of error.
Specifications in this manual may be changed for functional or performance improvements. Please make sure your manual is the latest edition.

Applications

Camera, Home appliances, Portable equipment, Audio, office equipment, etc.

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Description

Pin Configuration

Figures 1.1.1 show the pin configurations (top view).

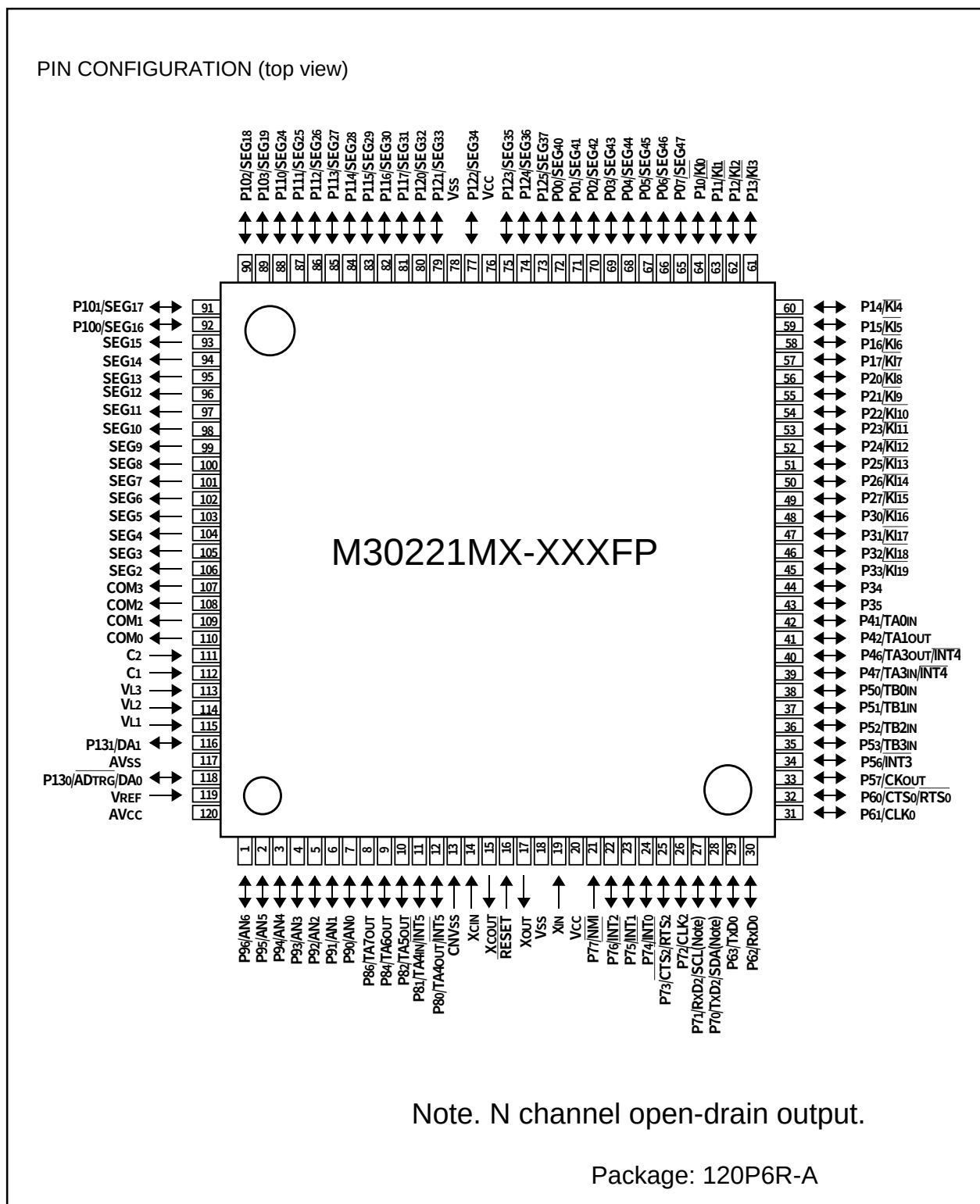


Figure 1.1.1. Pin configuration for the M30221 group (top view)

Block Diagram

Figure 1.1.2 is a block diagram of the M30221 group.

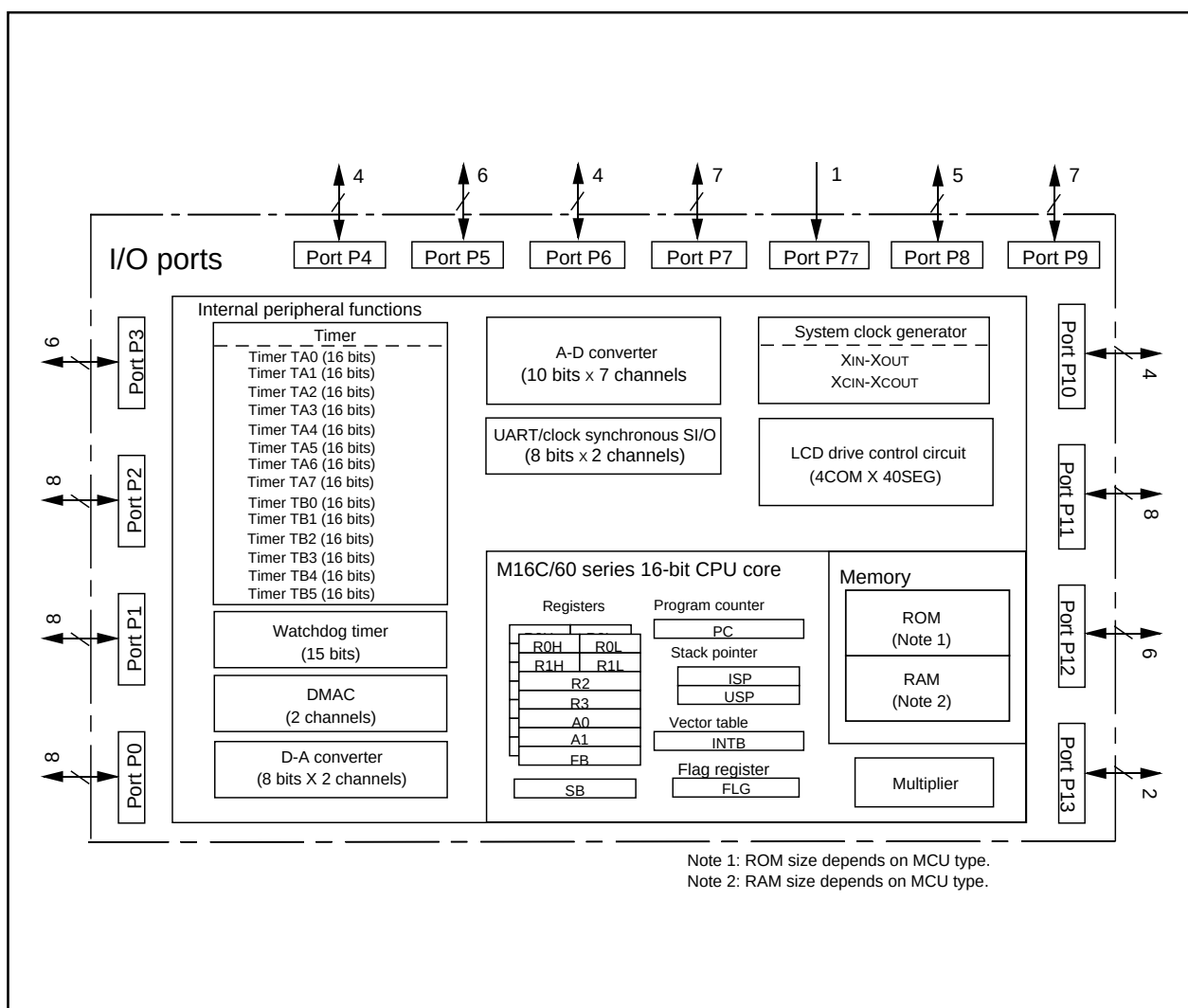


Figure 1.1.2. Block diagram of M30221 group

Description

Performance Outline

Table 1.1.1 is performance outline of M30221 group.

Table 1.1.1. Performance outline of M30221 group

Item			Performance
Number of basic instructions			91 instructions
Shortest instruction execution time			100ns (f(XIN)=10MHz
Memory capacity	ROM		24 Kbytes
	RAM		1.5 Kbytes
I/O port	P0 to P13 (except P77)		8 bits x 4, 2 bits x 1, 6 bits x 3, 7 bits x 2 5 bits x 1, 4 bits x 3
Input port	P77		1 bit x 1
Output port	SEG2 to SEG15		2 bits x 7
Multifunction timer	TA0 to TA7		16 bits x 8
	TB0 to TB5		16 bits x 6
Real time port outputs			8 bits x 3 lines,6 bits x 1 lines
Serial I/O	UART0 , UART2		(UART or clock synchronous) x 2
A-D converter			10 bits x 7 channels
D-A converter			8 bits x 2 channels
DMAC			2 channel(trigger:24 sources)
LCD	COM0 to COM3		4 lines
	SEG2 to SEG47		40 lines (26 lines are shared with I/O ports)
Watchdog timer			15 bits x 1 (with prescaler)
Interrupt			24 internal and 8 external sources, 4 software sources
Clock generating circuit			2 built-in clock generation circuits (built-in feedbackresistor, and external ceramic or quartz oscillator)
Supply voltage			4.0 to 5.5V (f(XIN)=10MHz)
			2.7 to 5.5V (f(XIN)=7MHz with software one-wait)
Power consumption			18 mW (Vcc=3.3V, f(XIN)=7MHz with software one-wait)
I/O char-acteristics	I/O withstand voltage (P0 to P13)		5 V
	Output current	P1 to P9,P13	5 mA
		P0, P10 to P12	0.1mA("H" output), 2.5mA("L" output)
Device configuration			CMOS silicon gate
Package			120-pin plastic mold QFP

Description

Mitsubishi plans to release the following products in the M30221 group:

- (1) Support for mask ROM version, flash memory version
- (2) Memory capacity
- (3) Package

120P6R-A : Plastic molded QFP (mask ROM and flash memory versions)

Figure 1.1.3 shows the memory expansion and figure 1.1.4 shows the Type No., memory size, and package.

April, 2001

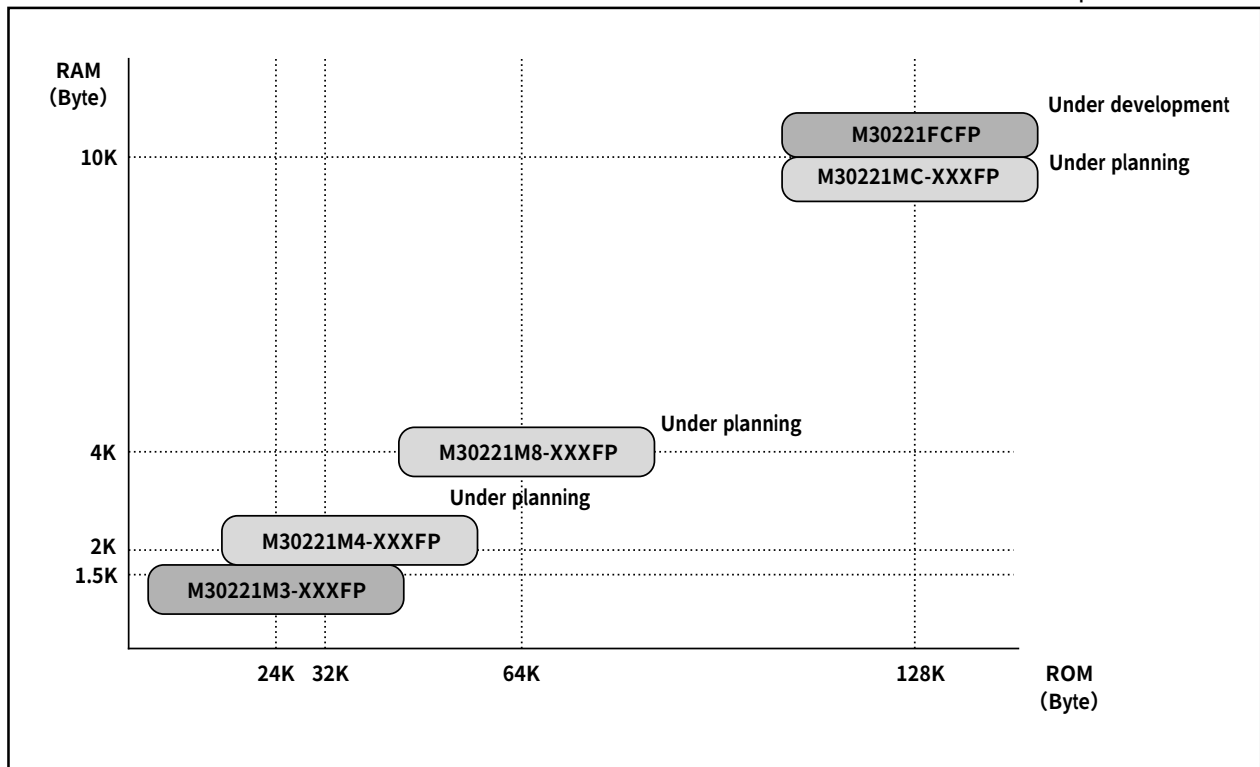


Figure 1.1.3. Memory expansion

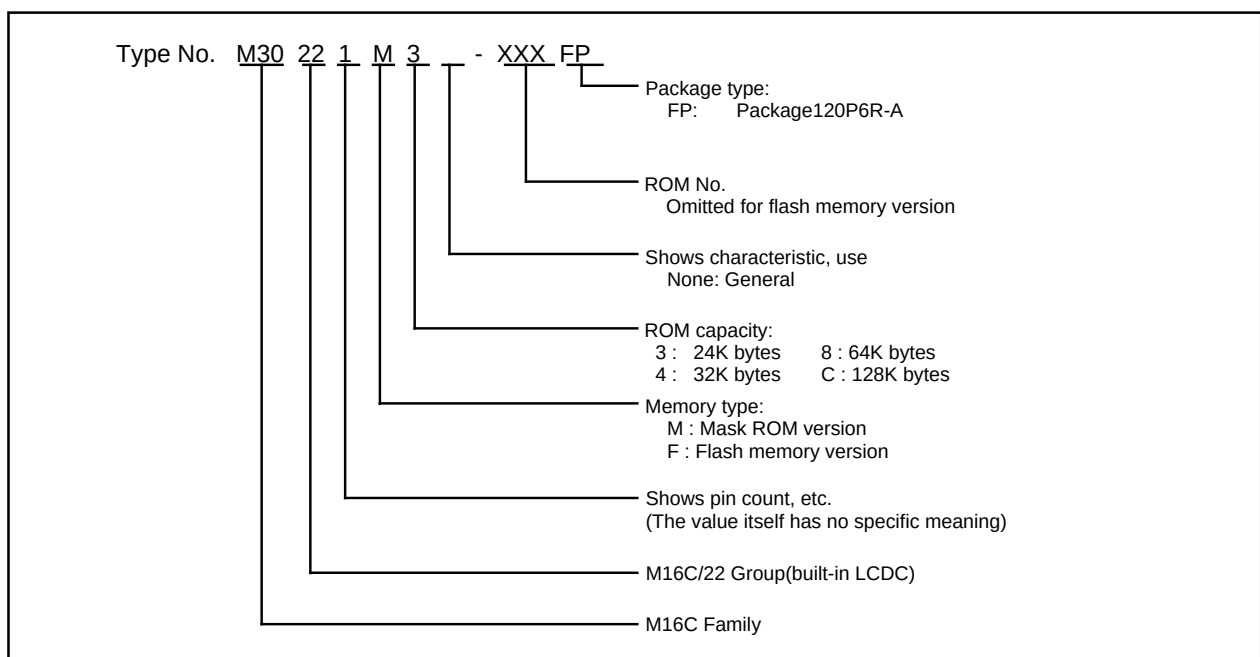


Figure 1.1.4. Type No., memory size, and package

Pin Description

Pin Description

Pin name	Signal name	I/O	Function
VCC, VSS	Power supply input		Supply 2.7 to 5.5 V to the VCC pin. Supply 0 V to the VSS pin.
CNVSS	CNVSS	I	Connect it to the VSS pin.
RESET	Reset input	I	A "L" on this input resets the microcomputer.
XIN XOUT	Clock input Clock output	I O	These pins are provided for the main clock generating circuit. Connect a ceramic resonator or crystal between the XIN and the XOUT pins. To use an externally derived clock, input it to the XIN pin and leave the XOUT open.
XCIN XCOUT	Clock input Clock output	I O	These pins are provided for the sub clock generating circuit. Connect a ceramic resonator or crystal between the XCIN and the XCOUT pins. To use an externally derived clock, input it to the XCIN pin and leave the XCOUT open.
AVCC	Analog power supply input		This pin is a power supply input for the A-D converter. Connect it to VCC.
AVSS	Analog power supply input		This pin is a power supply input for the A-D converter. Connect it to VSS.
VREF	Reference voltage input	I	This pin is a reference voltage input for the A-D converter.
P00 to P07	I/O port P0	I/O	This is an 8-bit CMOS I/O port. It has an input/output port direction register that allows the user to set each pin for input or output individually. When set for input, the user can specify in units of four bits via software whether or not they are tied to a pull-up resistor. Pins in this port also use as LCD segment output and real time port output.
P10 to P17	I/O port P1	I/O	This is an 8-bit I/O port equivalent to P0. Pins in this port also function as input pins for the key input interrupt function and real time port output.
P20 to P27	I/O port P2	I/O	This is an 8-bit I/O port equivalent to P0. Pins in this port also function as input pins for the key input interrupt function and real time port output.
P30 to P35	I/O port P3	I/O	This is a 6-bit I/O port equivalent to P0. P30 to P33 also function as input pins for the key input interrupt function.
P41, P42, P46, P47	I/O port P4	I/O	This is a 4-bit I/O port equivalent to P0. The P41 pin is shared with timer A0 input. The P42 pin is shared with timer A1 output. The P46 pin is shared with timer A3 output and INT4. The P47 pin is shared with timer A3 input and INT4.
P50 to P53, P56, P57	I/O port P5	I/O	This is a 6-bit I/O port equivalent to P0. The P50, P51, P52, and P53 pins are shared with timer B0, B1, B2, and B3 input, respectively. The P56 pin is shared with INT3. The P57 pin is shared with CKOUT output.
P60 to P63	I/O port P6	I/O	This is an 4-bit I/O port equivalent to P0. The P60 pin is shared with CTS0 and RTS0. The P61, P62, and P63 pins are shared with CLK0, RxD0, and TxD0, respectively.

Pin Description

Pin Description

Pin name	Signal name	I/O	Function
P70 to P76 P77	I/O port P7	I/O I	P70 to P76 are I/O ports equivalent to P0 (P70 and P71 are N channel open-drain output). The P70, P71, and P72 pins are shared with TxD2, RxD2, and CLK2, respectively. The P73 is shared with CTS2 and RTS2. The P74, P75 and P76 pins are shared with INT0, INT1 and INT2, respectively. P77 is an input-only port that also functions for $\overline{\text{NMI}}$.
P80 to P82, P84, P86	I/O port P8	I/O	This is a 5-bit I/O port equivalent to P0. The P80 pin is shared with timer A4 output and INT5 input. The P81 pin is shared with timer A4 input and INT5 input. The P82 pin is shared with timer A5 output. The P84 pin is shared with timer A6 output. The P86 pin is shared with timer A7 output.
P90 to P96	I/O port P9	I/O	This is an 7-bit I/O port equivalent to P0. Pins in this port also function as A-D converter input pins.
P100 to P103	I/O port P10	I/O	This is an 4-bit I/O port equivalent to P0. Pins in this port also function as SEG output for LCD.
P110 to P117	I/O port P11	I/O	This is an 8-bit I/O port equivalent to P0. Pins in this port also function as SEG output for LCD.
P120 to P125	I/O port P12	I/O	This is an 6-bit I/O port equivalent to P0. Pins in this port also function as SEG output for LCD and real time port output.
P130, P131	I/O port P13	I/O	This is an 2-bit I/O port equivalent to P0. P130 pins in this port also function as D-A converter output pins or start trigger for A-D input pins. P131 pins in this port also function as D-A converter output pins.
SEG2 to SEG15	Segment output	O	Pins in this port function as SEG output for LCD drive circuit.
COM0 to COM3	Common output	O	Pins in this port function as common output for LCD drive circuit.
VL1 to VL3	Power supply input for LCD		Power supply input for LCD drive circuit.
C1, C2	Step-up condenser connect port		Pins in this port function as external pin for LCD step-up condenser. Connect a condenser between C1 and C2.

Memory

Operation of Functional Blocks

The M30221 group accommodates certain units in a single chip. These units include ROM and RAM to store instructions and data and the central processing unit (CPU) to execute arithmetic/logic operations. Also included are peripheral units such as timers, real time port, serial I/O, LCD drive control circuit, D-A converter, A-D converter, DMAC and I/O ports.

Memory

Figure 1.4.1 is a memory map of the M30221 group. The address space extends the 1M bytes from address 00000_{16} to $FFFFF_{16}$. From $FFFFF_{16}$ down is ROM. For example, in the M30221M3-XXXFP, there is 24K bytes of internal ROM from $FA000_{16}$ to $FFFFF_{16}$. The vector table for fixed interrupts such as the reset and $\overline{NMI}$ are mapped to $FFFDC_{16}$ to $FFFFF_{16}$. The starting address of the interrupt routine is stored here. The address of the vector table for timer interrupts, etc., can be set as desired using the internal register (INTB). See the section on interrupts for details.

From 00400_{16} up is RAM. For example, in the M30221M3-XXXFP, 1.5K bytes of internal RAM is mapped to the space from 00400_{16} to $009FF_6$. In addition to storing data, the RAM also stores the stack used when calling subroutines and when interrupts are generated.

The SFR area is mapped to 00000_{16} to $003FF_{16}$. This area accommodates the control registers for peripheral devices such as I/O ports, A-D converter, serial I/O, timers, and LCD, etc. Figures 1.7.1 to 1.7.3 are location of peripheral unit control registers. Any part of the SFR area that is not occupied is reserved and cannot be used for other purposes.

The special page vector table is mapped to $FFE00_{16}$ to $FFFDB_{16}$. If the starting addresses of subroutines or the destination addresses of jumps are stored here, subroutine call instructions and jump instructions can be used as 2-byte instructions, reducing the number of program steps.

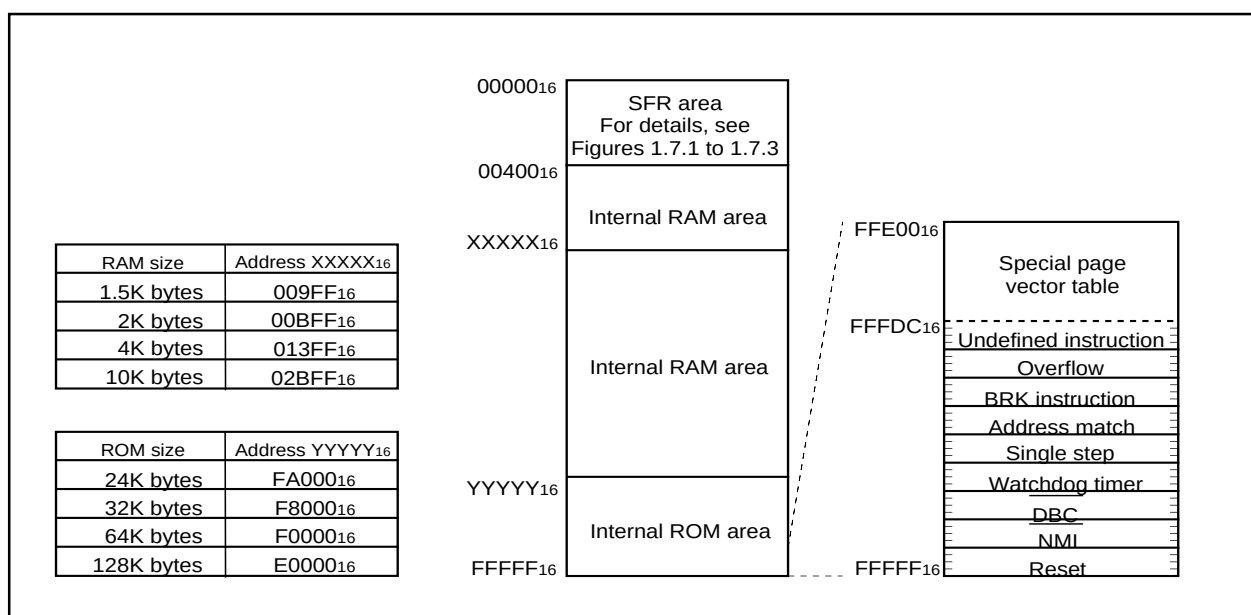


Figure 1.4.1. Memory map

CPU

Central Processing Unit (CPU)

The CPU has a total of 13 registers shown in Figure 1.5.1. Seven of these registers (R0, R1, R2, R3, A0, A1, and FB) come in two sets; therefore, these have two register banks.

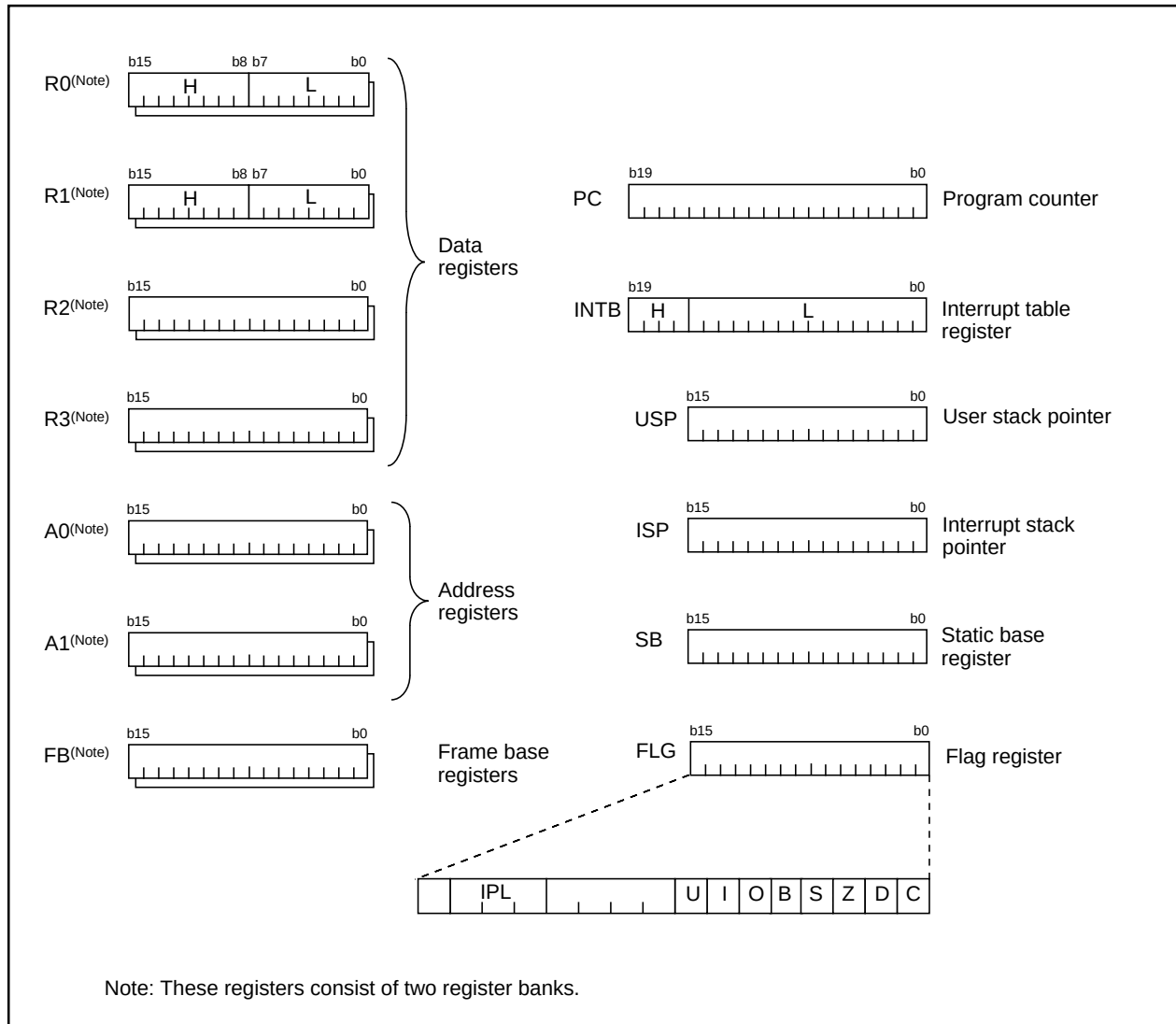


Figure 1.5.1. Central processing unit register

(1) Data registers (R0, R0H, R0L, R1, R1H, R1L, R2, and R3)

Data registers (R0, R1, R2, and R3) are configured with 16 bits, and are used primarily for transfer and arithmetic/logic operations.

Registers R0 and R1 each can be used as separate 8-bit data registers, high-order bits as (R0H/R1H), and low-order bits as (R0L/R1L). In some instructions, registers R2 and R0, as well as R3 and R1 can use as 32-bit data registers (R2R0/R3R1).

(2) Address registers (A0 and A1)

Address registers (A0 and A1) are configured with 16 bits, and have functions equivalent to those of data registers. These registers can also be used for address register indirect addressing and address register relative addressing.

In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

(3) Frame base register (FB)

Frame base register (FB) is configured with 16 bits, and is used for FB relative addressing.

(4) Program counter (PC)

Program counter (PC) is configured with 20 bits, indicating the address of an instruction to be executed.

(5) Interrupt table register (INTB)

Interrupt table register (INTB) is configured with 20 bits, indicating the start address of an interrupt vector table.

(6) Stack pointer (USP/ISP)

Stack pointer comes in two types: user stack pointer (USP) and interrupt stack pointer (ISP), each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by a stack pointer select flag (U flag).

This flag is located at the position of bit 7 in the flag register (FLG).

(7) Static base register (SB)

Static base register (SB) is configured with 16 bits, and is used for SB relative addressing.

(8) Flag register (FLG)

Flag register (FLG) is configured with 11 bits, each bit is used as a flag. Figure 1.5.2 shows the flag register (FLG). The following explains the function of each flag:

- **Bit 0: Carry flag (C flag)**

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

- **Bit 1: Debug flag (D flag)**

This flag enables a single-step interrupt.

When this flag is "1", a single-step interrupt is generated after instruction execution. This flag is cleared to "0" when the interrupt is acknowledged.

- **Bit 2: Zero flag (Z flag)**

This flag is set to "1" when an arithmetic operation resulted in 0; otherwise, cleared to "0".

- **Bit 3: Sign flag (S flag)**

This flag is set to "1" when an arithmetic operation resulted in a negative value; otherwise, cleared to "0".

- **Bit 4: Register bank select flag (B flag)**

This flag chooses a register bank. Register bank 0 is selected when this flag is "0"; register bank 1 is selected when this flag is "1".

- **Bit 5: Overflow flag (O flag)**

This flag is set to "1" when an arithmetic operation resulted in overflow; otherwise, cleared to "0".

- **Bit 6: Interrupt enable flag (I flag)**

This flag enables a maskable interrupt.

An interrupt is disabled when this flag is "0", and is enabled when this flag is "1". This flag is cleared to "0" when the interrupt is acknowledged.

- **Bit 7: Stack pointer select flag (U flag)**

Interrupt stack pointer (ISP) is selected when this flag is “0” ; user stack pointer (USP) is selected when this flag is “1”.

This flag is cleared to “0” when a hardware interrupt is acknowledged or an INT instruction of software interrupt Nos. 0 to 31 is executed.

- **Bits 8 to 11: Reserved area**

- **Bits 12 to 14: Processor interrupt priority level (IPL)**

Processor interrupt priority level (IPL) is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than the processor interrupt priority level (IPL), the interrupt is enabled.

- **Bit 15: Reserved area**

The C, Z, S, and O flags are changed when instructions are executed. See the software manual for details.

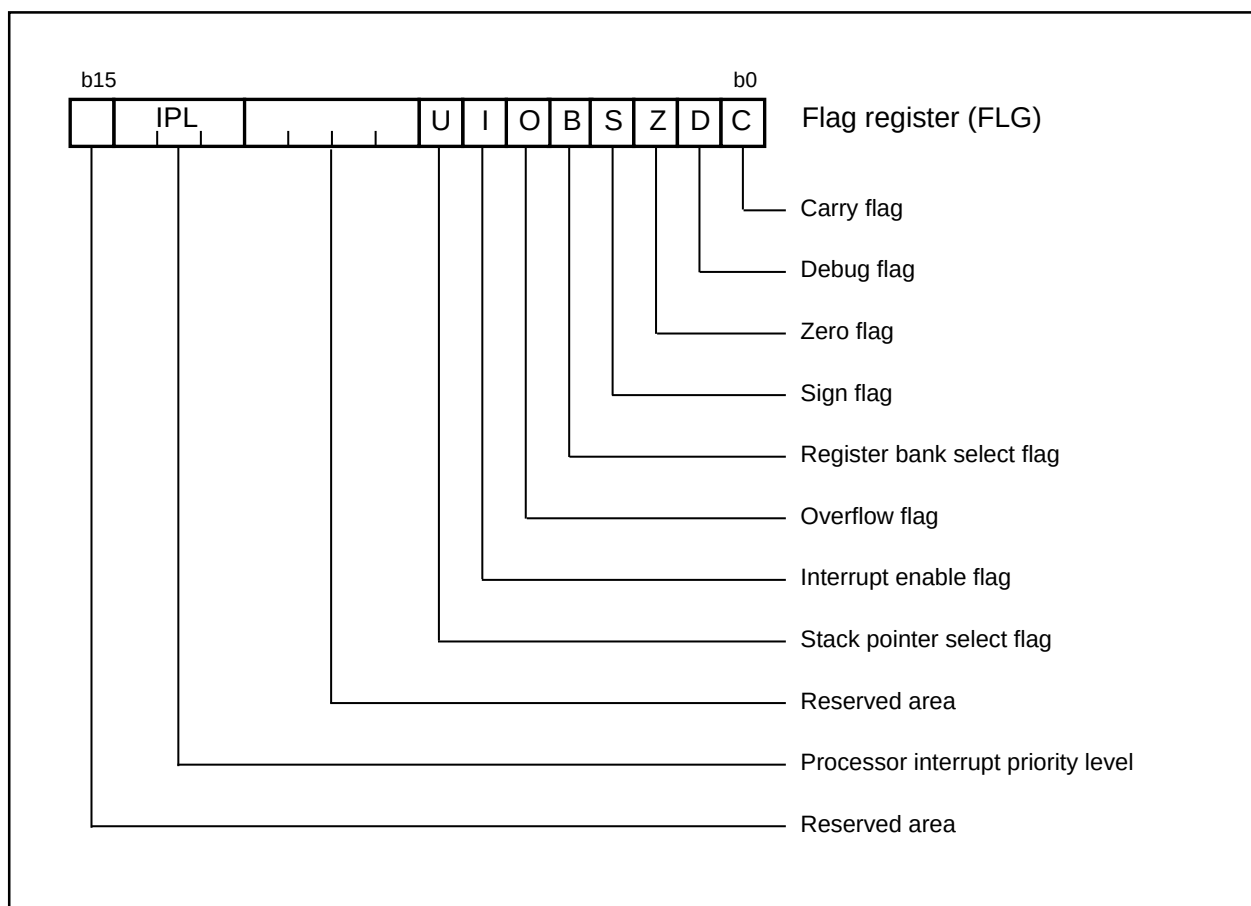


Figure 1.5.2. Flag register (FLG)

Reset

Reset

There are two kinds of resets; hardware and software. In both cases, operation is the same after the reset. (See "Software Reset" for details of software resets.) This section explains on hardware resets.

When the supply voltage is in the range where operation is guaranteed, a reset is effected by holding the reset pin level "L" (0.2V_{CC} max.) for at least 20 cycles. When the reset pin level is then returned to the "H" level while main clock is stable, the reset status is cancelled and program execution resumes from the address in the reset vector table.

Figure 1.6.1 shows the example reset circuit. Figure 1.6.2 shows the reset sequence.

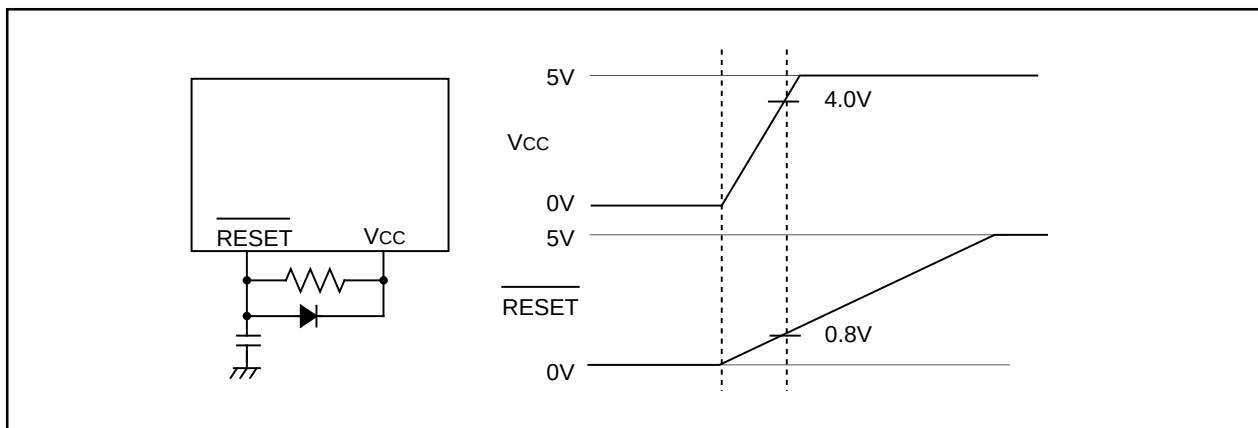


Figure 1.6.1. Example reset circuit

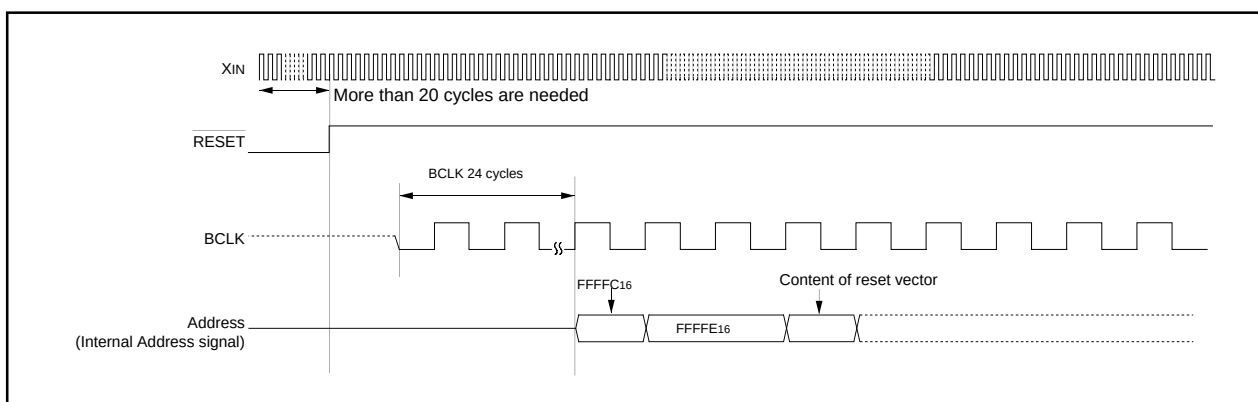


Figure 1.6.2. Reset sequence

Table 1.6.1 shows the statuses of the other pins while the $\overline{\text{RESET}}$ pin level is "L". Figures 1.6.3 and 1.6.4 show the internal status of the microcomputer immediately after the reset is cancelled.

Table 1.6.1. Pin status when $\overline{\text{RESET}}$ pin level is "L"

Pin name	Status
P0, P10 to P12	Input port(with a pull up resistor)
P1 to P9, P13	Input port (floating)
SEG2 to SEG15	"H" level is output
COM0 to COM3	"H" level is output

Reset

(1)Processor mode register 0	(000416)***		(27)Timer A0 interrupt control register	(005516)***	
(2)Processor mode register 1	(000516)***		(28)Timer A1 interrupt control register	(005616)***	
(3)System clock control register 0	(000616)***		(29)Timer A2 interrupt control register	(005716)***	
(4)System clock control register 1	(000716)***		(30)Timer A3 interrupt control register	(005816)***	
(5)Address match interrupt enable register	(000916)***		(31)Timer A4 interrupt control register	(005916)***	
(6)Protect register	(000A16)***		(32)Timer B0 interrupt control register	(005A16)***	
(7)Watchdog timer control register	(000F16)***		(33)Timer B1 interrupt control register	(005B16)***	
(8)Address match interrupt register 0	(001016)***		(34)Timer B2 interrupt control register	(005C16)***	
	(001116)***		(35)INT0 interrupt control register	(005D16)***	
	(001216)***		(36)INT1 interrupt control register	(005E16)***	
(9)Address match interrupt register 1	(001416)***		(37)INT2 interrupt control register	(005F16)***	
	(001516)***		(38)LCD mode register	(012016)***	
	(001616)***		(39)Segment output enable register	(012216)***	
(10)DMA0 control register	(002C16)***		(40)Key input mode register	(012616)***	
(11)DMA1 control register	(003C16)***		(41)Count start flag 1	(034016)***	
(12)INT3 interrupt control register	(004416)***		(42)One-shot start flag 1	(034216)***	
(13)Timer B5 interrupt control register	(004516)***		(43)Trigger select flag 1	(034316)***	
(14)Timer B4 interrupt control register	(004616)***		(44)Up-down flag 1	(034416)***	
(15)Timer B3 interrupt control register	(004716)***		(45)Timer A5 mode register	(035616)***	
(16)Timer A7 interrupt control register	(004816)***		(46)Timer A6 mode register	(035716)***	
(17)Timer A6 interrupt control register	(004916)***		(47)Timer A7 mode register	(035816)***	
(18)Timer A5 interrupt control register	(004A16)***		(48)Timer B3 mode register	(035B16)***	
(19)DMA0 interrupt control register	(004B16)***		(49)Timer B4 mode register	(035C16)***	
(20)DMA1 interrupt control register	(004C16)***		(50)Timer B5 mode register	(035D16)***	
(21)Key input interrupt control register	(004D16)***		(51)Interrupt cause select register 0	(035E16)***	
(22)A-D conversion interrupt control register	(004E16)***		(52)Interrupt cause select register 1	(035F16)***	
(23)UART2 transmit interrupt control register	(004F16)***		(53)Clock division counter control register	(036016)***	
(24)UART2 receive interrupt control register	(005016)***		(54)UART2 special mode register 2	(037616)***	
(25)UART0 transmit interrupt control register	(005116)***		(55)UART2 special mode register	(037716)***	
(26)UART0 receive interrupt control register	(005216)***		(56)UART2 transmit/receive mode register	(037816)***	

The content of other registers and RAM is undefined when the microcomputer is reset. The initial values must therefore be set.

x : Nothing is mapped to this bit
? : Undefined

Figure 1.6.3. Device's internal status after a reset is cleared(1)

Reset

(57)UART2 transmit/receive control register 0	(037C16) ···	0 0 0 0 1 0 0 0	(83)Port P0 direction register	(03E216) ···	0016
(58)UART2 transmit/receive control register 1	(037D16) ···	0 0 0 0 0 0 1 0	(84)Port P1 direction register	(03E316) ···	0016
(59)Count start flag 0	(038016) ···	0016	(85)Port P2 direction register	(03E616) ···	0016
(60)Clock prescaler reset flag	(038116) ···	0 X X X X X X X	(86)Port P3 direction register	(03E716) ···	X X 0 0 0 0 0 0
(61)One-shot start flag 0	(038216) ···	0 0 X 0 0 0 0 0	(87)Port P4 direction register	(03EA16) ···	0016
(62)Trigger select flag 0	(038316) ···	0016	(88)Port P5 direction register	(03EB16) ···	0016
(63)Up-down flag 0	(038416) ···	0016	(89)Port P6 direction register	(03EE16) ···	0016
(64)Timer A0 mode register	(039616) ···	0016	(90)Port P7 direction register	(03EF16) ···	X 0 0 0 0 0 0 0
(65)Timer A1 mode register	(039716) ···	0016	(91)Port P8 direction register	(03F216) ···	0016
(66)Timer A2 mode register	(039816) ···	0016	(92)Port P9 direction register	(03F316) ···	0016
(67)Timer A3 mode register	(039916) ···	0016	(93)Port P10 direction register	(03F616) ···	0016
(68)Timer A4 mode register	(039A16) ···	0016	(94)Port P11 direction register	(03F716) ···	0016
(69)Timer B0 mode register	(039B16) ···	0 0 ? X 0 0 0 0	(95)Port P12 direction register	(03FA16) ···	0016
(70)Timer B1 mode register	(039C16) ···	0 0 ? X 0 0 0 0	(96)Port P13 direction register	(03FB16) ···	X X X X X 0 0 0
(71)Timer B2 mode register	(039D16) ···	0 0 ? X 0 0 0 0	(97)Pull-up control register 0	(03FC16) ···	0 0 0 0 0 0 1 1
(72)UART0 transmit/receive mode register	(03A016) ···	0016	(98)Pull-up control register 1	(03FD16) ···	0016
(73)UART0 transmit/receive control register 0	(03A416) ···	0 0 0 0 1 0 0 0	(99)Pull-up control register 2	(03FE16) ···	1 1 1 1 0 0 0 0
(74)UART0 transmit/receive control register 1	(03A516) ···	0 0 0 0 0 0 1 0	(100)Real time port control register	(03FF16) ···	0016
(75)UART transmit/receive control register 2	(03B016) ···	X 0 0 0 0 0 0 0	(101)Data registers (R0/R1/R2/R3)	···	000016
(76)Flash memory control register (Note)	(03B416) ···	X X X X 0 X 0 1	(102)Address registers (A0/A1)	···	000016
(77)DMA0 cause select register	(03B816) ···	0016	(103)Frame base register (FB)	···	000016
(78)DMA1 cause select register	(03BA16) ···	0016	(104)Interrupt table register (INTB)	···	0000016
(79)A-D control register 2	(03D416) ···	X X X X 0 0 0 0	(105)User stack pointer (USP)	···	000016
(80)A-D control register 0	(03D616) ···	X X 0 0 0 ? ? ?	(106)Interrupt stack pointer (ISP)	···	000016
(81)A-D control register 1	(03D716) ···	0016	(107)Static base register (SB)	···	000016
(82)D-A control register	(03DC16) ···	X X X X 0 0 0 0	(108)Flag register (FLG)	···	000016

x : Nothing is mapped to this bit
? : Undefined

The content of other registers and RAM is undefined when the microcomputer is reset. The initial values must therefore be set.

Note : This register is only exist in flash memory version.

Figure 1.6.4. Device's internal status after a reset is cleared(2)

0000 ₁₆		0040 ₁₆	
0001 ₁₆		0041 ₁₆	
0002 ₁₆		0042 ₁₆	
0003 ₁₆		0043 ₁₆	
0004 ₁₆	Processor mode register 0 (PM0)	0044 ₁₆	INT3 interrupt control register (INT3IC)
0005 ₁₆	Processor mode register 1 (PM1)	0045 ₁₆	Timer B5 interrupt control register (TB5IC)
0006 ₁₆	System clock control register 0 (CM0)	0046 ₁₆	Timer B4 interrupt control register (TB4IC)
0007 ₁₆	System clock control register 1 (CM1)	0047 ₁₆	Timer B3 interrupt control register (TB3IC)
0008 ₁₆		0048 ₁₆	Timer A7 interrupt control register (TA7IC)
0009 ₁₆	Address match interrupt enable register (AIER)	0049 ₁₆	Timer A6 interrupt control register (TA6IC)
000A ₁₆	Protect register (PRCR)	004A ₁₆	Timer A5 interrupt control register (TA5IC)
000B ₁₆			Bus collision detection interrupt control register (BCNIC)
000C ₁₆		004B ₁₆	DMA0 interrupt control register (DM0IC)
000D ₁₆		004C ₁₆	DMA1 interrupt control register (DM1IC)
000E ₁₆	Watchdog timer start register (WDTS)	004D ₁₆	Key input interrupt control register (KUPIC)
000F ₁₆	Watchdog timer control register (WDC)	004E ₁₆	A-D conversion interrupt control register (ADIC)
0010 ₁₆		004F ₁₆	UART2 transmit interrupt control register (S2TIC)
0011 ₁₆	Address match interrupt register 0 (RMAD0)	0050 ₁₆	UART2 receive interrupt control register (S2RIC)
0012 ₁₆		0051 ₁₆	UART0 transmit interrupt control register (S0TIC)
0013 ₁₆		0052 ₁₆	UART0 receive interrupt control register (S0RIC)
0014 ₁₆		0053 ₁₆	UART1 transmit interrupt control register (S1TIC)
0015 ₁₆	Address match interrupt register 1 (RMAD1)	0054 ₁₆	UART1 receive interrupt control register (S1RIC)
0016 ₁₆		0055 ₁₆	Timer A0 interrupt control register (TA0IC)
0017 ₁₆		0056 ₁₆	Timer A1 interrupt control register (TA1IC)
0018 ₁₆		0057 ₁₆	Timer A2 interrupt control register (TA2IC)
0019 ₁₆		0058 ₁₆	Timer A3 interrupt control register (TA3IC)
001A ₁₆			INT4 interrupt control register (INT4IC)
001B ₁₆		0059 ₁₆	Timer A4 interrupt control register (TA4IC)
001C ₁₆			INT5 interrupt control register (INT5IC)
001D ₁₆		005A ₁₆	Timer B0 interrupt control register (TB0IC)
001E ₁₆		005B ₁₆	Timer B1 interrupt control register (TB1IC)
001F ₁₆		005C ₁₆	Timer B2 interrupt control register (TB2IC)
0020 ₁₆		005D ₁₆	INT0 interrupt control register (INT0IC)
0021 ₁₆	DMA0 source pointer (SAR0)	005E ₁₆	INT1 interrupt control register (INT1IC)
0022 ₁₆		005F ₁₆	INT2 interrupt control register (INT2IC)
0023 ₁₆			
0024 ₁₆		0100 ₁₆	LCD RAM0(LRAM0)
0025 ₁₆	DMA0 destination pointer (DAR0)	0101 ₁₆	LCD RAM1(LRAM1)
0026 ₁₆		0102 ₁₆	LCD RAM2(LRAM2)
0027 ₁₆		0103 ₁₆	LCD RAM3(LRAM3)
0028 ₁₆	DMA0 transfer counter (TCR0)	0104 ₁₆	LCD RAM4(LRAM4)
0029 ₁₆		0105 ₁₆	LCD RAM5(LRAM5)
002A ₁₆		0106 ₁₆	LCD RAM6(LRAM6)
002B ₁₆		0107 ₁₆	LCD RAM7(LRAM7)
002C ₁₆	DMA0 control register (DM0CON)	0108 ₁₆	LCD RAM8(LRAM8)
002D ₁₆		0109 ₁₆	LCD RAM9(LRAM9)
002E ₁₆		010A ₁₆	
002F ₁₆		010B ₁₆	
0030 ₁₆		010C ₁₆	LCD RAM12(LRAM12)
0031 ₁₆	DMA1 source pointer (SAR1)	010D ₁₆	LCD RAM13(LRAM13)
0032 ₁₆		010E ₁₆	LCD RAM14(LRAM14)
0033 ₁₆		010F ₁₆	LCD RAM15(LRAM15)
0034 ₁₆		0110 ₁₆	LCD RAM16(LRAM16)
0035 ₁₆	DMA1 destination pointer (DAR1)	0111 ₁₆	LCD RAM17(LRAM17)
0036 ₁₆		0112 ₁₆	LCD RAM18(LRAM18)
0037 ₁₆		0113 ₁₆	
0038 ₁₆		0114 ₁₆	LCD RAM20(LRAM20)
0039 ₁₆	DMA1 transfer counter (TCR1)	0115 ₁₆	LCD RAM21(LRAM21)
003A ₁₆		0116 ₁₆	LCD RAM22(LRAM22)
003B ₁₆		0117 ₁₆	LCD RAM23(LRAM23)
003C ₁₆	DMA1 control register (DM1CON)		
003D ₁₆		0120 ₁₆	LCD mode register (LCMD)
003E ₁₆		0121 ₁₆	
003F ₁₆		0122 ₁₆	Segment output enable register (SEG)
		0123 ₁₆	
		0124 ₁₆	LCD frame frequency counter (LCDTIM)
		0125 ₁₆	
		0126 ₁₆	Key input mode register (KUPM)

Note : Locations in the SFR area where nothing is allocated are reserved areas. Do not access these areas for read or write.

Figure 1.7.1. Location of peripheral unit control registers (1)

0340 ₁₆	Count start flag 1 (TABSR1)	0380 ₁₆	Count start flag 0 (TABSR0)
0341 ₁₆		0381 ₁₆	Clock prescaler reset flag (CPSRF)
0342 ₁₆	One-shot start flag 1 (ONSF1)	0382 ₁₆	One-shot start flag 0 (ONSF0)
0343 ₁₆	Trigger select register 1 (TRGSR1)	0383 ₁₆	Trigger select register 0 (TRGSR0)
0344 ₁₆	Up-down flag 1(UDF1)	0384 ₁₆	Up-down flag 0 (UDF0)
0345 ₁₆		0385 ₁₆	
0346 ₁₆	Timer A5 register (TA5)	0386 ₁₆	Timer A0 register (TA0)
0347 ₁₆		0387 ₁₆	
0348 ₁₆	Timer A6 register (TA6)	0388 ₁₆	Timer A1 register (TA1)
0349 ₁₆		0389 ₁₆	
034A ₁₆	Timer A7 register (TA7)	038A ₁₆	Timer A2 register (TA2)
034B ₁₆		038B ₁₆	
034C ₁₆		038C ₁₆	Timer A3 register (TA3)
034D ₁₆		038D ₁₆	
034E ₁₆		038E ₁₆	Timer A4 register (TA4)
034F ₁₆		038F ₁₆	
0350 ₁₆	Timer B3 register (TB3)	0390 ₁₆	Timer B0 register (TB0)
0351 ₁₆		0391 ₁₆	
0352 ₁₆	Timer B4 register (TB4)	0392 ₁₆	Timer B1 register (TB1)
0353 ₁₆		0393 ₁₆	
0354 ₁₆	Timer B5 register (TB5)	0394 ₁₆	Timer B2 register (TB2)
0355 ₁₆		0395 ₁₆	
0356 ₁₆	Timer A5 mode register (TA5MR)	0396 ₁₆	Timer A0 mode register (TA0MR)
0357 ₁₆	Timer A6 mode register (TA6MR)	0397 ₁₆	Timer A1 mode register (TA1MR)
0358 ₁₆	Timer A7 mode register (TA7MR)	0398 ₁₆	Timer A2 mode register (TA2MR)
0359 ₁₆		0399 ₁₆	Timer A3 mode register (TA3MR)
035A ₁₆		039A ₁₆	Timer A4 mode register (TA4MR)
035B ₁₆	Timer B3 mode register (TB3MR)	039B ₁₆	Timer B0 mode register (TB0MR)
035C ₁₆	Timer B4 mode register (TB4MR)	039C ₁₆	Timer B1 mode register (TB1MR)
035D ₁₆	Timer B5 mode register(TB5MR)	039D ₁₆	Timer B2 mode register (TB2MR)
035E ₁₆	Interrupt cause select register 0 (IFSR0)	039E ₁₆	
035F ₁₆	Interrupt cause select register 1 (IFSR1)	039F ₁₆	
0360 ₁₆	Clock division counter control register (CDCC)	03A0 ₁₆	UART0 transmit/receive mode register (U0MR)
0361 ₁₆		03A1 ₁₆	UART0 bit rate generator (U0BRG)
0362 ₁₆		03A2 ₁₆	UART0 transmit buffer register (U0TB)
0363 ₁₆		03A3 ₁₆	
0364 ₁₆		03A4 ₁₆	UART0 transmit/receive control register 0 (U0C0)
0365 ₁₆		03A5 ₁₆	UART0 transmit/receive control register 1 (U0C1)
0366 ₁₆		03A6 ₁₆	UART0 receive buffer register (U0RB)
0367 ₁₆		03A7 ₁₆	
0368 ₁₆		03A8 ₁₆	
0369 ₁₆		03A9 ₁₆	
036A ₁₆		03AA ₁₆	
036B ₁₆		03AB ₁₆	
036C ₁₆		03AC ₁₆	
036D ₁₆		03AD ₁₆	
036E ₁₆	Clock division counter (CDC)	03AE ₁₆	
036F ₁₆		03AF ₁₆	
0370 ₁₆		03B0 ₁₆	UART transmit/receive control register 2 (UCON)
0371 ₁₆		03B1 ₁₆	
0372 ₁₆		03B2 ₁₆	
0373 ₁₆		03B3 ₁₆	
0374 ₁₆		03B4 ₁₆	Flash memory control register (FMCR)(Note)
0375 ₁₆		03B5 ₁₆	
0376 ₁₆	UART2 special mode register 2(U2SMR2)	03B6 ₁₆	
0377 ₁₆	UART2 special mode register (U2SMR)	03B7 ₁₆	
0378 ₁₆	UART2 transmit/receive mode register (U2MR)	03B8 ₁₆	DMA0 request cause select register (DM0SL)
0379 ₁₆	UART2 bit rate generator (U2BRG)	03B9 ₁₆	
037A ₁₆	UART2 transmit buffer register (U2TB)	03BA ₁₆	DMA1 request cause select register (DM1SL)
037B ₁₆		03BB ₁₆	
037C ₁₆	UART2 transmit/receive control register 0 (U2C0)	03BC ₁₆	
037D ₁₆	UART2 transmit/receive control register 1 (U2C1)	03BD ₁₆	
037E ₁₆	UART2 receive buffer register (U2RB)	03BE ₁₆	
037F ₁₆		03BF ₁₆	

Note1 : This register is only exist in flash memory version.

Note2 : Locations in the SFR area where nothing is allocated are reserved areas. Do not access these areas for read or write.

Figure 1.7.2. Location of peripheral unit control registers (2)

03C0 ₁₆	A-D register 0 (AD0)
03C1 ₁₆	
03C2 ₁₆	A-D register 1 (AD1)
03C3 ₁₆	
03C4 ₁₆	A-D register 2 (AD2)
03C5 ₁₆	
03C6 ₁₆	A-D register 3 (AD3)
03C7 ₁₆	
03C8 ₁₆	A-D register 4 (AD4)
03C9 ₁₆	
03CA ₁₆	A-D register 5 (AD5)
03CB ₁₆	
03CC ₁₆	A-D register 6 (AD6)
03CD ₁₆	
03CE ₁₆	
03CF ₁₆	
03D0 ₁₆	
03D1 ₁₆	
03D2 ₁₆	
03D3 ₁₆	
03D4 ₁₆	A-D control register 2 (ADCON2)
03D5 ₁₆	
03D6 ₁₆	A-D control register 0 (ADCON0)
03D7 ₁₆	A-D control register 1 (ADCON1)
03D8 ₁₆	D-A register 0 (DA0)
03D9 ₁₆	
03DA ₁₆	D-A register 1 (DA1)
03DB ₁₆	
03DC ₁₆	D-A control register (DACON)
03DD ₁₆	
03DE ₁₆	
03DF ₁₆	
03E0 ₁₆	Port P0 register (P0)
03E1 ₁₆	Port P1 register (P1)
03E2 ₁₆	Port P0 direction register (PD0)
03E3 ₁₆	Port P1 direction register (PD1)
03E4 ₁₆	Port P2 register (P2)
03E5 ₁₆	Port P3 register (P3)
03E6 ₁₆	Port P2 direction register (PD2)
03E7 ₁₆	Port P3 direction register (PD3)
03E8 ₁₆	Port P4 register (P4)
03E9 ₁₆	Port P5 register (P5)
03EA ₁₆	Port P4 direction register (PD4)
03EB ₁₆	Port P5 direction register (PD5)
03EC ₁₆	Port P6 register (P6)
03ED ₁₆	Port P7 register (P7)
03EE ₁₆	Port P6 direction register (PD6)
03EF ₁₆	Port P7 direction register (PD7)
03F0 ₁₆	Port P8 register (P8)
03F1 ₁₆	Port P9 register (P9)
03F2 ₁₆	Port P8 direction register (PD8)
03F3 ₁₆	Port P9 direction register (PD9)
03F4 ₁₆	Port P10 register (P10)
03F5 ₁₆	Port P11 register (P11)
03F6 ₁₆	Port P10 direction register (PD10)
03F7 ₁₆	Port P11 direction register (PD11)
03F8 ₁₆	Port P12 register (P12)
03F9 ₁₆	Port P13 register (P13)
03FA ₁₆	Port P12 direction register (PD12)
03FB ₁₆	Port P13 direction register (PD13)
03FC ₁₆	Pull-up control register 0 (PUR0)
03FD ₁₆	Pull-up control register 1 (PUR1)
03FE ₁₆	Pull-up control register 2 (PUR2)
03FF ₁₆	Real time port control register (RTP)

Note : Locations in the SFR area where nothing is allocated are reserved areas.
Do not access these areas for read or write.

Figure 1.7.3. Location of peripheral unit control registers (3)

Programmable I/O Port

Programmable I/O Ports

There are 83 programmable I/O ports: P0 to P13 (excluding P77). Each port can be set independently for input or output using the direction register. A pull-up resistance for each block of 4 ports can be set. P77 is an input-only port and has no built-in pull-up resistance.

Figures 1.19.1 to 1.19.4 show the programmable I/O ports. Figure 1.19.5 shows the I/O pins.

Each pin functions as a programmable I/O port and as the I/O for the built-in peripheral devices.

To use the pins as the inputs for the built-in peripheral devices, set the direction register of each pin to input mode. When the pins are used as the outputs for the built-in peripheral devices (other than the D-A converter), they function as outputs regardless of the contents of the direction registers. When pins are to be used as the outputs for the D-A converter, do not set the direction registers to output mode.

(1) Direction registers

These registers are used to choose the direction of the programmable I/O ports. Each bit in these registers corresponds one for one to each I/O pin.

Note: There is no direction register bit for P77.

(2) Port registers

These registers are used to write and read data for input and output to and from an external device. A port register consists of a port latch to hold output data and a circuit to read the status of a pin. Each bit in port registers corresponds one for one to each I/O pin.

(3) Pull-up control registers

The pull-up control register can be set to apply a pull-up resistance to each block of 4 ports. When ports are set to have a pull-up resistance, the pull-up resistance is connected only when the direction register is set for input. The pull-up resistance is not connected for pins that are set for output from peripheral functions, regardless of the setting in the pull-up control register. When pull-up is ON for ports P1 and P2, an intermittent pull-up that pulls up the port for only a set period of time, can be performed from the key input mode register.

(4) Key input mode register

With bits 0 and 1 of this register, it is possible to select both edges or the fall edge of the key input for P1 and P2. Also, with bit 2, it is possible to make the pull-up for a port (P1 or P2), which is set for pull-up using the pull-up control register, automatically connect as an intermittent pull-up. And, using the significant 3 bits, the pull-up resistance can be connected to and disconnected from ports P12 and P13.

(5) Real-time port control register

The real-time port control register can be used to set the registers of ports P0, P1, P2 and P12 for real-time port output, whereby output is synchronized with timer overflow of timers A0, A1, A5 and A6 in the timer mode.

Programmable I/O Port

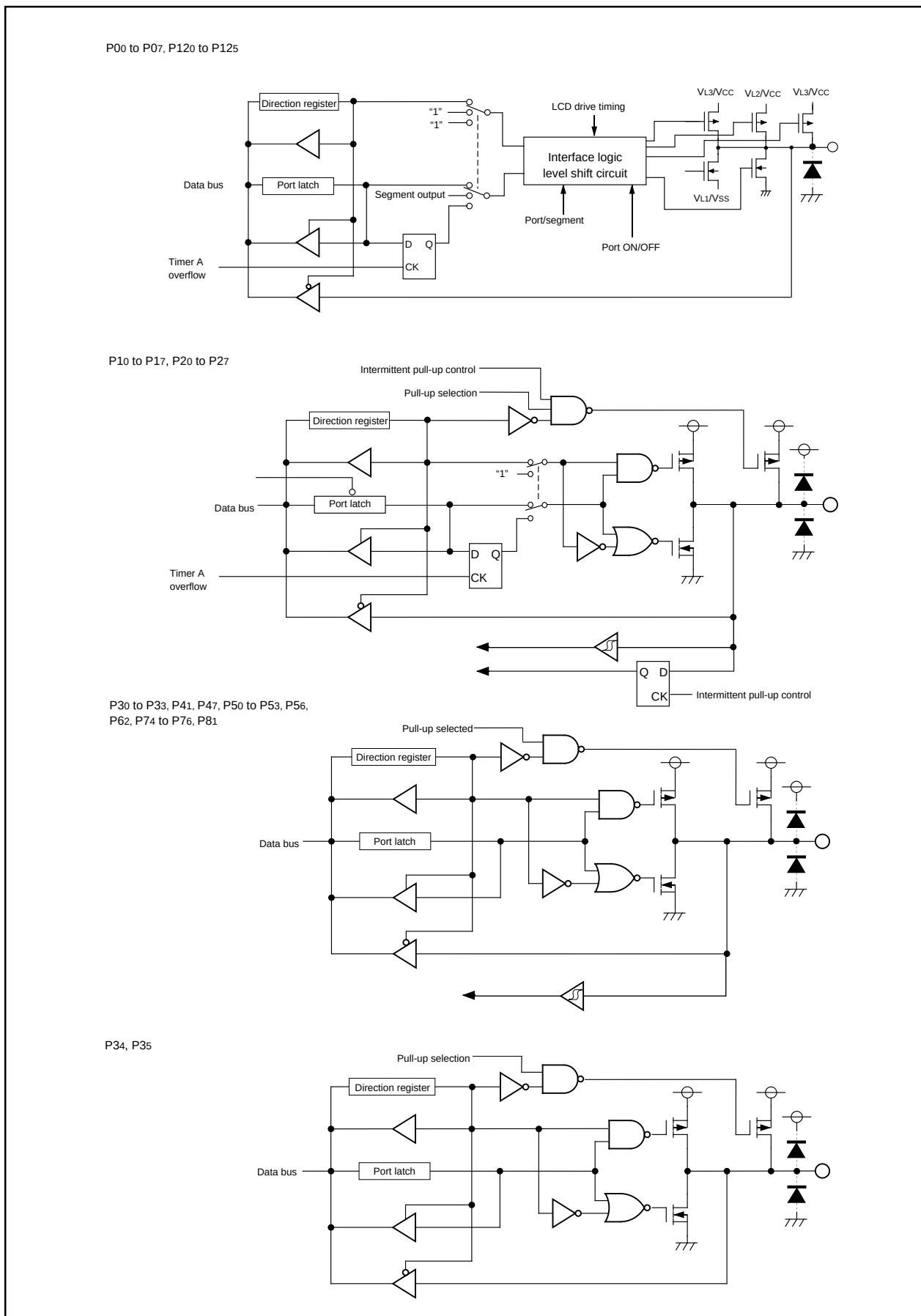


Figure 1.19.1. Programmable I/O ports (1)

Programmable I/O Port

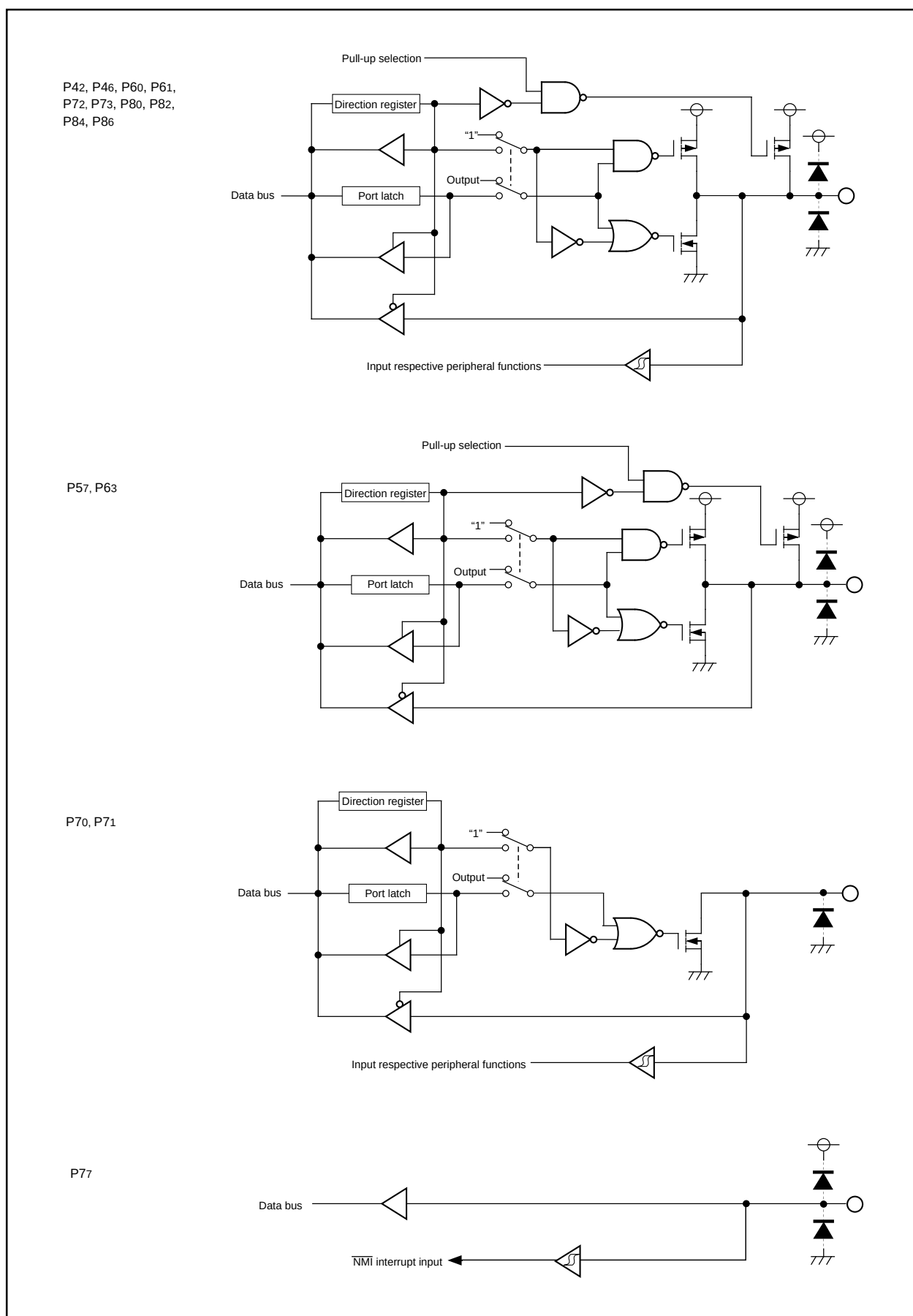


Figure 1.19.2. Programmable I/O ports (2)

Programmable I/O Port

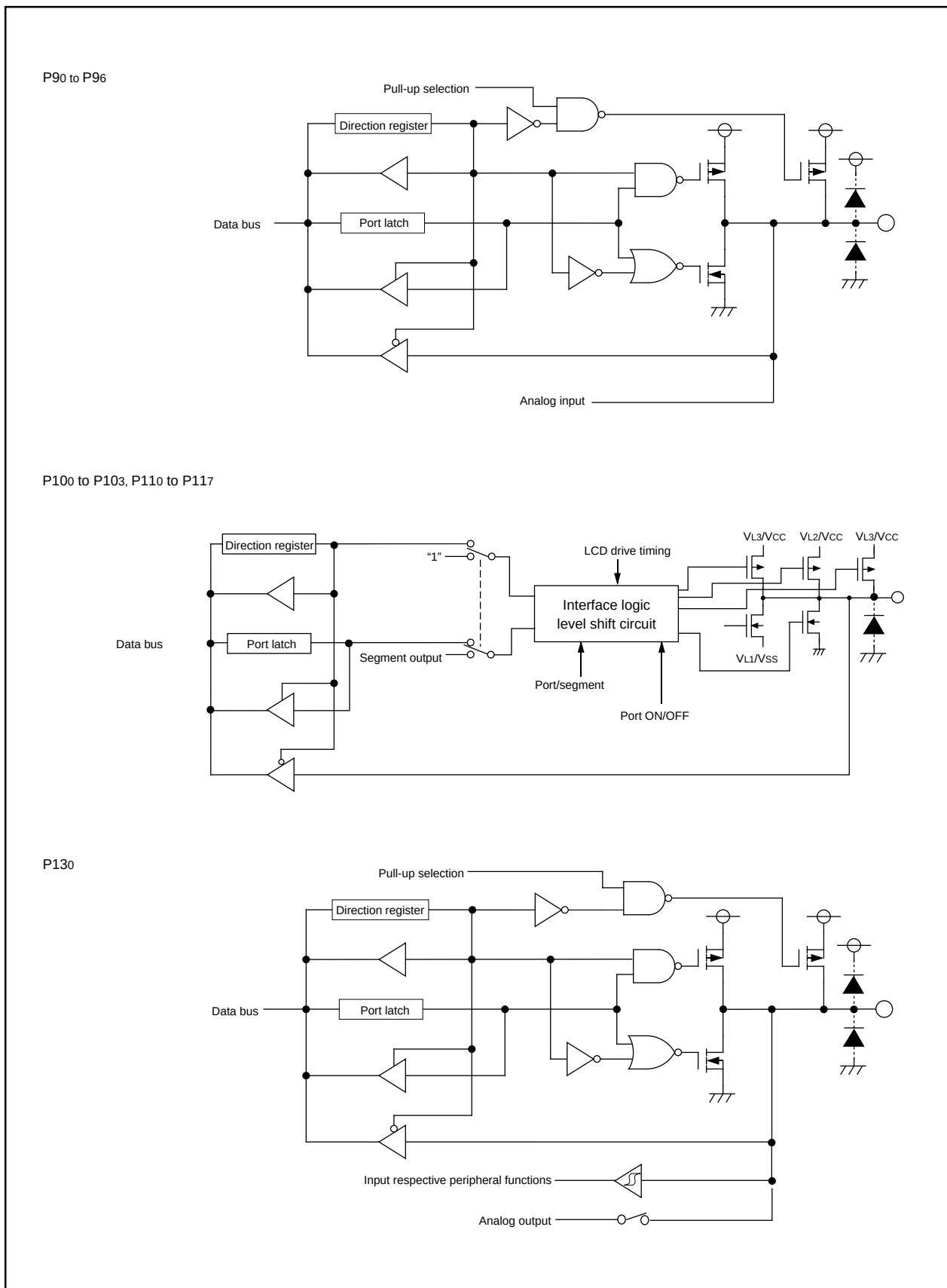


Figure 1.19.3. Programmable I/O ports (3)

Programmable I/O Port

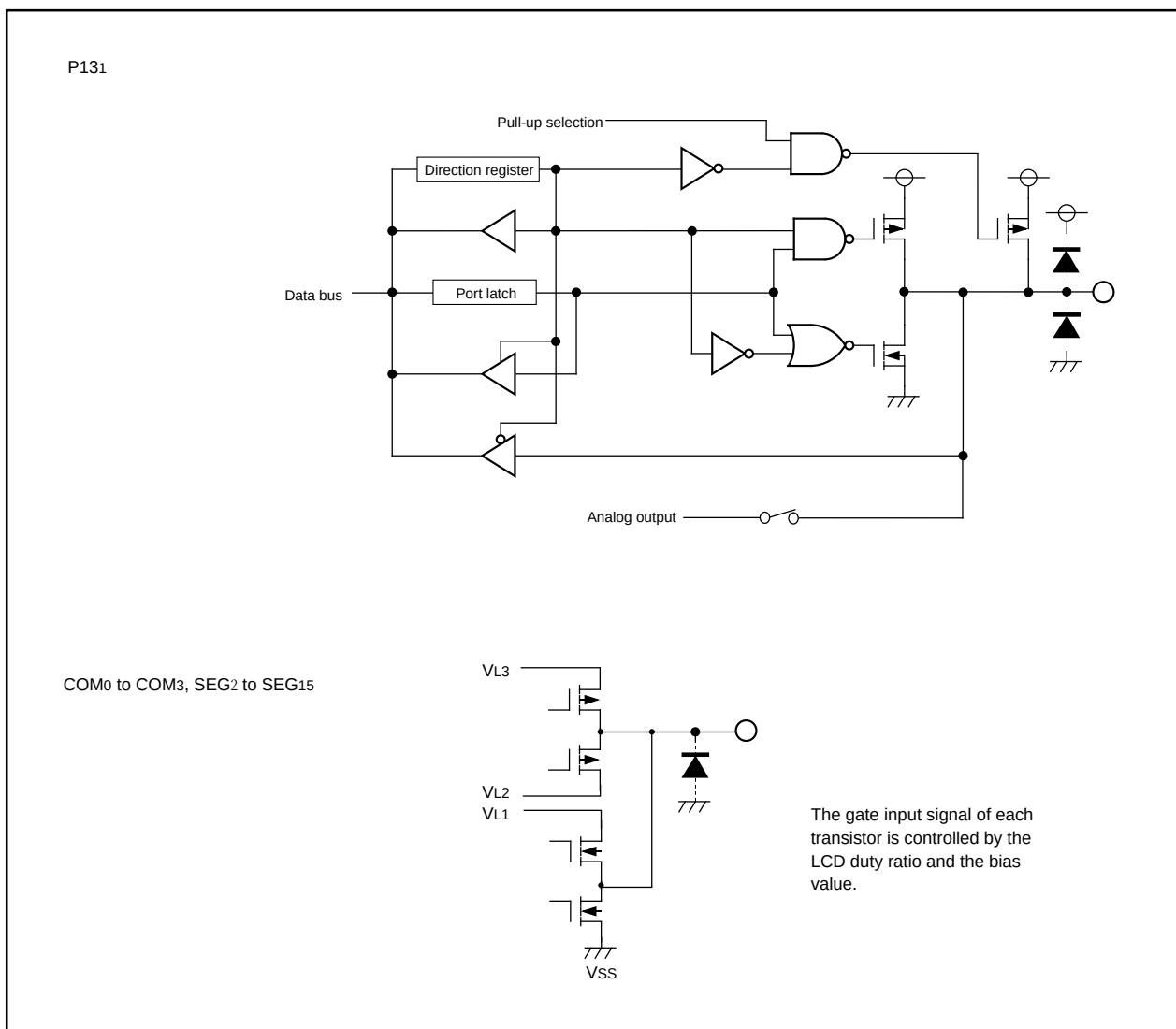


Figure 1.19.4. Programmable I/O ports (4)

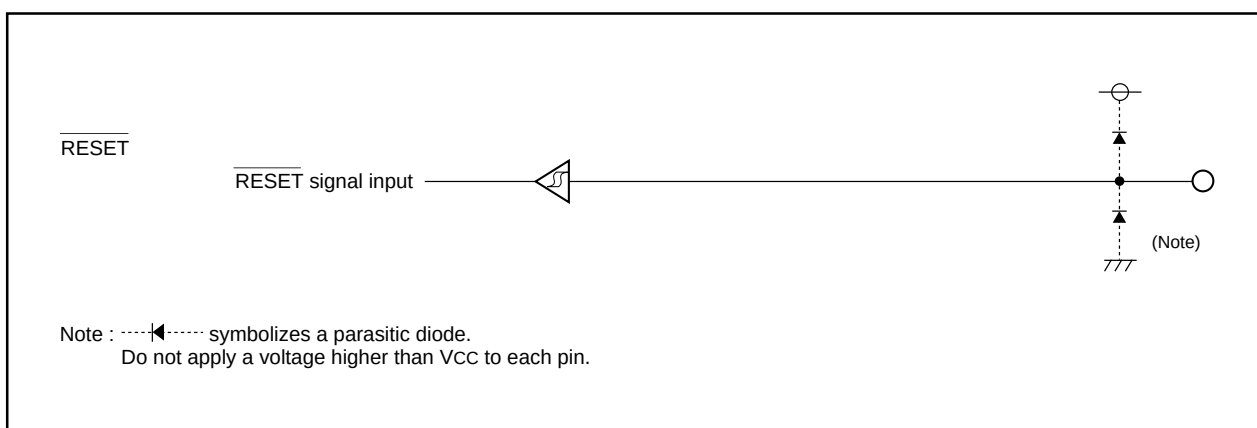


Figure 1.19.5. I/O pins

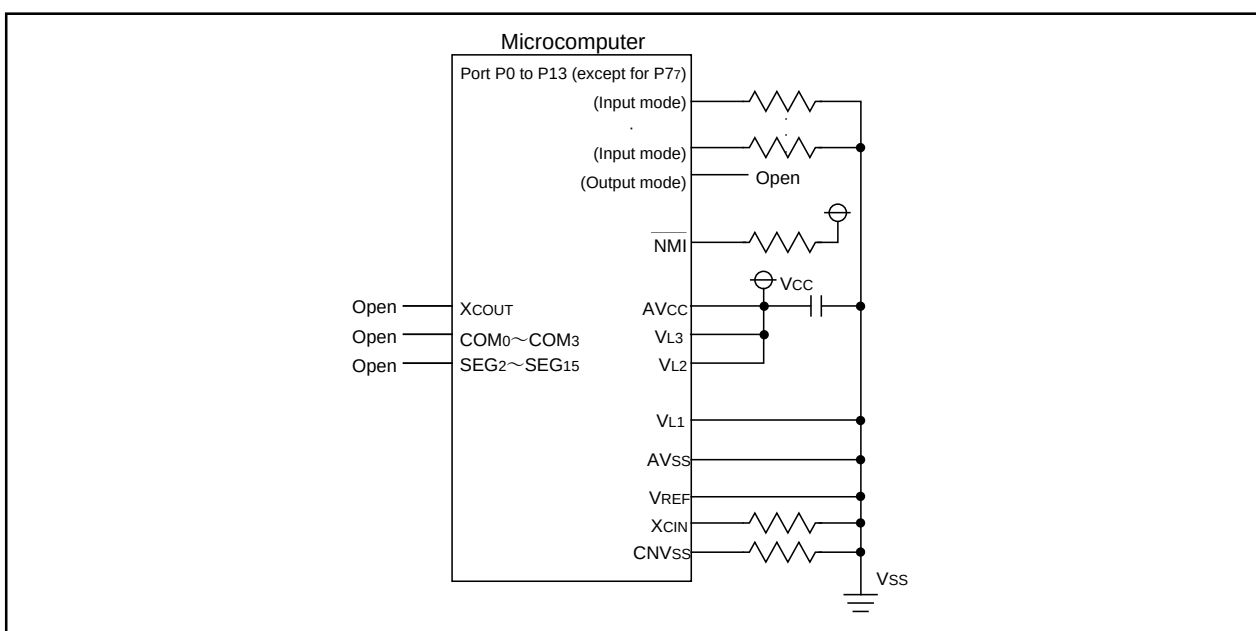
Table 1.19.1. Example connection of unused pins in single-chip mode

Pin name	Connection
Ports P0 to P13 (excluding P77)	After setting for output mode, leave these pins open; or after setting for input mode, connect every pin to Vss via a resistor.(Note1,Note3)
XOUT (Note 2),XCOUT	Open
XCIN	Connect via resistor to Vss (pull-down)
NMI	Connect via resistor to Vcc (pull-up)
AVCC	Connect to Vcc
AVSS, VREF	Connect to Vss
COM0~COM3	Open
SEG2~SEG15	Open
C1, C2	Open
VL2, VL3	Connect to Vcc
VL1	Connect to Vss
CNVss	Connect via resistor to Vss

Note 1: If setting these pins in output mode and opening them, ports are in input mode until switched into output mode by use of software after reset. Thus the voltage levels of the pins become unstable, and there can be instances in which the power source current increases while the ports are in input mode. In view of an instance in which the contents of the direction registers change due to a runaway generated by noise or other causes, setting the contents of the direction registers periodically by use of software increases program reliability.

Note 2: With external clock input to XIN pin.

Note 3: Output "L" if port P70 and P71 are set to output mode. Port P70 and P71 are N channel open drain.

**Figure 1.19.13. Example connection of unused pins**

Usage precaution

Usage Precaution

Timer A (timer mode)

- (1) Reading the timer Ai register while a count is in progress allows reading, with arbitrary timing, the value of the counter. Reading the timer Ai register with the reload timing gets "FFFF₁₆". Reading the timer Ai register after setting a value in the timer Ai register with a count halted but before the counter starts counting gets a proper value.

Timer A (event counter mode)

- (1) Reading the timer Ai register while a count is in progress allows reading, with arbitrary timing, the value of the counter. Reading the timer Ai register with the reload timing gets "FFFF₁₆" by underflow or "0000₁₆" by overflow. Reading the timer Ai register after setting a value in the timer Ai register with a count halted but before the counter starts counting gets a proper value.
- (2) When stop counting in free run type, set timer again.

Timer A (one-shot timer mode)

- (1) Setting the count start flag to "0" while a count is in progress causes as follows:
 - The counter stops counting and a content of reload register is reloaded.
 - The TAIOUT pin outputs "L" level.
 - The interrupt request generated and the timer Ai interrupt request bit goes to "1".
- (2) The timer Ai interrupt request bit goes to "1" if the timer's operation mode is set using any of the following procedures:
 - Selecting one-shot timer mode after reset.
 - Changing operation mode from timer mode to one-shot timer mode.
 - Changing operation mode from event counter mode to one-shot timer mode.
 Therefore, to use timer Ai interrupt (interrupt request bit), set timer Ai interrupt request bit to "0" after the above listed changes have been made.

Timer A (pulse width modulation mode)

- (1) The timer Ai interrupt request bit becomes "1" if setting operation mode of the timer in compliance with any of the following procedures:
 - Selecting PWM mode after reset.
 - Changing operation mode from timer mode to PWM mode.
 - Changing operation mode from event counter mode to PWM mode.
 Therefore, to use timer Ai interrupt (interrupt request bit), set timer Ai interrupt request bit to "0" after the above listed changes have been made.
- (2) Setting the count start flag to "0" while PWM pulses are being output causes the counter to stop counting. If the TAIOUT pin is outputting an "H" level in this instance, the output level goes to "L", and the timer Ai interrupt request bit goes to "1". If the TAIOUT pin is outputting an "L" level in this instance, the level does not change, and the timer Ai interrupt request bit does not becomes "1".

Timer B (timer mode, event counter mode)

- (1) Reading the timer Bi register while a count is in progress allows reading, with arbitrary timing, the value of the counter. Reading the timer Bi register with the reload timing gets "FFFF₁₆". Reading the timer Bi register after setting a value in the timer Bi register with a count halted but before the counter starts counting gets a proper value.

Usage precaution

Timer B (pulse period/pulse width measurement mode)

- (1) If changing the measurement mode select bit is set after a count is started, the timer Bi interrupt request bit goes to "1".
- (2) When the first effective edge is input after a count is started, an indeterminate value is transferred to the reload register. At this time, timer Bi interrupt request is not generated.

Real time port

- (1) Make sure timer Ai for real time port output is set for timer mode, and is set to have "no gate function" using the gate function select bit.
- (2) Before setting the real time port mode select bit to "1", temporarily turn off the timer Ai used and write its set value to the timer Ai register.

Serial I/O

- (1) In case IIC mode select bit (bit 0 of address 0377₁₆) is set to "1" with UART2. When setting up port direction P7 (address 03EF₁₆), write immediate values. If you use Read/Modify/Write instructions (BSET, BCLR, AND, OR, etc..) on the P7 direction register, the value of P7₁ direction register may change to unknown data.
- (2) MASK ROM version ONRY when IIC mode select bit (bit 0 of address 0377₁₆) and the internal/external select bit (bit 3 of address 0378₁₆) are both set to "1". The function of "SCL wait output bit 2 (bit 5 of address 0376₁₆)" does not work.
- (3) MASK ROM version ONRY when IIC mode select bit (bit 0 of address 0377₁₆) and the internal/external select bit (bit 3 of address 0378₁₆) are both set to "1". According to the datasheet, when IICM is set to "1", the port terminal is readable by the CPU even though "1" is assigned to P7₁ of the direction register. However, the CPU cannot read port P7₁ data if the P7₁ direction register is set to "1".

A-D Converter

- (1) Write to each bit (except bit 6) of A-D control register 0, to each bit of A-D control register 1, and to bit 0 of A-D control register 2 when A-D conversion is stopped (before a trigger occurs).
In particular, when the Vref connection bit is changed from "0" to "1", start A-D conversion after an elapse of 1 μ s or longer.
- (2) When changing A-D operation mode, select analog input pin again.
- (3) Using one-shot mode or single sweep mode
Read the correspondence A-D register after confirming A-D conversion is finished. (It is known by A-D conversion interrupt request bit.)
- (4) Using repeat mode, repeat sweep mode 0 or repeat sweep mode 1
Use the undivided main clock as the internal CPU clock.

Stop Mode and Wait Mode

- (1) When returning from stop mode by hardware reset, $\overline{\text{RESET}}$ pin must be set to "L" level until main clock oscillation is stabilized.
- (2) When switching to either wait mode or stop mode, instructions occupying four bytes either from the WAIT instruction or from the instruction that sets the every-clock stop bit to "1" within the instruction queue are prefetched and then the program stops. So put at least four NOPs in succession either to the WAIT instruction or to the instruction that sets the every-clock stop bit to "1".
- (3) When the MCU running in low-speed or low power dissipation mode, do not enter WAIT mode with peripheral function clock stop bit (CM02) set to "1".

Usage precaution

Interrupts

(1) Reading address 00000₁₆

- When maskable interrupt is occurred, CPU read the interrupt information (the interrupt number and interrupt request level) in the interrupt sequence.

The interrupt request bit of the certain interrupt written in address 00000₁₆ will then be set to "0".

Reading address 00000₁₆ by software sets enabled highest priority interrupt source request bit to "0".

Though the interrupt is generated, the interrupt routine may not be executed.

Do not read address 00000₁₆ by software.

(2) Setting the stack pointer

- The value of the stack pointer immediately after reset is initialized to 0000₁₆. Accepting an interrupt before setting a value in the stack pointer may become a factor of runaway. Be sure to set a value in the stack pointer before accepting an interrupt.

When using the $\overline{\text{NMI}}$ interrupt, initialize the stack point at the beginning of a program. Concerning the first instruction immediately after reset, generating any interrupts including the $\overline{\text{NMI}}$ interrupt is prohibited.

(3) The $\overline{\text{NMI}}$ interrupt

- The $\overline{\text{NMI}}$ interrupt can not be disabled. Be sure to connect $\overline{\text{NMI}}$ pin to Vcc via a pull-up resistor if unused.
- Do not get either into stop mode with the $\overline{\text{NMI}}$ pin set to "L".

(4) External interrupt

- When the polarity of the INT0 to INT5 pins is changed, the interrupt request bit is sometimes set to "1". After changing the polarity, set the interrupt request bit to "0".

Usage precaution

(5) Rewrite the interrupt control register

- To rewrite the interrupt control register, do so at a point that does not generate the interrupt request for that register. If there is possibility of the interrupt request occur, rewrite the interrupt control register after the interrupt is disabled. The program examples are described as follow:

Example 1:

```

INT_SWITCH1:
  FCLR    I           ; Disable interrupts.
  AND.B   #00h, 0055h ; Clear TA0IC int. priority level and int. request bit.
  NOP                               ; Four NOP instructions are required when using HOLD function.
  NOP
  FSET    I           ; Enable interrupts.

```

Example 2:

```

INT_SWITCH2:
  FCLR    I           ; Disable interrupts.
  AND.B   #00h, 0055h ; Clear TA0IC int. priority level and int. request bit.
  MOV.W   MEM, R0     ; Dummy read.
  FSET    I           ; Enable interrupts.

```

Example 3:

```

INT_SWITCH3:
  PUSHC   FLG         ; Push Flag register onto stack
  FCLR    I           ; Disable interrupts.
  AND.B   #00h, 0055h ; Clear TA0IC int. priority level and int. request bit.
  POPC    FLG         ; Enable interrupts.

```

- When a instruction to rewrite the interrupt control register is executed but the interrupt is disabled, the interrupt request bit is not set sometimes even if the interrupt request for that register has been generated. This will depend on the instruction. If this creates problems, use the below instructions to change the register.

Instructions : AND, OR, BCLR, BSET

Table 1.21.1. Absolute maximum ratings

Symbol	Parameter		Condition	Rated value	Unit
V _{cc}	Supply voltage		V _{cc} =AV _{cc}	– 0.3 to 6.5	V
AV _{cc}	Analog supply voltage		V _{cc} =AV _{cc}	– 0.3 to 6.5	V
V _i	Input voltage	RESET, V _{REF} , X _{IN} P0 ₀ to P0 ₇ , P1 ₀ to P1 ₇ , P2 ₀ to P2 ₇ , P3 ₀ to P3 ₅ , P4 ₁ , P4 ₂ , P4 ₆ , P4 ₇ , P5 ₀ to P5 ₃ , P5 ₆ , P5 ₇ , P6 ₀ to P6 ₃ , P7 ₂ to P7 ₇ , P8 ₀ to P8 ₂ , P8 ₄ , P8 ₆ , P9 ₀ to P9 ₆ , P10 ₀ to P10 ₃ , P11 ₀ to P11 ₇ , P12 ₀ to P12 ₅ , P13 ₀ , P13 ₁ (Mask ROM version CNVss)		– 0.3 to V _{cc} +0.3	V
		VL1		– 0.3 to VL2	
		VL2		VL1 to VL3	
		VL3		VL2 to 6.5	
		P7 ₀ , P7 ₁ , C1, C2 (flash memory version CNVss)		– 0.3 to 6.5	
V _o	Output voltage	P1 ₀ to P1 ₇ , P2 ₀ to P2 ₇ , P3 ₀ to P3 ₅ , P4 ₁ , P4 ₂ , P4 ₆ , P4 ₇ , P5 ₀ to P5 ₃ , P5 ₆ , P5 ₇ , P6 ₀ to P6 ₃ , P7 ₂ to P7 ₆ , P8 ₀ to P8 ₂ , P8 ₄ , P8 ₆ , P9 ₀ to P9 ₆ , P13 ₀ , P13 ₁ , X _{OUT}		– 0.3 to V _{cc} +0.3	V
		P0 ₀ to P0 ₇ , P10 ₀ to P10 ₃ , P11 ₀ to P11 ₇ , P12 ₀ to P12 ₅	When output port	– 0.3 to V _{cc}	
			When segment output	– 0.3 to VL3	
		P7 ₀ , P7 ₁		– 0.3 to 6.5	
P _d	Power dissipation		T _a = 25°C	300	mW
T _{opr}	Operating ambient temperature			– 20 to 85	°C
T _{stg}	Storage temperature			– 40 to 150	°C

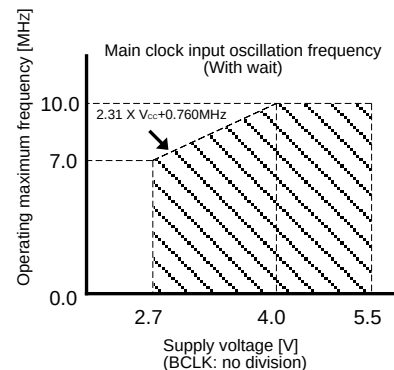
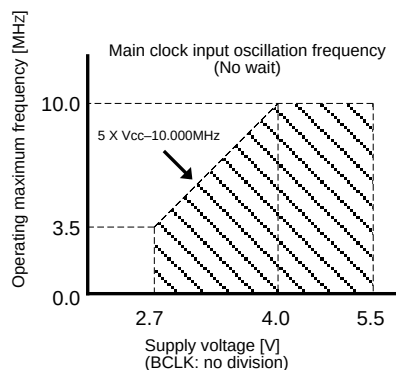
Table 1.21.2. Recommended operating conditions (referenced to $V_{CC} = 2.7V$ to $5.5V$ at $T_a = -20$ to $85^\circ C$ unless otherwise specified)

Symbol	Parameter			Standard			Unit	
				Min.	Typ.	Max.		
Vcc	Supply voltage			2.7	5.0	5.5	V	
AVcc	Analog supply voltage				Vcc		V	
Vss	Analog supply voltage				0		V	
AVss	Analog supply voltage				0		V	
VIH	HIGH input voltage	P00 to P07, P10 to P17, P20 to P27, P30 to P35, P41, P42, P46, P47, P50 to P53, P56, P57, P60 to P63, P72 to P77, P80 to P82, P84, P86, P90 to P96, P100 to P103, P110 to P117, P120 to P125, P130, P131, XIN, RESET, CNVss		0.8Vcc		Vcc	V	
		P70, P71		0.8Vcc		6.5		
VIL	LOW input voltage	P00 to P07, P10 to P17, P20 to P27, P30 to P35, P41, P42, P46, P47, P50 to P53, P56, P57, P60 to P63, P70 to P77, P80 to P82, P84, P86, P90 to P96, P100 to P103, P110 to P117, P120 to P125, P130, P131, XIN, RESET, CNVss		0		0.2Vcc	V	
IOH (peak)	HIGH peak output current (Note 2)	P00 to P07, P100 to P103, P110 to P117, P120 to P125				−0.5	mA	
		P10 to P17, P20 to P27, P30 to P35, P41, P42, P46, P47, P50 to P53, P56, P57, P60 to P63, P72 to P76, P80 to P82, P84, P86, P90 to P96, P130, P131,				−10.0		
IOH (avg)	HIGH average output current (Note 1)	P00 to P07, P100 to P103, P110 to P117, P120 to P125				−0.1	mA	
		P10 to P17, P20 to P27, P30 to P35, P41, P42, P46, P47, P50 to P53, P56, P57, P60 to P63, P72 to P76, P80 to P82, P84, P86, P90 to P96, P130, P131,				−5.0		
IOL (peak)	LOW peak output current (Note 2)	P00 to P07, P100 to P103, P110 to P117, P120 to P125				5.0	mA	
		P10 to P17, P20 to P27, P30 to P35, P41, P42, P46, P47, P50 to P53, P56, P57, P60 to P63, P70 to P76, P80 to P82, P84, P86, P90 to P96, P130, P131,				10.0		
IOL (avg)	LOW average output current (Note 1)	P00 to P07, P100 to P103, P110 to P117, P120 to P125				2.5	mA	
		P10 to P17, P20 to P27, P30 to P35, P41, P42, P46, P47, P50 to P53, P56, P57, P60 to P63, P70 to P76, P80 to P82, P84, P86, P90 to P96, P130, P131,				5.0		
f(XIN)	Main clock input oscillation frequency (Note 3)		No wait	Vcc=4.0V to 5.5V	0		10	MHz
				Vcc=2.7V to 4.0V	0		5 × Vcc −10.000	MHz
			With wait	Vcc=4.0V to 5.5V	0		10	MHz
				Vcc=2.7V to 4.0V	0		2.31 × Vcc +0.760	MHz
f(XCIN)	Subclock oscillation frequency				32.768	50	kHz	

Note 1: The mean output current is the mean value within 100ms.

Note 2: The total I_{OL} (peak) for ports P0, P1, P2, P30 to P35, P4, P5, P6, P70 to P76 and P122 to P127 must be 80mA max. The total I_{OH} (peak) for ports P0, P1, P2, P30 to P35, P4, P5, P6, P72 to P76 and P122 to P127 must be 80mA max. The total I_{OL} (peak) for ports P8, P9, P10, P11, P120, P121 and P130 to P132 must be 80mA max. The total I_{OH} (peak) for ports P8, P9, P10, P11, P120, P121 and P130 to P132 must be 80mA max.

Note 3: Relationship between main clock oscillation frequency and supply voltage.



Electric characteristics (VCC = 5V)

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

VCC = 5V

Table 1.21.3. Electrical characteristics (referenced to VCC = 5V, VSS = 0V at Ta = 25°C, f(XIN)=10MHz unless otherwise specified)

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
VOH	HIGH output voltage	P00 to P07, P100 to P103, P110 to P117, P120 to P125	IOH = -0.1mA	3.0			V
VOH	HIGH output voltage	P10 to P17, P20 to P27, P30 to P35, P41, P42, P46, P47, P50 to P53, P56, P57, P60 to P63, P72 to P76, P80 to P82, P84, P86, P90 to P96, P130, P131	IOH = -5mA	3.0			V
			IOH = -200μA	4.7			
VOH	HIGH output voltage	XOUT	HIGHPOWER	IOH = -1mA	3.0		V
			LOWPOWER	IOH = -0.5mA	3.0		
VOH	HIGH output voltage	XCOUT	HIGHPOWER	With no load applied	3.0		V
			LOWPOWER	With no load applied	1.6		
VOL	LOW output voltage	P00 to P07, P10 to P17, P20 to P27, P30 to P35, P41, P42, P46, P47, P50 to P53, P56, P57, P60 to P63, P70 to P76, P80 to P82, P84, P86, P90 to P96, P100 to P103, P110 to P117, P120 to P125, P130, P131	IOL = 5mA			2.0	V
			IOL = 200μA			0.45	
VOL	LOW output voltage	XOUT	HIGHPOWER	IOL = 1mA		2.0	V
			LOWPOWER	IOL = 0.5mA		2.0	
VOL	LOW output voltage	XCOUT	HIGHPOWER	With no load applied	0		V
			LOWPOWER	With no load applied	0		
VT+ - VT-	Hysteresis	TA0IN, TA3IN, TA4IN, TB0IN to TB3IN, INT0 to INT5, ADTRG, CTS0, CLK0, NMI, TA3OUT, TA4OUT, TA7OUT, K10 to K15 (Note), K16 to K19		0.2		0.8	V
VT+ - VT-	Hysteresis	RESET		0.2		1.8	V
IiH	HIGH input current	P00 to P07, P10 to P17, P20 to P27, P30 to P35, P41, P42, P46, P47, P50 to P53, P56, P57, P60 to P63, P70 to P77, P80 to P82, P84, P86, P90 to P96, P100 to P103, P110 to P117, P120 to P125, P130, P131, XIN, RESET, CNVSS	Vi = 5V			5.0	μA
IiL	LOW input current	P00 to P07, P10 to P17, P20 to P27, P30 to P35, P41, P42, P46, P47, P50 to P53, P56, P57, P60 to P63, P70 to P77, P80 to P82, P84, P86, P90 to P96, P100 to P103, P110 to P117, P120 to P125, P130, P131, XIN, RESET, CNVSS	Vi = 0V			-5.0	μA
RPULLUP	Pull-up resistance	P00 to P07, P10 to P17, P20 to P27, P30 to P35, P41, P42, P46, P47, P50 to P53, P56, P57, P60 to P63, P72 to P76, P80 to P82, P84, P86, P90 to P96, P100 to P103, P110 to P117, P120 to P125, P130, P131	Vi = 0V	30.0	50.0	167.0	k
RfXIN	Feedback resistance	XIN			1.0		M
RfXCIN	Feedback resistance	XCIN			6.0		M
VRAM	RAM retention voltage		When clock is stopped	2.0			V

Note : Has no effect during intermittent pullup operation.

VCC = 5V

Table 1.21.4. Electrical characteristics (referenced to VCC = 5V, VSS = 0V at Ta = 25°C, f(XIN)=10MHz unless otherwise specified)

Symbol	Parameter		Measuring condition		Standard			Unit
					Min.	Typ.	Max.	
Icc	Power supply current	I/o pin is no load applied		f(XIN)=10MHz Square wave, no division		19.0	38.0	mA
			Mask ROM version	f(XCIN)=32kHz Square wave		90.0		μA
			Flash memory version	f(XCIN)=32kHz Square wave		200.0		μA
				f(XCIN)=32kHz When a WAIT instruction is executed		4.0		μA
				When clock is stopped Ta=25 °C			1.0	μA
				When clock is stopped Ta=85 °C			20.0	
VL1	Supply voltage (VL1)		When voltage multiplier used		1.3	1.7	2.1	V
IL1	Power supply current (VL1)		VL1=1.7V,f(LCDCK)=200Hz			3.0	6.0	μA

Table 1.21.5. A-D conversion characteristics (referenced to VCC = AVCC = VREF = 5V, VSS = AVSS = 0V at Ta = 25°C, f(XIN) = 10MHz unless otherwise specified)

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
—	Resolution		VREF = VCC			10	Bits
—	Absolute accuracy	Sample & hold function not available	VREF = VCC = 5V			±3	LSB
		Sample & hold function available(10bit)	VREF = VCC = 5V			±3	LSB
		Sample & hold function available(8bit)	VREF = VCC = 5V			±2	LSB
RLADDER	Ladder resistance		VREF = VCC	10		40	k
tCONV	Conversion time(10bit)			3.3			μs
tCONV	Conversion time(8bit)			2.8			μs
tsAMP	Sampling time			0.3			μs
VREF	Reference voltage			2		VCC	V
VIA	Analog input voltage			0		VREF	V

Table 1.21.6. D-A conversion characteristics (referenced to VCC = AVCC = VREF = 5V, VSS = AVSS = 0V at Ta = 25°C, f(XIN) = 10MHz unless otherwise specified)

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
—	Resolution					8	Bits
—	Absolute accuracy					1.0	%
tsu	Setup time					3	μs
Ro	Output resistance			4	10	20	k
IvREF	Reference power supply input current		(Note)			1.5	mA

Note: This applies when using one D-A converter, with the D-A register for the unused D-A converter set to "0016".

The A-D converter's ladder resistance is not included.

Also, when the Vref is unconnected at the A-D control register, IvREF is sent.

Timing (VCC = 5V)

VCC = 5V

Timing requirements (referenced to VCC = 5V, VSS = 0V at Ta = 25°C unless otherwise specified)

Table 1.21.7. External clock input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc	External clock input cycle time	100		ns
tw(H)	External clock input HIGH pulse width	40		ns
tw(L)	External clock input LOW pulse width	40		ns
tr	External clock rise time		15	ns
tf	External clock fall time		15	ns

Table 1.21.8. Timer A input (counter input in event counter mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	100		ns
tw(TAH)	TAiIN input HIGH pulse width	40		ns
tw(TAL)	TAiIN input LOW pulse width	40		ns

Table 1.21.9. Timer A input (gating input in timer mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	400		ns
tw(TAH)	TAiIN input HIGH pulse width	200		ns
tw(TAL)	TAiIN input LOW pulse width	200		ns

Table 1.21.10. Timer A input (external trigger input in one-shot timer mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	200		ns
tw(TAH)	TAiIN input HIGH pulse width	100		ns
tw(TAL)	TAiIN input LOW pulse width	100		ns

Table 1.21.11. Timer A input (external trigger input in pulse width modulation mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tw(TAH)	TAiIN input HIGH pulse width	100		ns
tw(TAL)	TAiIN input LOW pulse width	100		ns

Table 1.21.12. Timer A input (up/down input in event counter mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(UP)	TAiOUT input cycle time	2000		ns
tw(UPH)	TAiOUT input HIGH pulse width	1000		ns
tw(UPL)	TAiOUT input LOW pulse width	1000		ns
tsu(UP-TIN)	TAiOUT input setup time	400		ns
th(TIN-UP)	TAiOUT input hold time	400		ns

Timing (VCC = 5V)

VCC = 5V

Timing requirements (referenced to VCC = 5V, VSS = 0V at Ta = 25°C unless otherwise specified)

Table 1.21.13. Timer B input (counter input in event counter mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (TB)	TBiIN input cycle time (counted on one edge)	100		ns
t _w (TBH)	TBiIN input HIGH pulse width (counted on one edge)	40		ns
t _w (TBL)	TBiIN input LOW pulse width (counted on one edge)	40		ns
t _c (TB)	TBiIN input cycle time (counted on both edges)	200		ns
t _w (TBH)	TBiIN input HIGH pulse width (counted on both edges)	80		ns
t _w (TBL)	TBiIN input LOW pulse width (counted on both edges)	80		ns

Table 1.21.14. Timer B input (pulse period measurement mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (TB)	TBiIN input cycle time	400		ns
t _w (TBH)	TBiIN input HIGH pulse width	200		ns
t _w (TBL)	TBiIN input LOW pulse width	200		ns

Table 1.21.15. Timer B input (pulse width measurement mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (TB)	TBiIN input cycle time	400		ns
t _w (TBH)	TBiIN input HIGH pulse width	200		ns
t _w (TBL)	TBiIN input LOW pulse width	200		ns

Table 1.21.16. A-D trigger input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (AD)	ADTRG input cycle time (trigger able minimum)	1000		ns
t _w (ADL)	ADTRG input LOW pulse width	125		ns

Table 1.21.17. Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (CK)	CLKi input cycle time	200		ns
t _w (CKH)	CLKi input HIGH pulse width	100		ns
t _w (CKL)	CLKi input LOW pulse width	100		ns
t _d (C-Q)	TxDi output delay time		80	ns
t _h (C-Q)	TxDi hold time	0		ns
t _{su} (D-C)	RxDi input setup time	30		ns
t _h (C-D)	RxDi input hold time	90		ns

Table 1.21.18. External interrupt INTi inputs

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _w (INH)	INTi input HIGH pulse width	250		ns
t _w (INL)	INTi input LOW pulse width	250		ns

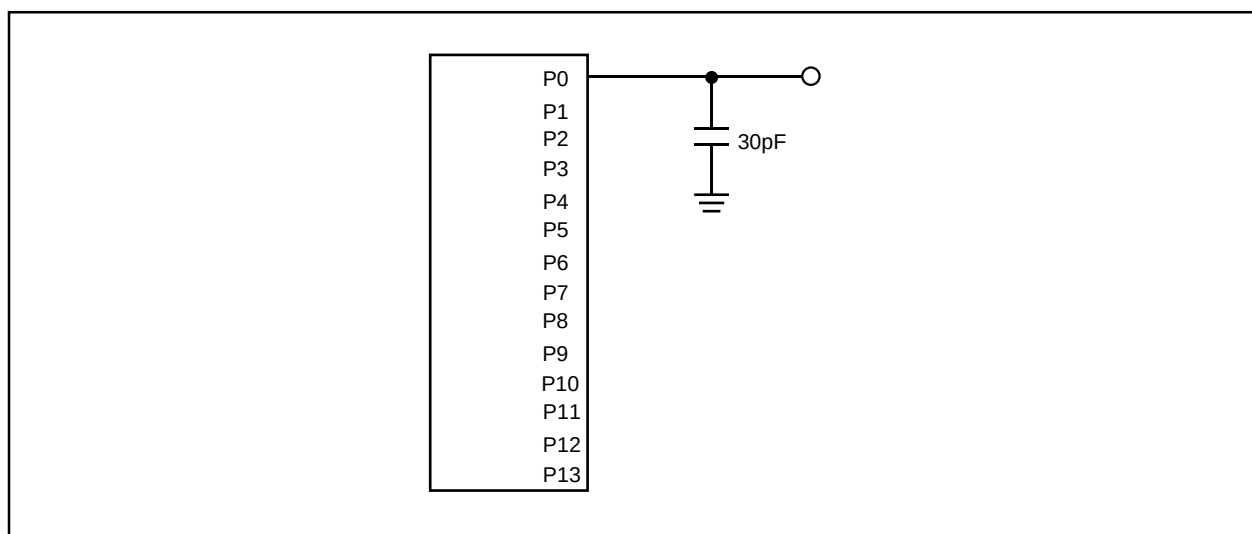
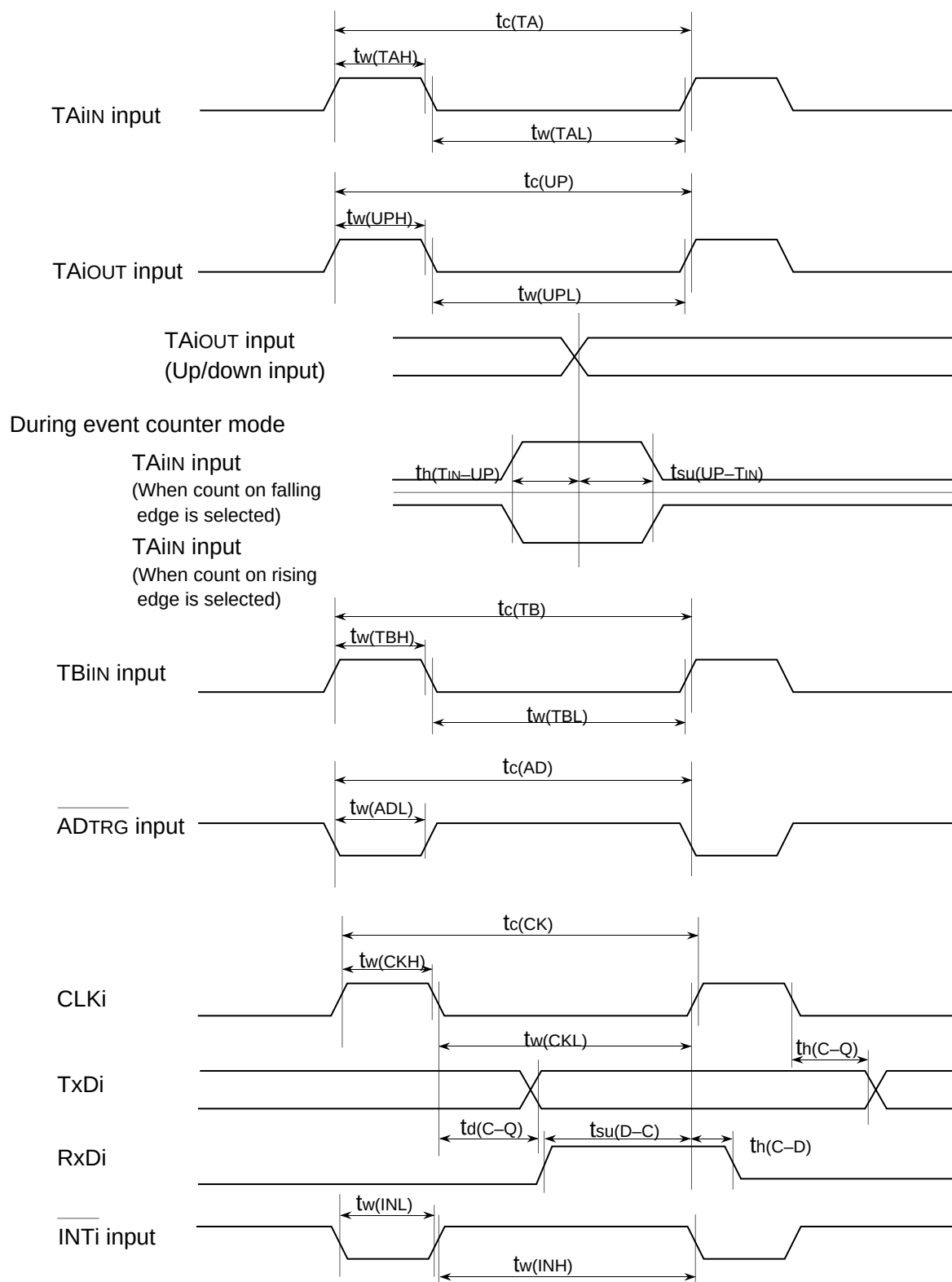


Figure 1.21.1. Port P0 to P13 measurement circuit

Timing ($V_{CC} = 5V$) $V_{CC} = 5V$ 

VCC = 3V

Table 1.21.19. Electrical characteristics (referenced to VCC = 3V, VSS = 0V at Ta = 25°C, f(XIN) = 7MHz, with wait)

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
VOH	HIGH output voltage	P00 to P07, P100 to P103, P110 to P117, P120 to P125	IOH = -20μA	2.0			V
VOH	HIGH output voltage	P10 to P17, P20 to P27, P30 to P35, P41, P42, P46, P47, P50 to P53, P56, P57, P60 to P63, P72 to P76, P80 to P82, P84, P86, P90 to P96, P130, P131	IOH = -1mA	2.5			V
VOH	HIGH output voltage	XOUT	HIGHPOWER	IOH = -0.1mA	2.5		V
			LOWPOWER	IOH = -50μA	2.5		
VOH	HIGH output voltage	XCOUT	HIGHPOWER	With no load applied	3.0		V
			LOWPOWER	With no load applied	1.6		
VOL	LOW output voltage	P00 to P07, P10 to P17, P20 to P27, P30 to P35, P41, P42, P46, P47, P50 to P53, P56, P57, P60 to P63, P70 to P76, P80 to P82, P84, P86, P90 to P96, P100 to P103, P110 to P117, P120 to P125, P130, P131	IOL = 1mA			0.5	V
VOL	LOW output voltage	XOUT	HIGHPOWER	IOH = 0.1mA		0.5	V
			LOWPOWER	IOH = 50μA		0.5	
VOL	LOW output voltage	XCOUT	HIGHPOWER	With no load applied	0		V
			LOWPOWER	With no load applied	0		
VT+-VT-	Hysteresis	TA0IN, TA3IN, TA4IN, TB0IN to TB3IN, INT0 to INT5, ADTRG, CTS0, CLK0, NMI, TA3OUT, TA4OUT, TA7OUT, K10 to K15 (Note), K16 to K19		0.2		0.8	V
VT+-VT-	Hysteresis	RESET		0.2		1.8	V
IiH	HIGH input current	P00 to P07, P10 to P17, P20 to P27, P30 to P35, P41, P42, P46, P47, P50 to P53, P56, P57, P60 to P63, P70 to P77, P80 to P82, P84, P86, P90 to P96, P100 to P103, P110 to P117, P120 to P125, P130, P131, XIN, RESET, CNVSS	Vi = 3V			4.0	μA
IiL	LOW input current	P00 to P07, P10 to P17, P20 to P27, P30 to P35, P41, P42, P46, P47, P50 to P53, P56, P57, P60 to P63, P70 to P77, P80 to P82, P84, P86, P90 to P96, P100 to P103, P110 to P117, P120 to P125, P130, P131, XIN, RESET, CNVSS	Vi = 0V			-4.0	μA
RPULLUP	Pull-up resistance	P00 to P07, P10 to P17, P20 to P27, P30 to P35, P41, P42, P46, P47, P50 to P53, P56, P57, P60 to P63, P72 to P76, P80 to P82, P84, P86, P90 to P96, P100 to P103, P110 to P117, P120 to P125, P130, P131	Vi = 0V	66.0	120.0	500.0	k
RXIN	Feedback resistance	XIN			3.0		M
RXCIN	Feedback resistance	XCIN			10.0		M
VRAM	RAM retention voltage		When clock is stopped	2.0			V

Note : Has no effect during intermittent pullup operation.

Electric characteristics ($V_{CC} = 3V$)

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 $V_{CC} = 3V$ **Table 1.21.20. Electrical characteristics (referenced to $V_{CC} = 3V$, $V_{SS} = 0V$ at $T_a = 25^\circ C$, $f(X_{IN}) = 7MHz$, with wait)**

Symbol	Parameter		Measuring condition		Standard			Unit
					Min.	Typ.	Max.	
Icc	Power supply current	I/o pin is no load applied		f(XIN)=7MHz Square wave, no division		6.0	15.0	mA
			Mask ROM version	f(XCIN)=32kHz Square wave		40.0		μA
			Flash memory version	f(XCIN)=32kHz Square wave		150.0		μA
				f(XCIN)=32kHz When a WAIT instruction is executed Oscillation capacity High (Note)		2.8		μA
				f(XCIN)=32kHz When a WAIT instruction is executed Oscillation capacity Low (Note)		0.9		μA
				When clock is stopped Ta=25 °C			1.0	μA
				When clock is stopped Ta=85 °C			20.0	
VL1	Supply voltage (VL1)		When voltage multiplier used		1.3	1.7	2.1	V
IL1	Power supply current (VL1)		VL1=1.7V,f(LCDCK)=200Hz			3.0	6.0	μA

Note: With one timer operated using fc32.

Table 1.21.21. A-D conversion characteristics (referenced to $V_{CC} = AV_{CC} = V_{REF} = 3V$, $V_{SS} = AV_{SS} = 0V$ at $T_a = 25^\circ C$, $f(X_{IN}) = 7MHz$, with wait unless otherwise specified)

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
—	Resolution		$V_{REF} = V_{CC}$			10	Bits
—	Absolute accuracy	Sample & hold function not available(8bit)	$V_{REF} = V_{CC} = 3V$, $\phi_{AD} = f_{AD}/2$			± 2	LSB
R _{LADDER}	Ladder resistance		$V_{REF} = V_{CC}$	10		40	k
t _{CONV}	Conversion time(8bit)			14.0			μs
V _{REF}	Reference voltage			2.7		V _{CC}	V
V _{IA}	Analog input voltage			0		V _{REF}	V

Table 1.21.22. D-A conversion characteristics (referenced to $V_{CC} = AV_{CC} = V_{REF} = 3V$, $V_{SS} = AV_{SS} = 0V$, at $T_a = 25^\circ C$, $f(X_{IN}) = 7MHz$ unless otherwise specified)

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
—	Resolution					8	Bits
—	Absolute accuracy					1.0	%
t _{su}	Setup time					3	μs
R _o	Output resistance			4	10	20	k
I _{VREF}	Reference power supply input current		(Note)			1.0	mA

Note : This applies when using one D-A converter, with the D-A register for the unused D-A converter set to "0016". The A-D converter's ladder resistance is not included.

Also, when the V_{ref} is unconnected at the A-D control register, I_{VREF} is sent.

$V_{CC} = 3V$ Timing requirements (referenced to $V_{CC} = 3V$, $V_{SS} = 0V$ at $T_a = 25^\circ C$ unless otherwise specified)

Table 1.21.23. External clock input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External clock input cycle time	143		ns
$t_{w(H)}$	External clock input HIGH pulse width	60		ns
$t_{w(L)}$	External clock input LOW pulse width	60		ns
t_r	External clock rise time		18	ns
t_f	External clock fall time		18	ns

Table 1.21.24. Timer A input (counter input in event counter mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c(TA)$	TA _{IN} input cycle time	150		ns
$t_{w(TAH)}$	TA _{IN} input HIGH pulse width	60		ns
$t_{w(TAL)}$	TA _{IN} input LOW pulse width	60		ns

Table 1.21.25. Timer A input (gating input in timer mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c(TA)$	TA _{IN} input cycle time	600		ns
$t_{w(TAH)}$	TA _{IN} input HIGH pulse width	300		ns
$t_{w(TAL)}$	TA _{IN} input LOW pulse width	300		ns

Table 1.21.26. Timer A input (external trigger input in one-shot timer mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c(TA)$	TA _{IN} input cycle time	300		ns
$t_{w(TAH)}$	TA _{IN} input HIGH pulse width	150		ns
$t_{w(TAL)}$	TA _{IN} input LOW pulse width	150		ns

Table 1.21.27. Timer A input (external trigger input in pulse width modulation mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TA _{IN} input HIGH pulse width	150		ns
$t_{w(TAL)}$	TA _{IN} input LOW pulse width	150		ns

Table 1.21.28. Timer A input (up/down input in event counter mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c(UP)$	TA _{IOUT} input cycle time	3000		ns
$t_{w(UPH)}$	TA _{IOUT} input HIGH pulse width	1500		ns
$t_{w(UPL)}$	TA _{IOUT} input LOW pulse width	1500		ns
$t_{su}(UP-TIN)$	TA _{IOUT} input setup time	600		ns
$t_h(TIN-UP)$	TA _{IOUT} input hold time	600		ns

Timing ($V_{CC} = 3V$) $V_{CC} = 3V$ Timing requirements (referenced to $V_{CC} = 3V$, $V_{SS} = 0V$ at $T_a = 25^\circ C$ unless otherwise specified)

Table 1.21.29. Timer B input (counter input in event counter mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiN input cycle time (counted on one edge)	150		ns
$t_{w(TBH)}$	TBiN input HIGH pulse width (counted on one edge)	60		ns
$t_{w(TBL)}$	TBiN input LOW pulse width (counted on one edge)	60		ns
$t_{c(TB)}$	TBiN input cycle time (counted on both edges)	300		ns
$t_{w(TBH)}$	TBiN input HIGH pulse width (counted on both edges)	160		ns
$t_{w(TBL)}$	TBiN input LOW pulse width (counted on both edges)	160		ns

Table 1.21.30. Timer B input (pulse period measurement mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiN input cycle time	600		ns
$t_{w(TBH)}$	TBiN input HIGH pulse width	300		ns
$t_{w(TBL)}$	TBiN input LOW pulse width	300		ns

Table 1.21.31. Timer B input (pulse width measurement mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiN input cycle time	600		ns
$t_{w(TBH)}$	TBiN input HIGH pulse width	300		ns
$t_{w(TBL)}$	TBiN input LOW pulse width	300		ns

Table 1.21.32. A-D trigger input

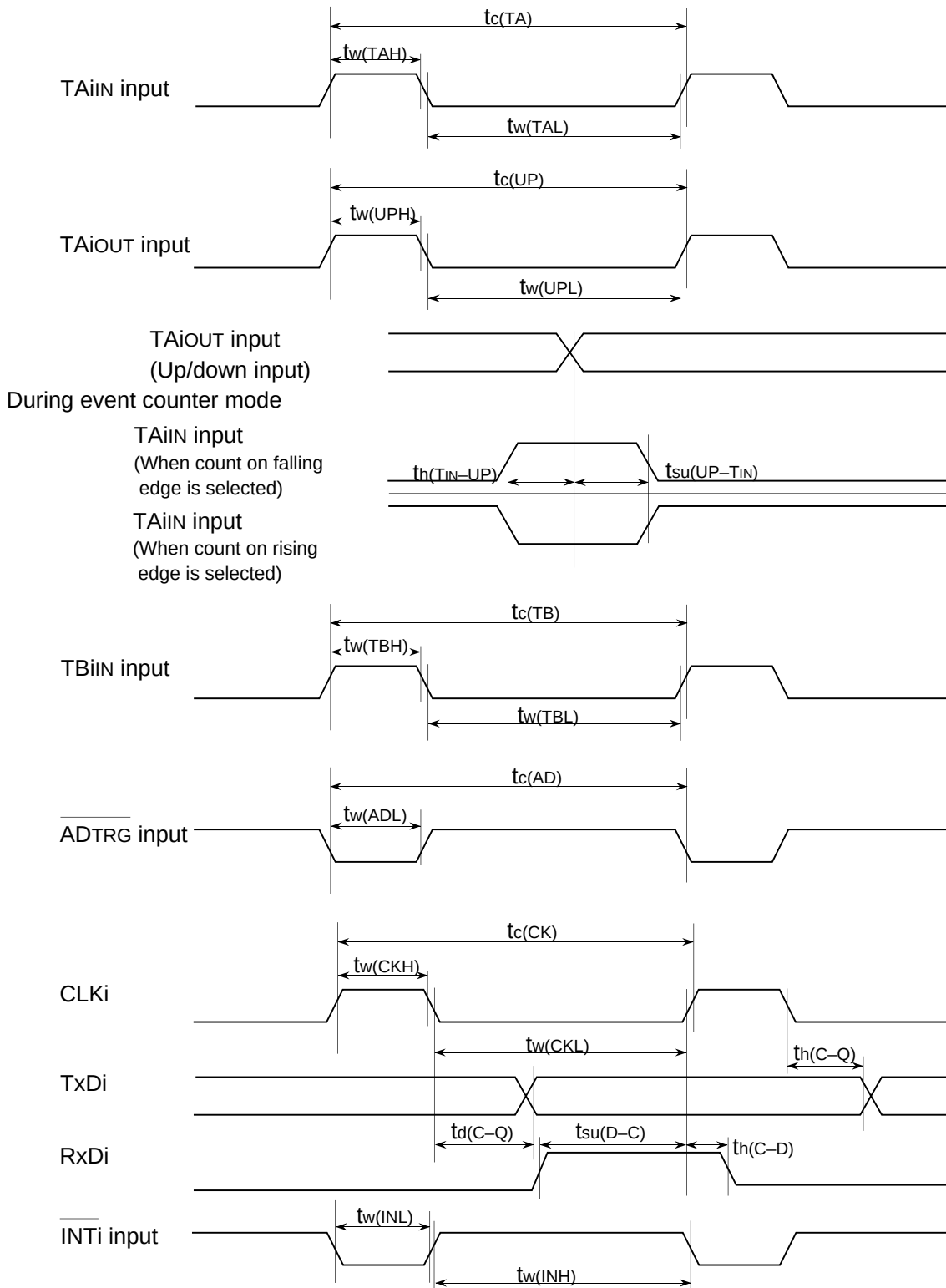
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(AD)}$	ADTRG input cycle time (trigger able minimum)	1500		ns
$t_{w(ADL)}$	ADTRG input LOW pulse width	200		ns

Table 1.21.33. Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300		ns
$t_{w(CKH)}$	CLKi input HIGH pulse width	150		ns
$t_{w(CKL)}$	CLKi input LOW pulse width	150		ns
$t_d(C-Q)$	TxDi output delay time		160	ns
$t_h(C-Q)$	TxDi hold time	0		ns
$t_{su}(D-C)$	RxDi input setup time	50		ns
$t_h(C-D)$	RxDi input hold time	90		ns

Table 1.21.34. External interrupt $\overline{INT_i}$ inputs

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INT_i}$ input HIGH pulse width	380		ns
$t_{w(INL)}$	$\overline{INT_i}$ input LOW pulse width	380		ns

Timing ($V_{CC} = 3V$) $V_{CC} = 3V$ 

Usage precaution against the differences between M30220 Group and M30221 Group

Differences between M30220 Group and M30221 Group

Items		M30220 Group			M30221 Group			
Internal Memory	ROM (Byte)	64K ^{***}	96K	128K ^{**}	24K	32K ^{***}	64K ^{***}	128K ^{**}
	RAM (Byte)	4K ^{***}	6K	10K ^{**}	1.5K	2K ^{***}	4K ^{***}	10K ^{**}
I/O Ports	Input only / Output only	Input only : 1 / Output only : 16 (shared with LCD outputs)			Input only : 1 / Output only : 14 (shared with LCD outputs)			
	CMOS I/O	102 (32 lines are shared with LCD outputs)			81 (26 lines are shared with LCD outputs)			
	N-channel open-drain				2			
DMAC (channels)					2			
16-bit timers					8+6			
CRC Operation Circuit					—			
Serial I/O	Clock Sync. / UART	3			2			
	Clock Synchronous				—			
	UART only				—			
A-D Converter (resolution × channels)		10bits×8			10bits×7			
D-A Converter (resolution × channels)		8bits×3			8bits×2			
External Interrupts (source)					8			
Watchdog Timer					Available			
LCD Controller / Driver	Segment (lines)	48			40			
	Common (lines)				4			
	Charge pump				Available			
Real Time Output Ports (bits × ports)		8×4			8×3, 6×1			
Key-on Wake up (lines)					Max.20 (16 lines have Intermittent pull-up operation)			
Sub Clock Generating Circuit					Available			
Packages		144-pin TQFP (144PFB-A) 144-pin LQFP (144P6Q-A)			120-pin LQFP (120P6R-A)			
Power Source Voltage (V)					2.7 to 5.5 (7MHz with 1wait)、4.0 to 5.5 (10MHz)			
Operating Temperature Range (°C)					-20 to 85、-40 to 85			
Minimum Instruction Execution Time (ns)					100 (10MHz)			
Number of Basic Instructions					91			

★★ : Under development ★★★ : Under planning (April, 2001)

Deleted pins from M30220 Group

Port	Deleted pin name
P0	—
P1	—
P2	—
P3	—
P4	P40/TA0OUT、P43/TA1IN、P44/TA2OUT、P45/TA2IN
P5	P54/TB4IN、P55/TB5IN
P6	P64/CTS1/RTS1/CLKS1、P65/CLK1、P66/RxD1、P67/TxD1
P7	—
P8	P83/TA5IN、P85/TA6IN、P87/TA7IN
P9	P97/AN7
P10	P104/SEG20、P105/SEG21、P106/SEG22、P107/SEG23
P11	—
P12	P126/SEG38、P127/SEG39
P13	P132/DA2
others	SEG0、SEG1、VSS(1 pin)

Usage precaution against timer A

Mode	Function	Not available timer Ai
Timer mode	Pulse output	Timer A0 and A2 are not available.
	Gate input	Timer A1 , A2 , and A5 to A7 are not available.
Event counter mode	Pulse output	Timer A0 and A2 are not available.
	Count source input	Timer A1 , A2 , and A5 to A7 are not available.
	Up / down count select input	Timer A0 and A2 are not available.
	Two-phase pulse input	Timer A2 and A7 are not available.(Note 1)
One-shot timer mode	Pulse output	Timer A0 and A2 are not available.
	Trigger input	Timer A1 , A2 , and A5 to A7 are not available.
Pulse width modulation mode		Timer A0 and A2 are not available.
	Trigger input	Timer A1 and A5 to A7 are not available.

Note 1. Timer A3 and A4 are available.

Usage precaution against timer B

Mode	Function	Not available timer Bi
Event counter mode	Count source input	Timer B4 and B5 are not available.
Pulse period / pulse width measurement mode		Timer B4 and B5 are not available.

Usage precaution against real time port outputs

- (1) Pins P126 and P127 are deleted.

Usage precaution against serial I/O

- (1) UART1 is not available.

Usage precaution against LCD controller / driver

- (1) Pins SEG0 , SEG1 , SEG20 to SEG23 , SEG38 and SEG39 are deleted.
- (2) Addresses of the designated RAM for the LCD display 010016 , 010A16 , 010B16 and 011316 are reserved area.
- (3) Bit 5 of the segment output enable register (address 012216) is reserved bit. Must always be clear to "0".

Usage precaution against A-D converter

- (1) AN7 pin is deleted.
- (2) Do not set the analog input pin select bit (bit 0 to 2 at address 03D616) to "111" in one-shot mode and in repeat mode.
- (3) When the A-D sweep pin select bit (bit 0, 1 at address 03D716) is set to "11" in single sweep mode, the interrupt request generation timing of the A-D conversion is the A-D conversion time of all 8 pins.
- (4) The sweep time is the A-D conversion time of all 8 pins in repeat sweep mode 1 and when the A-D sweep pin select bit (bit 0, 1 at address 03D716) is set to "11" in repeat sweep mode 0.

Usage precaution against D-A converter

- (1) DA2 pin is deleted.
- (2) Bit 2 of the D-A control register (address 03DC16) is reserved bit. Must always be clear to "0".
- (3) Address 03DE16 must always be clear to "0016".

Usage precaution against programmable I/O

- (1) Reserved bits of the port Pi direction register and the port Pi register

Register	Bit	Register	Bit
PD0、P0	—	PD7、P7	—
PD1、P1	—	PD8、P8	b3、b5、b7(Note 1)
PD2、P2	—	PD9、P9	b7(Note 1)
PD3、P3	—	PD10、P10	b4~b7(Note 1)
PD4、P4	b0、b3~b5(Note 1)	PD11、P11	—
PD5、P5	b4、b5(Note 1)	PD12、P12	b6、b7(Note 1)
PD6、P6	b4~b7(Note 1)	PD13、P13	b2(Note 1)

Note 1. These are reserved bits. Must always be clear to "0".

- (2) Reserved bits of the pull-up control register
 Bit 5 of the pull-up control register 1 (address 03FD16) and bit 5 of the pull-up control register 2 (address 03FE16) are reserved bits. Must always be clear to "0".

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