NTD5802N

Power MOSFET
40 V, Single N−Channel, 101 A DPAK

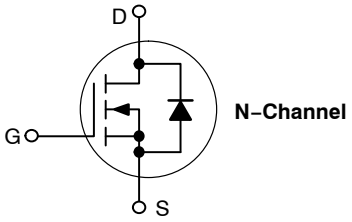
ON Semiconductor®

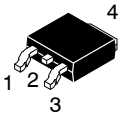
http://onsemi.com

Features
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- MSL 1/260°C
- AEC Q101 Qualified
- 100% Avalanche Tested
- These are Pb−Free Devices

Applications
- CPU Power Delivery
- DC−DC Converters
- Motor Driver

$V_{(BR)DSS}$	$R_{DS(on)}$	I_D
40 V	4.4 mΩ @ 10 V	101 A
	7.8 mΩ @ 5.0 V	50 A





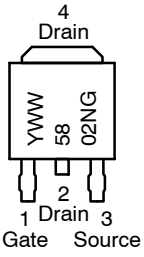
CASE 369C
DPAK
(Bent Lead)
STYLE 2

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	40	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current ($R_{\theta JC}$) (Note 1)	Steady State	T_C = 25°C	I_D	101	A
		T_C = 85°C		78	
Power Dissipation ($R_{\theta JC}$) (Note 1)		T_C = 25°C	P_D	93.75	W
Continuous Drain Current ($R_{\theta JA}$) (Note 1)		T_A = 25°C	I_D	16.4	A
		T_A = 85°C		12.7	
Power Dissipation ($R_{\theta JA}$) (Note 1)		T_A = 25°C	P_D	2.5	W
Pulsed Drain Current	t_p=10μs	T_A = 25°C	I_{DM}	300	A
Current Limited by Package		T_A = 25°C	$I_{DmaxPkg}$	45	A
Operating Junction and Storage Temperature			T_J, T_{stg}	−55 to 175	°C
Source Current (Body Diode)			I_S	50	A
Drain to Source dV/dt			dV/dt	6.0	V/ns
Single Pulse Drain−to−Source Avalanche Energy (V_{DD} = 32 V, V_{GS} = 10 V, L = 0.3 mH, $I_{L(pk)}$ = 40 A, R_G = 25 Ω)			E_{AS}	240	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

MARKING DIAGRAMS & PIN ASSIGNMENT



Y = Year
WW = Work Week
5802N = Device Code
G = Pb−Free Package

ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case (Drain)	$R_{\theta JC}$	1.6	°C/W
Junction−to−Ambient − Steady State (Note 1)	$R_{\theta JA}$	60	
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	105	

1. Surface−mounted on FR4 board using 1 in sq pad size, 1 oz Cu.
2. Surface−mounted on FR4 board using the minimum recommended pad size.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10 μA		40			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				40		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 40 V	T_J = 25°C			1.0	μA
			T_J = 150°C			50	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.5		3.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				−7.4		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 50 A			3.6	4.4	mΩ
		V_{GS} = 5.0 V, I_D = 50 A			6.5	7.8	
Forward Transconductance	gFS	V_{DS} = 15 V, I_D = 15 A			16.8		S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 12 V			5300		pF
Output Capacitance	C_{oss}				850		
Reverse Transfer Capacitance	C_{rss}				550		
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 25 V			5025		pF
Output Capacitance	C_{oss}				580		
Reverse Transfer Capacitance	C_{rss}				400		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 15 V, I_D = 50 A			75	100	nC
Threshold Gate Charge	$Q_{G(TH)}$				6.0		
Gate−to−Source Charge	Q_{GS}				18		
Gate−to−Drain Charge	Q_{GD}				15		
SWITCHING CHARACTERISTICS (Note 4)							
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 20 V, I_D = 50 A, R_G = 2.0 Ω			14		ns
Rise Time	t_r				52		
Turn−Off Delay Time	$t_{d(off)}$				39		
Fall Time	t_f				8.5		

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 50 A	T_J = 25°C		0.9	1.2	V
		V_{GS} = 0 V, I_S = 20 A	T_J = 25°C		0.8	1.0	
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dIs/dt = 100 A/μs, I_S = 50 A			25		ns
Charge Time	ta				15		
Discharge Time	tb				10		
Reverse Recovery Charge	Q_{RR}				15		nC

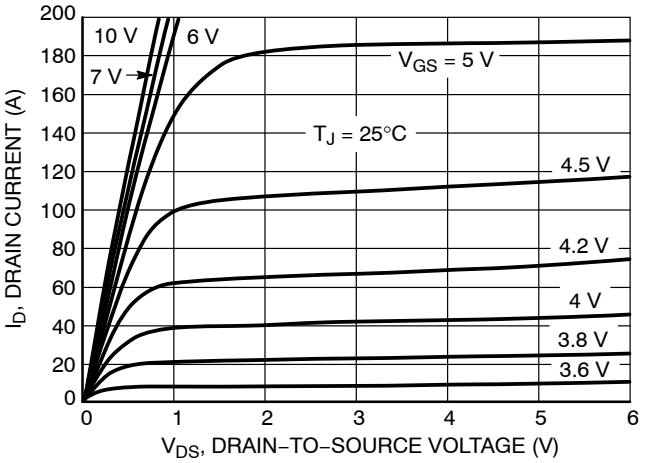


Figure 1. On−Region Characteristics

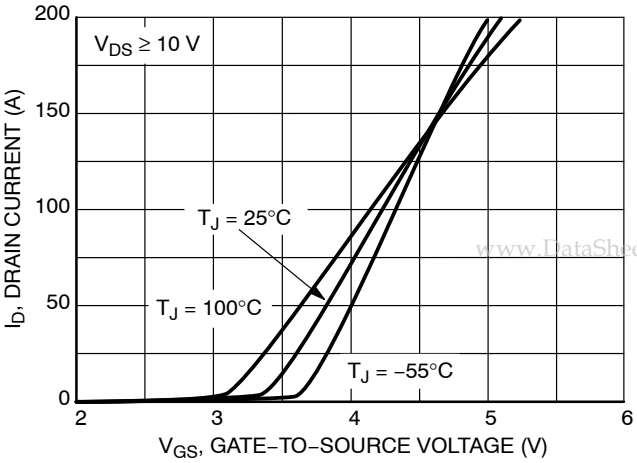


Figure 2. Transfer Characteristics

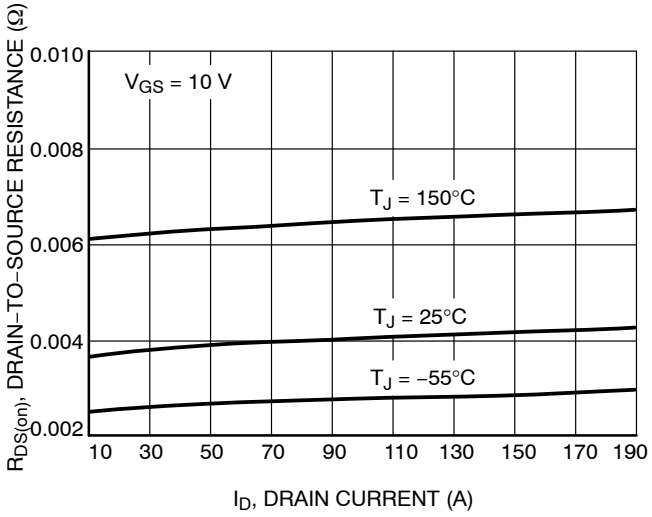


Figure 3. On−Resistance vs. Drain Current

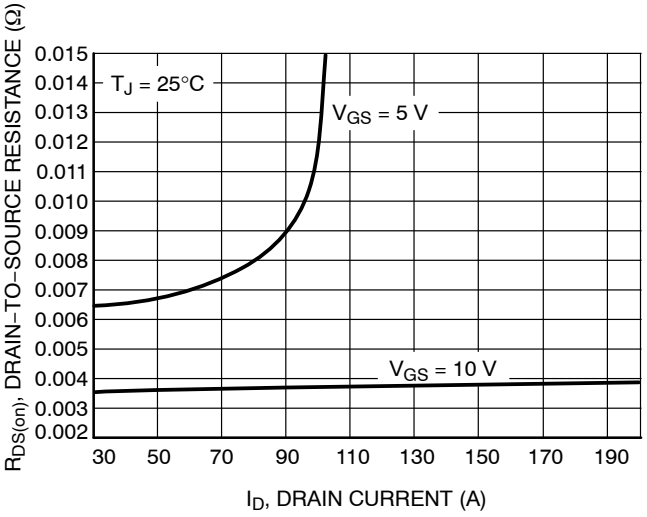


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

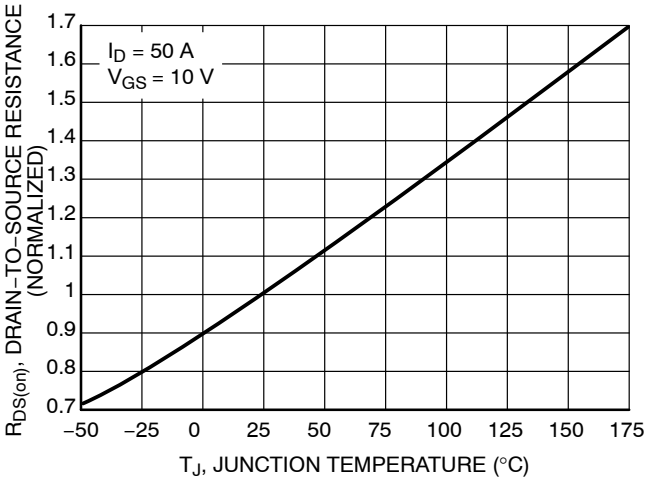


Figure 5. On−Resistance Variation with Temperature

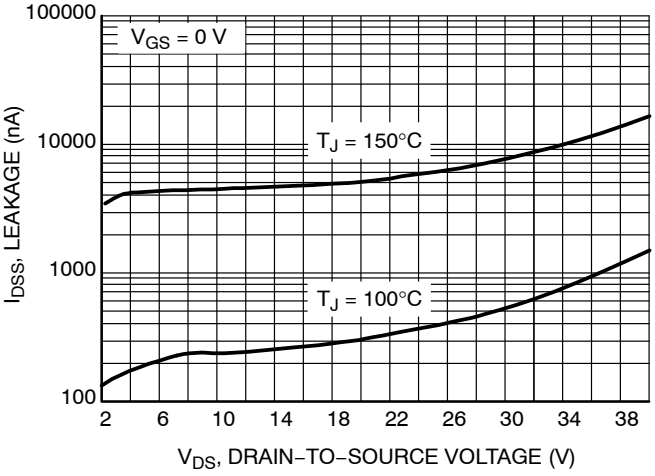


Figure 6. Drain−to−Source Leakage Current vs. Voltage

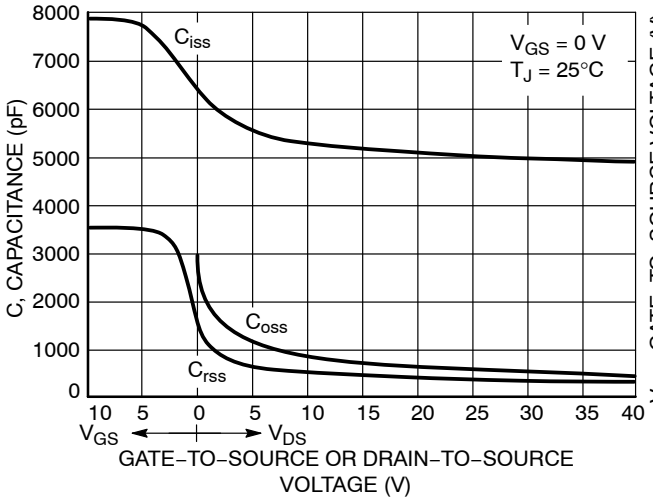


Figure 7. Capacitance Variation

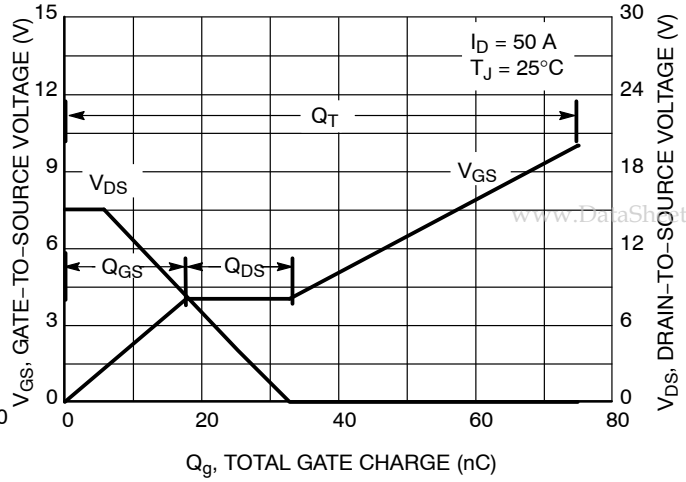


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

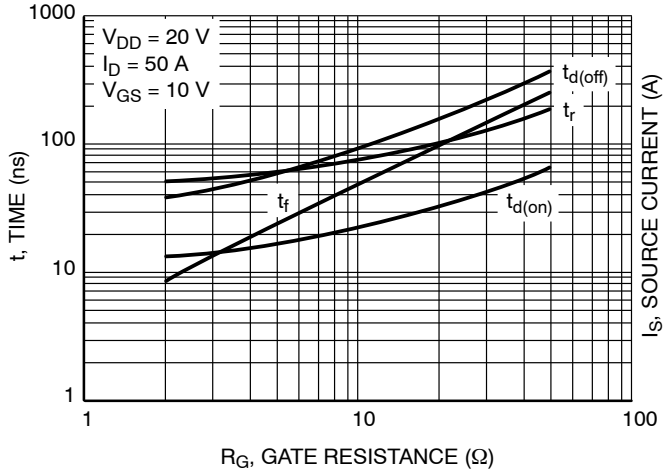


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

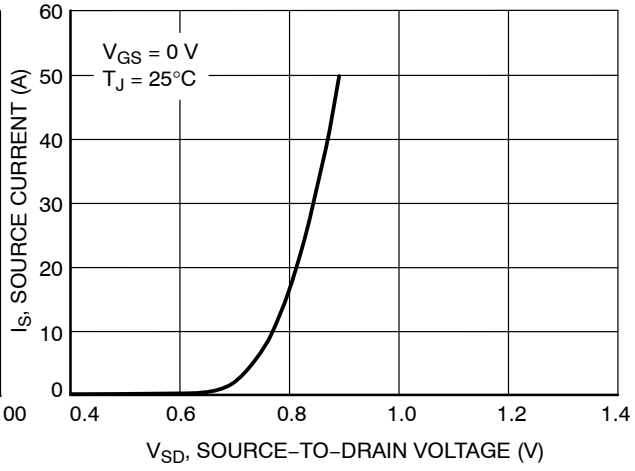


Figure 10. Diode Forward Voltage vs. Current

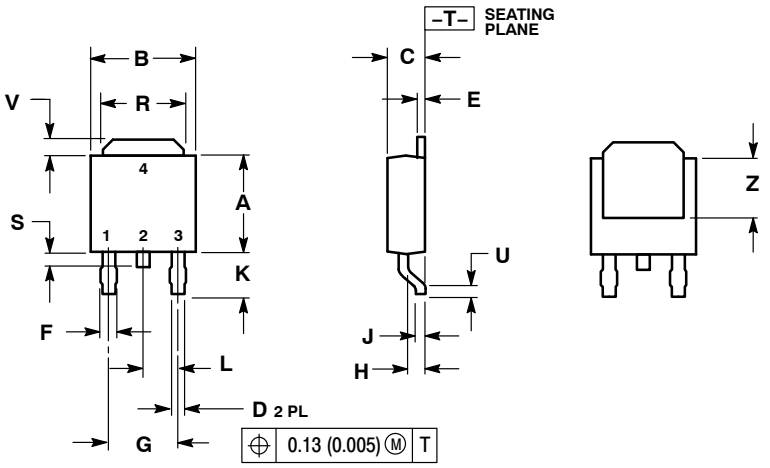
ORDERING INFORMATION

Order Number	Package	Shipping†
NTD5802NT4G	DPAK (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

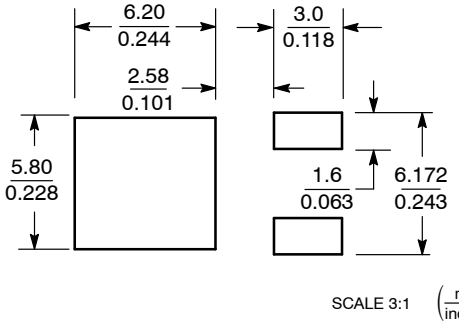
DPAK
CASE 369C−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	−−−	0.51	−−−
V	0.035	0.050	0.89	1.27
Z	0.155	−−−	3.93	−−−

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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