



STB7N52K3 - STD7N52K3 STF7N52K3 - STP7N52K3

N-channel 525 V, 0.84 Ω , 6.3 A, D²PAK, DPAK, TO-220FP, TO-220
SuperMESH3™ Power MOSFET

Preliminary Data

Features

Type	V _{DSS}	R _{DS(on)} max	I _D	P _w
STB7N52K3	525 V	< 0.98 Ω	6.3 A	90 W
STD7N52K3	525 V	< 0.98 Ω	6.3 A	90 W
STF7N52K3	525 V	< 0.98 Ω	6.3 A ⁽¹⁾	25 W
STP7N52K3	525 V	< 0.98 Ω	6.3 A	90 W

1. Limited by package

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitances
- Improved diode reverse recovery characteristics
- Zener-protected

Application

- Switching applications

Description

The new SuperMESH3™ series is obtained through the combination of a further fine tuning of ST's well established strip-based PowerMESH™ layout with a new optimization of the vertical structure. In addition to reducing on-resistance significantly versus previous generation, special attention has been taken to ensure a very good dv/dt capability and higher margin in breakdown voltage for the most demanding application.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STB7N52K3	7N52K3	D ² PAK	Tape and reel
STD7N52K3	7N52K3	DPAK	Tape and reel
STF7N52K3	7N52K3	TO-220FP	Tube
STP7N52K3	7N52K3	TO-220	Tube

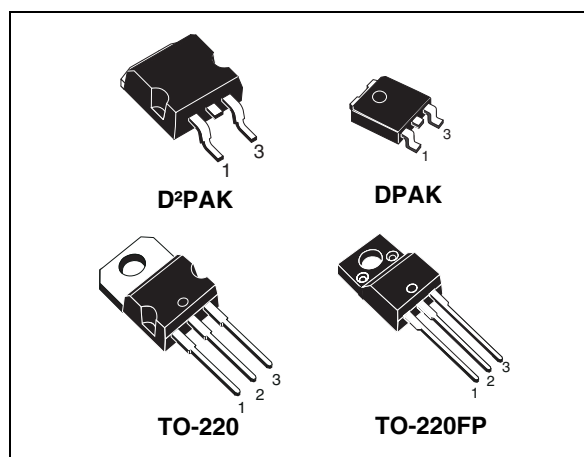
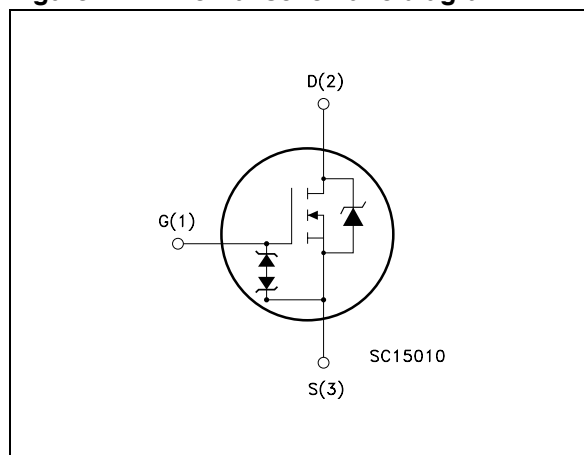


Figure 1. Internal schematic diagram



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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value				Unit
		TO-220	DPAK	D ² PAK	TO-220FP	
V _{DS}	Drain-source voltage (V _{GS} = 0)	525				V
V _{GS}	Gate- source voltage	± 30				V
I _D	Drain current (continuous) at T _C = 25 °C	6.3			6.3 ⁽¹⁾	A
I _D	Drain current (continuous) at T _C = 100 °C	4			4 ⁽¹⁾	A
I _{DM} ⁽²⁾	Drain current (pulsed)	25			25 ⁽¹⁾	A
P _{TOT}	Total dissipation at T _C = 25 °C	90			25	W
	Derating factor	0.72			0.2	W/°C
V _{ESD(G-S)}	Gate source ESD(HBM-C = 100 pF, R = 1.5 kΩ)	2500				V
dv/dt ⁽³⁾	Peak diode recovery voltage slope	TBD				V/ns
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T _C = 25 °C)	--			2500	V
T _{stg}	Storage temperature	-55 to 150				°C
T _j	Max. operating junction temperature	150				°C

- Limited by package
- Pulse width limited by safe operating area
- $I_{SD} \leq 6.3\text{ A}$, $di/dt = \text{TBD}$, $V_{DD} = 80\% V_{(BR)DSS}$.

Table 3. Thermal data

Symbol	Parameter	TO-220	DPAK	D ² PAK	TO-220FP	Unit
$R_{thj-case}$	Thermal resistance junction-case max	1.39			5	$^{\circ}\text{C/W}$
$R_{thj-pcb}$	Thermal resistance junction-pcb max	--	50	30	--	$^{\circ}\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	--	--	62.5	$^{\circ}\text{C/W}$
T_l	Maximum lead temperature for soldering purpose	300				$^{\circ}\text{C}$

Table 4. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	6.3	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	TBD	mJ

2 Electrical characteristics

($T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	525			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}$, $T_C = 125\text{ }^{\circ}\text{C}$			1 50	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 50\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 3.1\text{ A}$		0.84	0.98	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs} (1)$	Forward transconductance	$V_{DS} = 15\text{ V}$, $I_D = 3.1\text{ A}$		TBD		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$		TBD TBD TBD		pF pF pF
$C_{OSS\text{ eq}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0$, $V_{DS} = 0\text{ to }420\text{ V}$		TBD		pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain		TBD		Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 420\text{ V}$, $I_D = 6.3\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 3)		TBD TBD TBD		nC nC nC

1. $C_{OSS\text{ eq}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 262\text{ V}$, $I_D = 3.1\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 2)		TBD		ns
t_r	Rise time			TBD		ns
$t_{d(off)}$	Turn-off-delay time			TBD		ns
t_f	Fall time			TBD		ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current				6.3	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				25	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 6.3 \text{ A}$, $V_{GS} = 0$			1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 6.3 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 30 \text{ V}$ (see Figure 7)		TBD		ns
Q_{rr}	Reverse recovery charge			TBD		nC
I_{RRM}	Reverse recovery current			TBD		A
t_{rr}	Reverse recovery time	$I_{SD} = 6.3 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 30 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$ (see Figure 7)		TBD		ns
Q_{rr}	Reverse recovery charge			TBD		nC
I_{RRM}	Reverse recovery current			TBD		A

1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

Table 9. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$BV_{GSO}^{(1)}$	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{ mA}$ (open drain)	30			V

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components

Test circuits

STB7N52K3 - STD7N52K3 - STF7N52K3 - STP7N52K3

3 Test circuits

Figure 2. Switching times test circuit for resistive load

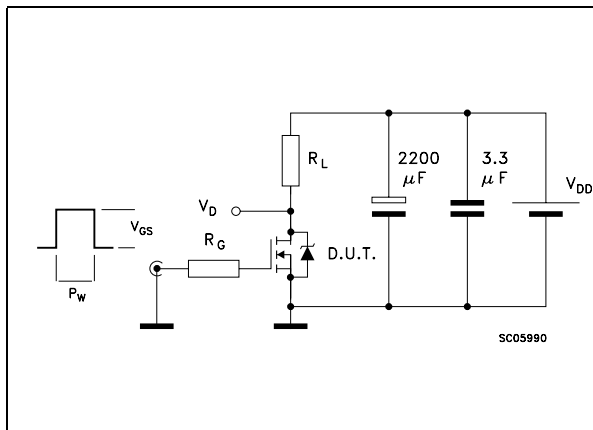


Figure 3. Gate charge test circuit

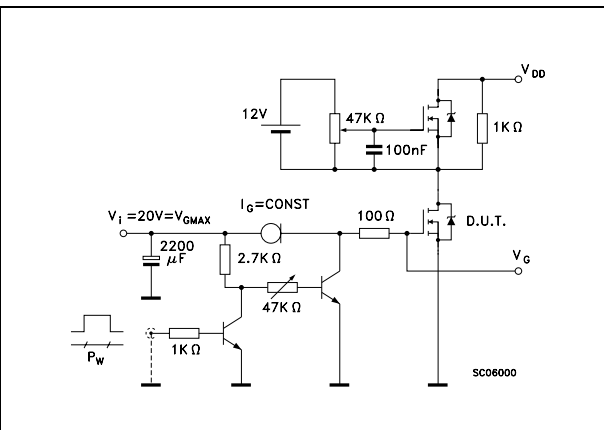


Figure 4. Test circuit for inductive load switching and diode recovery times

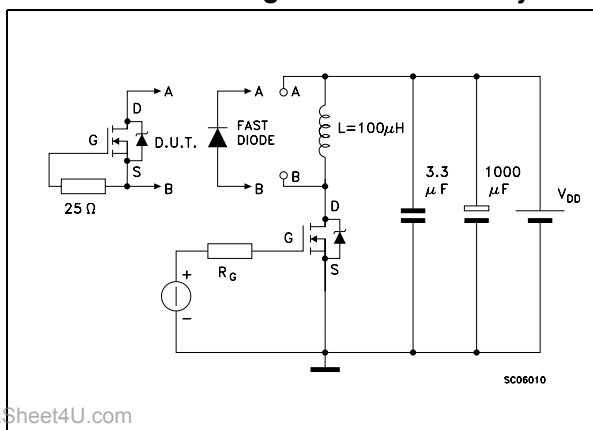


Figure 5. Unclamped Inductive load test circuit

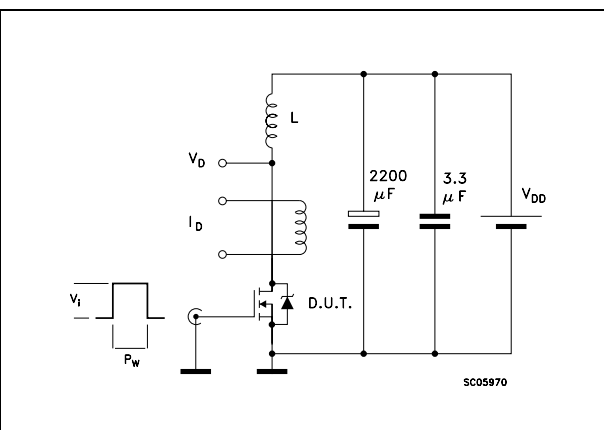


Figure 6. Unclamped inductive waveform

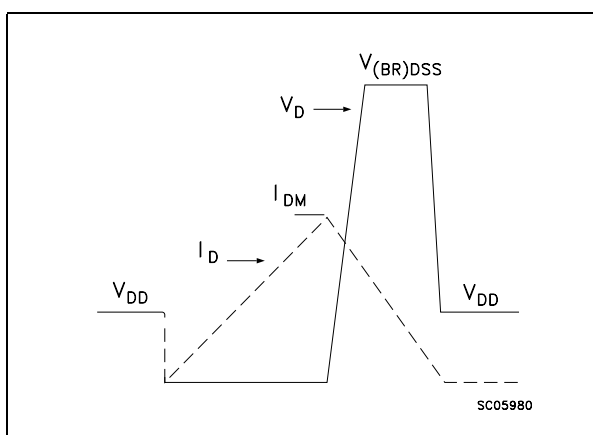
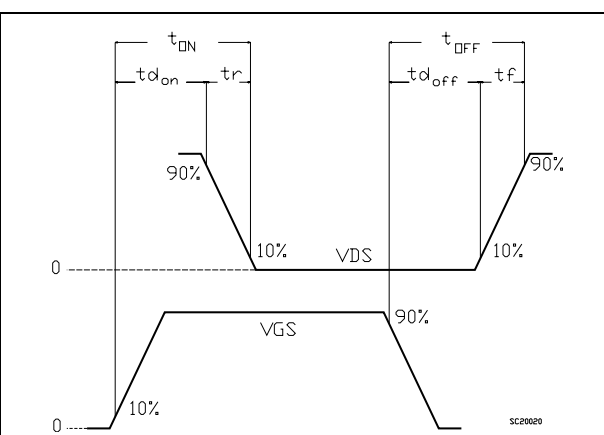


Figure 7. Switching time waveform



4 Package mechanical data

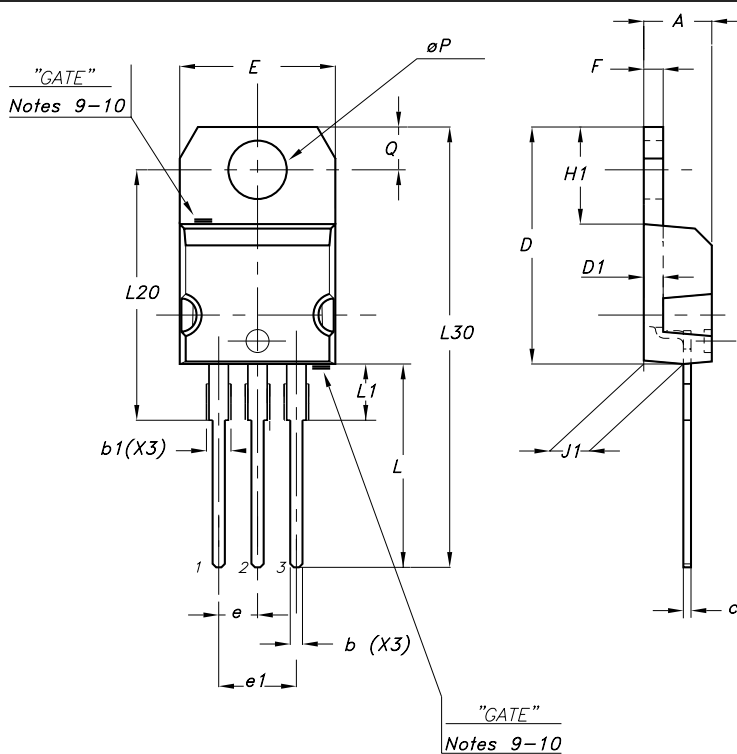
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Package mechanical data

STB7N52K3 - STD7N52K3 - STF7N52K3 - STP7N52K3

TO-220 mechanical data

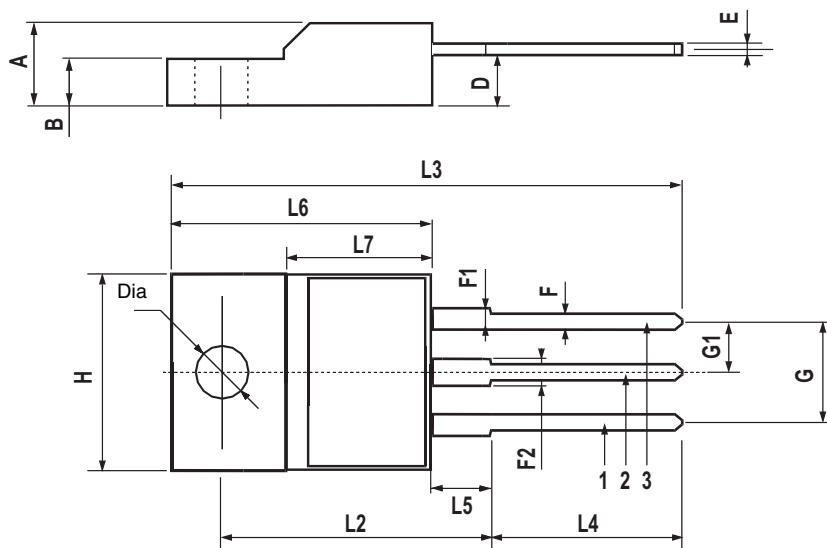
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	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.48		0.70	0.019		0.027
D	15.25		15.75	0.6		0.62
D1		1.27			0.050	
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.051
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
ØP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



0015988_Rev_R

TO-220FP mechanical data

Dim.	mm.			inch		
	Min.	Typ	Max.	Min.	Typ.	Max.
A	4.40		4.60	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.70	0.017		0.027
F	0.75		1.00	0.030		0.039
F1	1.15		1.50	0.045		0.067
F2	1.15		1.50	0.045		0.067
G	4.95		5.20	0.195		0.204
G1	2.40		2.70	0.094		0.106
H	10		10.40	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.80		10.60	0.385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.90		16.40	0.626		0.645
L7	9		9.30	0.354		0.366
Dia	3		3.2	0.118		0.126



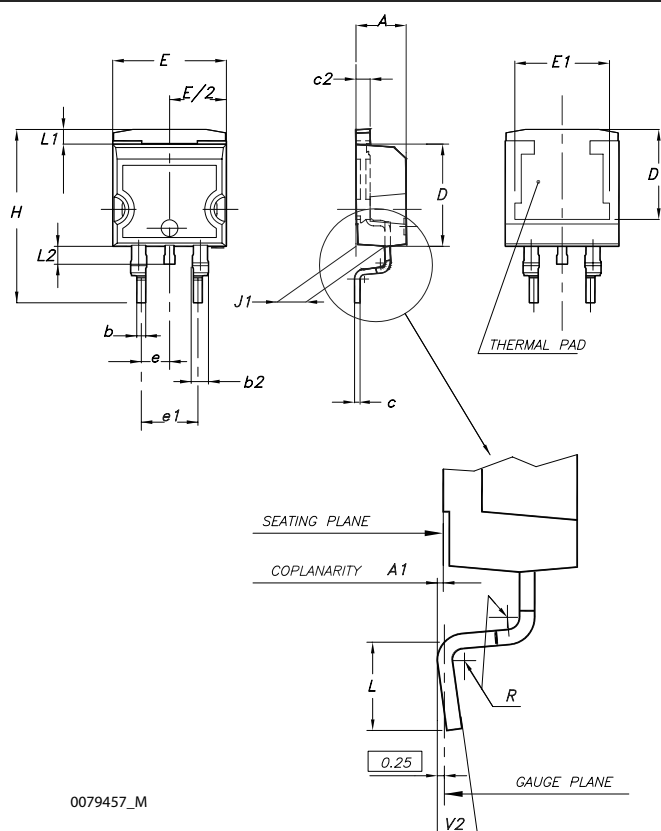
www.DataSheet4U.com

Package mechanical data

STB7N52K3 - STD7N52K3 - STF7N52K3 - STP7N52K3

D²PAK (TO-263) mechanical data

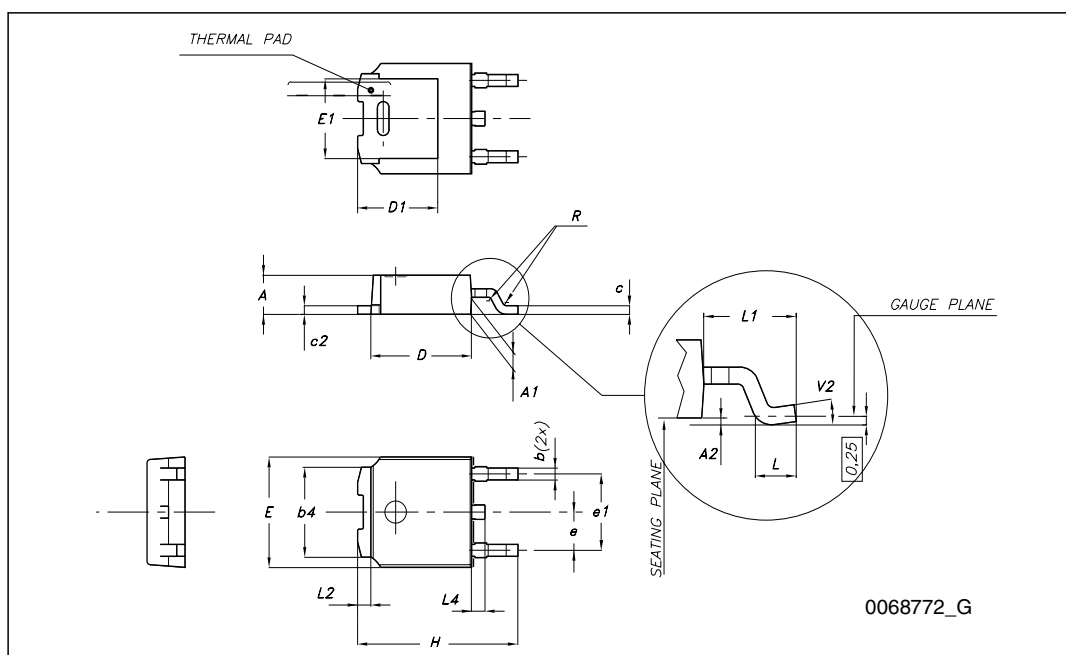
Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
A1	0.03		0.23	0.001		0.009
b	0.70		0.93	0.027		0.037
b2	1.14		1.70	0.045		0.067
c	0.45		0.60	0.017		0.024
c2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1	7.50			0.295		
E	10		10.40	0.394		0.409
E1	8.50			0.334		
e		2.54			0.1	
e1	4.88		5.28	0.192		0.208
H	15		15.85	0.590		0.624
J1	2.49		2.69	0.099		0.106
L	2.29		2.79	0.090		0.110
L1	1.27		1.40	0.05		0.055
L2	1.30		1.75	0.051		0.069
R		0.4			0.016	
V2	0°		8°	0°		8°



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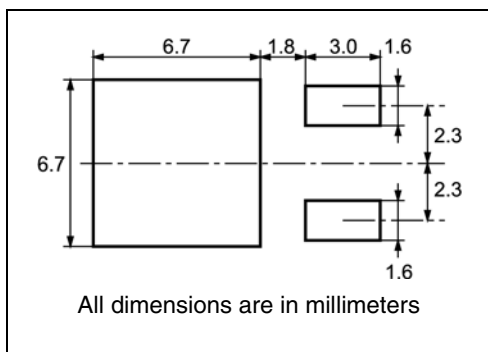
TO-252 (DPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0 °		8 °

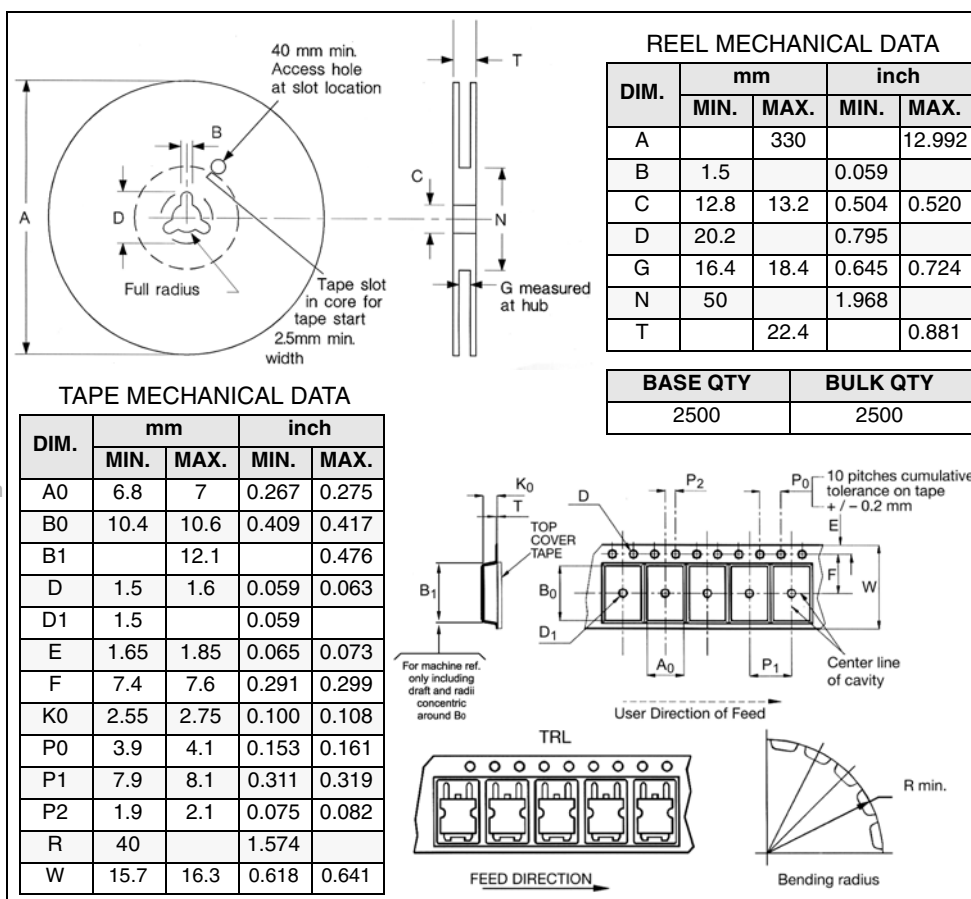


5 Package mechanical data

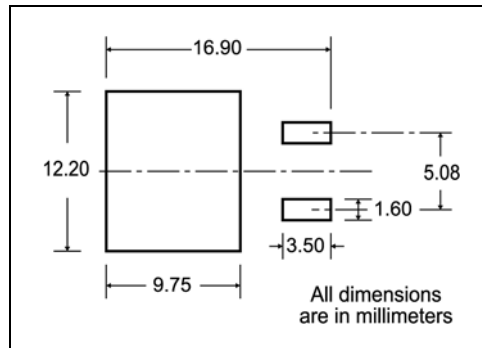
DPAK FOOTPRINT



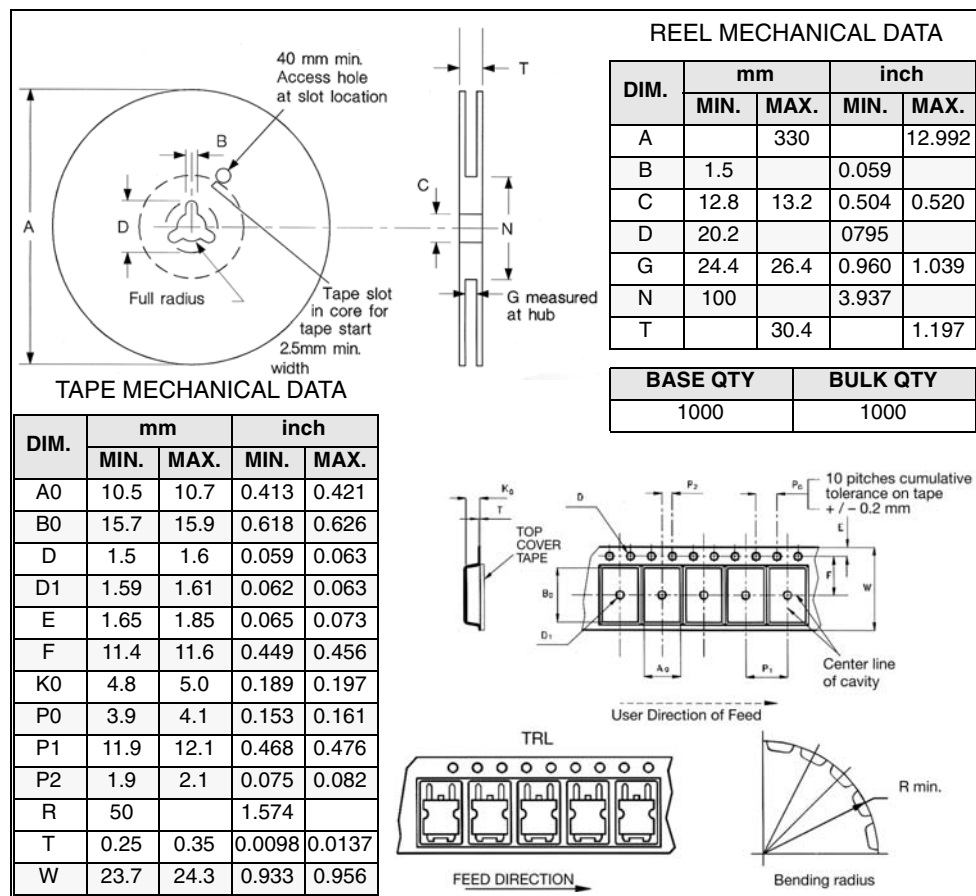
TAPE AND REEL SHIPMENT



D²PAK FOOTPRINT



TAPE AND REEL SHIPMENT



* on sales type

6 Revision history

Table 10. Document revision history

Date	Revision	Changes
07-Jul-2008	1	First release

STB7N52K3 - STD7N52K3 - STF7N52K3 - STP7N52K3

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