



# AK7756

## DSP with Mono CODEC + Mic/Lineout Amp

### GENERAL DESCRIPTION

The AK7756 is a highly integrated digital signal processor, including a mono voice audio codec, a MIC pre-amplifier and digital audio I/F. The audio DSP has 9216step at  $f_s = 8\text{kHz}$  parallel processing power. As the AK7756 is a RAM based DSP, it is programmable for user requirements such as hands free and acoustic effect. The AK7756EN is available in a space saving small 28pin QFN package and the AK7756VF is available in a 30pin VSOP package.

### FEATURES

- DSP
  - Word length: 24bit (Data RAM 24bit floating point)
  - Instruction cycle: 13.6 ns (9216 steps at  $f_s=8\text{ kHz}$ )
  - Multiplier 20 x 20 → 36bit (double precision available)
  - Divider 20 / 20 → 20bit
  - ALU: 36bit arithmetic operation (with overflow margin 4bit) 24bit floating point arithmetic and logic operation
  - Program RAM: 3072 x 36bit
  - Coefficient RAM: 2048 x 20bit
  - Data RAM: 1024 x 24-bit (24bit floating point)
  - Delay RAM: 3072 x 20bit, 3072 x 20bit
  - Master Clock: 4.6MHz ~ 73.7MHz
  - JX pins (Interrupt)
- Audio Serial I/F
  - Master / Slave operation
  - Right / Left justified and I<sup>2</sup>S
  - PCM (Short / Long Frame)
  - 16bit linear, 8bit A-law, 8bit  $\mu$ -law
- Mono CODEC
  - Sampling Rate 8KHz, 16KHz
  - DAC S/N: 91dB, S/(N+D): 83dB ( $f_s:16\text{kHz}$ )
  - ADC S/N: 86dB, S/(N+D): 77dB ( $f_s:16\text{kHz}$ )
- Microphone interface
  - Differential or single-ended input
  - Programmable Gain (+33dB ~ +15dB and 0dB, 3dB step)
  - Low Noise Microphone Bias
- Automatic Power Down (CODEC, DSP)
- $\mu$ P I/F : SPI, I<sup>2</sup>C-slave
- I<sup>2</sup>C bootloader
- Power supply
  - Analog (AVDD) : 3.0V ~ 3.6V (typ.3.3V)
  - Digital1 (DVDD) : 3.0V ~ 3.6V (typ.3.3V)
  - Digital2 (DVDD18) : 1.7V ~ 1.9V (typ.1.8V)
- Operating temperature range: -20°C ~ 85°C (AK7756EN), -40°C ~ 85°C (AK7756VF)
- Package: 28pin QFN (AK7756EN)  
          30pin VSOP (AK7756VF)

■ Block Diagram

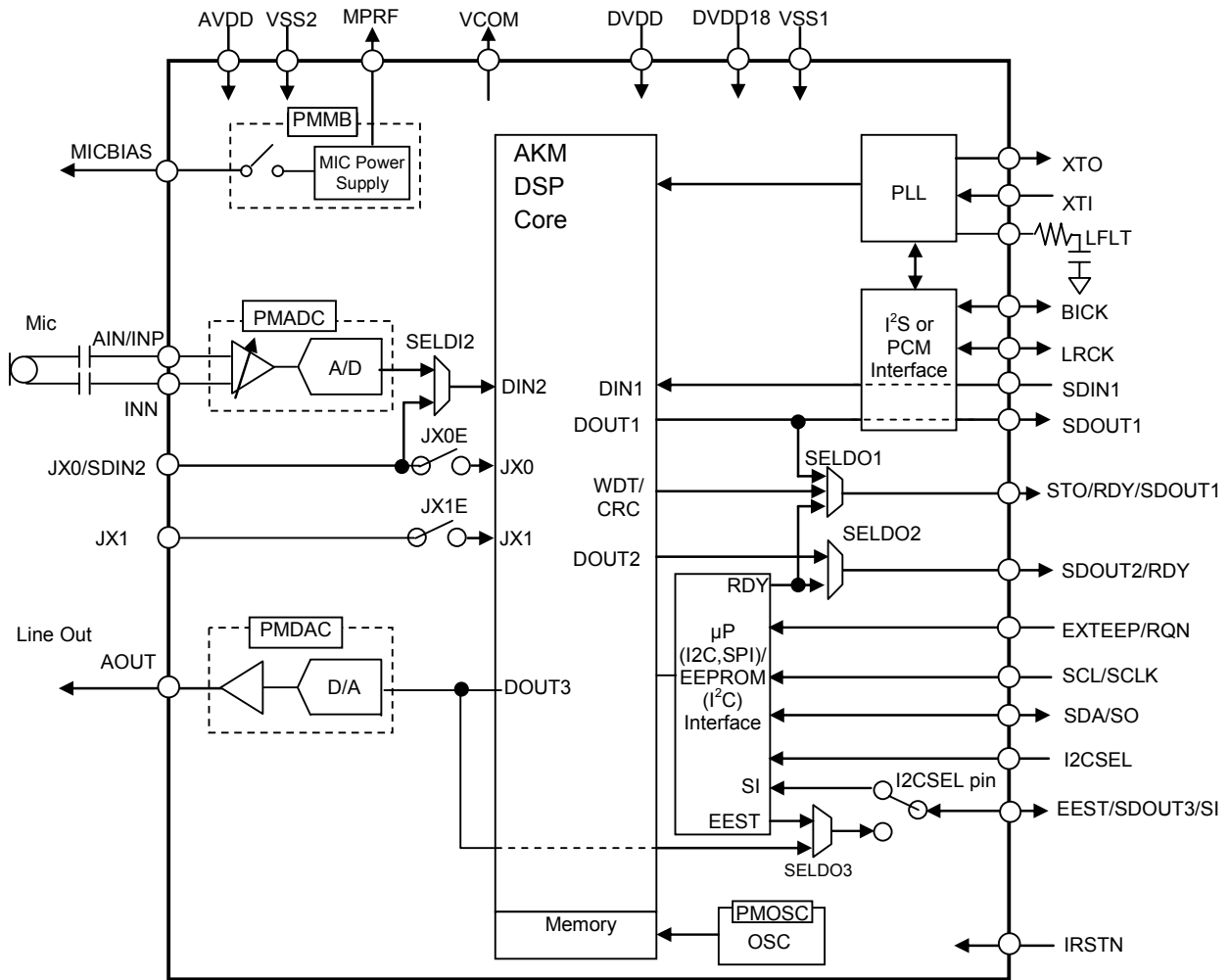


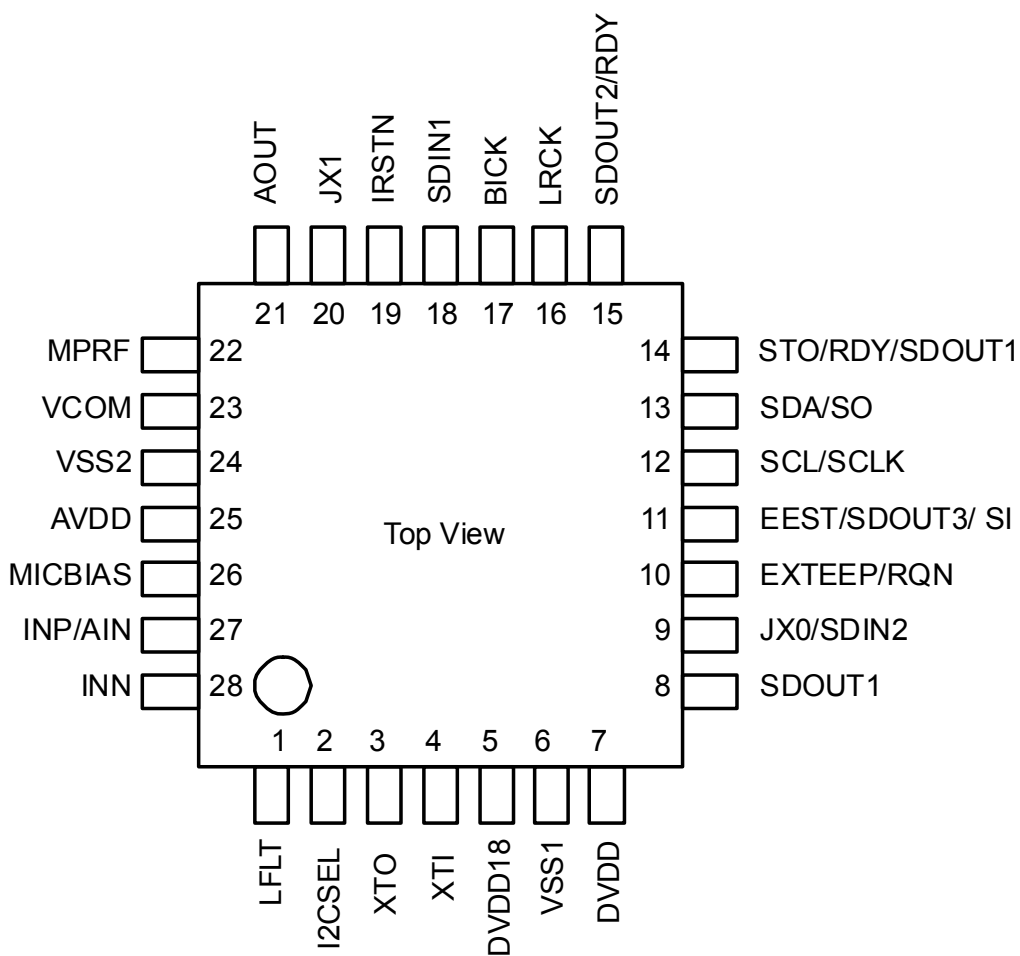
Figure 1. Block Diagram

■ Ordering Guide

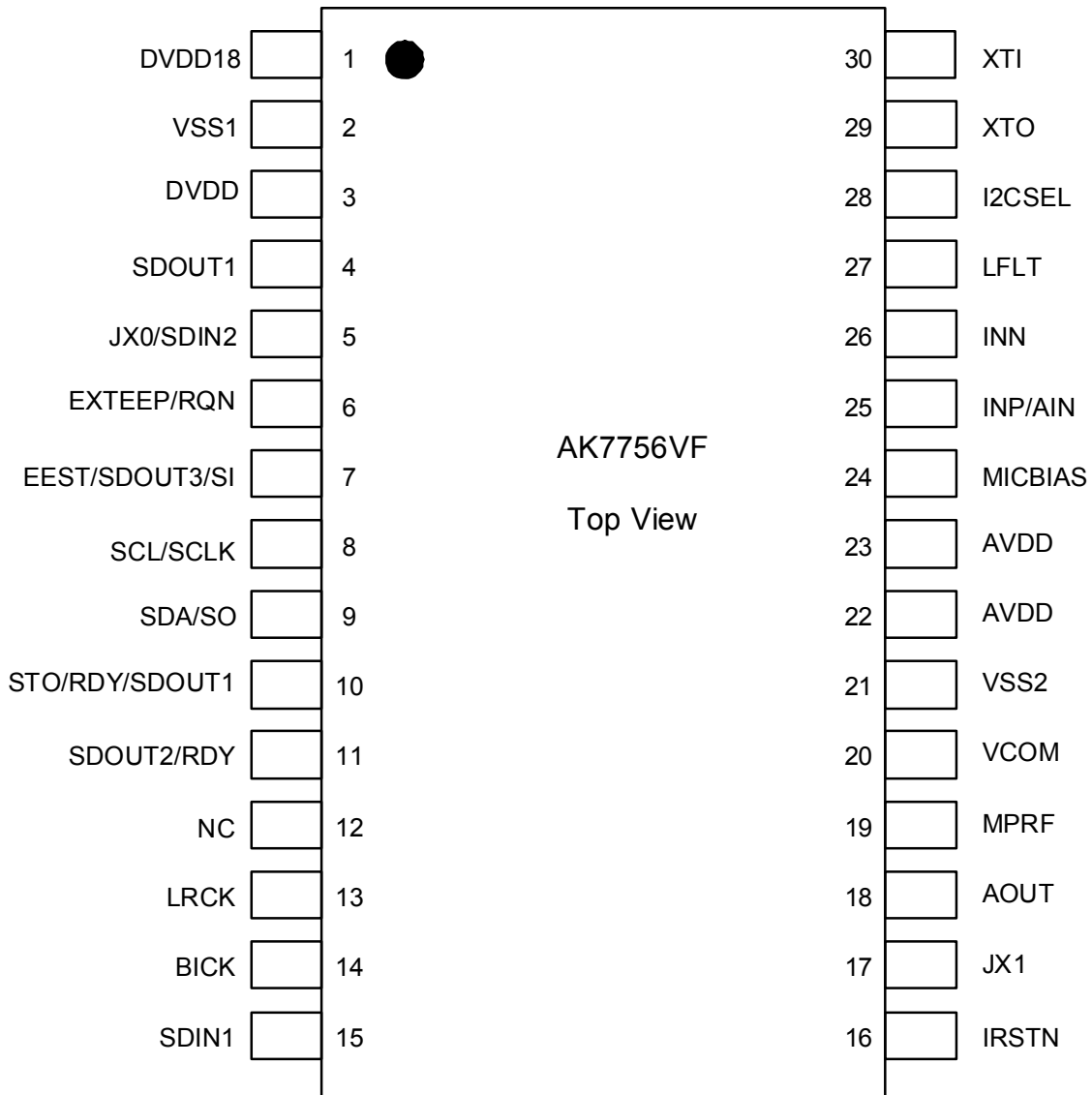
|            |                             |            |
|------------|-----------------------------|------------|
| AK7756EN   | -20 ~ +85°C                 | 28pin QFN  |
| AK7756VF   | -40 ~ +85°C                 | 30pin VSOP |
| AKD7756HFS | Evaluation Board for AK7756 |            |

■ Pin Layout

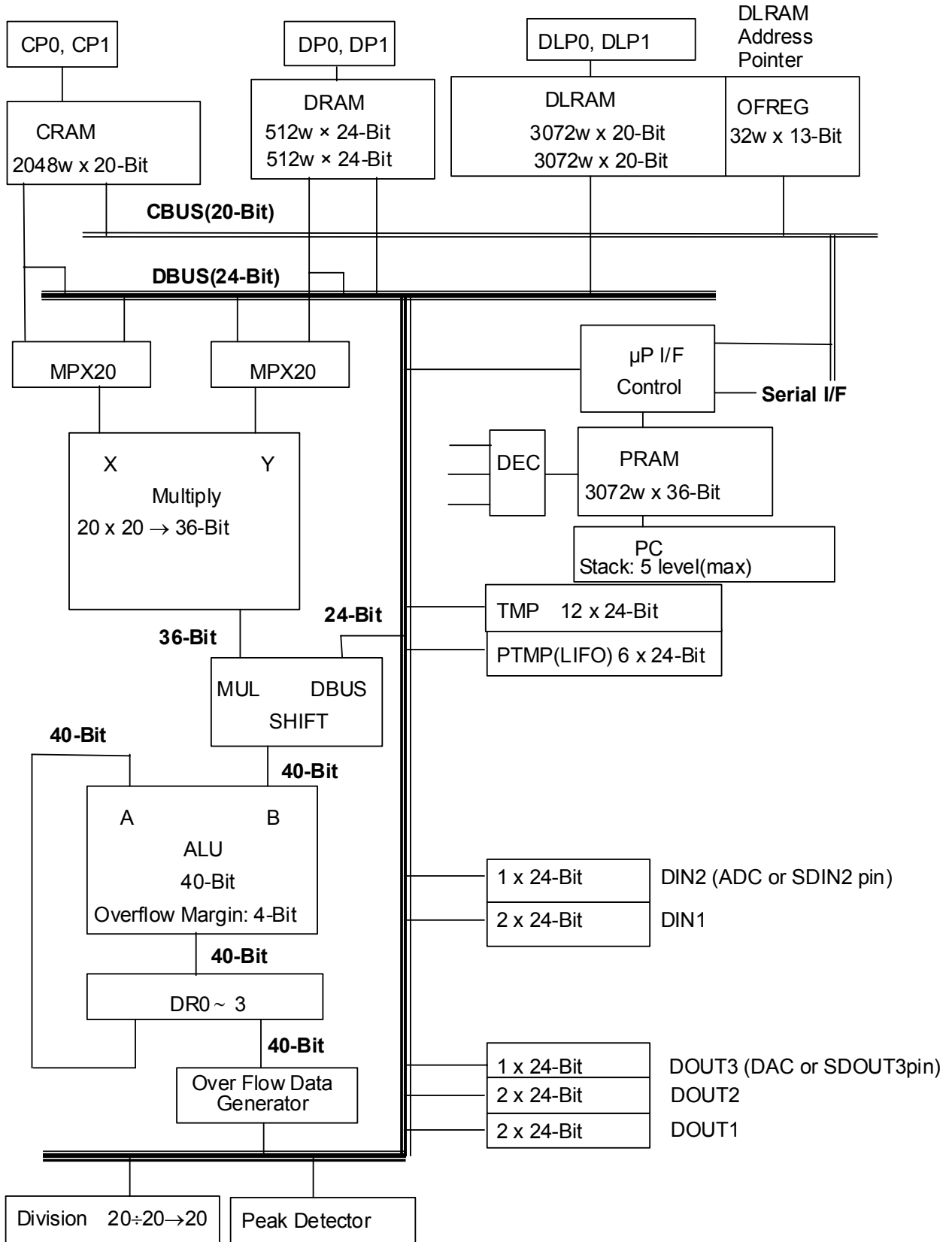
**AK7756EN**



**AK7756VF**



■ DSP Block Diagram



## PIN/FUNCTION (AK7756EN)

| No. | Pin Name | I/O | Function  |
|-----|----------|-----|---|
| 1   | LFLT     | O   | Output Pin for Loop Filter of PLL Circuit<br>This pin must be connected to VSS2 with 8.2KΩ and 33nF in series.<br>Outputs "L" during initial reset.                   |
| 2   | I2CSEL   | I   | μP Control Mode Select Pin "H": I <sup>2</sup> C, "L": SPI  |
| 3   | XTO      | O   | Master Clock Output Pin. Outputs Hi-Z during initial reset.   |
| 4   | XTI      | I   | External Master Clock Input Pin   |
| 5   | DVDD18   | -   | Digital Power Supply 2 Pin. 1.7 ~ 1.9V  |
| 6   | VSS1     | -   | Ground Pin  |
| 7   | DVDD     | -   | Digital Power Supply 1 Pin. 3.0 ~ 3.6V  |
| 8   | SDOUT1   | O   | Audio Serial Data Output1 Pin. Outputs "L" during initial reset.  |
| 9   | JX0      | I   | Conditional Jump Pin0 (JXOE bit = "1")  |
|     | SDIN2    | I   | Audio Serial Data Input 2 Pin (JXOE bit = "0")  |
| 10  | EXTEEP   | I   | Start to Download from external EEPROM (I2CSEL pin = "H" : I <sup>2</sup> C Bus Mode)<br>"H": start download (download from external memory)<br>"L": normal operation |
|     | RQN      | I   | μP I/F Write Request Pin (I2CSEL pin = "L" : SPI Mode)<br>When initial reset and μP I/F are not in use, leave the RQN pin High level.                                 |
| 11  | EEST     | O   | EEPROM download busy output (I2CSEL pin = "H" and SELDO3 bit = "0")<br>H: Download is busy. L: download is complete.<br>Outputs "L" during initial reset.             |
|     | SDOUT3   | O   | Audio Serial Data Output Pin3 (I2CSEL pin = "H" and SELDO3 bit = "1")<br>Outputs "L" during initial reset.  |
|     | SI       | I   | Control Data Input Pin (I2CSEL pin = "L": SPI Mode)   |
| 12  | SCL      | I   | Control Data Clock Pin (I2CSEL pin = "H": I <sup>2</sup> C Bus Mode)<br>Outputs Hi-Z during initial reset.  |
|     | SCLK     | I   | Control Data Clock Pin (I2CSEL pin = "L": SPI Mode)<br>Set this pin to "H" when there are no clock inputs.  |
| 13  | SDA      | I/O | Control Data Input /Output Pin (I2CSEL pin = "H": I <sup>2</sup> C Bus Mode)<br>Outputs Hi-Z during initial reset.  |
|     | SO       | O   | Control Data output Pin (I2CSEL pin = "L": SPI Mode)<br>Outputs "L" during initial reset.   |
| 14  | STO      | O   | Status Output Pin   |
|     | RDY      | O   | Data Write Ready Output Pin for μP Interface  |
|     | SDOUT1   | O   | Audio Serial Data Output Pin1<br>Outputs "H" during initial reset.  |
| 15  | SDOUT2   | O   | Audio Serial Data Output2 Pin   |
|     | RDY      | O   | Data Write Ready Output Pin for μP Interface<br>Outputs "L" during initial reset.   |
| 16  | LRCK     | I/O | Audio channel select Pin  |
| 17  | BICK     | I/O | Audio Serial Data Clock Pin   |
| 18  | SDIN1    | I   | Audio Serial Data Input 1 Pin   |
| 19  | IRSTN    | I   | Reset Pin (active low) The AK7756 must be reset once upon power-up.<br>"H": Power-up, "L": Initialize the control register.   |
| 20  | JX1      | I   | Conditional Jump Pin1   |
| 21  | AOUT     | O   | Analog Output Outputs. Outputs VSS2 during initial reset.   |
| 22  | MPRF     | O   | Output Pin for Ripple Filter of MICBIAS Circuit<br>Connect 1.0μF capacitor to VSS2. Outputs AVDD during initial reset.  |

|    |         |   |   |
|----|---------|---|---|
| 23 | VCOM    | O | Analog Common Voltage Output Pin<br>Connect 0.1 $\mu$ F and 2.2 $\mu$ F capacitor to VSS2. Outputs VSS2 during initial reset. |
| 24 | VSS2    | - | Ground Pin  |
| 25 | AVDD    | - | Analog Power Supply Pin 3.0 ~ 3.6V  |
| 26 | MICBIAS | O | Microphone bias. Outputs Hi-Z during initial reset.   |
| 27 | AIN     | I | Single-ended Analog Input pin (MDIF bit = "0")  |
|    | INP     | I | Positive Microphone input pin (MDIF bit = "1")  |
| 28 | INN     | I | Negative Microphone input pin (MDIF bit = "1")  |

Note 1. All digital input pins must not be left floating.

Note 2. DVDD or VSS1 voltage must be input to the I2CSEL pin.

Note 3. All analog input pins (INP/AIN, INN pins) must be supplied signal via AC-coupling capacitor.

Note 4. Analog output pins (AOUT pin) must deliver signal via AC-coupling capacitor

### PIN/FUNCTION (AK7756VF)

| No. | Pin Name | I/O | Function  |
|-----|----------|-----|---|
| 1   | DVDD18   | -   | Digital Power Supply 2 Pin. 1.7 ~ 1.9V  |
| 2   | VSS1     | -   | Ground Pin  |
| 3   | DVDD     | -   | Digital Power Supply 1 Pin. 3.0 ~ 3.6V  |
| 4   | SDOUT1   | O   | Audio Serial Data Output1 Pin.<br>Outputs "L" during initial reset.   |
| 5   | JX0      | I   | Conditional Jump Pin0 (JXOE bit = "1")  |
|     | SDIN2    | I   | Audio Serial Data Input 2 Pin (JXOE bit = "0")  |
| 6   | EXTEEP   | I   | Start to Download from external EEPROM (I2CSEL pin = "H" : I <sup>2</sup> C Bus Mode)<br>"H": start download (download from external memory)<br>"L": normal operation |
|     | RQN      | I   | $\mu$ P I/F Write Request Pin (I2CSEL pin = "L" : SPI Mode)<br>When initial reset and $\mu$ P I/F are not in use, leave the RQN pin High level.                       |
| 7   | EEST     | O   | EEPROM download busy output (I2CSEL pin = "H" and SELDO3 bit = "0")<br>H: Download is busy. L: download is complete.<br>Outputs "L" during initial reset.             |
|     | SDOUT3   | O   | Audio Serial Data Output Pin3 (I2CSEL pin = "H" and SELDO3 bit = "1")<br>Outputs "L" during initial reset.  |
|     | SI       | I   | Control Data Input Pin (I2CSEL pin = "L": SPI Mode)   |
| 8   | SCL      | I   | Control Data Clock Pin (I2CSEL pin = "H": I <sup>2</sup> C Bus Mode)<br>Outputs Hi-Z during initial reset.  |
|     | SCLK     | I   | Control Data Clock Pin (I2CSEL pin = "L": SPI Mode)<br>Set this pin to "H" when there are no clock inputs.  |
| 9   | SDA      | I/O | Control Data Input /Output Pin (I2CSEL pin = "H": I <sup>2</sup> C Bus Mode)<br>Outputs Hi-Z during initial reset.  |
|     | SO       | O   | Control Data output Pin (I2CSEL pin = "L": SPI Mode)<br>Outputs "L" during initial reset.   |
| 10  | STO      | O   | Status Output Pin   |
|     | RDY      | O   | Data Write Ready Output Pin for $\mu$ P Interface   |
|     | SDOUT1   | O   | Audio Serial Data Output Pin1<br>Outputs "H" during initial reset.  |
| 11  | SDOUT2   | O   | Audio Serial Data Output2 Pin   |
|     | RDY      | O   | Data Write Ready Output Pin for $\mu$ P Interface.<br>Outputs "L" during initial reset.   |
| 12  | NC       | -   | No Connect Pin.<br>This pin must be connected to VSS1.  |

|    |         |     |   |
|----|---------|-----|---|
| 13 | LRCK    | I/O | Audio channel select Pin  |
| 14 | BICK    | I/O | Audio Serial Data Clock Pin   |
| 15 | SDIN1   | I   | Audio Serial Data Input 1 Pin   |
| 16 | IRSTN   | I   | Reset Pin (active low) The AK7756VF must be reset once upon power-up.<br>“H”: Power-up, “L”: Initialize the control register.                               |
| 17 | JX1     | I   | Conditional Jump Pin1   |
| 18 | AOUT    | O   | Analog Output Outputs. Outputs VSS2 during initial reset.   |
| 19 | MPRF    | O   | Output Pin for Ripple Filter of MICBIAS Circuit<br>Connect 1.0 $\mu$ F capacitor to VSS2. Outputs AVDD during initial reset.                                |
| 20 | VCOM    | O   | Analog Common Voltage Output Pin<br>Connect 0.1 $\mu$ F and 2.2 $\mu$ F capacitor to VSS2. Outputs VSS2 during initial reset.                               |
| 21 | VSS2    | -   | Ground Pin  |
| 22 | AVDD    | -   | Analog Power Supply Pin 3.0 ~ 3.6V  |
| 23 | AVDD    | -   | Analog Power Supply Pin 3.0 ~ 3.6V  |
| 24 | MICBIAS | O   | Microphone bias. Outputs Hi-Z during initial reset.   |
| 25 | AIN     | I   | Single-ended Analog Input pin (MDIF bit = “0”)  |
|    | INP     | I   | Positive Microphone input pin (MDIF bit = “1”)  |
| 26 | INN     | I   | Negative Microphone input pin (MDIF bit = “1”)  |
| 27 | LFLT    | O   | Output Pin for Loop Filter of PLL Circuit<br>This pin must be connected to VSS2 with 8.2K $\Omega$ and 33nF in series.<br>Outputs “L” during initial reset. |
| 28 | I2CSEL  | I   | $\mu$ P Control Mode Select Pin “H”: I <sup>2</sup> C, “L”: SPI   |
| 29 | XTO     | O   | Master Clock Output Pin. Outputs Hi-Z during initial reset.   |
| 30 | XTI     | I   | External Master Clock Input Pin   |

Note 1. All digital input pins must not be left floating.

Note 2. DVDD or VSS1 voltage must be input to the I2CSEL pin.

Note 3. All analog input pins (INP/AIN, INN pins) must be supplied signal via AC-coupling capacitor.

Note 4. Analog output pins (AOUT pin) must deliver signal via AC-coupling capacitor

## ■ Handling of Unused Pin

The unused I/O pins must be processed appropriately as below.

| Classification | Pin Name  | Setting                               |
|----------------|---|---------------------------------------|
| Analog         | MICBIAS, INP/AIN, INN, AOUT, MPRF                           | These pins must be open.              |
| Digital        | SDOUT1, STO/RDY/SDOUT1, SDOUT2/RDY,<br>SDOUT3/EEST/ SI, XTO | These pins must be open.              |
|                | EXTEEP/RQN, SDIN1, XTI, JX0/SDIN2, JX1                      | These pins must be connected to VSS1. |



|                                 |
|---------------------------------|
| <b>ABSOLUTE MAXIMUM RATINGS</b> |
|---------------------------------|

(VSS1=VSS2=0V; Note 5)

| Parameter                              | Symbol                | min    | max               | Units |    |
|--|-----------------------|--------|-------------------|-------|----|
| Power Supplies:                        | Analog                | AVDD   | -0.3              | 4.3   | V  |
|  | Digital 1             | DVDD   | -0.3              | 4.3   | V  |
|  | Digital 2             | DVDD18 | -0.3              | 2.5   | V  |
|  | Difference(VSS1~VSS2) | ΔGND   | -0.3              | 0.3   | V  |
| Input Current, Any Pin Except Supplies | IIN                   | -      | ±10               | mA    |    |
| Analog Input Voltage (Note 6)          | VINA                  | -0.3   | (AVDD+0.3) or 4.3 | V     |    |
| Digital Input Voltage (Note 7)         | VIND1                 | -0.3   | (DVDD+0.3) or 4.3 | V     |    |
| Ambient Temperature (powered applied)  | AK7756EN              | Ta     | -20               | 85    | °C |
|  | AK7756VF              | Ta     | -40               | 85    | °C |
| Storage Temperature                    | Tstg                  | -65    | 150               | °C    |    |

Note 5. All voltages with respect to ground. VSS1 and VSS2 must be the same voltage.

Note 6. INP/AIN, INN pins

Note 7. IRSTN, I2CSEL, EXTEEP, SI/EEST, SDA/SO, SCL/SCLK, JX1, JX0, SDIN1, LRCK, and BICK pins

Note 8. Pull-up resistors at SDA and SCL pins must be connected to the DVDD voltage or less.

Do not turn off the power supplies when the SDA and SCL pins are pulled-up to DVDD.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.

Normal operation is not guaranteed at these extremes.

|   |
|---|
| <b>RECOMMENDED OPERATING CONDITIONS</b> |
|---|

(VSS1=VSS2=0V; Note 5)

| Parameter                  | Symbol      | min         | typ  | max | Units |   |
|----------------------------|-------------|-------------|------|-----|-------|---|
| Power Supplies<br>(Note 9) | Analog      | AVDD        | 3.0  | 3.3 | 3.6   | V |
|                            | Digital     | DVDD        | 3.0  | 3.3 | 3.6   | V |
|                            | Digital     | DVDD18      | 1.7  | 1.8 | 1.9   | V |
|                            | Difference1 | AVDD – DVDD | -0.3 | 0   | +0.3  | V |

Note 5. All voltages with respect to ground. VSS1 and VSS2 must be the same voltage.

Note 9. The power-up sequence between AVDD, DVDD and DVDD18 is not critical. But all power supplies must be ON before starting operation of the AK7756.

\* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

|                                       |
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| <b>ANALOG CHARACTERISTICS (CODEC)</b> |
|---------------------------------------|

### ■ ADC Characteristics

(Ta=25°C; AVDD=DVDD=3.3V, DVDD18=1.8V; VSS1=VSS2=0V; BICK=64fs; Signal Frequency 1kHz; Measurement frequency =20Hz~8 kHz, fs=16 kHz, CKM mode 6, unless otherwise specified.)

| Parameter                                    | min  | typ          | max        | Units |      |      |
|--|--|--------------|------------|-------|------|------|
| <b>MIC Input Programmable Gain Amplifier</b> |  |              |            |       |      |      |
| Input Resistance (INP, INN pins)             |  |              |            |       |      |      |
| (MGAIN = 0dB)                                | 22.5   | 30           | 37.5       | kΩ    |      |      |
| Gain   |  |              |            |       |      |      |
| Min (MGAIN2-0 bit = "0H")                    | -  | 0            | -          | dB    |      |      |
| Max (MGAIN2-0 bit = "7H")                    | -  | +33          | -          | dB    |      |      |
| Step size (MGAIN2-0bit = "1H" ~ "7H")        |  | 3            |            | dB    |      |      |
| <b>Microphone Bias Supply: MICBIAS pin</b>   |  |              |            |       |      |      |
| Bias Output Voltage (Note 10)                |  | 2.32         |            | V     |      |      |
| Load Resistance                              | 2.0  | -            | -          | kΩ    |      |      |
| Load Capacitance                             | -  | -            | 30         | pF    |      |      |
| <b>Mono ADC</b>                              | Resolution   |              |            | 24    | Bits |      |
|  | <b>Dynamic Characteristics</b> AIN pin→ Mono ADC→ SDOUT1 |              |            |       |      |      |
|  | S/(N+D) (-1dBFS)   | MGAIN=21dB   |            | 72    |      | dB   |
|  |  | MGAIN= 0dB   | 69         | 77    |      |      |
|  | Dynamic Range  | MGAIN=21dB   |            | 77    |      | dB   |
|  |  | MGAIN= 0dB   | 78         | 86    |      |      |
|  | S/N  | MGAIN=21dB   |            | 77    |      | dB   |
|  |  | MGAIN= 0dB   | 78         | 86    |      |      |
|  | <b>Microphone Analog Inputs INP,INN (Note 11)</b>        |              |            |       |      |      |
|  | Full-scale Input Voltage                                 | Differential | MGAIN= 0dB | ±2.0  | ±2.2 | ±2.4 |
| Single-ended                                 |  | MGAIN= 0dB   | 2.0        | 2.2   | 2.4  | VPP  |

Note 10. The output voltage is proportional to AVDD. Vmic bias=0.70 \* AVDD, Iout=1mA

Note 11. The input voltage is proportional to AVDD. Vin=0.67 x AVDD (typ.) @MGAIN = 0dB

## ■ DAC Characteristics

(Ta=25°C; AVDD=DVDD=3.3V, DVDD18=1.8V; VSS1=VSS2=0V; BICK=64fs; Signal frequency 1 kHz; Measurement frequency=20Hz~8 kHz, fs=16 kHz, CKM mode 6, unless otherwise specified.)

| Mono DAC  | Parameter  | min  | typ | max  | Unit |
|---|------------|------|-----|------|------|
|   | Resolution |      |     |      | 24   |
| <b>Dynamic Characteristics; Mono DAC→AOUT pin</b> |            |      |     |      |      |
| S/(N+D)   | (0dBFS)    | 75   | 83  |      | dB   |
| S/N   |            | 83   | 91  |      | dB   |
| <b>Analog Output</b>                              |            |      |     |      |      |
| Full-scale Output Voltage (Note 12)               |            | 2.09 | 2.2 | 2.31 | Vpp  |
| Load Resistance                                   |            | 10   |     |      | kΩ   |
| Load Capacitance                                  |            |      |     | 30   | pF   |

Note 12. Full scale output voltage. The output voltage is proportional to AVDD.  $V_{out}=0.67 \times AVDD$  (typ.)

**DC CHARACTERISTICS**

(Ta=Tmin~Tmax; AVDD=DVDD=3.0~3.6V; DVDD18=1.7~1.9V; VSS1=VSS2=0V)

| Parameter  | Symbol | min      | typ | max     | Unit |
|--|--------|----------|-----|---------|------|
| High level input voltage (Note 13)               | VIH    | 80%DVDD  |     |         | V    |
| Low level input voltage (Note 13)                | VIL    |          |     | 20%DVDD | V    |
| SCL, SDA High level input voltage                | VIH    | 70%DVDD  |     |         | V    |
| SCL, SDA Low level input voltage                 | VIL    |          |     | 30%DVDD | V    |
| High level output voltage: Iout=-100μA (Note 14) | VOH    | DVDD-0.4 |     |         | V    |
| Low level output voltage: Iout=100μA (Note 14)   | VOL    |          |     | 0.4     | V    |
| SDA Low level output voltage Iout=3mA            | VOL    |          |     | 0.4     | V    |
| Input leak current (Note 15)                     | Iin    |          |     | ±10     | μA   |
| Input leak current XTI pin                       | Iix    |          | 26  |         | μA   |

Note 13. Except for the SCL/SCLK, SDA/SO pins.

Note 14. Except for the SDA/SO pin.

Note 15. Except for the XTI pin.

**POWER CONSUMPTION**

(Ta=25°C; AVDD=DVDD=3.3V; DVDD18=1.8V; VSS1=VSS2=0V, fin=1 KHz, 24 bit, fs=8 KHz (CKM mode = 0), DSPS=BITFS=PMOSC bits="0" PMMB bit="1", DSP running with programmed connecting DIN2 with DOUT1 and DIN1 with DOUT3.)

| Parameter  | min            | typ  | max | Units |
|--|----------------|------|-----|-------|
| <b>Power Supplies: (Note 16)</b>                                 |                |      |     |       |
| Power-Up (IRSTN pin = "H") CODEC+DSP                             |                |      |     |       |
| All Circuit Power-up   |                |      |     |       |
| AVDD+DVDD  | AVDD=DVDD=3.3V | 11.0 | -   | mA    |
| DVDD18   | DVDD18=1.8V    | 6    | -   | mA    |
| Power Consumption  |                | 47   |     | mW    |
| AVDD+DVDD  | AVDD=DVDD=3.6V |      | 15  | mA    |
| DVDD18   | DVDD18=1.9V    |      | 60  | mA    |
| Reset (IRSTN pin = "L"), Power-down condition (Note 17, Note 18) |                |      |     |       |
| AVDD+DVDD  | -              | 1    | 10  | μA    |
| DVDD18   |                | 3    | 200 | μA    |

Note 16. The Consumption of DVDD18 depends on the master clock frequency and the step size of the DSP program.  
(BITFS bit = "2h" and DSPS bit = "0")

Note 17. All digital input pins are fixed to each supply pin (DVDD or VSS1).

Note 18. The condition of maximum values specifies Ta=Tmin~Tmax, AVDD=DVDD=3.0~3.6V and DVDD18=1.7~1.9V.

|                                       |
|---------------------------------------|
| <b>DIGITAL FILTER CHARACTERISTICS</b> |
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### ■ ADC Block

#### 1. fs=8kHz

(Ta= Tmin~Tmax, AVDD= DVDD=3.0~3.6V, DVDD18=1.7~1.9V, VSS1=VSS2=0V; fs=8 kHz)

| Parameter   | Symbol | min  | typ  | max  | Unit |
|---|--------|------|------|------|------|
| Passband (±0.1dB) (Note 19, Note 20)<br>(-0.02dB)<br>(-3.0dB) | PB     | 0    |      | 3.15 | kHz  |
|   |        |      | 3.63 |      | kHz  |
|   |        |      | 3.83 |      | kHz  |
| Stopband  | SB     | 4.66 |      |      | kHz  |
| Passband Ripple (Note 20)                                     | PR     |      |      | ±0.1 | dB   |
| Stopband Attenuation (Note 21, Note 22)                       | SA     | 68   |      |      | dB   |
| Group Delay Distortion  | ΔGD    |      |      | 0    | μs   |
| Group Deley (Ts=1/fs)   | GD     |      | 16   |      | Ts   |

Note 19. The characteristic of the high pass filter is not included.

Note 20. The passband is from DC to 3.15kHz

Note 21. The stopband is 4.66kHz to 507.34kHz.

Note 22. The analog modulator samples the input signal at 512kHz.

#### 2. fs=16kHz

(Ta= Tmin~Tmax, AVDD= DVDD=3.0~3.6V, DVDD18=1.7~1.9V, VSS1=VSS2=0V; fs=16 kHz)

| Parameter   | Symbol | min  | typ  | max  | Unit |
|---|--------|------|------|------|------|
| Passband (±0.1dB) (Note 23, Note 24)<br>(-0.02dB)<br>(-3.0dB) | PB     | 0    |      | 6.3  | kHz  |
|   |        |      | 7.26 |      | kHz  |
|   |        |      | 7.66 |      | kHz  |
| Stopband  | SB     | 9.32 |      |      | kHz  |
| Passband Ripple (Note 24)                                     | PR     |      |      | ±0.1 | dB   |
| Stopband Attenuation (Note 25, Note 26)                       | SA     | 68   |      |      | dB   |
| Group Delay Distortion  | ΔGD    |      |      | 0    | μs   |
| Group Deley (Ts=1/fs)   | GD     |      | 16   |      | Ts   |

Note 23. The characteristic of the high pass filter is not included.

Note 24. The passband is from DC to 6.3kHz

Note 25. The stopband is 9.32kHz to 1014.68kHz.

Note 26. The analog modulator samples the input signal at 1024kHz.

## ■ DAC Block

### 1. fs=8kHz

(Ta= Tmin~Tmax, AVDD=DVDD= 3.0V ~ 3.6V, DVDD18= 1.7V ~ 1.9V; VSS1=VSS2=0V; fs=8 kHz)

| Parameter                                | Symbol      | min  | typ  | max   | Unit |
|--|-------------|------|------|-------|------|
| Passband (±0.05dB) (Note 27)<br>(-6.0dB) | PB          | 0    |      | 3.62  | kHz  |
|  |             |      | 4    |       | kHz  |
| Stopband (Note 27)                       | SB          | 4.37 |      |       | kHz  |
| Passband Ripple                          | PR          |      |      | ±0.01 | dB   |
| Stopband Attenuation                     | SA          | 64   |      |       | dB   |
| Group Delay (Ts=1/fs) (Note 28)          | GD          |      | 24   |       | Ts   |
| <b>Digital Filter + Analog Filter</b>    |             |      |      |       |      |
| Amplitude characteristic                 | 20Hz~3.5kHz |      | ±0.5 |       | dB   |

Note 27. Pass band and stop band parameters are related to sampling frequency (fs). PB=0.4535fs (at-0.05dB),  
SB=0.5465fs.

Note 28. The digital filter's delay is calculated as the time from setting 16-bit data into the input register until an analog signal is output.

### 2. fs=16kHz

(Ta= Tmin~Tmax, AVDD=DVDD= 3.0V ~ 3.6V, DVDD18= 1.7V ~ 1.9V; VSS1=VSS2=0V; fs=16kHz)

| Parameter                                | Symbol      | min  | typ  | max   | Unit |
|--|-------------|------|------|-------|------|
| Passband (±0.05dB) (Note 27)<br>(-6.0dB) | PB          | 0    |      | 7.24  | kHz  |
|  |             |      | 8    |       | kHz  |
| Stopband (Note 27)                       | SB          | 8.74 |      |       | kHz  |
| Passband Ripple                          | PR          |      |      | ±0.01 | dB   |
| Stopband Attenuation                     | SA          | 64   |      |       | dB   |
| Group Delay (Ts=1/fs) (Note 28)          | GD          |      | 24   |       | Ts   |
| <b>Digital Filter + Analog Filter</b>    |             |      |      |       |      |
| Amplitude characteristic                 | 20Hz~7.0kHz |      | ±0.5 |       | dB   |

|                                  |
|----------------------------------|
| <b>SWITCHING CHARACTERISTICS</b> |
|----------------------------------|

### ■ System Clock

(Ta= Tmin~Tmax, AVDD=DVDD= 3.0V ~ 3.6V, DVDD18= 1.7V ~ 1.9V, VSS1=VSS2=0V, CL=20pF)

| Parameter                                     | Symbol | min  | typ            | max  | Unit |
|---|--------|------|----------------|------|------|
| <b>Master operation</b>                       |        |      |                |      |      |
| a) XTI/XTO with a X'tal, External Clock input |        |      |                |      |      |
| CKM[2:0]bits=6h(768x16KHz)                    | fXTI   | 11.0 | 12.288         | 12.4 | MHz  |
| Duty Cycle                                    |        | 40   | 50             | 60   | %    |
| <b>Slave mode operation</b>                   |        |      |                |      |      |
| LRCK Frequency                                | fs     | 8    |                | 16   | kHz  |
| BICK Frequency                                | fBICK  | 0.1  | 32fs/48fs/64fs | 1.1  | MHz  |
|   | Duty   | 40   |                | 60   | %    |

### ■ Reset

(Ta= Tmin~Tmax, AVDD=DVDD=3.0~3.6V; DVDD18=1.7~1.9V; VSS1=VSS2=0V)

| Parameter                      | Symbol | min | typ | max | Unit |
|--------------------------------|--------|-----|-----|-----|------|
| Reset pulse width<br>(Note 29) | tRST   | 600 |     |     | ns   |

Note 29. The IRSTN pin must be put to "H" after all power supplies are powered up.

## ■ Digital Audio Interface (SDIN1, SDOUT1, 2)

1) SDIN1/2, SDOUT1/2/3

(Ta= Tmin~Tmax, AVDD=DVDD= 3.0V ~ 3.6V, DVDD18= 1.7V ~ 1.9V, VSS1=VSS2=0V, CL=20pF)

| Parameter  | Symbol | min | typ | max | Unit |
|--|--------|-----|-----|-----|------|
| <b>I<sup>2</sup>S and PCM Interface Input Timing</b>           |        |     |     |     |      |
| Delay Time from BICK “↑” to LRCK (Note 30)                     | tBLRD  | 20  |     |     | ns   |
| Delay Time from LRCK to BICK “↑” (Note 30)                     | tLRBD  | 20  |     |     | ns   |
| Serial Data Input Latch Setup Time                             | tBSIDS | 80  |     |     | ns   |
| Serial Data Input Latch Hold Time                              | tBSIDH | 80  |     |     | ns   |
| Delay Time from LRCK to Serial Data Output (Note 31)           | tLRD   |     |     | 80  | ns   |
| Delay Time from BICK “↓” or “↑” to LRCK Output                 | tBSOD  |     |     | 80  | ns   |
| <b>I<sup>2</sup>S and PCM Interface Output Timing SDOUT1/2</b> |        |     |     |     |      |
| BICK Frequency   | fBICK  |     | 64  |     | fs   |
| BICK Duty cycle  |        |     | 50  |     | %    |
| Delay Time from BITCLK “↓” to LRCK Output                      | tMBL   | -20 |     | 40  | ns   |
| Serial Data Input Latch Setup Time                             | tBSIDS | 80  |     |     | ns   |
| Serial Data Input Latch Hold Time                              | tBSIDH | 80  |     |     | ns   |
| Delay Time from LRCK to Serial Data Output (Note 31)           | tLRD   |     |     | 80  | ns   |
| Delay Time from BICK “↓” or “↑” to LRCK Output                 | tBSOD  |     |     | 80  | ns   |

Note 30. BICK edge must not occur at the same time as LRCK edge.

Note 31. Except I<sup>2</sup>S.



### ■ $\mu$ P Interface (SPI mode)

(Ta= Tmin~Tmax; AVDD=DVDD=3.0~3.6V; DVDD18=1.7~1.9V, VSS1=VSS2=0V; CL=20pF)

| Parameter   | Symbol | min | typ | max | Unit    |
|---|--------|-----|-----|-----|---------|
| <b><math>\mu</math>P Interface Timing (SPI mode)</b>      |        |     |     |     |         |
| RQN Fall Time   | tWRF   |     |     | 30  | ns      |
| RQN Rise Time   | tWRR   |     |     | 30  | ns      |
| SCLK Fall Time  | tSF    |     |     | 30  | ns      |
| SCLK Rise Time  | tSR    |     |     | 30  | ns      |
| SCLK Frequency  | fSCLK  |     |     | 2.1 | MHz     |
| SCLK Low Level Width                                      | tSCLKL | 200 |     |     | ns      |
| SCLK High Level Width                                     | tSCLKH | 200 |     |     | ns      |
| RQN High Level Width                                      | tWRQH  | 500 |     |     | ns      |
| From RQN “ $\uparrow$ ” to IRSTN “ $\uparrow$ ”           | tRST1  | 600 |     |     | ns      |
| From IRSTN “ $\uparrow$ ” to RQN “ $\downarrow$ ”         | tIRRQ  | 100 |     |     | $\mu$ s |
| From RQN “ $\downarrow$ ” to SCLK “ $\downarrow$ ”        | tWSC   | 500 |     |     | ns      |
| From SCLK “ $\uparrow$ ” to RQN “ $\uparrow$ ”            | tSCW   | 800 |     |     | ns      |
| SI Latch Setup Time                                       | tSIS   | 200 |     |     | ns      |
| SI Latch Hold Time  | tSIH   | 200 |     |     | ns      |
| <b>AK7756 <math>\rightarrow</math> <math>\mu</math>P</b>  |        |     |     |     |         |
| Delay Time from SCLK “ $\downarrow$ ” to SO Output        | tSOS   |     |     | 200 | ns      |
| Hold Time from SCLK “ $\uparrow$ ” to SO Output (Note 32) | tSOH   | 200 |     |     | ns      |

Note 32. Except when writing to the 8th bit of command code.

### ■ $\mu$ P/EEPROM Interface (I<sup>2</sup>C BUS mode)

(Ta= Tmin~Tmax; AVDD=DVDD=3.0~3.6V, DVDD18=1.7~1.9V, VSS1=VSS2=0V; CL=20pF)

| Parameter   | Symbol  | min | typ | max | Unit    |
|---|---------|-----|-----|-----|---------|
| <b>I<sup>2</sup>C Timing</b>                              |         |     |     |     |         |
| SCL clock frequency                                       | fSCL    |     |     | 400 | kHz     |
| Bus Free Time Between Transmissions                       | tBUF    | 1.3 |     |     | $\mu$ s |
| Start Condition Hold Time<br>(prior to first Clock pulse) | tHD:STA | 0.6 |     |     | $\mu$ s |
| Clock Low Time  | tLOW    | 1.3 |     |     | $\mu$ s |
| Clock High Time   | tHIGH   | 0.6 |     |     | $\mu$ s |
| Setup Time for Repeated Start Condition                   | tSU:STA | 0.6 |     |     | $\mu$ s |
| SDA Hold Time from SCL Falling                            | tHD:DAT | 0   |     | 0.9 | $\mu$ s |
| SDA Setup Time from SCL Rising                            | tSU:DAT | 0.1 |     |     | $\mu$ s |
| Rise Time of Both SDA and SCL Lines                       | tR      |     |     | 0.3 | $\mu$ s |
| Fall Time of Both SDA and SCL Lines                       | tF      |     |     | 0.3 | $\mu$ s |
| Setup Time for Stop Condition                             | tSU:STO | 0.6 |     |     | $\mu$ s |
| Pulse Width of Spike Noise Suppressed<br>by Input Filter  | tSP     | 0   |     | 50  | ns      |
| Capacitive load on bus                                    | Cb      |     |     | 400 | pF      |

Note 33. I<sup>2</sup>C-bus is a trademark of NXP B.V.

■ Timing Diagram

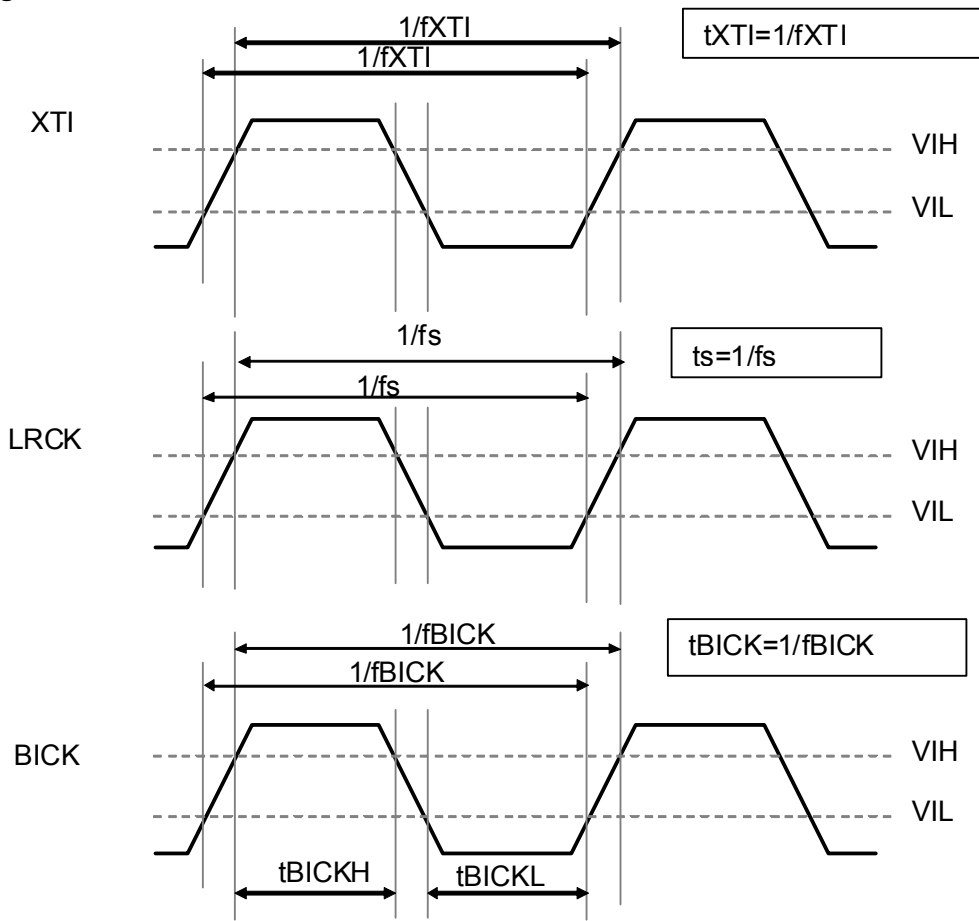


Figure 2. System Clock

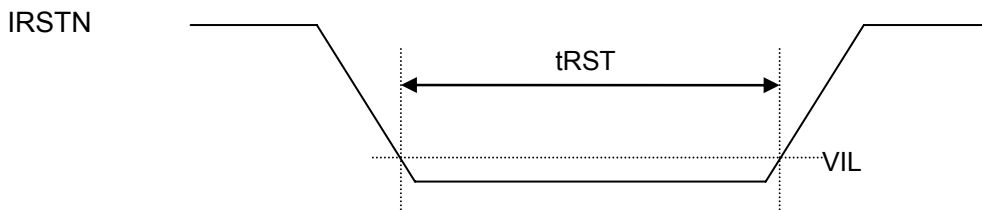


Figure 3. Reset Timing

Note 34. Set the IRSTN pin = "L" when power up and down the AK7756.

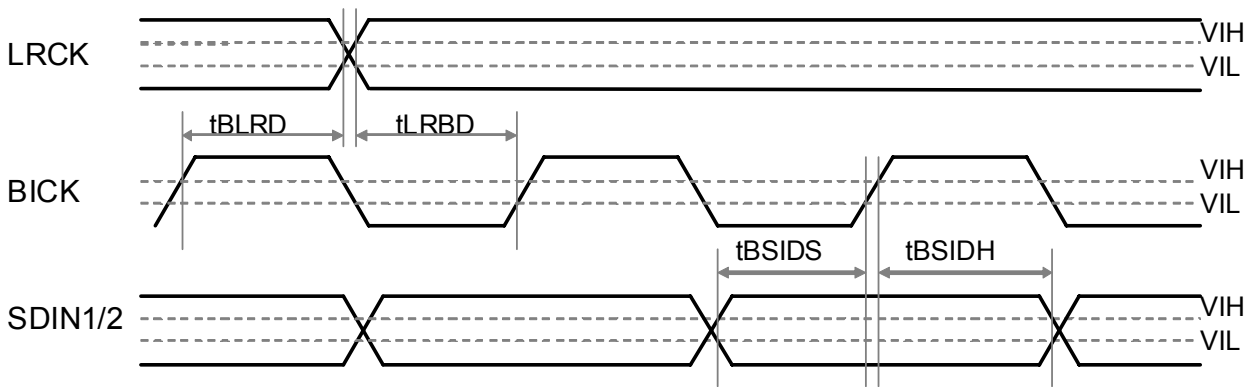


Figure 4. Audio Interface (Slave Mode Input)

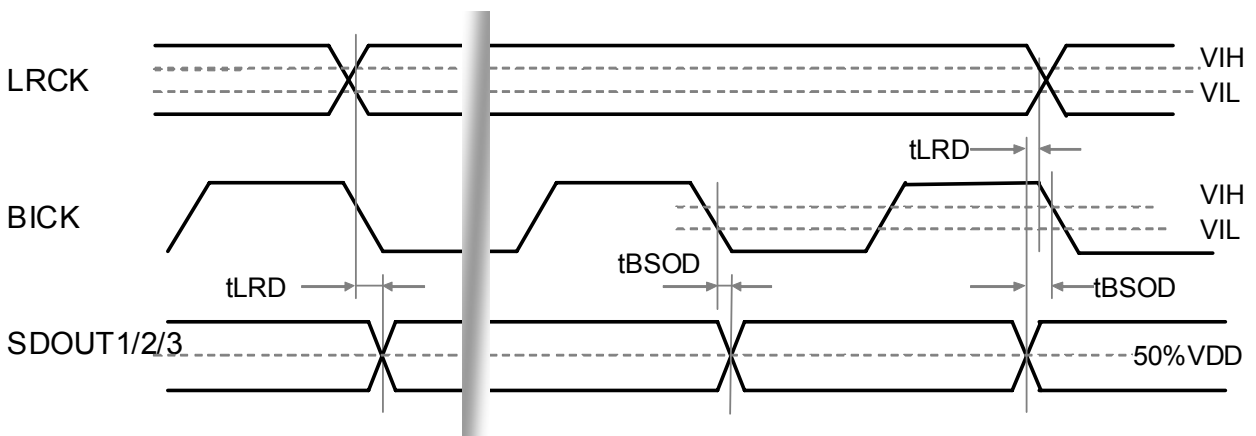


Figure 5. Audio Interface (Slave Mode Output)

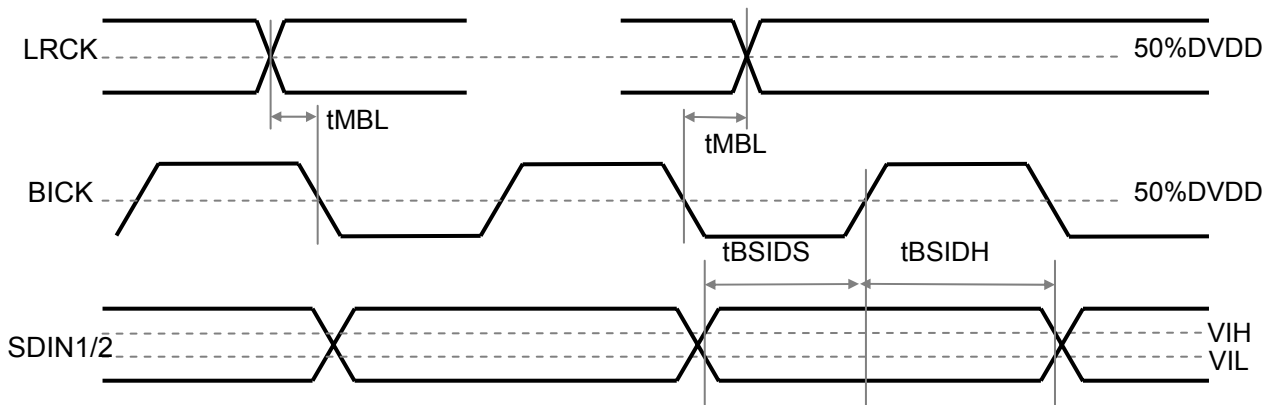


Figure 6. Audio Interface (Master Mode Input)

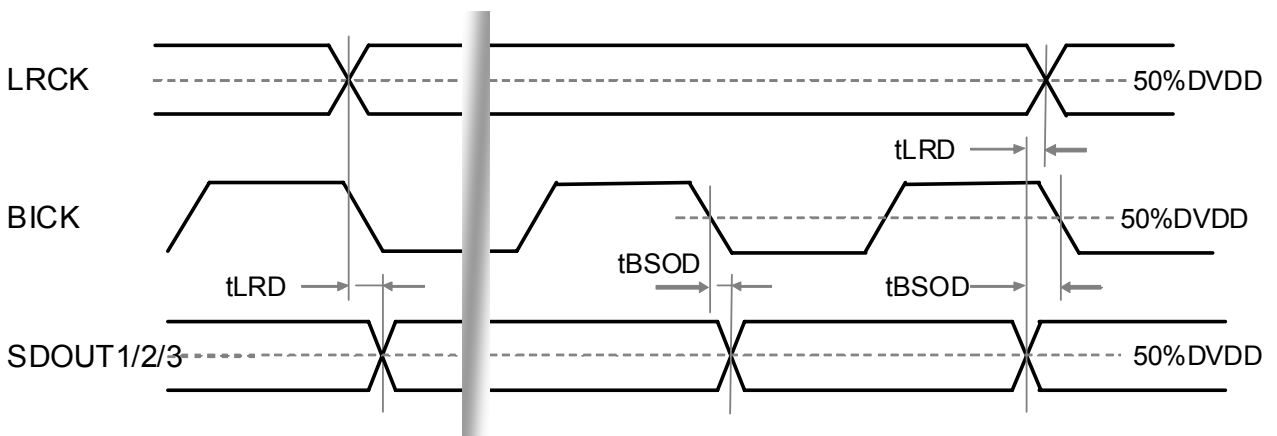


Figure 7. Audio Interface (Master Mode Output)

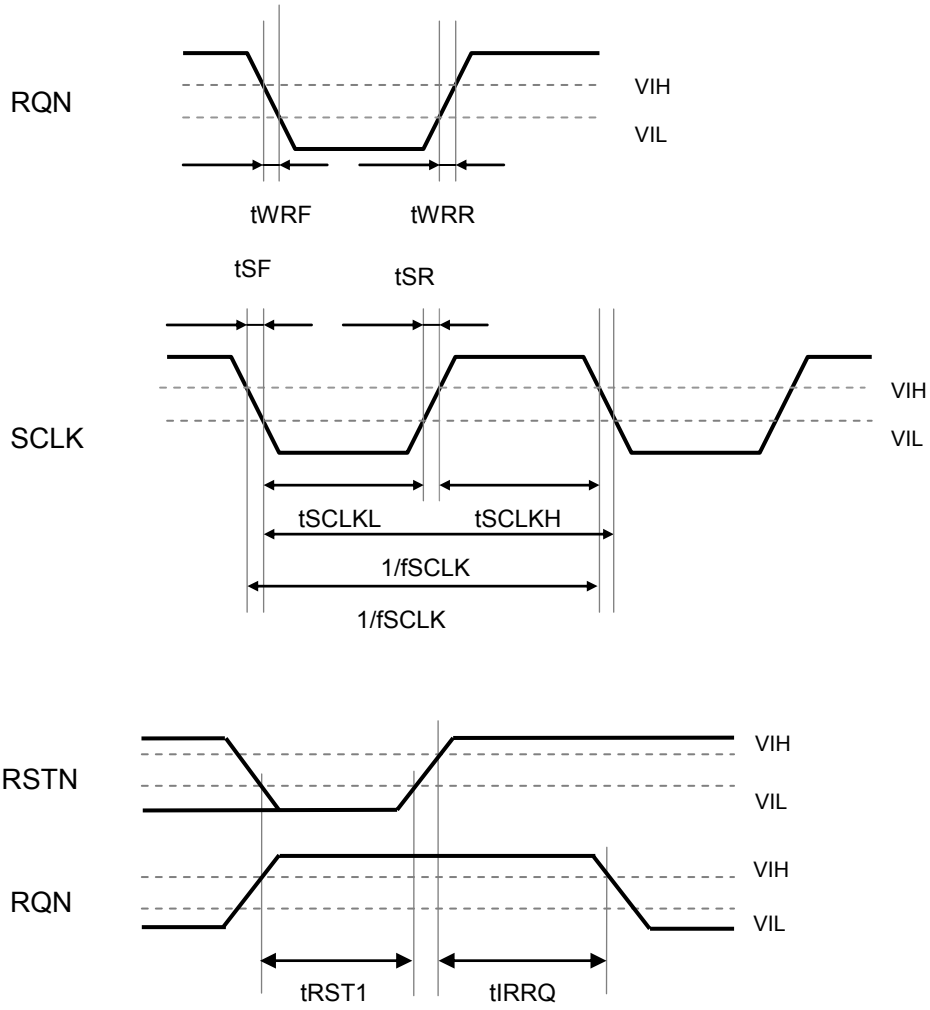


Figure 8.  $\mu$ P Interface 1 (SPI)

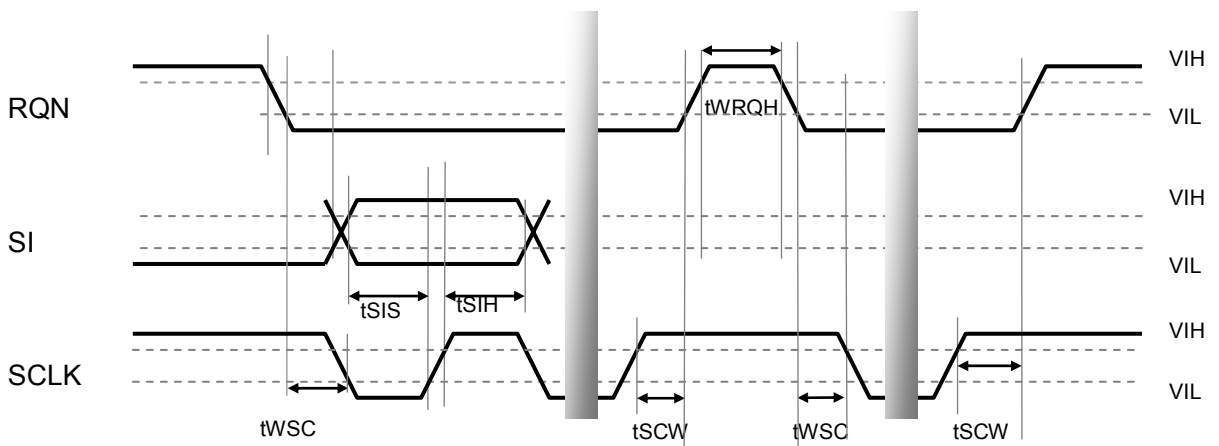


Figure 9.  $\mu$ P Interface 2 (SPI)

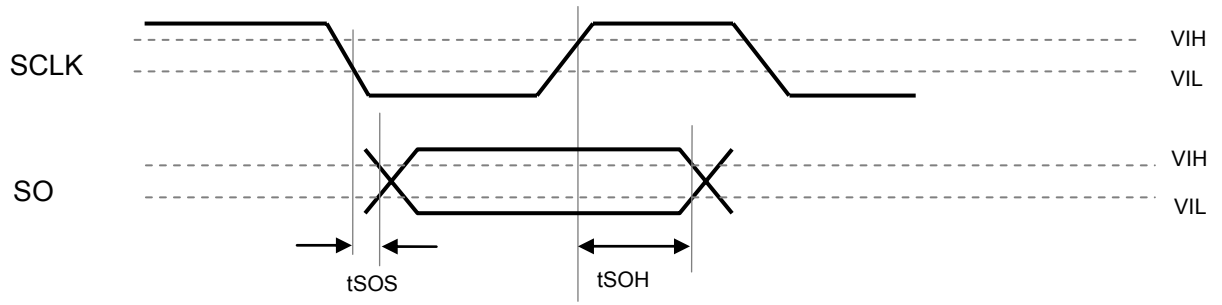


Figure 10.  $\mu$ P Interface 3 (SPI)

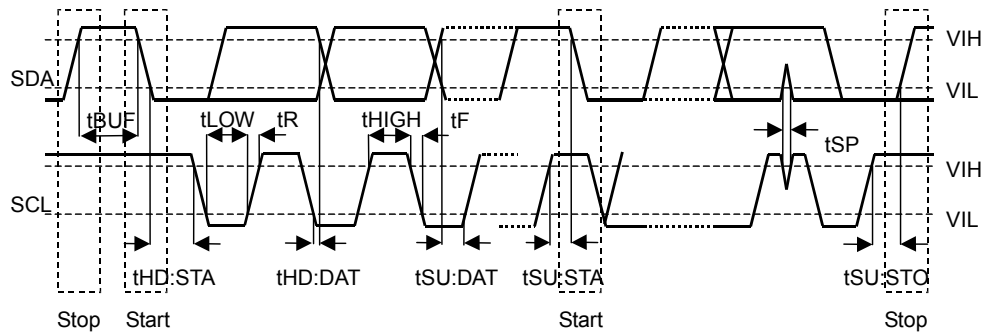
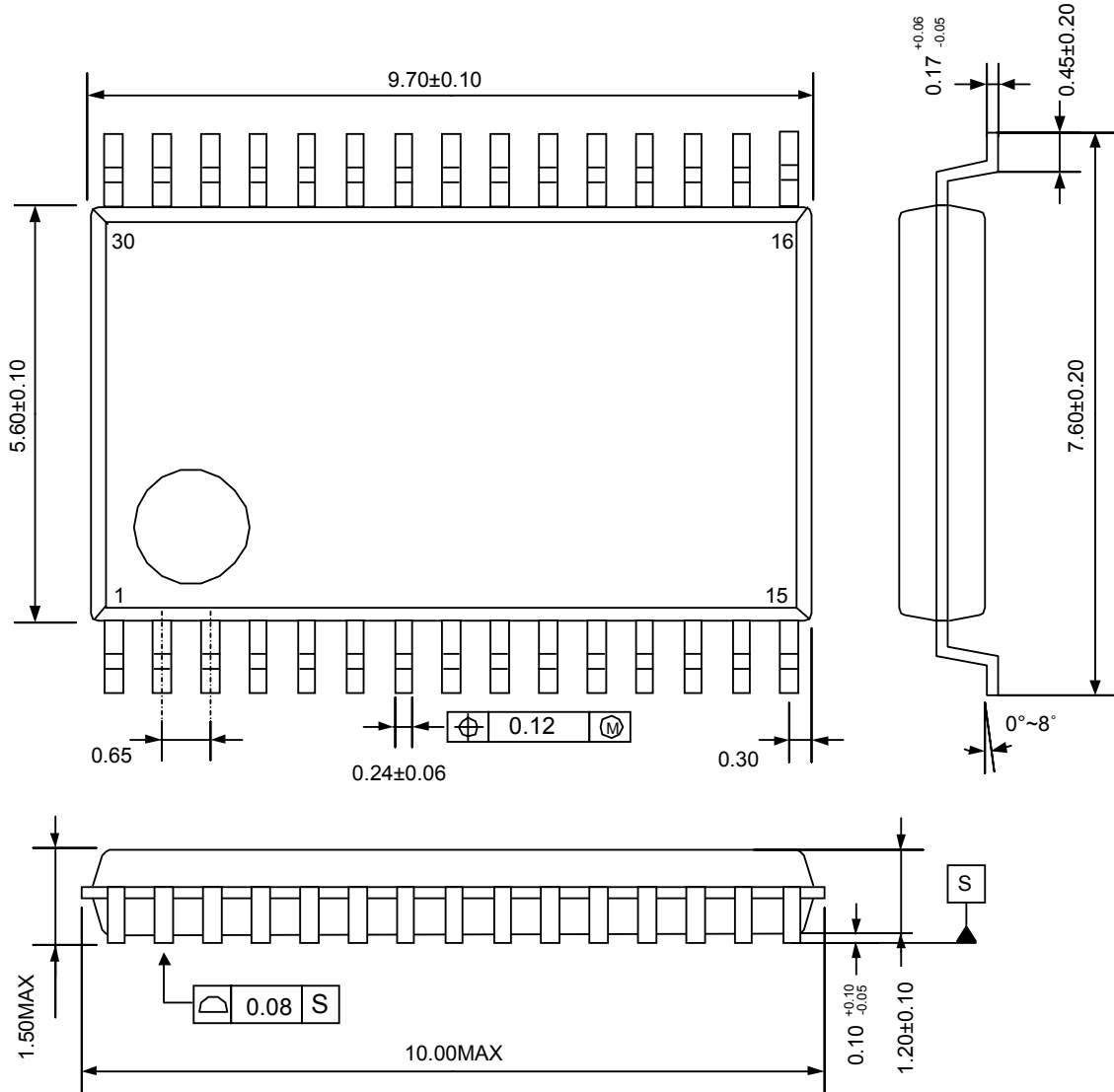


Figure 11.  $\mu$ P Interface ( $I^2C$  Bus)



**PACKAGE (AK7756VF)**

30Pin VSOP (Unit: mm)

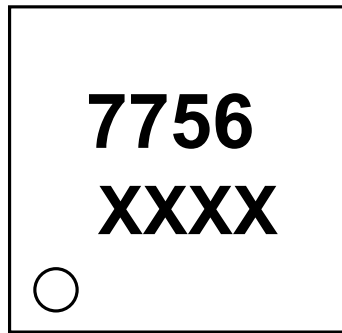


■ Package & Lead frame material

- Package molding compound: Epoxy
- Lead frame material: Cu
- Lead frame surface treatment: Solder (Pb free) plate



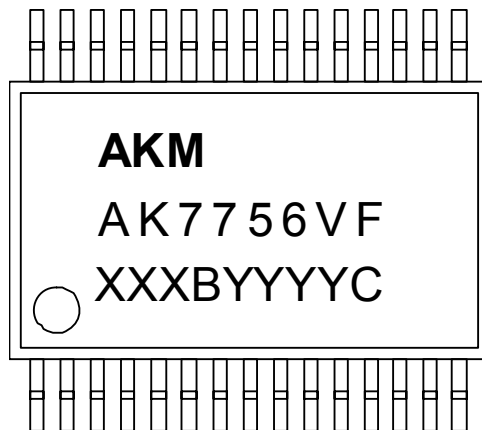
**MARKING (AK7756EN)**



1

XXXX : Date code identifier (4 digits)

**MARKING (AK7756VF)**



- 1) AKM Logo
- 2) Marketing Code: AK7756VF
- 3) Pin #1 identification
- 4) Date Code: XXXBYYYYC

XXXB: Lot number (X: Digit number, B: Alpha character)  
YYYYC: Assembly date (Y: Digit number, C: Alpha character)

|                         |
|-------------------------|
| <b>REVISION HISTORY</b> |
|-------------------------|

| Date (YY/MM/DD) | Revision | Reason        | Page | Contents |
|-----------------|----------|---------------|------|----------|
| 10/08/18        | 00       | First Edition |      |          |

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