512Kx37 Static RAM CMOS, High Speed Module

FEATURES

- 512Kx37 bit CMOS Static RAM
  - Access Times: 45 and 55ns
  - Individual Byte Selects
  - Fully Static, No Clocks
  - TTL Compatible I/O
- High Density Package
  - 72 lead SIMM, No. 418
  - Common Data Inputs and Outputs
- Single +5V (±10%) Supply Operation

DESCRIPTION

The EDI9F37512C is a high speed 20 megabit Static RAM module organized as 512K words x 37 bits. This module is constructed from five 512Kx8 Static RAMs in TSOP packages on an epoxy laminate (FR4) board.

Four write selects (W0-W3) are used to independently enable the four bytes. Reading and writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

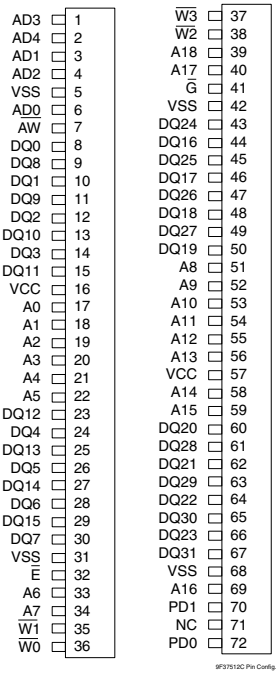
The EDI9F37512C is offered in a 72 lead SIMM which allows 20 megabits of memory to be placed in less than 1.5 square inch of board space.

All inputs and outputs are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry requires no clocks or refreshing for operation and provides equal access and cycle times for ease of use.

The SIMM module contains two Presence Detect pins which are used to identify module memory density in applications where alternate modules can be interchanged.

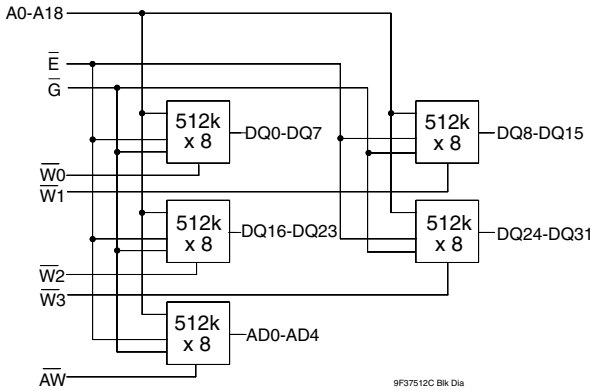
FIG. 1

PIN CONFIGURATIONS AND BLOCK DIAGRAM



PIN NAMES

AØ-A18	Address Inputs
$\overline{E}$	Chip Enables
$\overline{W0}$-$\overline{W3}$	Write Enable
$\overline{AW}$	Parity Write Enable
$\overline{G}$	Output Enable
DQØ-DQ31	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground
PD0-PD1	Presence Detect



AC CHARACTERISTICS READ CYCLE

Parameter	Symbo JEDEC	Alt.	45ns Min	45ns Max	55ns Min	55ns Max	Units
Read Cycle Time	TAVAV	TRC	45		55		ns
Address Access Time	TAVQV	TAA		45		55	ns
Chip Enable Access	TELQV	TACS		45		55	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	3		3		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ		18		25	ns
Output Hold from Address Change	TAVQX	TOH	3		3		ns
Output Enable to Output Valid	TGLQV	TOE		15		25	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	0		0		ns
Output Disable to Output in High Z(1)	TGHQZ	TOHZ		15		15	ns

Notes: 1. Parameter guaranteed, but not tested.

FIG. 2

READ CYCLE 1 - $\overline{W}$ HIGH, $\overline{G}$, $\overline{E}$ LOW

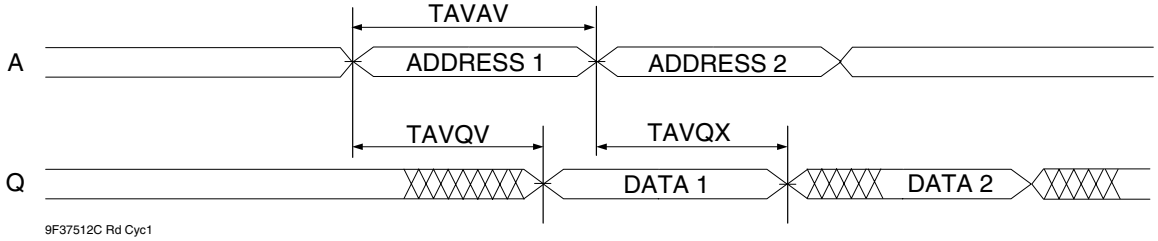
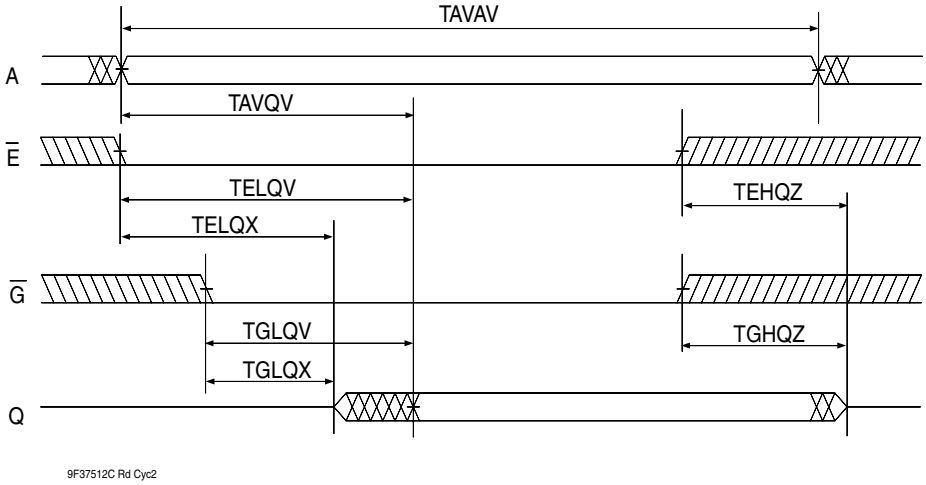


FIG. 3

READ CYCLE 2 - $\overline{W}$ HIGH



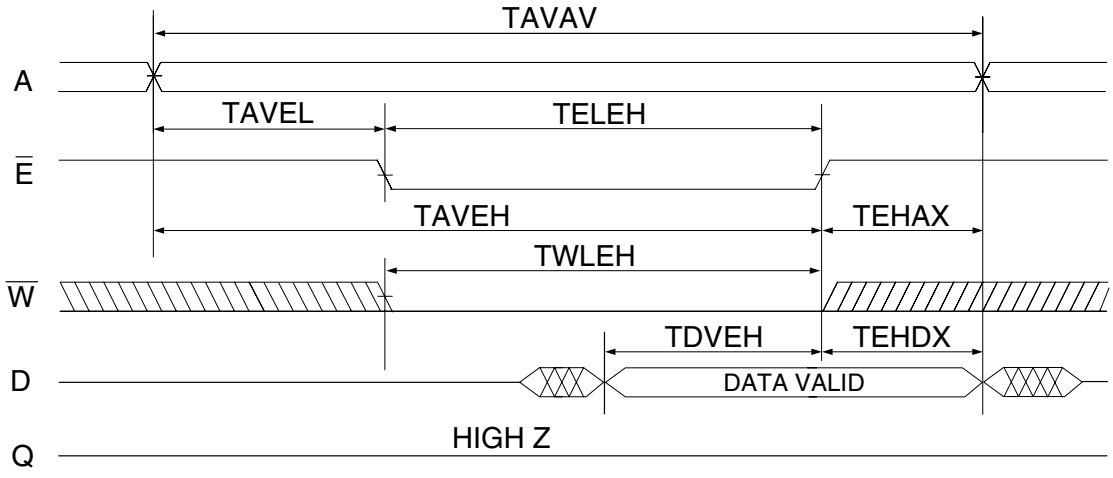
AC CHARACTERISTICS WRITE CYCLE

Parameter	Symbol JEDEC	Alt.	45ns Min	45ns Max	55ns Min	55ns Max	Units
Write Cycle Time	TAVAV	TWC	45		55		ns
Chip Enable to End of Write	TELWH	TCW	25		45		ns
	TWLEH	TCW	25		45		ns
Address Setup Time	TAVWL	TAS	0		0		ns
	TAVEL	TAS	0		0		ns
Address Valid to End of Write	TAVWH	TAW	25		45		ns
	TAVEH	TAW	25		45		ns
Write Pulse Width	TWLWH	TWP	25		40		ns
	TELEH	TWP	25		40		ns
Write Recovery Time	TWHAX	TWR	0		0		ns
	TEHAX	TWR	0		0		ns
Data Hold Time	TWHDX	TDH	0		0		ns
	TEHDX	TDH	0		0		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	6	0	28	ns
Data to Write Time	TDVWH	TDW	20		30		ns
	TDVEH	TDW	20		30		ns
Output Active from End of Write (1)	TWHQX	TWLZ	3		3		ns

Notes: 1. Parameter guaranteed, but not tested.

FIG. 4

WRITE CYCLE 2 - $\overline{E}$ CONTROLLED



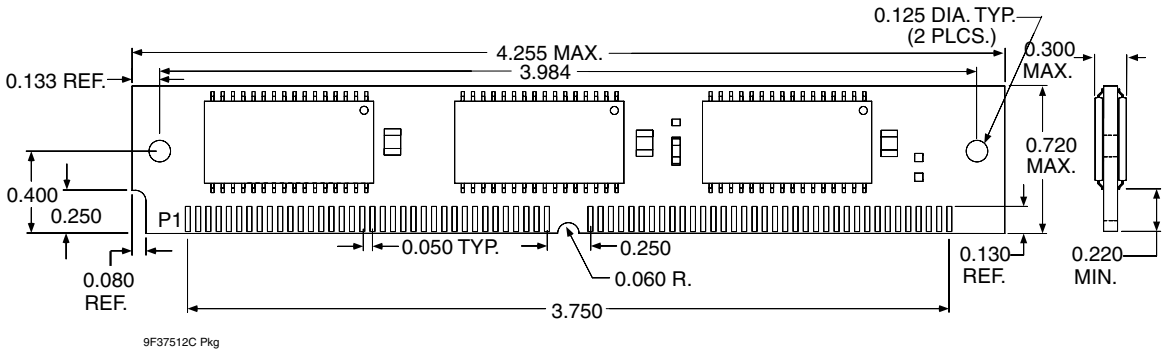
9F37512C Write Cyc2

ORDERING INFORMATION

Part Number	Speed (ns)	Package No.
EDI9F37512C45MMC	45	418
EDI9F37512C55MMC	55	418

PACKAGE DESCRIPTION

PACKAGE NO. 418: 72 PIN ZIP



ALL DIMENSIONS ARE IN INCHES

DATASHEET APPROVALS

EDI PART NO. ED19F37512C ECO# 15655 NEW REV 4A DATE 10/8/02

APPROVAL:	INITIAL	DATE	CORRECTION ON PAGES
~~JUAN GUZMAN~~ L.K.			
~~MUKESH TRIVEDI~~ M.A.			
PAUL MARIEN			
LARRY WINROTH			
DAVE KELLY			
MARK DOWNEY			
DAVE HARRISON			
TONY LEE			
BOB KHEDERIAN			
LUIS ESTELLA			

	YES	NO
WILL THIS DATASHEET GO ON THE WEB?		
IS THIS A NEW DATASHEET?		
WILL THIS DATASHEET REPLACE AN EXISTING DATASHEET THAT'S ALREADY ON THE WEB?		

LINE:_____
FAMILY:_____
PROD.TYPE:_____
ORG:_____
DENSITY:_____
SPEED:_____
PKG:_____
VOLTAGE:_____

IF YES, WHAT DATASHEET IS IT REPLACING? _____

WHAT SECTION SHOULD THIS DATASHEET BE PLACED IN ON THE WEB? _____

AFTER REVIEWING OR MAKING CORRECTIONS ON THE DATASHEET (S)
PLEASE SIGN-OFF ON THIS SHEET AND ,MAKE YOUR CORRECTIONS –ON **THE ORIGINAL COPY(S).**

AFTER REVIEWING THE DATA SHEET, TEST ENGINEERING WILL COMPLETE THE SECTION BELOW.

TEST PROGRAM CHANGE REQUIRED:
YES:_____NO_____DATE:_____

TEST ENGINEER SIGNATURE_____

IF YES, DO NOT RELEASE DATA SHEET UNTIL TEST PROGRAM CHANGE IS COMPLETED.
TEST PROGRAM CHANGE COMPLETION DATE:_____
TEST PROGRAM NAME AND REVISION_____
TEST ENGINEER SIGNATURE_____