Power Supply ICs for TFT-LCD Panels

Multi-channel System Power Supply IC for Small to Middle PANEL

BD8184MUV

No.11035EAT18

●Description

The BD8184MUV is a system power supply for the TFT-LCD panels used for liquid crystal Monitors and Note Display. Incorporates high-power FET with low on resistance for large currents that employ high-power packages, thus driving large current loads while suppressing the generation of heat. A charge pump controller is incorporated as well, thus greatly reducing the number of application components. Also Gate Shading Function is included.

●Features

1) Boost DC/DC converter; 18 V / 2.5 A switch current. (Target specification is ±1% accurate.)
2) Switching frequency: 1.2 MHz
3) Operational Amplifier (short current 200mA)
4) Incorporates Positive / Negative Charge-pump Controllers.
5) Gate Shading Function
6) VQFN024V4040 Package (4.0 mm x 4.0 mm)
7) Protection circuits: Under Voltage Lockout Protection Circuit
   Thermal Shutdown Circuit (Latch Mode)
   Over Current Protection Circuit (AVDD)
   Timer Latch Mode Short Circuit Protection (AVDD SRC VGL)
   Over / Under Voltage Protection Circuit for Boost DC/DC Output
   No SCP time included (160ms from UVLO-off)

●Applications

Power supply for the TFT-LCD panels used for LCD Monitors and Note Display

●**Absolute Maximum Ratings** (T_A = 25℃)

Parameter	Symbol	LIMIT	Unit
Supply Voltage 1	VIN	+7	V
Supply Voltage 2	AVDD	+20	V
Supply Voltage 3	SRC	+36	V
Switching Voltage	SW, DRP, DRN	+20	V
Input Voltage 1	RSTIN, DLY, CTL, FB, FBP, FBN	VIN+0.3	V
Input Voltage 2	INN, INP	+20	V
Output Voltage 1	RST, COMP, VREF	+7	V
Output Voltage 2	VCOM	+20	V
Output Voltage 3_1	GSOUT	+36	V
Output Voltage 3_2	SRC - GSOUT	+40	V
Junction Temperature	Tjmax	150	℃
Power Dissipation	Pd	3560*1	mW
Operating Temperature Range	Topr	-40～85	℃
Storage Temperature Range	Tstg	-55～150	℃

*1 Derating in done 28.5mW/℃ for operating above Ta≧25℃(On 4-layer 74.2mm×74.2mm×1.6mm board)

●**Operating Range** (Ta=-40℃～85℃)

Parameter	Symbol	MIN	MAX	Unit
Supply Voltage 1	VIN	2.0	5.5	V
Supply Voltage 2	AVDD	6	18	V
Supply Voltage 3	SRC	12	34	V

●**Electrical characteristics** (unless otherwise specified VIN = 3.3V, AVDD = 10V and TA=25℃)

Parameter	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
GENERAL						
Circuit Current	I_{VIN}	-	1.2	3	mA	No Switching
Under Voltage Lockout Threshold	V_{UVLO}	1.75	1.85	1.95	V	VIN rising
Internal Reference Output Voltage	VREF	1.238	1.250	1.262	V	No laod
Thermal Shutdown (rising)	TSD	-	160	-	℃	Junction Temp
Duration to Trigger Fault Condition	T_{SCP}	-	55	-	ms	FB , FBP or FBN below threshold
BOOST CONVERTER (AVDD)						
FB Regulation Voltage	V_{FB}	1.238	1.250	1.262	V	Voltage follower
FB Fault Trip Level	V_{TL_FB}	0.95	1.0	1.05	V	VFB falling
FB Input Bias Current	I_{FB}	-	0.1	1	μA	VFB= 1.5V
SW Leakage Current	I_{SW_L}	-	0	10	μA	VSW=20V
Maximum switching Duty Cycle	M_{DUTY}	85	90	95	%	VFB= 1.0V
SW ON-Resistance	R_{SW}	-	200	-	mΩ	ISW= 200mA
SW Current Limit	I_{SWLIM}	2.5	-	-	A	
Over Voltage Protection	V_{OVP}	-	20	-	V	AVDD rising
Under Voltage Protection	V_{UVP}	1.3	1.6	1.9	V	AVDD falling
BOOST Soft Start Time	T_{SS_FB}	-	13.6	-	ms	
Oscillator frequency	F_{SW}	1.0	1.2	1.4	MHz	
RESET						
RST Output Low Voltage	V_{RST}	-	0.05	0.2	V	IRST =1.2mA
RSTIN Threshold Voltage	V_{TH_L}	1.18	1.25	1.32	V	RSTIN falling
RSTIN Input Current	I_{RSTIN}	-	0	-	μA	VRSTIN=0 to VIN-0.3
RST Blanking Time	T_{NO_SCP}	146	163	180	ms	No SCP Zone
Operational Amp rifer						
Input Range	V_{RANGE}	0	-	AVDD	V	
Offset Voltage	V_{OS}	-	2	15	mV	VINP= 5.0V
Input Current	I_{INP}	-	0	-	μA	VINP= 5.0V
Output Swing Voltage (VINP= 5.0V)	V_{OH}	-	5.03	5.06	V	ICOM = +50mA
	V_{OL}	4.94	4.97	-	V	ICOM = -50mA
Short Circuit Current	I_{SHT_VCOM}	-	200	-	mA	
Slew Rate	SR	-	40	-	V/us	

●**Electrical characteristics** (unless otherwise specified VIN = 3.3V, AVDD = 10V and T_A=25℃) (Continued)

Parameter	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
Negative Charge pump driver (VGL)						
FBN Regulation Voltage	V_{FBN}	235	250	265	mV	
FBN Fault Trip Level	V_{TL_FBN}	400	450	500	mV	V_{FBN} rising
FBN Input Bias Current	I_{FBN}	-	0.1	1	μA	V_{FBN}= 0.1V
Oscillator frequency	F_{CPN}	500	600	700	kHz	
DRN Leakage Current	I_{DRN_L}	-	0	10	μA	V_{FBN}=1.0V
Positive Charge pump driver (SRC)						
FBP Regulation Voltage	V_{FBP}	1.23	1.25	1.27	V	
FBP Fault Trip Level	V_{TL_FBP}	0.95	1.0	1.05	V	V_{FBP} falling
FBP Input Bias Current	I_{FBP}	-	0.1	1	μA	V_{FBP}= 1.5V
Oscillator frequency	F_{CPP}	500	600	700	kHz	
DRP Leakage Current	I_{DRP_L}	-	0	10	μA	V_{FBP}= 1.5V
Soft-Start Time	T_{SSP}	-	3.4	-	ms	
Gate Shading Function (GSOUT)						
DLY Source Current	I_{DLY}	4	5	6	μA	
DLY Threshold Voltage	V_{TL_DLY}	1.22	1.25	1.28	V	V_{DLY} falling
CTL Input Voltage High	V_{IN_H}	2.0	-	-	V	
CTL Input Voltage Low	V_{IN_L}	-	-	0.5	V	
CTL Input Bias Current	I_{CTL}	-	0	-	μA	VRSTIN=0 to VIN-0.3
Propagation delay time (Rising)	T_{GS_R}	-	100	-	ns	V_{SRC}= 25V
Propagation delay time (Falling)	T_{GS_F}	-	100	-	ns	V_{SRC}= 25V
SRC -GSOUT ON Resistance	R_{GS_H}	-	15	-	Ω	V_{DLY} = 1.5V
GSOUT-RE ON Resistance	R_{GS_M}	-	30	-	Ω	V_{DLY} = 1.5V
GSOUT-GND ON Resistance	R_{GS_L}	-	2.5	-	kΩ	V_{DLY} = 1.0V

○This product is not designed for protection against radio active rays.

●Electrical characteristic curves (Reference data)

(Unless otherwise specified VIN = 3.3V, AVDD = 10V and T_A=25℃)

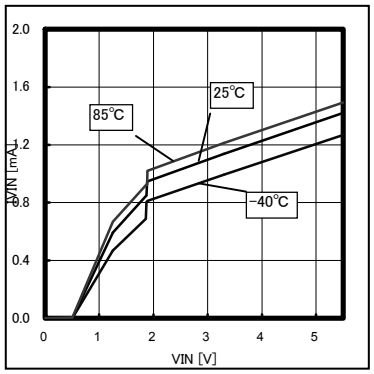


Fig.1 Curcuit Current (No switching)

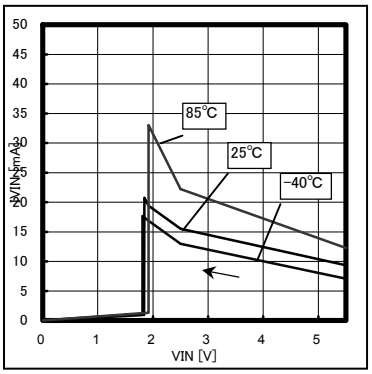


Fig.2 Curcuit Current (Switching)

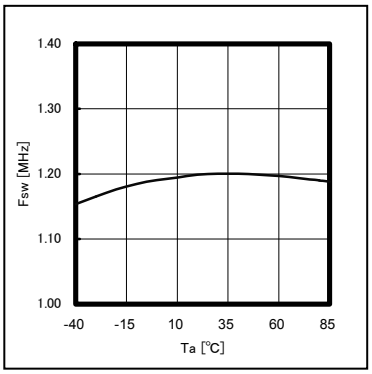


Fig.3 Dependent on Temparactue Freqency

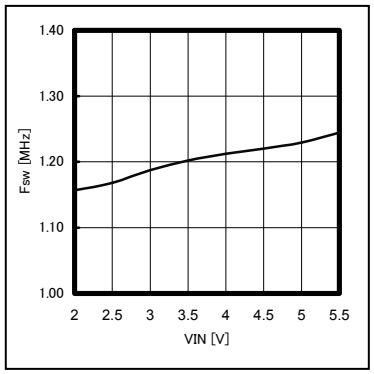


Fig.4 Dependent on Input Voltage Freqency

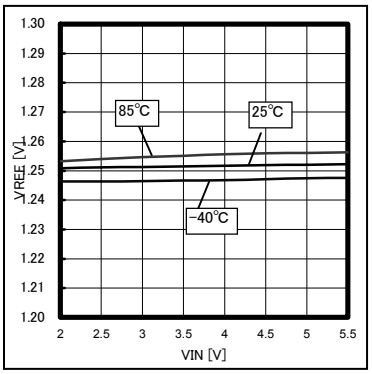


Fig.5 VREF Line Regulation

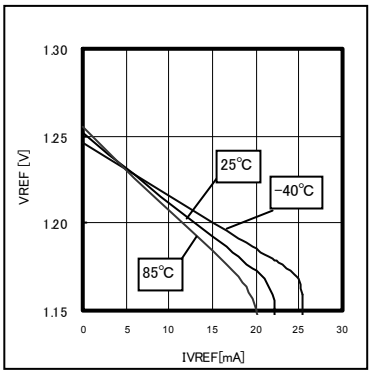


Fig.6 VREF Load Regulation

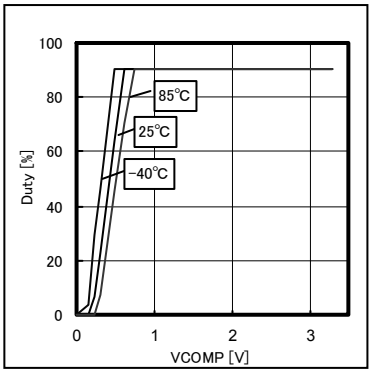


Fig.7 COMP V.S.CDUTY

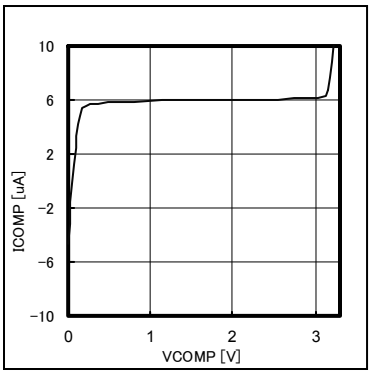


Fig.8 COMP Sink Current

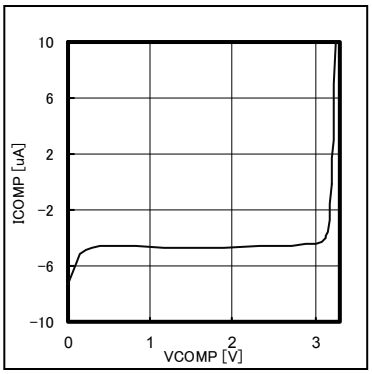


Fig.9 COMP Source Current

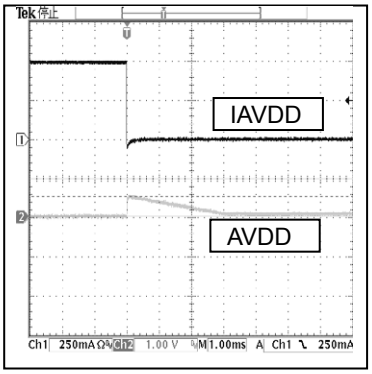


Fig.10 Load Transient Response Falling

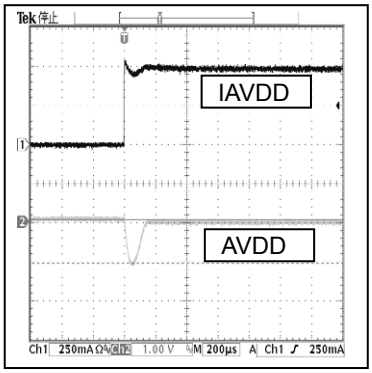


Fig.11 Load Transient Response Rising

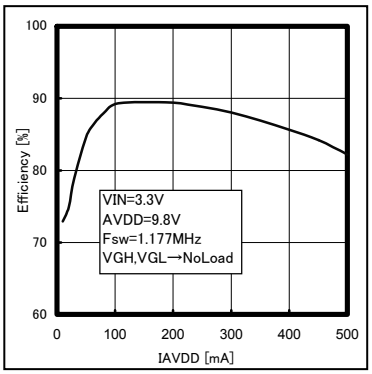


Fig.12 Boost Converter Efficiency

●**Electrical characteristic curves (Reference data) – Continued**

(Unless otherwise specified VIN = 3.3V, AVDD = 10V and T_A=25℃)

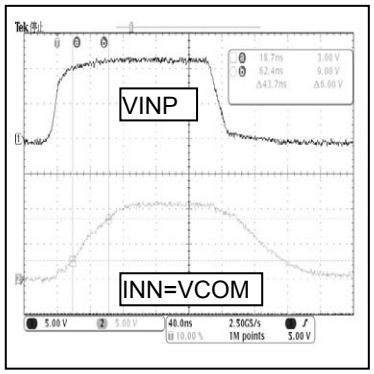


Fig.13 VCOM Slew Rate
（Rising）

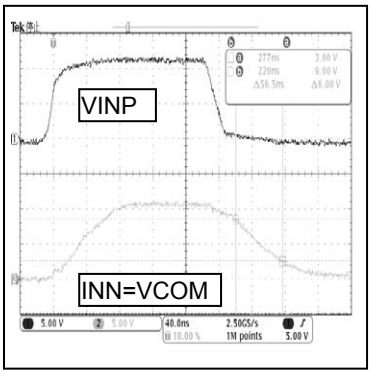


Fig.14 VCOM Slew Rate
（falling）

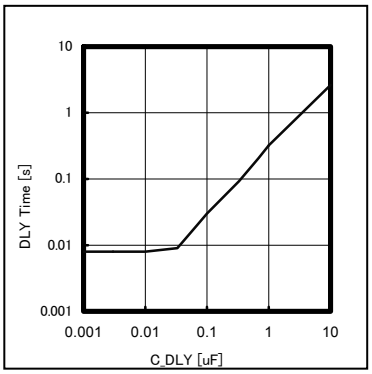


Fig.15 C_DLY vs. delay time

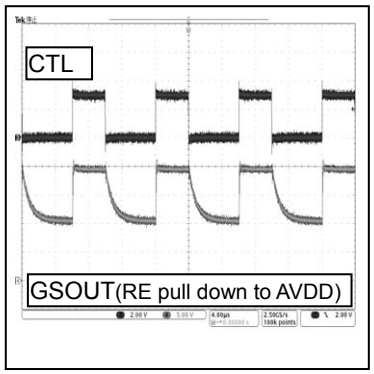


Fig. 16 Gate Sharding Wave form1

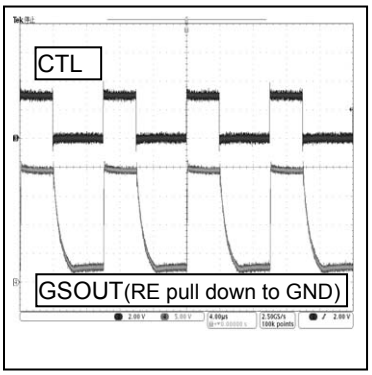


Fig.17 Gate Sharding Wave form2

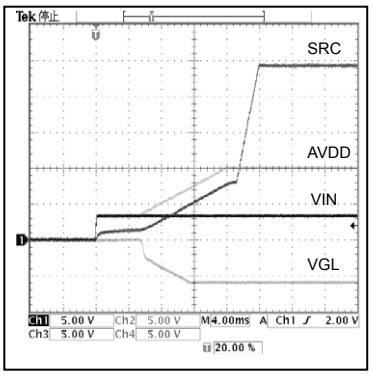


Fig.18 Power On Sequence1
(Main Output)

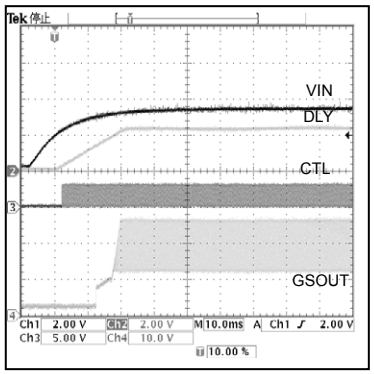


Fig.19 Power On Sequence2
(CTL=signal, RE pull down to AVDD)

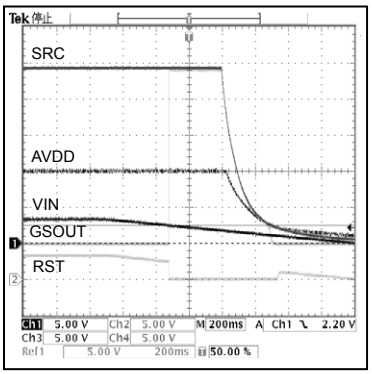


Fig.20 Power Off Sequence1
(R_RST_U=10k,R_RST_D=10k)

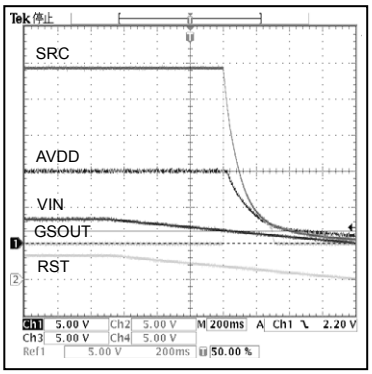


Fig.21 Power Off Sequence2
(R_RST_U=10k,R_RST_D=OPEN)

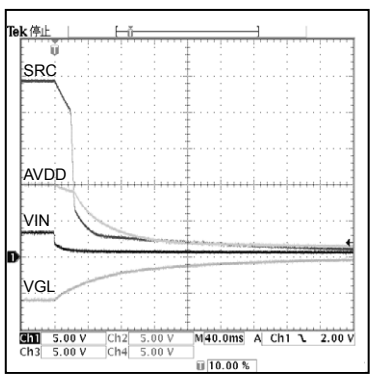


Fig.22 Power On Sequence3
(Main Output)

●Block Diagram

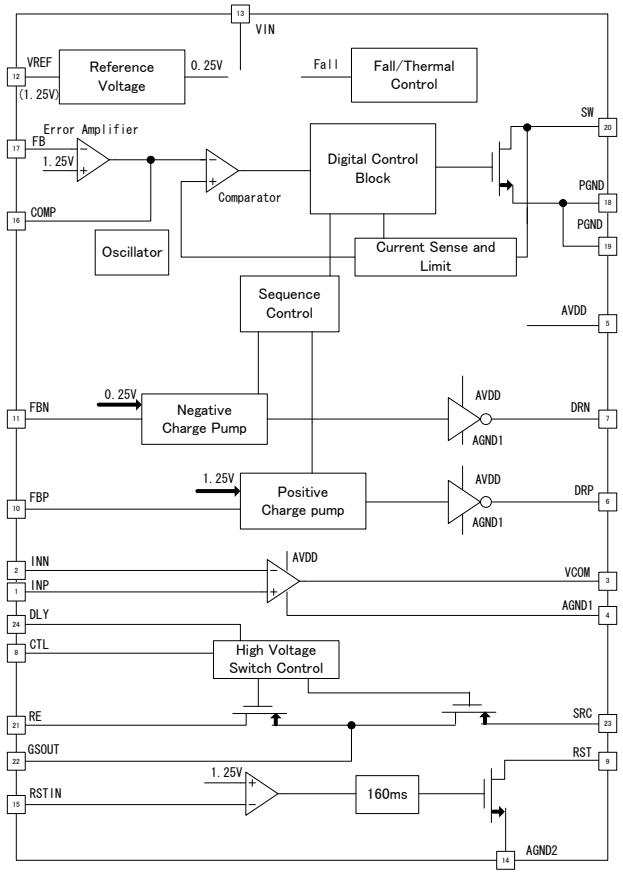


Fig.23 Block Diagram

●Pin Configuration

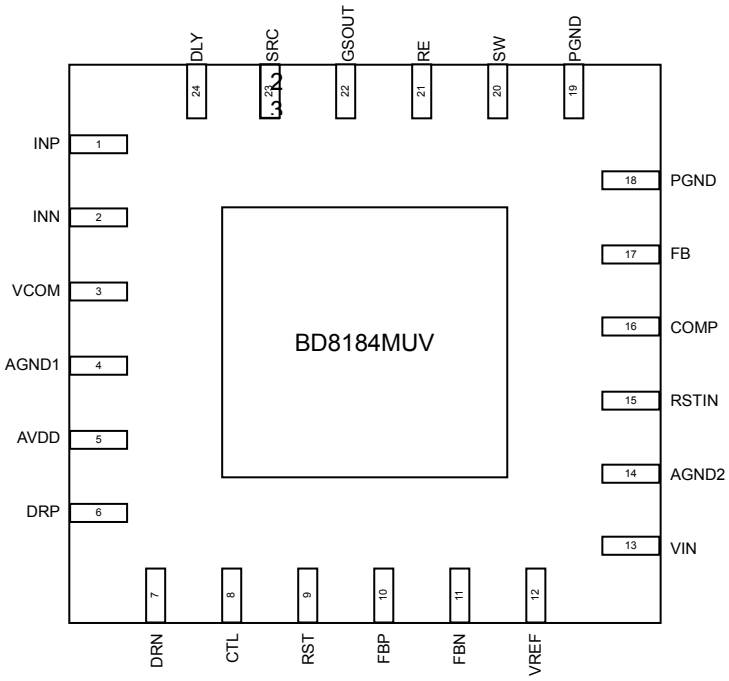


Fig.24 Pin Configuration

●Package Dimension

VQFN024V4040

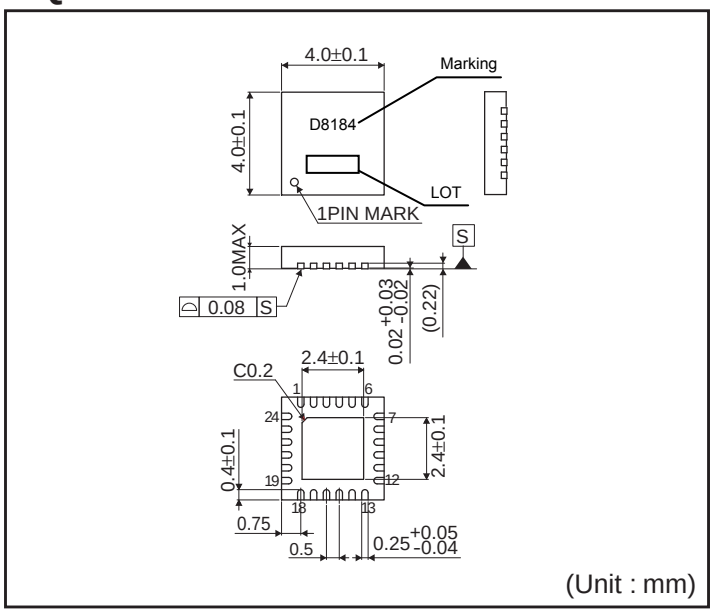


Fig.25 Package Dimension (UNIT : mm)

●Pin Assignments

PINNO.	Pin name	Function
1	INP	COM Amplifier input +
2	INN	COM Amplifier input -
3	VCOM	COM Amplifier output
4	AGND1	Ground
5	AVDD	Supply voltage input for com, charge pump
6	DRP	Drive pin of the positive charge pump
7	DRN	Drive pin of the negative charge pump
8	CTL	High voltage switch control pin
9	RST	Open drain reset output
10	FBP	Positive charge pump feed back
11	FBN	Negative charge pump feed back
12	VREF	Internal Reference voltage output
13	VIN	Supply voltage input for PWM
14	AGND2	Ground
15	RSTIN	Reset comparator input
16	COMP	BOOST amplifier output
17	FB	BOOST amplifier input
18	PGND1	BOOST FET ground
19	PGND2	BOOST FET ground
20	SW	BOOST FET Drain
21	RE	Gate High voltage Fall set pin
22	GSOUT	Gate High voltage output set pin
23	SRC	Gate High voltage input set pin
24	DLY	GSOUT Delay Adjust pin

●Main Block Function

・Boost Converter
A controller circuit for DC/DC boosting.
The switching duty is controlled so that the feedback voltage FB is set to 1.25 V (typ.).
A soft start operates at the time of starting.

・Positive Charge Pump
A controller circuit for the positive-side charge pump.
The switching amplitude is controlled so that the feedback voltage FBP will be set to 1.25 V (typ.).

・Negative Charge Pump
A controller circuit for the negative-side charge pump.
The switching amplitude is controlled so that the feedback voltage FBN will be set to 0.25 V (Typ.).

・Gate Shading Controller
A controller circuit for P-MOS FET Switch
The GSOUT switching synchronize with CTL input.
When VIN drops below UVLO threshold or RST=Low(=RSTIN<1.25V), GSOUT is pulled High(=SRC).

・VCOM
A 1-channel operational amplifier block.

・Reset
A open-drain output(RST) refer from RSTIN voltage(up to threshold voltage 1.25V)
RST is keep High(need a pull-up resistor connected to VIN) dulling to 163ms from start-up.

・VREF
A block that generates internal reference voltage of 1.25V (Typ.).
VREF is keep High when the thermal/short-current-protection shutdown circuit.

・TSD/UVLO/OVP/UVP
The thermal shutdown circuit is shut down at an IC internal temperature of 160℃.
The under-voltage lockout protection circuit shuts down the IC when the VIN is 1.85 V (Typ.) or below.
The over-voltage protection circuit when the SW is 19 V (Typ.) or over.
The under-voltage protection circuit when the SW is 1.3 V (Typ.) or under

・Start-up Controller
A control circuit for the starting sequence.
Controls to start in order of $V_{CC} \rightarrow V_{GL} \rightarrow V_{DD} \rightarrow SRC$
(Please refer to Fig.4 of next page for details.)

●Power Sequence

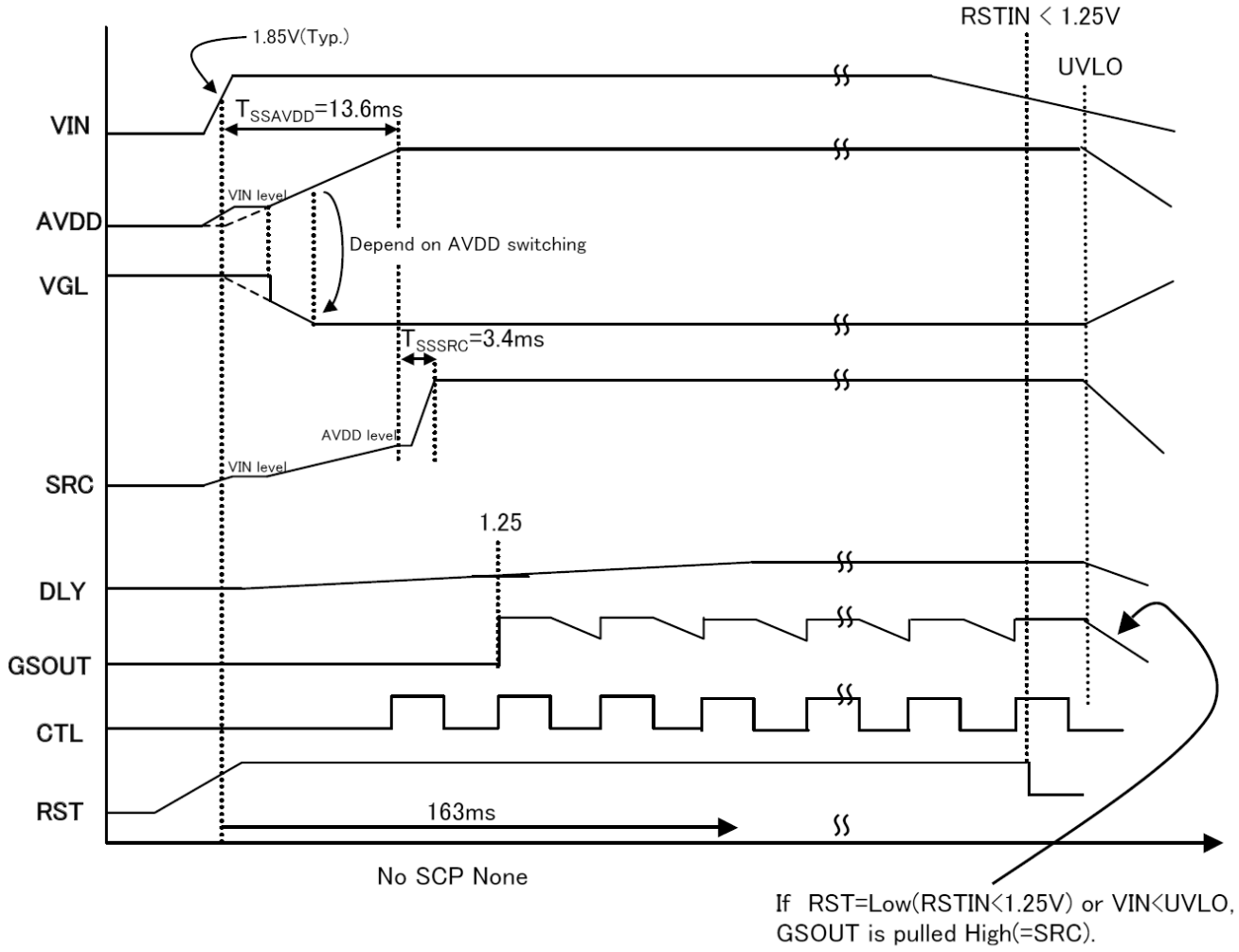


Fig.26 **Power Sequence**

●How to select parts of application

(1-1) Setting the Output L Constant (Boost Converter)

The coil to use for output is decided by the rating current I_{LR} and input current maximum value I_{INMAX} of the coil.

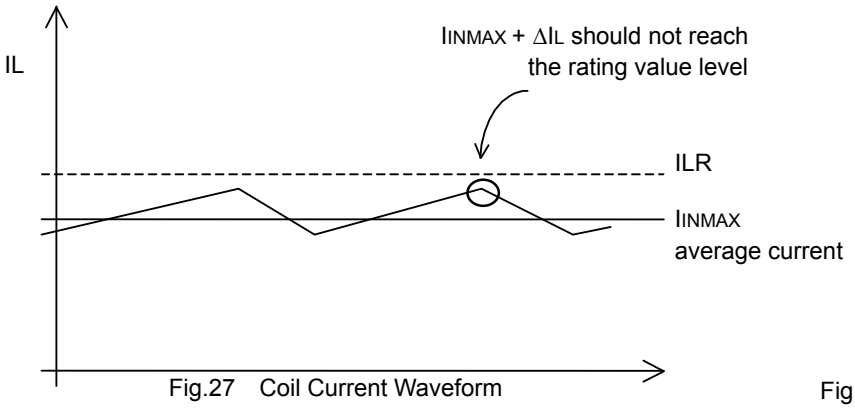


Fig.27 Coil Current Waveform

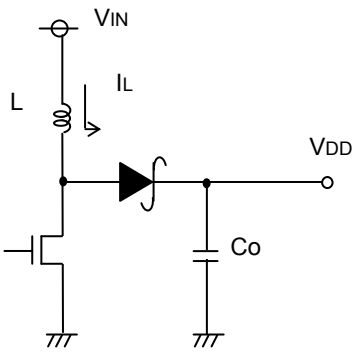


Fig. 28 Output Application Circuit Diagram

Adjust so that $I_{INMAX}+\Delta I_L$ does not reach the rating current value I_{LR}. At this time, ΔI_L can be obtained by the following equation.

$$\Delta I_L = \frac{1}{L} V_{IN} \times \frac{V_{DD}-V_{IN}}{V_{IN}} \times \frac{1}{f} \quad [A]$$

Here, f is the switching frequency.

Set with sufficient margin because the coil value may have the dispersion of ±30%. If the coil current exceeds the rating current I_{LR} of the coil, it may damage the IC internal element.

BD8164MUV uses the current mode DC/DC converter control and has the optimized design at the coil value. A coil inductance (L) of 4.7 uH to 15 uH is recommended from viewpoints of electric power efficiency, response, and stability.

(2) Output Capacity Settings

For the capacitor to use for the output, select the capacitor which has the larger value in the ripple voltage V_{PP} allowance value and the drop voltage allowance value at the time of sudden load change. Output ripple voltage is decided by the following equation.

Here, f is the switching frequency.

$$\Delta V_{PP} = I_{LMAX} \times R_{ESR} + \frac{1}{fCo} \times \frac{V_{IN}}{AVDD} \times \left(I_{LMAX} - \frac{\Delta I_L}{2}\right) \quad [V]$$

Perform setting so that the voltage is within the allowable ripple voltage range.

For the drop voltage during sudden load change; V_{DR}, please perform the rough calculation by the following equation.

$$V_{DR} = \frac{\Delta I}{Co} \times 10\ us \quad [V]$$

However, 10 μs is the rough calculation value of the DC/DC response speed. Please set the capacitance considering the sufficient margin so that these two values are within the standard value range.

(3) Selecting the Input Capacitor

Since the peak current flows between the input and output at the DC/DC converter, a capacitor is required to install at the input side. For the reason, the low ESR capacitor is recommended as an input capacitor which has the value more than 10 μF and less than 100 mΩ. If a capacitor out of this range is selected, the excessive ripple voltage is superposed on the input voltage, accordingly it may cause the malfunction of IC.

However these conditions may vary according to the load current, input voltage, output voltage, inductance and switching frequency. Be sure to perform the margin check using the actual product.

(4) Setting Rc, Cc of the Phase Compensation Circuit

In the current mode control, since the coil current is controlled, a pole (phase lag) made by the CR filter composed of the output capacitor and load resistor will be created in the low frequency range, and a zero (phase lead) by the output capacitor and ESR of capacitor will be created in the high frequency range. In this case, to cancel the pole of the power amplifier, it is easy to compensate by adding the zero point with Cc and Rc to the output from the error amp as shown in the illustration.

Open loop gain characteristics

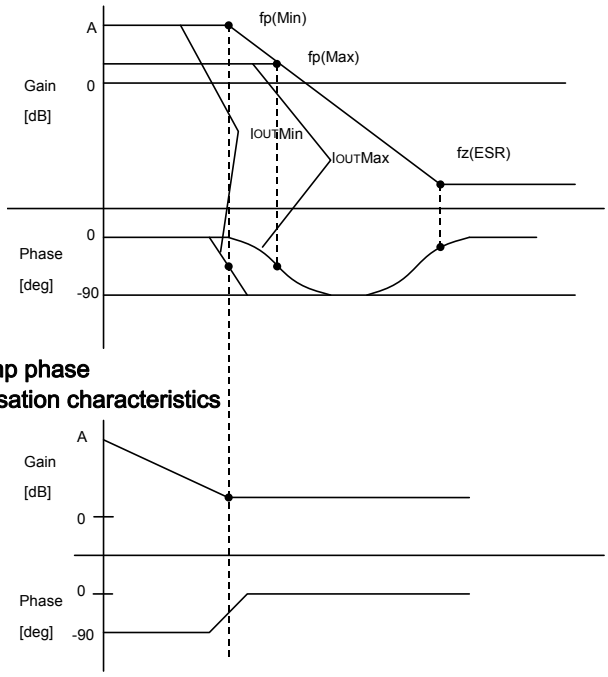


Fig. 29 Gain vs Phase

$$Fp = \frac{1}{2\pi \times RO \times CO} \text{ [Hz]}$$

$$fz(ESR) = \frac{1}{2\pi \times ESR \times CO} \text{ [Hz]}$$

Pole at the power amplification stage

When the output current reduces, the load resistance Ro increases and the pole frequency lowers.

$$fp(Min) = \frac{1}{2\pi \times ROMax \times CO} \text{ [Hz]} \leftarrow \text{at light load}$$

$$fz(Max) = \frac{1}{2\pi \times ROMin \times CO} \text{ [Hz]} \leftarrow \text{at heavy load}$$

Zero at the power amplification stage

When the output capacitor is set larger, the pole frequency lowers but the zero frequency will not change. (This is because the capacitor ESR becomes 1/2 when the capacitor becomes 2 times.)

$$fp(Amp.) = \frac{1}{2\pi \times Rc \times Cc} \text{ [Hz]}$$

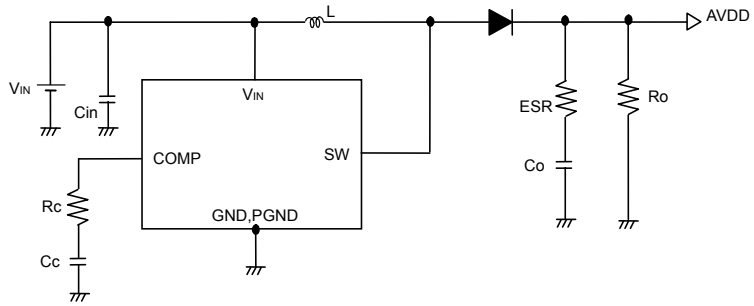


Fig. 30 Application Circuit Diagram

It is possible to realize the stable feedback loop by canceling the pole fp(Min.), which is created by the output capacitor and load resistor, with CR zero compensation of the error amp as shown below.

$$fz(Amp.) = fp(Min.)$$

$$\longrightarrow \frac{1}{2\pi \times Rc \times Cc} = \frac{1}{2\pi \times Romax \times Co} \text{ [Hz]}$$

(5) Design of the Feedback Resistor Constant

Refer to the following equation to set the feedback resistor. As the setting range, 6.8 kΩ to 330 kΩ is recommended. If the resistor is set lower than a 6.8 kΩ, it causes the reduction of power efficiency. If it is set more than 330 kΩ, the offset voltage becomes larger by the input bias current 0.1 μA(Typ.) in the internal error amplifier.

$$AVDD = \frac{R1 + R2}{R2} \times FB \quad [V]$$

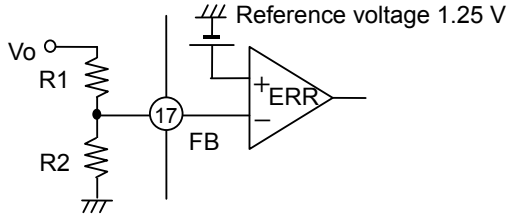


Fig. 31 Application Circuit Diagram

(6) Positive-side Charge Pump Settings

The IC incorporates a charge pump controller, thus making it possible to generate stable gate voltage.
The output voltage is determined by the following formula. As the setting range, 6.8 kΩ to 330 kΩ is recommended. If the resistor is set lower than a 6.8kΩ, it causes the reduction of power efficiency. If it is set more than 330 kΩ, the offset voltage becomes larger by the input bias current 0.1 μA (Typ.) in the internal error amp.

$$SRC = \frac{R3 + R4}{R4} \times FBP \quad [V]$$

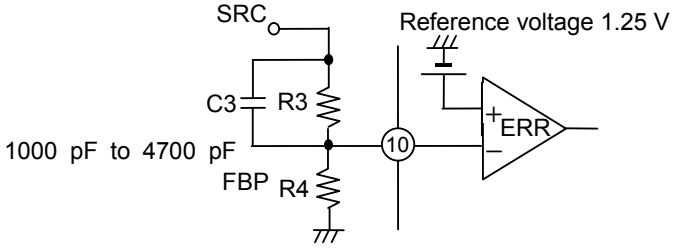


Fig. 32 Application Circuit Diagram

In order to prevent output voltage overshooting, add capacitor C3 in parallel with R3. The recommended capacitance is 1000 pF to 4700 pF. If a capacitor outside this range is inserted, the output voltage may oscillate.

(7) Negative-side Charge Pump Settings

This IC incorporates a charge pump controller for negative voltage, thus making it possible to generate stable gate voltage.
The output voltage is determined by the following formula. As the setting range, 6.8 kΩ to 330 kΩ is recommended. If the resistor is set lower than a 6.8 kΩ, it causes the reduction of power efficiency. If it is set more than 330 kΩ, the offset voltage becomes larger by the input bias current 0.1 μA (Typ.) in the internal error amp.

$$V_{GL} = (FBN - VREF) \frac{R5}{R6} + FBN \quad [V]$$

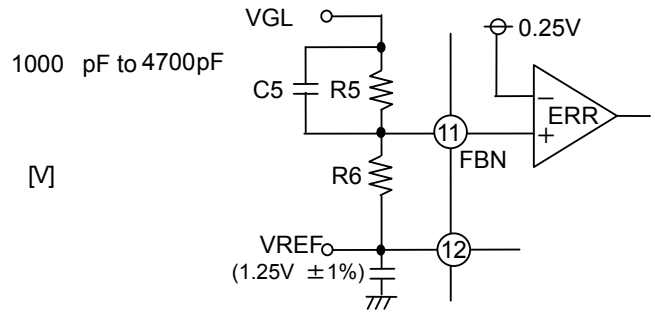


Fig. 33 Application Circuit Diagram

In order to prevent output voltage overshooting, insert capacitor C5 in parallel with R5. The recommended capacitance is 1000 pF to 4700 pF. If a capacitor outside this range is inserted, the output voltage may oscillate.

●Application Circuit

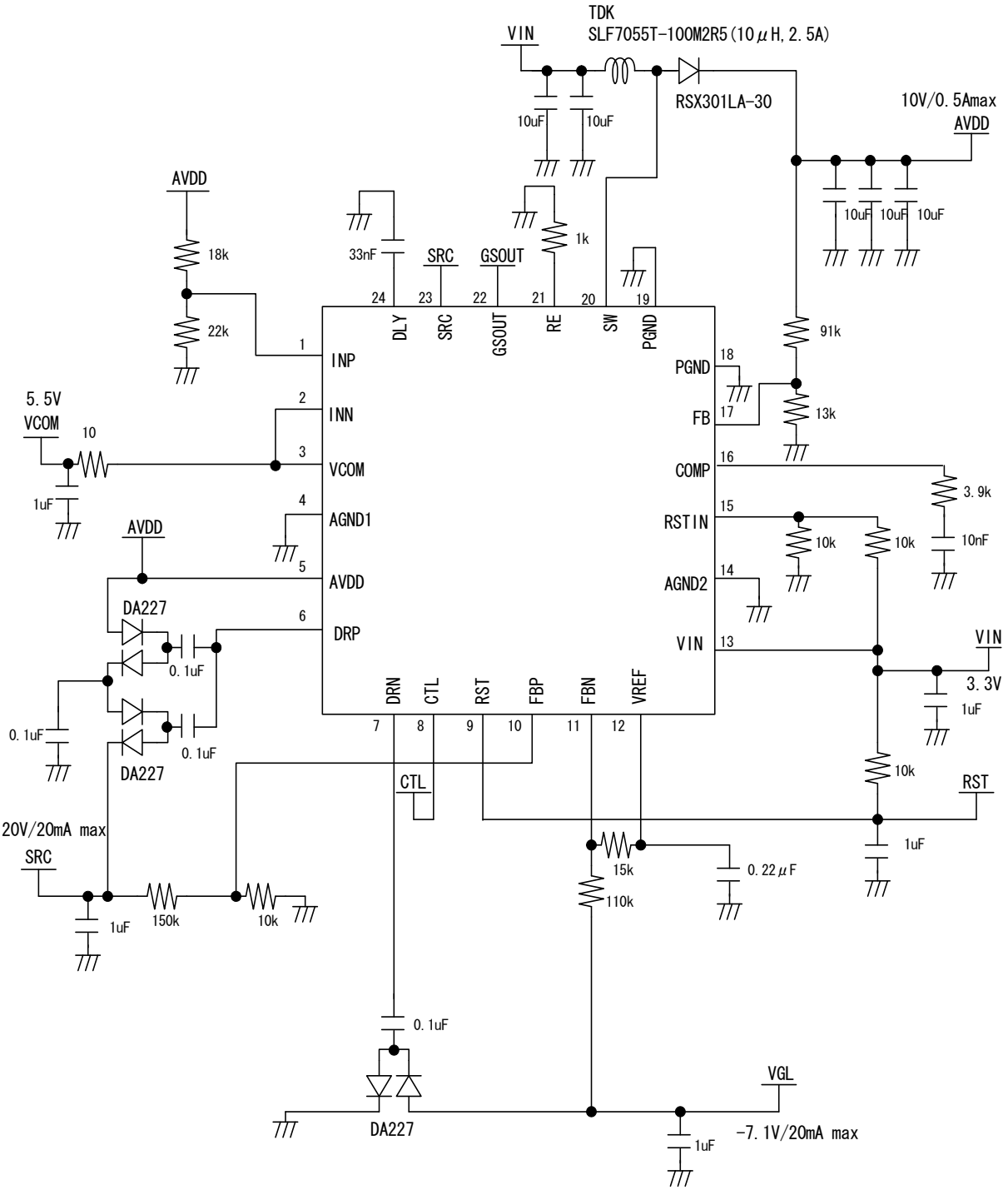
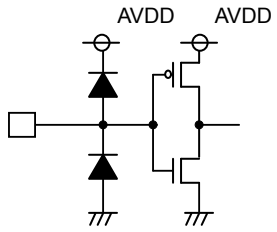
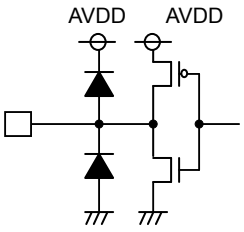
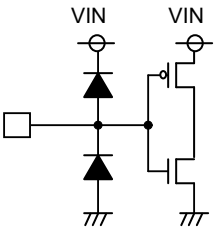
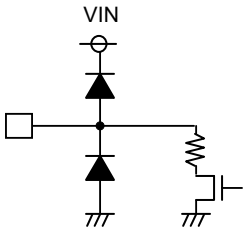
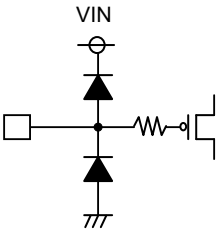
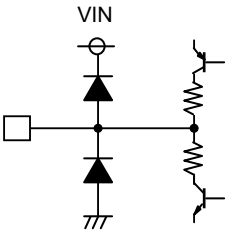
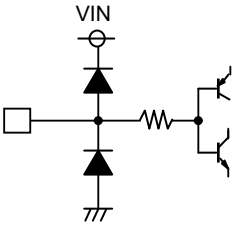
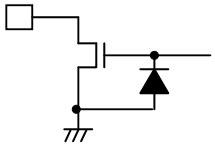
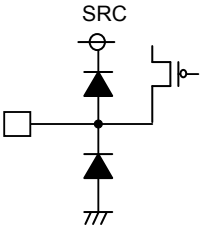
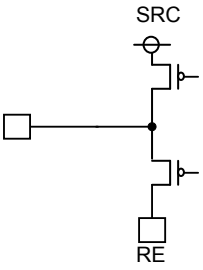
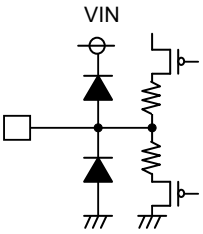


Fig. 34 Application Circuit

●I/O Equivalent Circuit Diagrams

(Except for 4.AGND1, 5.AVDD, 13.VIN, 14.AGND2, 18･19.PGND, 23.SRC)

1.INP 2.INN	3.VCOM 6.DRP 7.DRN	8.CTL
		
9.RST	10.FBP 11.FBN 15.RSTIN	16.COMP
		
17.FB	18.SW	21.RE
		
22.GSOUT	24.DLY	
		

●Operation Notes

1. Absolute maximum range
   This product are produced with strict quality control, but might be destroyed in using beyond absolute maximum ratings. Open IC destroyed a failure mode cannot be defined (like Short mode, or Open mode).
   Therefore physical security countermeasure, like fuse, is to be given when a specified mode to be beyond absolute maximum ratings is considered.

2. About Rush Current
   Rush current might flow momentarily by the order of turning on the power supply and rise time in IC with two or more power supplies. Therefore, please note drawing the width of the power supply and the GND pattern wiring, the output capacity, and the pattern and the current abilities.

3. Setting of heat
   Use a setting of heat that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

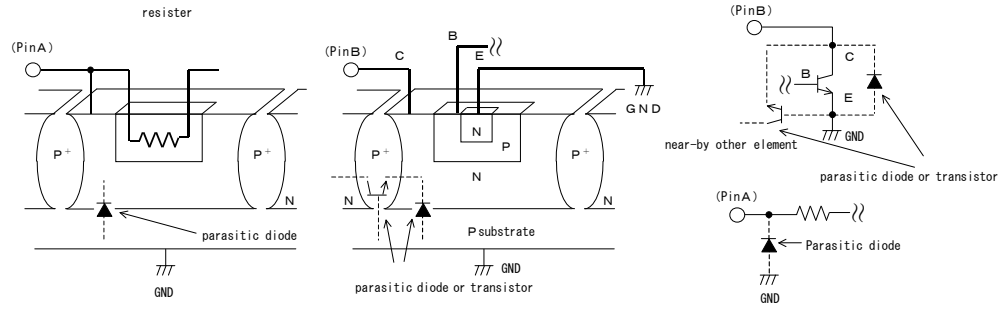
4. Short Circuit between Terminal and Soldering
   Don't short-circuit between Output pin and VIN pin, Output pin and GND pin, or VIN pin and GND pin.
   When soldering the IC on circuit board, please be unusually cautious about the orientation and the position of the IC. When the orientation is mistaken the IC may be destroyed.

5. Electromagnetic Field
   Mal-function may happen when the device is used in the strong electromagnetic field.

6. Ground wiring patterns
   When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage.
   Be careful not to change the GND wiring patterns of any external components.

7. This IC is a monolithic IC which has P+ isolation in the P substrate and between the various pins.
   A P-N junction is formed from this P layer and the N layer of each pin. For example, when a resistor and a transistor is connected to a pin. Parasitic diodes can occur inevitably in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits as well as operation faults and physical damage. Accordingly, you must not use methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND.
   (P substrate) voltage to an input pin. Please make sure all pins which is over GND even if include transient feature.

SIMPLIFIED STRUCTURE OF BI-POLAR IC



8. Over current protection circuit
   The over-current protection circuits are built in at output, according to their respective current outputs and prevent the IC from being damaged when the load is short-circuited or over-current. But, these protection circuits are effective for preventing destruction by unexpected accident. When it's in continuous protection circuit moving period don't use please. And for ability, because this chip has minus characteristic, be careful for heat plan.

9. Built-in thermal circuit
   A temperature control circuit is built in the IC to prevent the damage due to overheat.
   Therefore, all the outputs are turned off when the thermal circuit works and are turned on when the temperature goes down to the specified level.

10. Testing on application boards
    When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process.

●Ordering part number

B	D	8	1	8	4	M	U	V	-	E	2

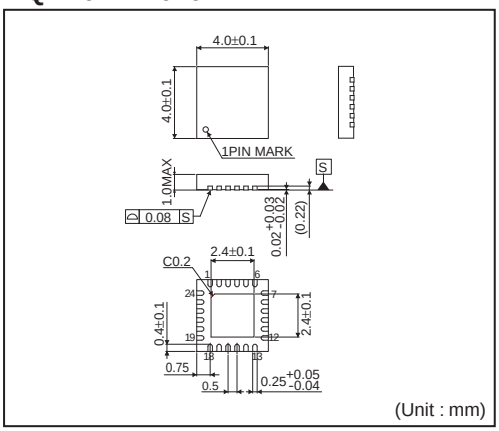
Part No.

Part No.

Package
MUV:VQFN024V4040

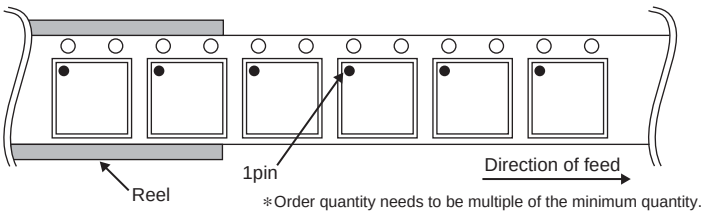
Packaging and forming specification
E2: Embossed tape and reel

VQFN024V4040



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notes

No copying or reproduction of this document, in part or in whole, is permitted without the consent of ROHM Co.,Ltd.

The content specified herein is subject to change for improvement without notice.

The content specified herein is for the purpose of introducing ROHM's products (hereinafter "Products"). If you wish to use any such Product, please be sure to refer to the specifications, which can be obtained from ROHM upon request.

Examples of application circuits, circuit constants and any other information contained herein illustrate the standard usage and operations of the Products. The peripheral conditions must be taken into account when designing circuits for mass production.

Great care was taken in ensuring the accuracy of the information specified in this document. However, should you incur any damage arising from any inaccuracy or misprint of such information, ROHM shall bear no responsibility for such damage.

The technical information specified herein is intended only to show the typical functions of and examples of application circuits for the Products. ROHM does not grant you, explicitly or implicitly, any license to use or exercise intellectual property or other rights held by ROHM and other parties. ROHM shall bear no responsibility whatsoever for any dispute arising from the use of such technical information.

The Products specified in this document are intended to be used with general-use electronic equipment or devices (such as audio visual equipment, office-automation equipment, communication devices, electronic appliances and amusement devices).

The Products specified in this document are not designed to be radiation tolerant.

While ROHM always makes efforts to enhance the quality and reliability of its Products, a Product may fail or malfunction for a variety of reasons.

Please be sure to implement in your equipment using the Products safety measures to guard against the possibility of physical injury, fire or any other damage caused in the event of the failure of any Product, such as derating, redundancy, fire control and fail-safe designs. ROHM shall bear no responsibility whatsoever for your use of any Product outside of the prescribed scope or not in accordance with the instruction manual.

The Products are not designed or manufactured to be used with any equipment, device or system which requires an extremely high level of reliability the failure or malfunction of which may result in a direct threat to human life or create a risk of human injury (such as a medical instrument, transportation equipment, aerospace machinery, nuclear-reactor controller, fuel-controller or other safety device). ROHM shall bear no responsibility in any way for use of any of the Products for the above special purposes. If a Product is intended to be used for any such special purpose, please contact a ROHM sales representative before purchasing.

If you intend to export or ship overseas any Product or technology specified herein that may be controlled under the Foreign Exchange and the Foreign Trade Law, you will be required to obtain a license or permit under the Law.

ROHM SEMICONDUCTOR

Thank you for your accessing to ROHM product informations.
More detail product informations and catalogs are available, please contact us.

ROHM Customer Support System

http://www.rohm.com/contact/