ICS8725I-01
1:5 DIFFERENTIAL-TO-HSTL ZERO DELAY CLOCK GENERATOR
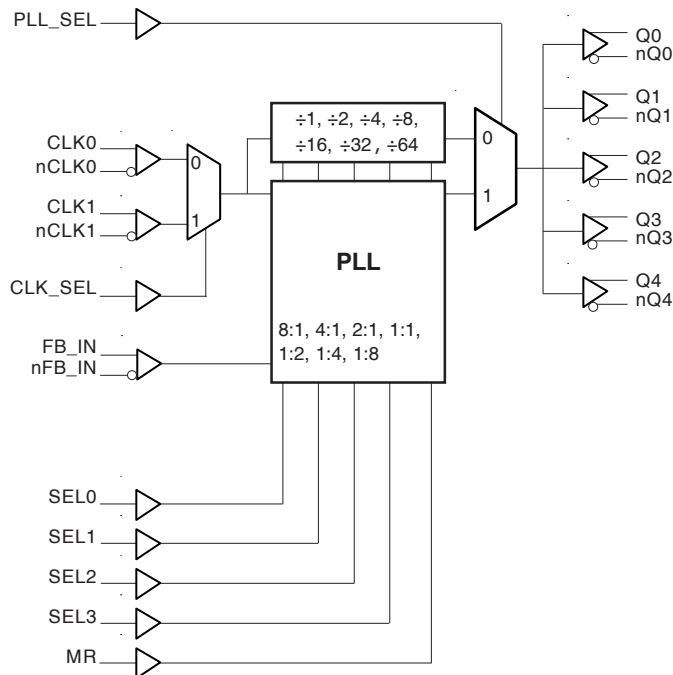
GENERAL DESCRIPTION

The ICS8725I-01 is a highly versatile 1:5 Differential-to-HSTL Clock Generator. The ICS8725I-01 has a fully integrated PLL and can be configured as zero delay buffer, multiplier or divider, and has an output frequency range of 31.25MHz to 630MHz. The reference divider, feedback divider and output divider are each programmable, thereby allowing for the following output-to-input frequency ratios: 8:1, 4:1, 2:1, 1:1, 1:2, 1:4, 1:8. The external feedback allows the device to achieve "zero delay" between the input clock and the output clocks. The PLL_SEL pin can be used to bypass the PLL for system test and debug purposes. In bypass mode, the reference clock is routed around the PLL and into the internal output dividers.

FEATURES

- 5 differential HSTL outputs

- Selectable differential CLKx, nCLKx input pairs

- CLKx, nCLKx pairs can accept the following differential input levels: LVDS, LVPECL, HSTL, SSTL, HCSL

- Output frequency range: 31.25MHz to 630MHz

- Input frequency range: 31.25MHz to 630MHz

- VCO range: 250MHz to 630MHz

- External feedback for "zero delay" clock regeneration with configurable frequencies

- Programmable dividers allow for the following output-to-input frequency ratios: 8:1, 4:1, 2:1, 1:1, 1:2, 1:4, 1:8

- Static phase offset: 30ps ± 125ps

- Cycle-to-cycle jitter: 35ps (maximum)

- Output skew: 50ps (maximum)

- 3.3V core, 1.8V output operating supply

- -40°C to 85°C ambient operating temperature

- Available in both standard (RoHS5) and lead-free (RoHS 6) packages

BLOCK DIAGRAM

PIN ASSIGNMENT
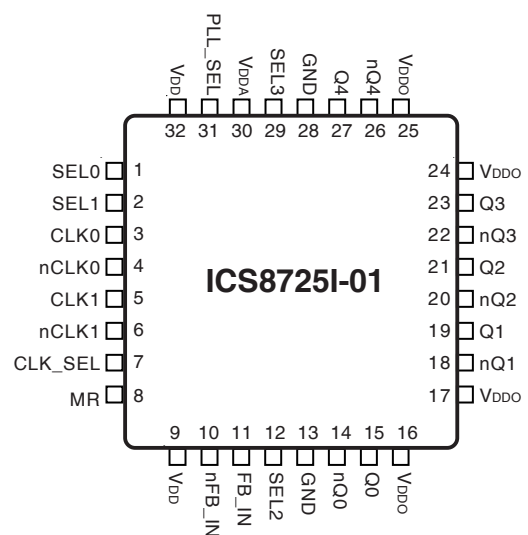
32-Lead LQFP
7mm x 7mm x 1.4mm package body
Y Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2, 12, 29	SEL0, SEL1, SEL2, SEL3	Input	Pulldown	Determines output divider values in Table 3. LVCMOS/LVTTL interface levels.
3	CLK0	Input	Pulldown	Non-inverting differential clock input.
4	nCLK0	Input	Pullup	Inverting differential clock input.
5	CLK1	Input	Pulldown	Non-inverting differential clock input.
6	nCLK1	Input	Pullup	Inverting differential clock input.
7	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK1, nCLK1. When LOW, selects CLK0, nCLK0. LVCMOS/LVTTL interface levels.
8	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
9, 32	V_{DD}	Power		Core supply pins.
10	nFB_IN	Input	Pullup	Feedback input to phase detector for regenerating clocks with "zero delay".
11	FB_IN	Input	Pulldown	Feedback input to phase detector for regenerating clocks with "zero delay".
13, 28	GND	Power		Power supply ground.
14, 15	nQ0, Q0	Output		Differential output pair. HSTL interface levels.
16, 17, 24, 25	V_{DDO}	Power		Output supply pins.
18, 19	nQ1, Q1	Output		Differential output pair. HSTL interface levels.
20, 21	nQ2, Q2	Output		Differential output pair. HSTL interface levels.
22, 23	nQ3, Q3	Output		Differential output pair. HSTL interface levels.
26, 27	nQ4, Q4	Output		Differential output pair. HSTL interface levels.
30	V_{DDA}	Power		Analog supply pin.
31	PLL_SEL	Input	Pullup	Selects between the PLL and reference clock as the input to the dividers. When LOW, selects reference clock. When HIGH, selects PLL. LVCMOS/LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ

TABLE 3A. CONTROL INPUT FUNCTION TABLE

Inputs					Outputs PLL_SEL = 1 PLL Enable Mode
SEL3	SEL2	SEL1	SEL0	Reference Frequency Range (MHz)*	Q0:Q4, nQ0:nQ4
0	0	0	0	250 - 630	÷ 1
0	0	0	1	125 - 315	÷ 1
0	0	1	0	62.5 - 157.5	÷ 1
0	0	1	1	31.25 - 78.75	÷ 1
0	1	0	0	250 - 630	÷ 2
0	1	0	1	125 - 315	÷ 2
0	1	1	0	62.5 - 157.5	÷ 2
0	1	1	1	250 - 630	÷ 4
1	0	0	0	125 - 315	÷ 4
1	0	0	1	250 - 630	÷ 8
1	0	1	0	125 - 315	x 2
1	0	1	1	62.5 - 157.5	x 2
1	1	0	0	31.25 - 78.75	x 2
1	1	0	1	62.5 - 157.5	x 4
1	1	1	0	31.25 - 78.75	x 4
1	1	1	1	31.25 - 78.75	x 8

*NOTE: VCO frequency range for all configurations above is 250MHz to 630MHz.

TABLE 3B. PLL BYPASS FUNCTION TABLE

Inputs				Outputs PLL_SEL = 0 PLL Bypass Mode
SEL3	SEL2	SEL1	SEL0	Q0:Q4, nQ0:nQ4
0	0	0	0	÷ 4
0	0	0	1	÷ 4
0	0	1	0	÷ 4
0	0	1	1	÷ 8
0	1	0	0	÷ 8
0	1	0	1	÷ 8
0	1	1	0	÷ 16
0	1	1	1	÷ 16
1	0	0	0	÷ 32
1	0	0	1	÷ 64
1	0	1	0	÷ 2
1	0	1	1	÷ 2
1	1	0	0	÷ 4
1	1	0	1	÷ 1
1	1	1	0	÷ 2
1	1	1	1	÷ 1

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, $T_A = -40°C$ TO $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		1.6	1.8	2.0	V
I_{DD}	Power Supply Current				137	mA
I_{DDA}	Analog Supply Current				17	mA
I_{DDO}	Output Supply Current	No Load		0		mA

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, $T_A = -40°C$ TO $85°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	CLK_SEL, MR, SEL0, SEL1, SEL2, SEL3	$V_{DD} = V_{IN} = 3.465V$ $V_{DDO} = 2V$			150	µA
		PLL_SEL	$V_{DD} = V_{IN} = 3.465V$ $V_{DDO} = 2V$			5	µA
I_{IL}	Input Low Current	CLK_SEL, MR, SEL0, SEL1, SEL2, SEL3	$V_{DD} = 3.465V$, $V_{DDO} = 2V$, $V_{IN} = 0V$	-5			µA
		PLL_SEL	$V_{DD} = 3.465V$, $V_{DDO} = 2V$, $V_{IN} = 0V$	-150			µA

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, $T_A = -40°C$ TO $85°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK0, CLK1, FB_IN	$V_{DD} = V_{IN} = 3.465V$			150	µA
		nCLK0, nCLK1, nFB_IN	$V_{DD} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	CLK0, CLK1, FB_IN	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-5			µA
		nCLK0, nCLK1, nFB_IN	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			0.5		V_{DD} - 0.85	V

NOTE 1: For single ended applications, the maximum input voltage for CLKx, nCLKx is V_{DD} + 0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 4D. HSTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		1		1.4	V
V_{OL}	Output Low Voltage; NOTE 1		0		0.4	V
V_{OX}	Output Crossover Voltage		40% x (V_{OH} - V_{OL}) + V_{OL}		60% x (V_{OH} - V_{OL}) + V_{OL}	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.1	V

NOTE 1: Outputs terminated with 50Ω to ground.

TABLE 5. INPUT FREQUENCY CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency	CLK0, nCLK0, CLK1, nCLK1	PLL_SEL = 1	31.25		630	MHz
			PLL_SEL = 0			630	MHz

TABLE 6. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				630	MHz
t_{PD}	Propagation Delay; NOTE 1	PLL_SEL = 0V $f \leq 630MHz$	3.4	3.9	4.5	ns
t(Ø)	Static Phase Offset; NOTE 2, 5	PLL_SEL = 3.3V	-95	30	155	ps
$t$sk(o)	Output Skew; NOTE 3, 5				50	ps
$t$jit(cc)	Cycle-to-Cycle Jitter; NOTE 5, 6				35	ps
$t$jit(Ø)	Phase Jitter; NOTE 4, 5, 6				±50	ps
t_L	PLL Lock Time				1	ms
t_R / t_F	Output Rise/Fall Time	20% to 80%	300		700	ps
t_{PW}	Output Pulse Width		t_{PERIOD}/2 - 85	t_{PERIOD}/2	t_{PERIOD}/2 + 85	ps

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as the time difference between the input reference clock and the averaged feedback input signal across alll conditions, when the PLL is locked and the input reference frequency is stable.
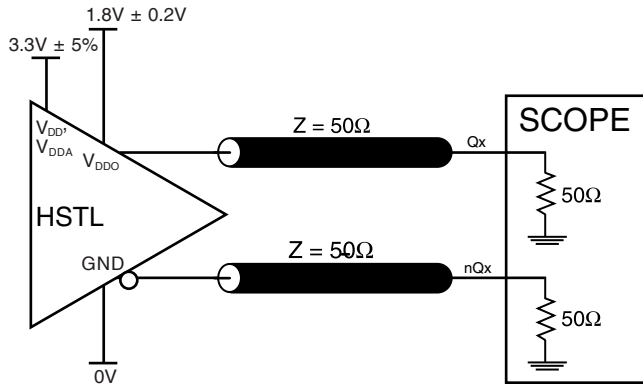NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at output differential cross points.
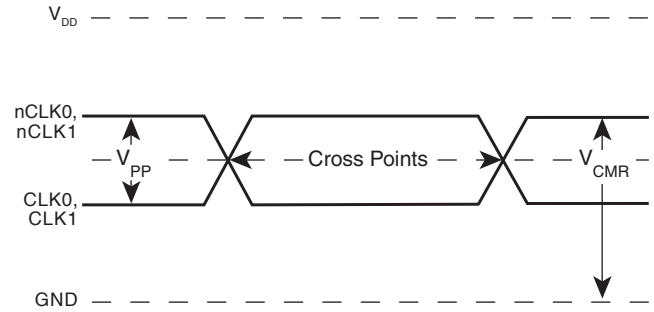NOTE 4: Phase jitter is dependent on the input source used.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.
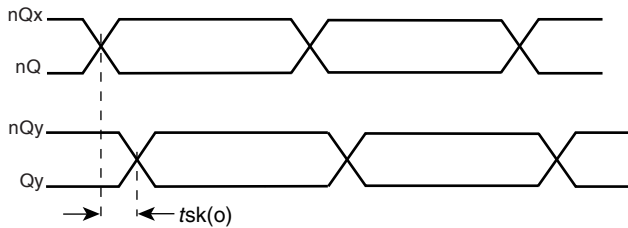NOTE 6: Characterized at VCO frequency of 622MHz.
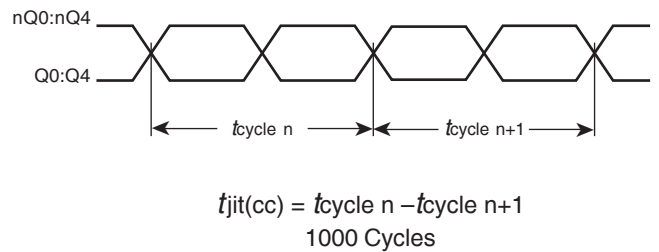
PARAMETER MEASUREMENT INFORMATION

3.3V ± 5%
1.8V ± 0.2V
V_{DD}, V_{DDA} V_{DDO}
Z = 50Ω
SCOPE
Qx
50Ω
HSTL
GND
Z = 50Ω
nQx
50Ω
0V

3.3V CORE/1.8V OUTPUT LOAD AC TEST CIRCUIT

V_{DD}
nCLK0, nCLK1
CLK0, CLK1
V_{PP} — Cross Points — V_{CMR}
GND

DIFFERENTIAL INPUT LEVEL

nQx
nQ
nQy
Qy
$t$sk(o)

OUTPUT SKEW

nQ0:nQ4
Q0:Q4
$t$cycle n
$t$cycle n+1

$$t\text{jit(cc)} = t\text{cycle n} - t\text{cycle n+1}$$
1000 Cycles

CYCLE-TO-CYCLE JITTER

nCLK0, nCLK1
CLK0, CLK1
V_{OH}
V_{OL}
nFB_IN
FB_IN
V_{OH}
V_{OL}
$t(\varnothing)$

$$t\text{jit}(\varnothing) = \left| t(\varnothing) - t(\varnothing)_{mean} \right| = \text{Phase Jitter}$$
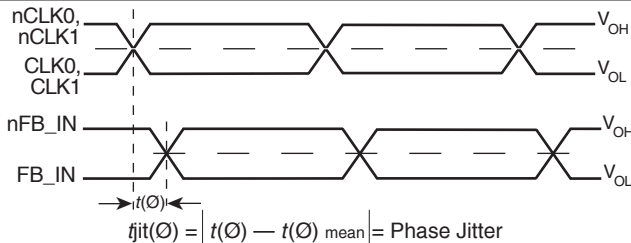
$$t(\varnothing)_{mean} = \text{Static Phase Offset}$$

(where $t(\varnothing)$ is any random sample, and $t(\varnothing)_{mean}$ is the average of the sampled cycles measured on controlled edges)

PHASE JITTER AND STATIC PHASE OFFSET

80%
80%
V_{OD}
Clock Outputs
20%
20%
t_R
t_F

OUTPUT RISE/FALL TIME

nQ0:nQ4
Q0:Q4
Pulse Width
t_{PERIOD}

$$odc = \frac{t_{PW}}{t_{PERIOD}}$$
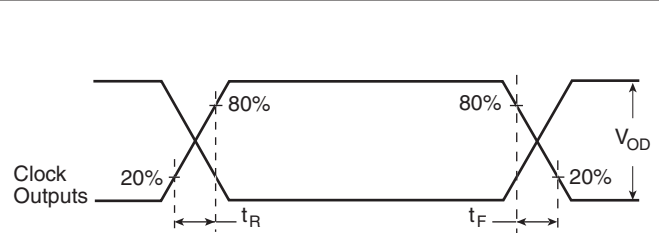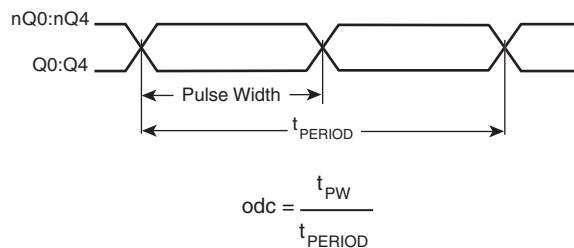
OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

nCLK0, nCLK1
CLK0, CLK1
nQ0:nQ4
Q0:Q4
t_{PD}
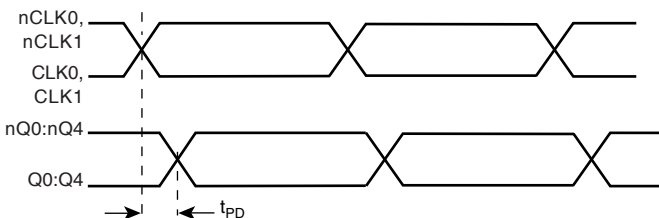
PROPAGATION DELAY

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, HSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 3A to 3D show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 3A,* the input termination applies for HSTL drivers. If you are using an HSTL driver from another vendor, use their termination recommendation.
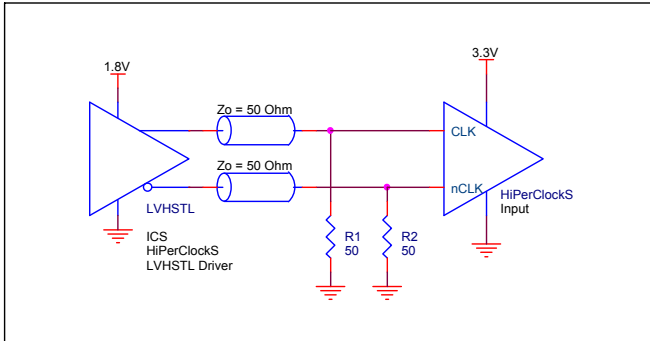
FIGURE 3A.   CLK/nCLK Input Driven by HSTL Driver
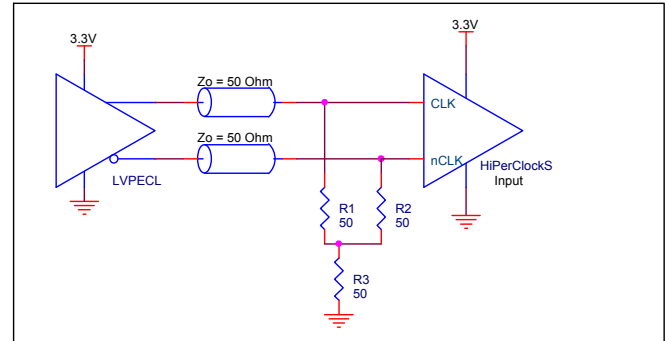
FIGURE 3B.   CLK/nCLK Input Driven by 3.3V LVPECL Driver
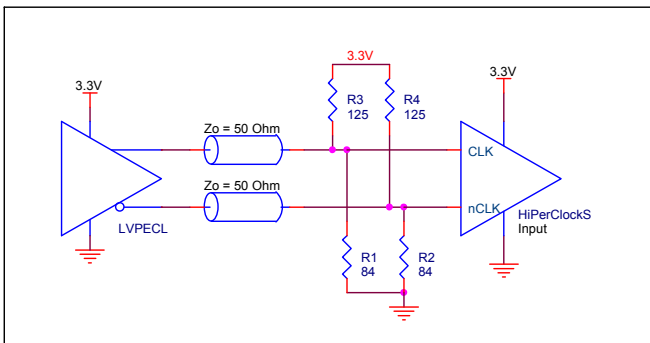
FIGURE 3C.   CLK/nCLK Input Driven by 3.3V LVPECL Driver
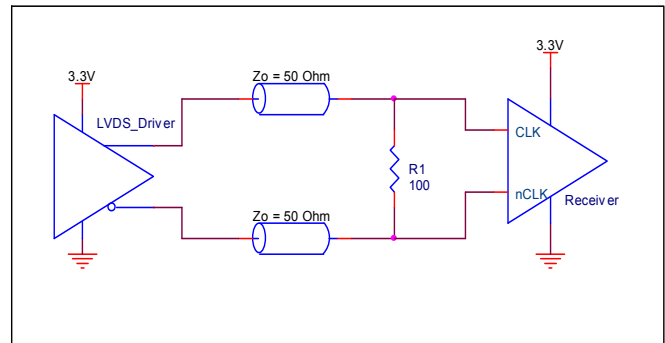
FIGURE 3D.   CLK/nCLK Input Driven by 3.3V LVDS Driver

LAYOUT GUIDELINE

The schematic of the ICS8725I-01 layout example is shown in *Figure 4A.* The ICS8725I-01 recommended PCB board layout for this example is shown in *Figure 4B.* This layout example is used as a general guideline. The layout in the actual system will depend on the selected component types, the density of the components, the density of the traces, and the stacking of the P.C. board.
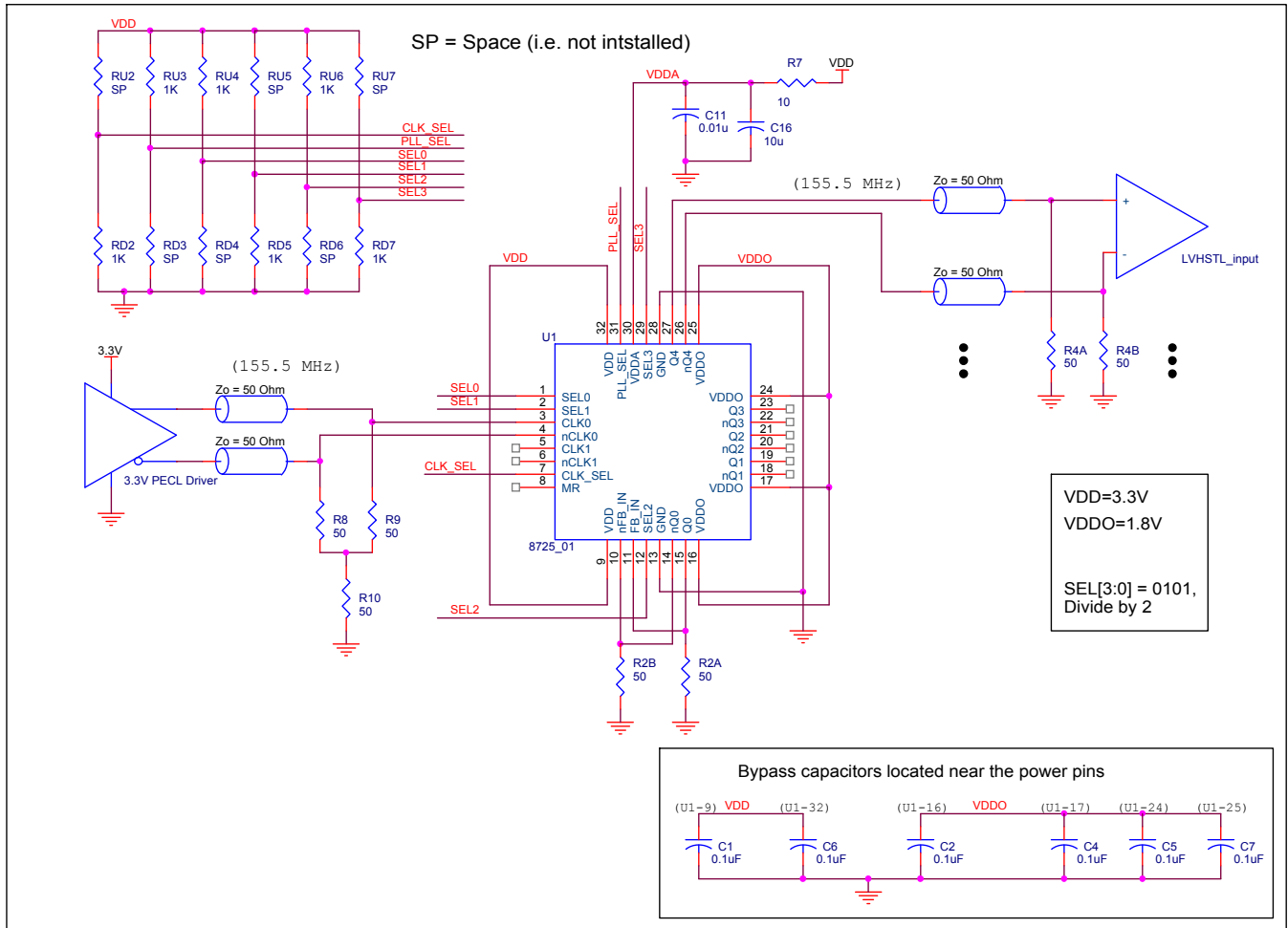

FIGURE 4A. ICS8725I-01 HSTL ZERO DELAY BUFFER SCHEMATIC EXAMPLE

The following component footprints are used in this layout example:

All the resistors and capacitors are size 0603.

POWER AND GROUNDING

Place the decoupling capacitors C1, C6, C2, C4, and C5, as close as possible to the power pins. If space allows, placement of the decoupling capacitor on the component side is preferred. This can reduce unwanted inductance between the decoupling capacitor and the power pin caused by the via.

Maximize the power and ground pad sizes and number of vias capacitors. This can reduce the inductance between the power and ground planes and the component power and ground pins.

The RC filter consisting of R7, C11, and C16 should be placed as close to the V_{DDA} pin as possible.

CLOCK TRACES AND TERMINATION

Poor signal integrity can degrade the system performance or cause system failure. In synchronous high-speed digital systems, the clock signal is less tolerant to poor signal integrity than other signals. Any ringing on the rising or falling edge or excessive ring back can cause system failure. The shape of the trace and the

trace delay might be restricted by the available space on the board and the component location. While routing the traces, the clock signal traces should be routed first and should be locked prior to routing other signal traces.

- The differential 50Ω output traces should have same length.

- Avoid sharp angles on the clock trace. Sharp angle turns cause the characteristic impedance to change on the transmission lines.

- Keep the clock traces on the same layer. Whenever possible, avoid placing vias on the clock traces. Placement of vias on the traces can affect the trace characteristic impedance and hence degrade signal integrity.

- To prevent cross talk, avoid routing other signal traces in parallel with the clock traces. If running parallel traces is unavoidable, allow a separation of at least three trace widths between the differential clock trace and the other signal trace.

- Make sure no other signal traces are routed between the clock trace pair.

- The matching termination resistors should be located as close to the receiver input pins as possible.
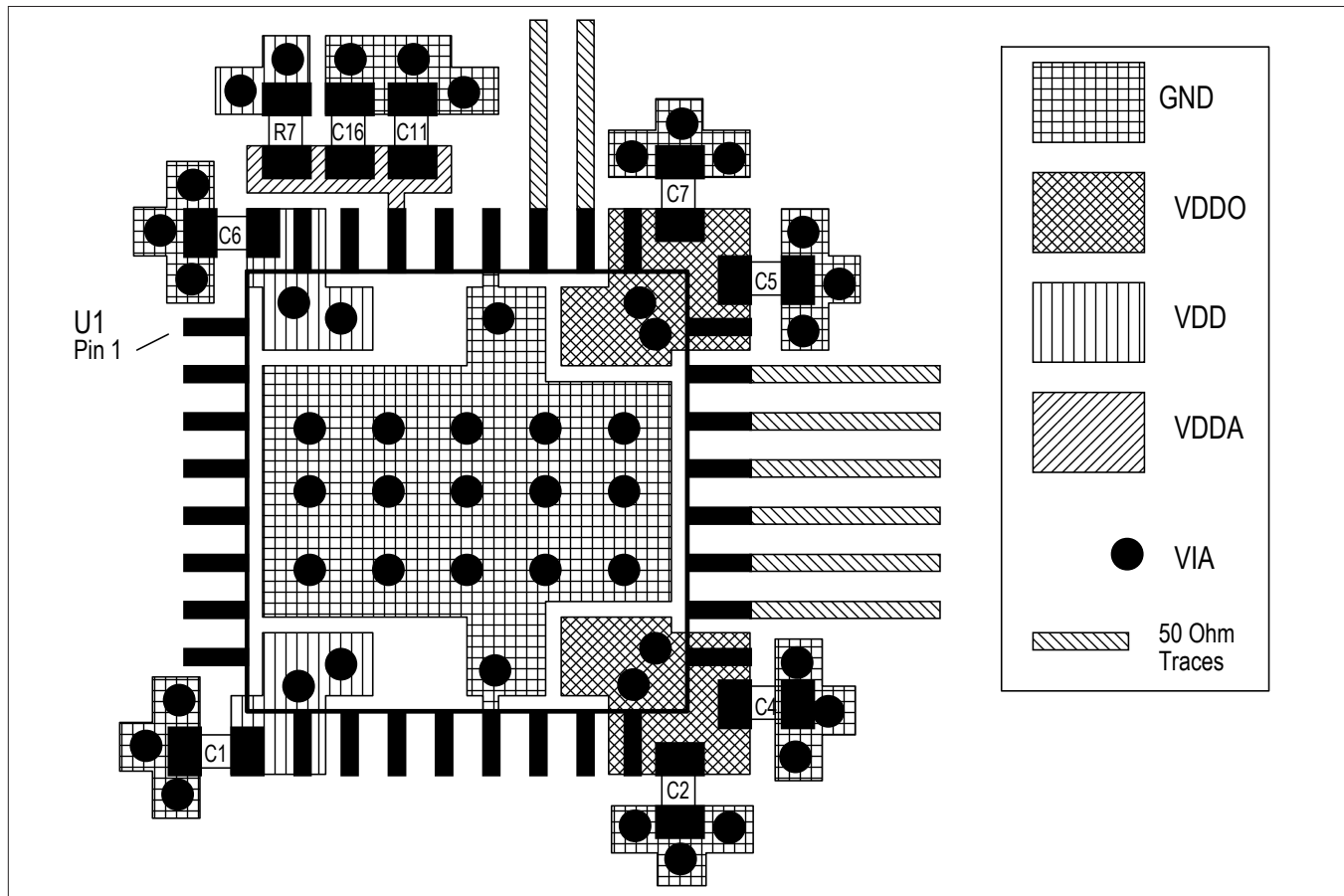

FIGURE 4B. PCB BOARD LAYOUT FOR ICS8725I-01

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS8725I-01.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS8725I-01 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{DD_MAX} * (I_{DD_MAX} + I_{DDA_MAX}) = 3.465V * (137mA + 17mA) = **499mW**

- Power (outputs)$_{MAX}$ = **32.8mW/Loaded Output pair**
  If all outputs are loaded, the total power is 5 * 32.8mW = **164mW**

Total Power$_{\_MAX}$ (3.465V, with all outputs switching) = 499mW + 164mW = **663mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for the devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 42.1°C/W per Table 7 below. Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.663W * 42.1°C/W = 113°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**Table 7. Thermal Resistance θ_{JA} for 32-pin LQFP, Forced Convection**

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

HSTL output driver circuit and termination are shown in *Figure 5*.
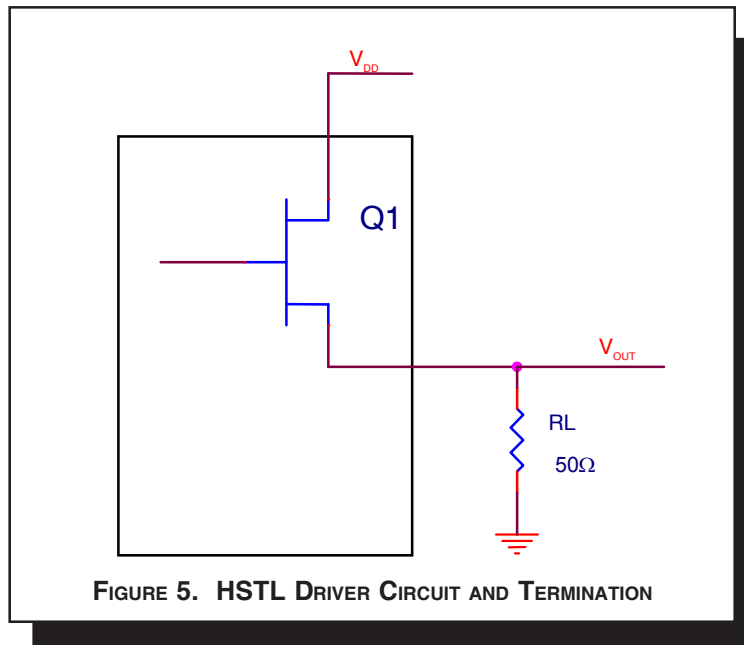
Figure 5. HSTL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load.

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$$Pd\_H = (V_{OH\_MIN}/R_L) * (V_{DD\_MAX} - V_{OH\_MIN})$$

$$Pd\_L = (V_{OL\_MAX}/R_L) * (V_{DD\_MAX} - V_{OL\_MAX})$$

Pd_H = (1V/50Ω) * (2V - 1V) = **20mW**
Pd_L = (0.4V/50Ω) * (2V - 0.4V) = **12.8mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **32.8mW**

RELIABILITY INFORMATION

TABLE 8. θ_{JA} **VS. AIR FLOW TABLE**

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS8725I-01 is: 2969

PACKAGE OUTLINE - Y SUFFIX
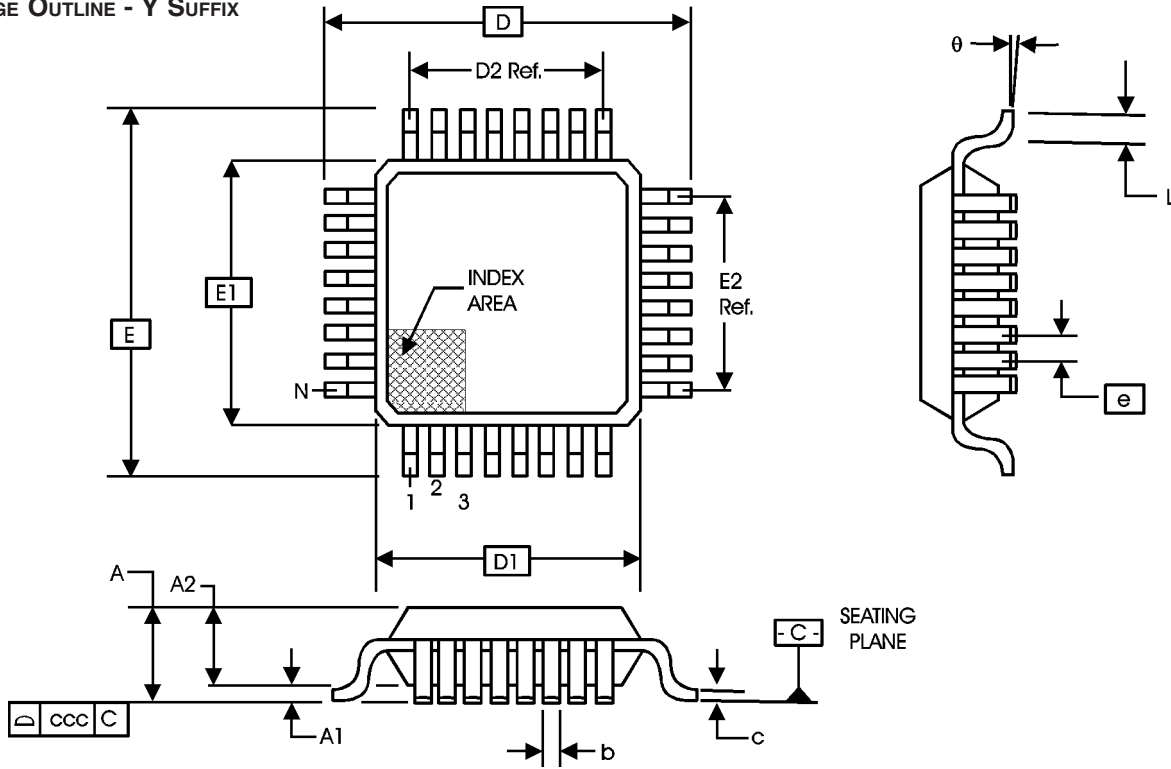
TABLE 9. PACKAGE DIMENSIONS

	JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS		
SYMBOL	**BBA**		
	MINIMUM	**NOMINAL**	**MAXIMUM**
N	32		
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D	9.00 BASIC		
D1	7.00 BASIC		
D2	5.60 Ref.		
E	9.00 BASIC		
E1	7.00 BASIC		
E2	5.60 Ref.		
e	0.80 BASIC		
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8725AYI-01	ICS8725AYI-01	32 Lead LQFP	tray	-40°C to 85°C
8725AYI-01T	ICS8725AYI-01	32 Lead LQFP	1000 Tape and Reel	-40°C to 85°C
8725AYI-01	ICS8725AI01L	32 Lead-Free LQFP	tray	-40°C to 85°C
8725AYI-01T	ICS8725AI01L	32 Lead-Free LQFP	1000 Tape and Reel	-40°C to 85°C

NOTE: Parts that are ordered with an ""LF"" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET					
Rev	**Table**	**Page**	**Description of Change**		**Date**
A	T10	15	Ordering Information - Added Lead-Free marking		12/19/07
A	T10	15 17	Updated datasheet's header/footer with IDT from ICS. Removed ICS prefix from Part/Order Number column. Added Contact Page.		8/9/10

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