

Actel's SmartFusion Intelligent Mixed Signal FPGAs

Microcontroller Subsystem (MSS)

- Hard 100 MHz 32-Bit ARM[®] Cortex[™]-M3
 - 1.25 DMIPS/MHz Throughput from Zero Wait State Memory
 - Memory Protection Unit (MPU)
 - Single Cycle Multiplication, Hardware Divide
 - JTAG Debug (4 wires), Serial Wire Debug (SWD, 2 wires), and Single Wire Viewer (SWV) Interfaces
- Internal Memory
 - Embedded Nonvolatile Flash Memory (eNVM), 128 Kbytes to 512 Kbytes
 - Embedded High-Speed SRAM (eSRAM), 16 Kbytes to 64 Kbytes, Implemented in 2 Physical Blocks to Enable Simultaneous Access from 2 Different Masters
- Multi-Layer AHB Communications Matrix
 - Provides up to 16 Gbps of On-Chip Memory Bandwidth,¹ Allowing Multi-Master Schemes
- 10/100 Ethernet MAC with RMII Interface²
- Programmable External Memory Controller, Which Supports:
 - Asynchronous Memories
 - NOR Flash, SRAM, PSRAM
 - Synchronous SRAMs
- Two I²C Peripherals
- Two 16550 Compatible UARTs
- Two SPI Peripherals
- Two 32-Bit Timers
- 32-Bit Watchdog Timer
- 8-Channel DMA Controller to Offload the Cortex-M3 from Data Transactions
- Clock Sources
 - 32 KHz to 20 MHz Main Oscillator
 - Battery-Backed 32 KHz Low Power Oscillator with Real-Time Counter (RTC)
 - 100 MHz Embedded RC Oscillator; 1% Accurate
 - Embedded Analog PLL with 4 Output Phases (0, 90, 180, 270)

High-Performance FPGA

- Based on Actel's proven ProASIC[®]3 FPGA Fabric
- Low Power, Firm-Error Immune 130-nm, 7-Layer Metal, Flash-Based CMOS Process
- Nonvolatile, Live at Power-Up, Retains Program When Powered Off
- 350 MHz System Performance
- Embedded SRAMs and FIFOs
 - Variable Aspect Ratio 4,608-Bit SRAM Blocks
 - x1, x2, x4, x9, and x18 Organizations
 - True Dual-Port SRAM (excluding x18)

- Programmable Embedded FIFO Control Logic
- Secure ISP with 128-Bit AES via JTAG
- FlashLock[®] to Secure FPGA Contents
- Five Clock Conditioning Circuits (CCCs) with up to 2 Integrated Analog PLLs
 - Phase Shift, Multiply/Divide, and Delay Capabilities
 - Frequency: Input 1.5–350 MHz, Output 0.75 to 350 MHz

Programmable Analog Analog Front-End (AFE)

- Up to Three 12-Bit SAR ADCs
 - 500 Ksps in 12-Bit Mode
 - 550 Ksps in 10-Bit Mode
 - 600 Ksps in 8-Bit Mode
- Internal 2.56 V Reference or Optional External Reference
- One First-Order $\Sigma\Delta$ DAC (sigma-delta) per ADC
 - 12-Bit 500 Ksps Update Rate
- Up to 5 High-Performance Analog Signal Conditioning Blocks (SCB) per Device, Each Including:
 - Two High-Voltage Bipolar Voltage Monitors (with 4 input ranges from ± 2.5 V to $-11.5/+14$ V) with 1% Accuracy
 - High Gain Current Monitor, Differential Gain = 50, up to 14 V Common Mode
 - Temperature Monitor (Resolution = $\frac{1}{4}^{\circ}\text{C}$ in 12-Bit Mode; Accurate from -55°C to 150°C)
- Up to Ten High-Speed Voltage Comparators ($t_{pd} = 15$ ns)

Analog Compute Engine (ACE)

- Offloads Cortex-M3–Based MSS from Analog Initialization and Processing of ADC, DAC, and SCBs
- Sample Sequence Engine for ADC and DAC Parameter Set-Up
- Post-Processing Engine for Functions such as Low-Pass Filtering and Linear Transformation
- Easily Configured via GUI in Libero[®] Integrated Design (IDE) Software

I/Os and Operating Voltage

- FPGA I/Os
 - LVDS, PCI, PCI-X, up to 24 mA I_{OH}/I_{OL}
 - Up to 350 MHz
- MSS I/Os
 - Schmitt Trigger, up to 6 mA I_{OH} , 8 mA I_{OL}
 - Up to 180 MHz
- Single 3.3 V Power Supply with On-Chip 1.5 V Regulator
- External 1.5 V Is Allowed by Bypassing Regulator (digital VCC = 1.5 V for FPGA and MSS, analog VCC = 3.3 V and 1.5 V)

¹ Theoretical maximum

² A2F200 and larger devices

SmartFusion Family Product Table

SmartFusion Device		A2F060 ¹	A2F200	A2F500
FPGA Fabric	System Gates	60,000	200,000	500,000
	Tiles (D-flip-flops)	1,536	4,608	11,520
	RAM Blocks (4,608 bits)	8	8	24
Microcontroller Subsystem (MSS)	Flash (Kbytes)	128	256	512
	SRAM (Kbytes)	16	64	64
	Cortex-M3 with memory protection unit (MPU)	Yes		
	10/100 Ethernet MAC	No	Yes	
	External Memory Controller (EMC)	24-bit address,16-bit data		
	DMA	8 Ch		
	I ² C	2		
	SPI	2		
	16550 UART	2		
	32-Bit Timer	2		
	PLL	1	1	2 ³
	32 KHz Low Power Oscillator	1		
	100 MHz On-Chip RC Oscillator	1		
	Main Oscillator (32 KHz to 20 MHz)	1		
Programmable Analog	ADCs (8-/10-/12-bit SAR)	1	2	3 ⁴
	DACs (12-bit sigma-delta)	1	2	3 ⁴
	Signal Conditioning Blocks (SCBs)	1	4	5 ⁴
	Comparators ²	2	8	10 ⁴
	Current Monitors ²	1	4	5 ⁴
	Temperature Monitors ²	1	4	5 ⁴
	Bipolar High Voltage Monitors ²	2	8	10 ⁴

Notes:

1. Under definition; subject to change.
2. These functions share I/O pins and may not all be available at the same time. See the Analog Front-End Overview section in the [SmartFusion Programmable Analog User's Guide](#) for details.
3. Two PLLs are available in CS288 and FG484 (one PLL in FG256).
4. Available on FG484 only. FG256 and CS288 packages offer the same programmable analog capabilities as A2F200.

Package I/Os: MSS + FPGA I/Os

Device	A2F060	A2F200			A2F500		
Package	FG256	CS288	FG256	FG484	CS288	FG256	FG484
Direct Analog Input	6	8	8	8	8	8	12
Total Analog Input	10	24	24	24	24	24	32
Total Analog Output	1	2	2	2	2	2	3
MSS I/Os ^{1,2}	25	31	25	41	31	25	41
FPGA I/Os	66	78	66	94	78	66	128
Total I/Os	102	135	117	161	135	117	204

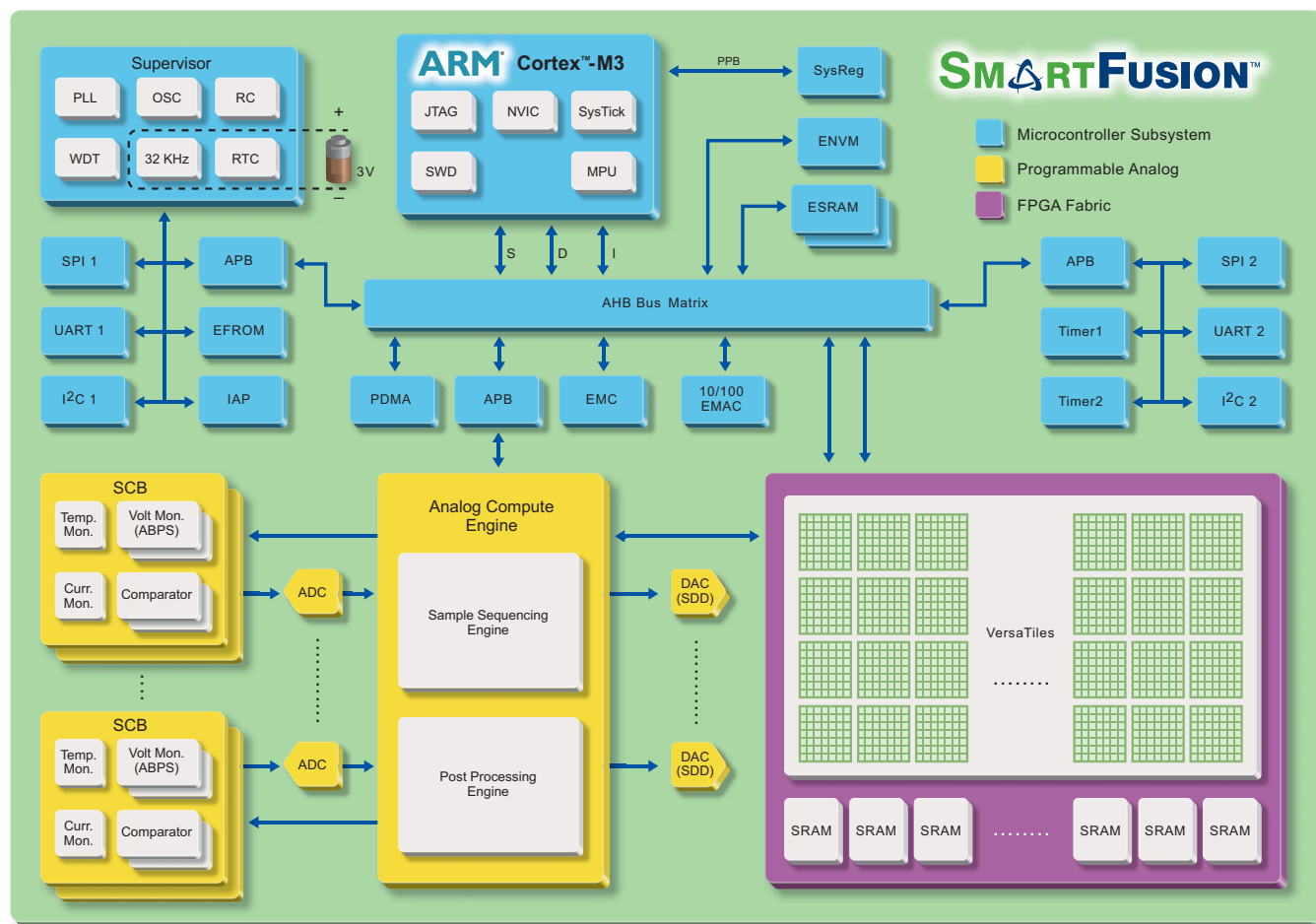
Notes:

1. 16 MSS I/Os are multiplexed and can be used as FPGA I/Os, if not needed for MSS. These I/Os support Schmitt triggers and support only LVTTTL and LVCMOS (1.5 / 1.8 / 2.5, 3.3 V) standards.
2. 9 MSS I/Os are primarily for 10/100 Ethernet MAC and are also multiplexed and can be used as FPGA I/Os if Ethernet MAC is not used in a design. These I/Os support Schmitt triggers and support only LVTTTL and LVCMOS (1.5 / 1.8 / 2.5, 3.3 V) standards.

SmartFusion Device Status

Device	Status
A2F060	Advance
A2F200	Production
A2F500	Production

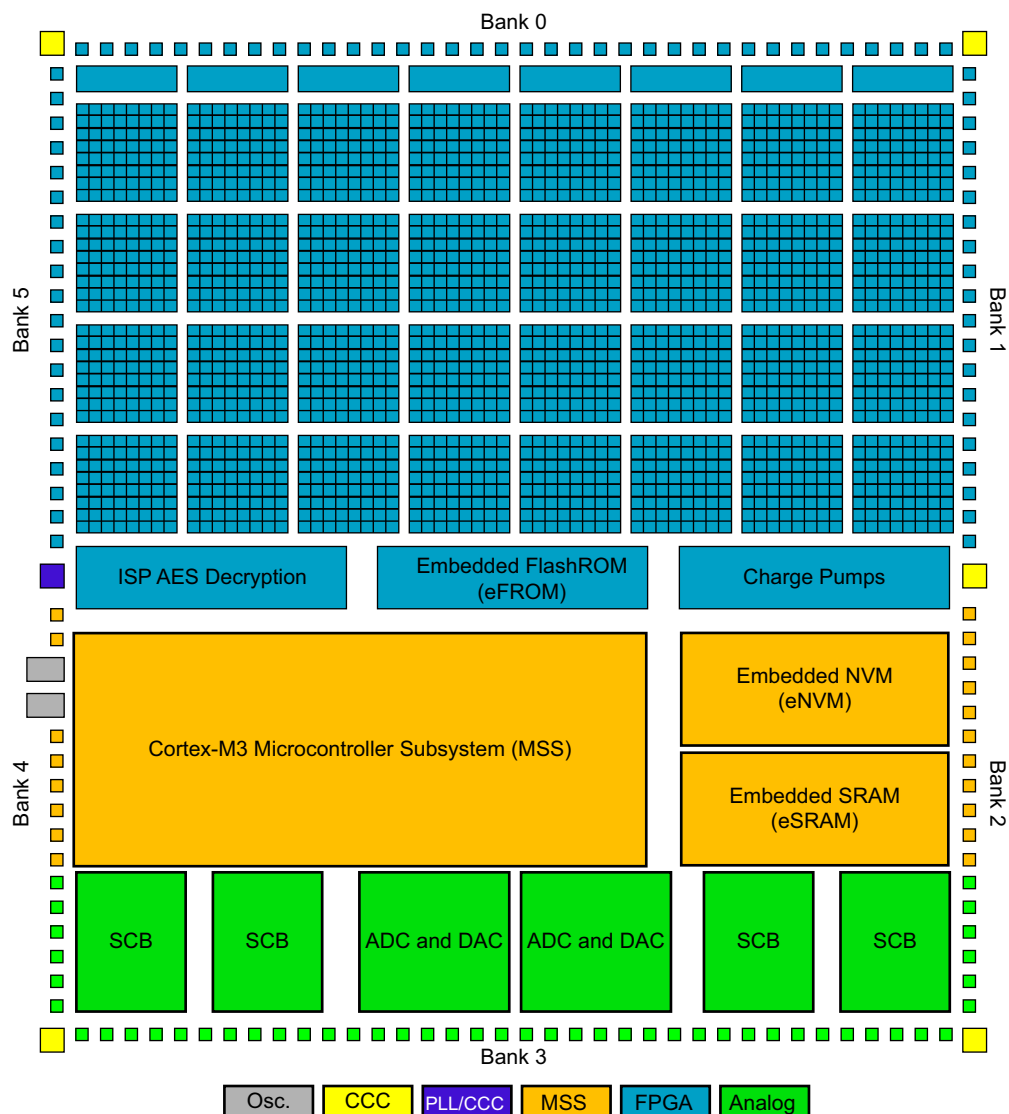
SmartFusion Block Diagram



Legend:

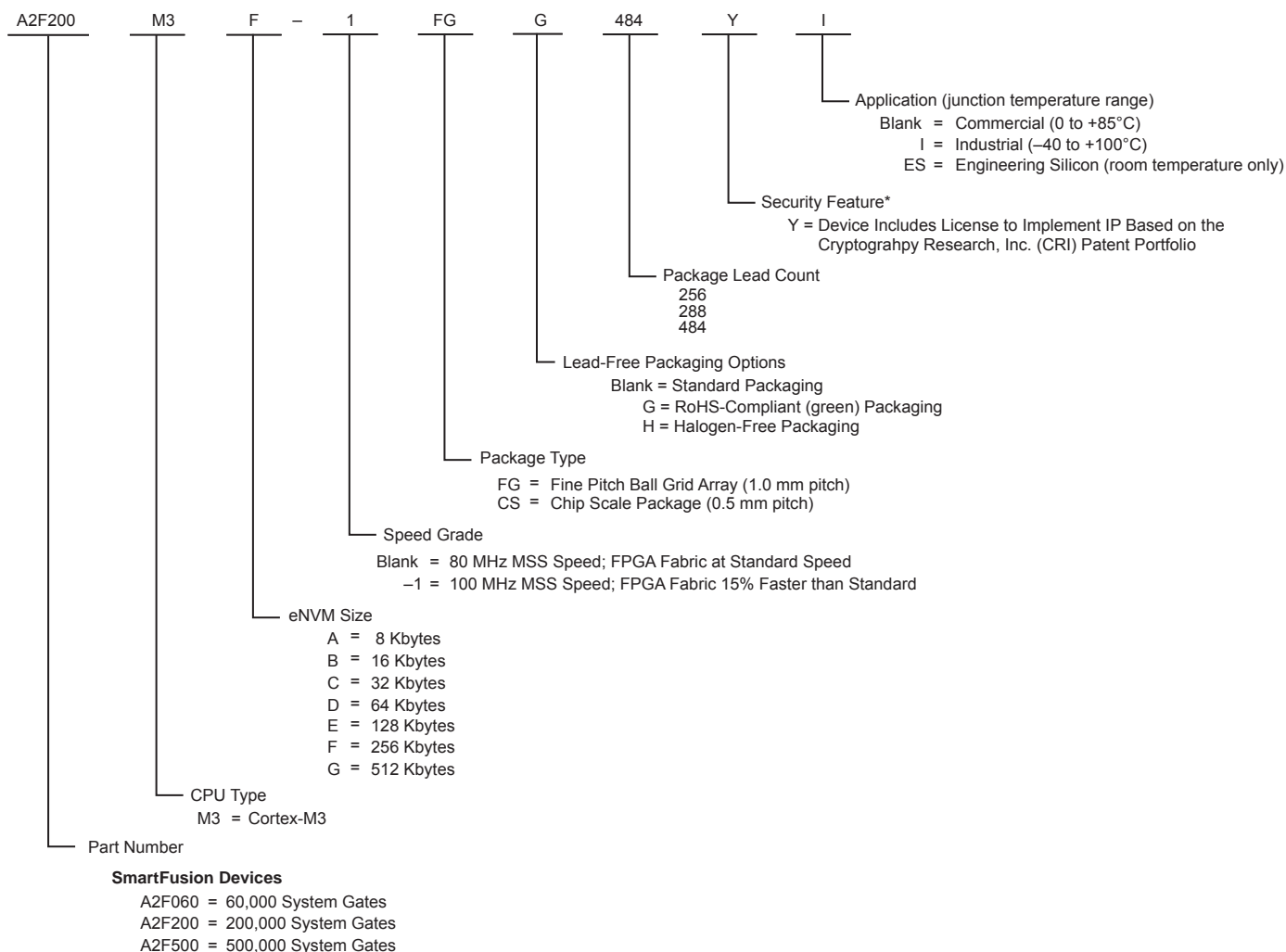
- SDD – Sigma-delta DAC
- SCB – Signal conditioning block
- PDMA – Peripheral DMA
- IAP – In-application programming
- ABPS – Active bipolar prescaler
- WDT – Watchdog Timer
- SWD – Serial Wire Debug

SmartFusion System Architecture



Note: Architecture for A2F500

Product Ordering Codes



Note: *Most devices in the SmartFusion family can be ordered with the Y suffix. Devices with a package size greater or equal to 5x5 mm are supported. Contact your local Actel sales representative for more information.

Temperature Grade Offerings

SmartFusion Devices	A2F060	A2F200	A2F500
CS288	–	C, I	C, I
FG256	C, I	C, I	C, I
FG484	–	C, I	C, I

Notes:

1. C = Commercial Temperature Range: 0°C to 85°C Junction
2. I = Industrial Temperature Range: -40°C to 100°C Junction

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1 – SmartFusion Device Family Overview

Introduction

The Actel SmartFusion™ family of intelligent mixed signal FPGAs builds on the technology first introduced with the Fusion mixed signal FPGAs. SmartFusion devices are made possible by integrating FPGA technology with programmable high-performance analog and hardened ARM® Cortex™-M3 microcontroller blocks on a flash semiconductor process. The SmartFusion family takes its name from the fact that these three discrete technologies are integrated on a single chip, enabling the lowest cost of ownership and smallest footprint solution to you.

General Description

Microcontroller Subsystem (MSS)

The MSS is composed of a 100 MHz Cortex-M3 processor and integrated peripherals, which are interconnected via a multi-layer AHB bus matrix (ABM). This matrix allows the Cortex-M3 processor, FPGA fabric master, Ethernet message authentication controller (MAC), when available, and peripheral DMA (PDMA) controller to act as masters to the integrated peripherals, FPGA fabric, embedded nonvolatile memory (eNVM), embedded synchronous RAM (eSRAM), external memory controller (EMC), and analog compute engine (ACE) blocks.

SmartFusion devices of different densities offer various sets of integrated peripherals. Available peripherals include SPI, I²C, and UART serial ports, embedded FlashROM (EFROM), 10/100 Ethernet MAC, timers, phase-locked loops (PLLs), oscillators, real-time counters (RTC), and peripheral DMA controller (PDMA).

Programmable Analog

Analog Front-End (AFE)

SmartFusion devices offer an enhanced analog front-end compared to Fusion devices. The successive approximation register analog-to-digital converters (SAR ADC) are similar to those found on Fusion devices. SmartFusion also adds first order sigma-delta digital-to-analog converters (SDD DAC).

SmartFusion can handle multiple analog signals simultaneously with its signal conditioning blocks (SCBs). SCBs are made of a combination of active bipolar prescalers (ABPS), comparators, current monitors and temperature monitors. ABPS modules allow larger bipolar voltages to be fed to the ADC. Current monitors take the voltage across an external sense resistor and convert it to a voltage suitable for the ADC input range. Similarly, the temperature monitor reads the current through an external PN-junction (diode or transistor) and converts it internally for the ADC. The SCB also includes comparators to monitor fast signal thresholds without using the ADC. The output of the comparators can be fed to the analog compute engine or the ADC.

Analog Compute Engine (ACE)

The mixed signal blocks found in SmartFusion are controlled and connected to the rest of the system via a dedicated processor called the analog compute engine (ACE). The role of the ACE is to offload control of the analog blocks from the Cortex-M3, thus offering faster throughput or better power consumption compared to a system where the main processor is in charge of monitoring the analog resources. The ACE is built to handle sampling, sequencing, and post-processing of the ADCs, DACs, and SCBs.

ProASIC3 FPGA Fabric

The Actel SmartFusion family, based on the proven, low power, firm-error immune ProASIC®3 flash FPGA architecture, benefits from the advantages only flash-based devices offer:

Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, high performance, and ease of use. Flash-based SmartFusion devices are live at power-up and do not need to be loaded from an external boot PROM at each power-up. On-board security mechanisms prevent access to the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system programming (ISP) to support future design iterations and critical field upgrades, with confidence that valuable IP cannot be compromised or copied. Secure ISP can be performed using the industry standard AES algorithm with MAC data authentication on the device.

Low Power

Flash-based SmartFusion devices exhibit power characteristics similar to those of an ASIC, making them an ideal choice for power-sensitive applications. With SmartFusion devices, there is no power-on current and no high current transition, both of which are common with SRAM-based FPGAs.

SmartFusion devices also have low dynamic power consumption and support both low power standby mode and very low power sleep mode, offering further power savings.

Security

As the nonvolatile, flash-based SmartFusion family requires no boot PROM, there is no vulnerable external bitstream. SmartFusion devices incorporate FlashLock®, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

SmartFusion devices utilize a 128-bit flash-based key lock and a separate AES key to secure programmed IP and configuration data. The FlashROM data in Fusion devices can also be encrypted prior to loading. Additionally, the flash memory blocks can be programmed during runtime using the AES-128 block cipher encryption standard (FIPS Publication 192).

SmartFusion devices with AES-based security allow for secure remote field updates over public networks, such as the Internet, and ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves. As an additional security measure, the FPGA configuration data of a programmed Fusion device cannot be read back, although secure design verification is possible. During design, the user controls and defines both internal and external access to the flash memory blocks.

Security, built into the FPGA fabric, is an inherent component of the SmartFusion family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. SmartFusion with FlashLock and AES security is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected, making secure remote ISP possible. A SmartFusion device provides the most impenetrable security for programmable logic designs.

Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based SmartFusion FPGAs do not require system configuration components such as electrically erasable programmable read-only memories (EEPROMs) or microcontrollers to load device configuration data during power-up. This reduces bill-of-materials costs and PCB area, and increases system security and reliability.

Live at Power-Up

Flash-based SmartFusion devices are live at power-up (LAPU). LAPU SmartFusion devices greatly simplify total system design and reduce total system cost by eliminating the need for complex programmable logic devices (CPLDs). SmartFusion LAPU clocking (PLLs) replaces off-chip clocking resources. In addition, glitches and brownouts in system power will not corrupt the SmartFusion device flash configuration. Unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables reduction or complete removal of expensive voltage monitor and

brownout detection devices from the PCB design. Flash-based SmartFusion devices simplify total system design and reduce cost and design risk, while increasing system reliability.

Immunity to Firm Errors

Firm errors occur most commonly when high-energy neutrons, generated in the atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O configuration behavior in an unpredictable way.

Another source of radiation-induced firm errors is alpha particles. For alpha radiation to cause a soft or firm error, its source must be in very close proximity to the affected circuit. The alpha source must be in the package molding compound or in the die itself. While low-alpha molding compounds are being used increasingly, this helps reduce but does not entirely eliminate alpha-induced firm errors.

Firm errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not occur in SmartFusion flash-based FPGAs. Once it is programmed, the flash cell configuration element of SmartFusion FPGAs cannot be altered by high energy neutrons and is therefore immune to errors from them. Recoverable (or soft) errors occur in the user data SRAMs of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

2 – SmartFusion DC and Switching Characteristics

General Specifications

Operating Conditions

Stresses beyond the operating conditions listed in [Table 2-1](#) may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in [Table 2-3 on page 2-3](#) is not implied.

Table 2-1 • Absolute Maximum Ratings

Symbol	Parameter	Limits	Units
VCC	DC core supply voltage	–0.3 to 1.65	V
VJTAG	JTAG DC voltage	–0.3 to 3.75	V
VPP	Programming voltage	–0.3 to 3.75	V
VCCPLLx	Analog power supply (PLL)	–0.3 to 1.65	V
VCCFPGAIOBx	DC FPGA I/O buffer supply voltage	–0.3 to 3.75	V
VCCMSSIOBx	DC MSS I/O buffer supply voltage	–0.3 to 3.75	V
VI	I/O input voltage	–0.3 V to 3.6 V (when I/O hot insertion mode is enabled) –0.3 V to (VCCxxxxIOBx + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot- insertion mode is disabled)	V
VCC33A	Analog clean 3.3 V supply to the analog circuitry	–0.3 to 3.75	V
VCC33ADCx	Analog 3.3 V supply to ADC	–0.3 to 3.75	V
VCC33AP	Analog clean 3.3 V supply to the charge pump	–0.3 to 3.75	V
VCC33SDDx	Analog 3.3 V supply to the sigma-delta DAC	–0.3 to 3.75	V
VAREFx	Voltage reference for ADC	1.0 to 3.75	V
VCCRCOSC	Analog supply to the integrated RC oscillator	–0.3 to 3.75	V
VDDBAT	External battery supply	–0.3 to 3.75	V
VCCMAINXTAL	Analog supply to the main crystal oscillator	–0.3 to 3.75	V
VCCLPXTAL	Analog supply to the low power 32 kHz crystal oscillator	–0.3 to 3.75	V
VCCENVM	Embedded nonvolatile memory supply	–0.3 to 1.65	V
VCC15A	Analog 1.5 V supply to the analog circuitry	–0.3 to 1.65	V
VCC15ADCx	Analog 1.5 V supply to the ADC	–0.3 to 1.65	V

Note: The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in [Table 2-5 on page 2-4](#).

Table 2-2 • Analog Maximum Ratings

Parameter	Conditions	Min.	Max.	Units
ABPS[n] pad voltage (relative to ground)	GDEC[1:0] = 00 (± 15.36 V range)			
	Absolute maximum	–11.5	14.4	V
	Recommended	–11	14	V
	GDEC[1:0] = 01 (± 10.24 V range)	–11.5	12	V
	GDEC[1:0] = 10 (± 5.12 V range)	–6	6	V
	GDEC[1:0] = 11 (± 2.56 V range)	–3	3	V
CM[n] pad voltage relative to ground)	CMB_DI_ON = 0 (ADC isolated) COMP_EN = 0 (comparator off, for the associated even-numbered comparator)			
	Absolute maximum	–0.3	14.4	V
	Recommended	–11	14	V
	CMB_DI_ON = 0 (ADC isolated) COMP_EN = 1 (comparator on)	–0.3	3	V
	TMB_DI_ON = 1 (direct ADC in)	–0.3	3	V
TM[n] pad voltage (relative to ground)	TMB_DI_ON = 0 (ADC isolated) COMP_EN = 1 (comparator on)	–0.3	3	V
	TMB_DI_ON = 1 (direct ADC in)	–0.3	3	V
ADC[n] pad voltage (relative to ground)		–0.3	3.6	V

Table 2-3 • Recommended Operating Conditions

Symbol	Parameter ¹		Commercial	Industrial	Units
T _J	Junction temperature		0 to +85	–40 to +100	°C
VCC ²	1.5 V DC core supply voltage		1.425 to 1.575	1.425 to 1.575	V
VJTAG	JTAG DC voltage		1.425 to 3.6	1.425 to 3.6	V
VPP	Programming voltage	Programming mode	3.15 to 3.45	3.15 to 3.45	V
		Operation ³	0 to 3.6	0 to 3.6	V
VCCPLLx	Analog power supply (PLL)		1.425 to 1.575	1.425 to 1.575	V
VCCFPGAIOBx/ VCCMSSIOBx ⁴	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.3 V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V
	LVDS differential I/O		2.375 to 2.625	2.375 to 2.625	V
	LVPECL differential I/O		3.0 to 3.6	3.0 to 3.6	V
VCC33A ⁵	Analog clean 3.3 V supply to the analog circuitry		3.15 to 3.45	3.15 to 3.45	V
VCC33ADCx ⁵	Analog 3.3 V supply to ADC		3.15 to 3.45	3.15 to 3.45	V
VCC33AP ⁵	Analog clean 3.3 V supply to the charge pump		3.15 to 3.45	3.15 to 3.45	V
VCC33SDDx ⁵	Analog 3.3 V supply to sigma-delta DAC		3.15 to 3.45	3.15 to 3.45	V
VAREF _x	Voltage reference for ADC		2.527 to 3.3	2.527 to 3.3	V
VCCRCOSC	Analog supply to the integrated RC oscillator		3.15 to 3.45	3.15 to 3.45	V
VDDBAT	External battery supply		2.7 to 3.63	2.7 to 3.63	V
VCCMAINXTAL ⁵	Analog supply to the main crystal oscillator		3.15 to 3.45	3.15 to 3.45	V
VCCLPXTAL ⁵	Analog supply to the low power 32 KHz crystal oscillator		3.15 to 3.45	3.15 to 3.45	V
VCCENVM	Embedded nonvolatile memory supply		1.425 to 1.575	1.425 to 1.575	V
VCC15A ²	Analog 1.5 V supply to the analog circuitry		1.425 to 1.575	1.425 to 1.575	V
VCC15ADCx ²	Analog 1.5 V supply to the ADC		1.425 to 1.575	1.425 to 1.575	V

Notes:

1. All parameters representing voltages are measured with respect to GND unless otherwise specified.
2. The following 1.5 V supplies should be connected together while following proper noise filtering practices: VCC, VCC15A, and VCC15ADCx.
3. VPP can be left floating during operation (not programming mode).
4. The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in [Table 2-18 on page 2-25](#). VCCxxxIOBx should be at the same voltage within a given I/O bank.
5. The following 3.3 V supplies should be connected together while following proper noise filtering practices: VCC33A, VCC33ADCx, VCC33AP, VCC33SDDx, VCCMAINXTAL, and VCCLPXTAL.

Table 2-4 • FPGA and Embedded Flash Programming, Storage and Operating Limits

Product Grade	Storage Temperature	Element	Grade Programming Cycles	Retention
Commercial	Min. $T_J = 0^{\circ}\text{C}$ Min. $T_J = 85^{\circ}\text{C}$	FPGA/FlashROM	500	20 years
		Embedded Flash	< 1,000	20 years
			< 10,000	10 years
			< 15,000	5 years
Industrial	Min. $T_J = -40^{\circ}\text{C}$ Min. $T_J = 100^{\circ}\text{C}$	FPGA/FlashROM	500	20 years
		Embedded Flash	< 1,000	20 years
			< 10,000	10 years
			< 15,000	5 years

Table 2-5 • Overshoot and Undershoot Limits ¹

VCCxxxxIOBx	Average VCCxxxxIOBx–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle ²	Maximum Overshoot/Undershoot ²
2.7 V or less	10%	1.4 V
	5%	1.49 V
3 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Notes:

1. Based on reliability requirements at 85°C .
2. The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.
3. This table does not provide PCI overshoot/undershoot limits.

Power Supply Sequencing Requirement

SmartFusion devices have an on-chip 1.5 V regulator, but usage of an external 1.5 V supply is also allowed while the on-chip regulator is disabled. In that case, the 3.3 V supplies (VCC33A, etc.) should be powered before 1.5 V (VCC, etc.) supplies. The 1.5 V supplies should be enabled only after 3.3 V supplies reach a value higher than 2.7 V.

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every SmartFusion[®] device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in [Figure 2-1 on page 2-6](#).

There are five regions to consider during power-up.

SmartFusion I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCxxxxIOBx are above the minimum specified trip points ([Figure 2-1 on page 2-6](#)).
2. VCCxxxxIOBx > VCC – 0.75 V (typical)

3. Chip is in the SoC Mode.

VCCxxxxIOBx Trip Point:

Ramping up: $0.6\text{ V} < \text{trip_point_up} < 1.2\text{ V}$

Ramping down: $0.5\text{ V} < \text{trip_point_down} < 1.1\text{ V}$

VCC Trip Point:

Ramping up: $0.6\text{ V} < \text{trip_point_up} < 1.1\text{ V}$

Ramping down: $0.5\text{ V} < \text{trip_point_down} < 1\text{ V}$

VCC and VCCxxxxIOBx ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCxxxxIOBx.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

PLL Behavior at Brownout Condition

Actel recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until VCC and VCCPLLx exceed brownout activation levels. The VCC activation level is specified as 1.1 V worst-case (see [Figure 2-1 on page 2-6](#) for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels ($0.75\text{ V} \pm 0.25\text{ V}$), the PLL output lock signal goes low and/or the output clock is lost. Refer to the "Power-Up/-Down Behavior of Low Power Flash Devices" chapter of the [ProASIC3 FPGA Fabric User's Guide](#) for information on clock and lock recovery.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers

Output buffers, after 200 ns delay from input buffer activation

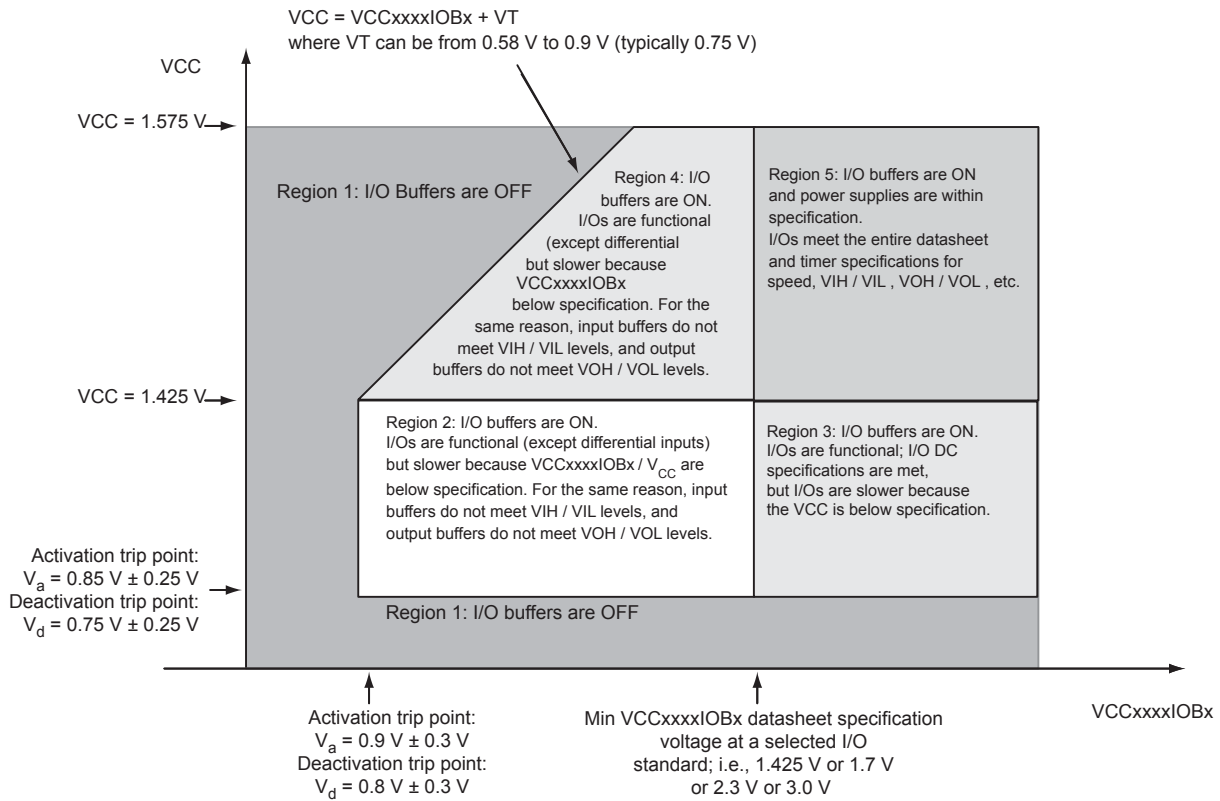


Figure 2-1 • I/O State as a Function of $VCC_{xxxxIOBx}$ and VCC Voltage Levels

Thermal Characteristics

Introduction

The temperature variable in the Actel Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction temperature to be higher than the ambient, case, or board temperatures. EQ 1 through EQ 3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

EQ 1

$$\theta_{JB} = \frac{T_J - T_B}{P}$$

EQ 2

$$\theta_{JC} = \frac{T_J - T_C}{P}$$

EQ 3

where

θ_{JA} = Junction-to-air thermal resistance

θ_{JB} = Junction-to-board thermal resistance

θ_{JC} = Junction-to-case thermal resistance

T_J = Junction temperature

T_A = Ambient temperature

T_B = Board temperature (measured 1.0 mm away from the package edge)

T_C = Case temperature

P = Total power dissipated by the device

Table 2-6 • Package Thermal Resistance

Product	Die Size (mm)	θ_{JA}			θ_{JC}	θ_{JB}	Units
		Still Air	1.0 m/s	2.5 m/s			
A2F200M3F-FG256	X = 4.0; Y = 5.6	33.7	30.0	28.3	9.3	24.8	°C/W
A2F200M3F-FG484	X = 5.10; Y = 7.3	21.8	18.2	16.7	7.7	16.8	°C/W

Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in actual performance of the product. It should be used with caution but is useful for comparing the thermal performance of one package to another.

A sample calculation showing the maximum power dissipation allowed for the A2F200-FG484 package under forced convection of 1.0 m/s and 75°C ambient temperature is as follows:

$$\text{Maximum Power Allowed} = \frac{T_{J(\text{MAX})} - T_{A(\text{MAX})}}{\theta_{JA}}$$

EQ 4

where

θ_{JA} = 19.00°C/W (taken from Table 2-6 on page 2-7).

T_A = 75.00°C

$$\text{Maximum Power Allowed} = \frac{100.00^\circ\text{C} - 75.00^\circ\text{C}}{19.00^\circ\text{C/W}} = 1.3 \text{ W}$$

EQ 5

The power consumption of a device can be calculated using the Actel power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package. If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink can be attached on top of the case, or the airflow inside the system must be increased.

Theta-JB

Junction-to-board thermal resistance (θ_{JB}) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from junction to board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks. Constant temperature is applied to the surface in consideration and acts as a boundary condition. This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

Calculation for Heat Sink

For example, in a design implemented in an A2F200-FG484 package with 2.5 m/s airflow, the power consumption value using the power calculator is 3.00 W. The user-dependent T_a and T_j are given as follows:

T_J = 100.00°C

T_A = 70.00°C

From the datasheet:

θ_{JA} = 17.00°C/W

θ_{JC} = 8.28°C/W

$$P = \frac{T_J - T_A}{\theta_{JA}} = \frac{100^\circ\text{C} - 70^\circ\text{C}}{17.00^\circ\text{C/W}} = 1.76 \text{ W}$$

EQ 6

The 1.76 W power is less than the required 3.00 W. The design therefore requires a heat sink, or the airflow where the device is mounted should be increased. The design's total junction-to-air thermal resistance requirement can be estimated by EQ 7:

$$\theta_{JA(\text{total})} = \frac{T_J - T_A}{P} = \frac{100^\circ\text{C} - 70^\circ\text{C}}{3.00 \text{ W}} = 10.00^\circ\text{C/W}$$

EQ 7

Determining the heat sink's thermal performance proceeds as follows:

$$\theta_{JA(\text{TOTAL})} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

EQ 8

where

$$\theta_{JA} = 0.37^\circ\text{C/W}$$

= Thermal resistance of the interface material between the case and the heat sink, usually provided by the thermal interface manufacturer

$$\theta_{SA} = \text{Thermal resistance of the heat sink in } ^\circ\text{C/W}$$

$$\theta_{SA} = \theta_{JA(\text{TOTAL})} - \theta_{JC} - \theta_{CS}$$

EQ 9

$$\theta_{SA} = 13.33^\circ\text{C/W} - 8.28^\circ\text{C/W} - 0.37^\circ\text{C/W} = 5.01^\circ\text{C/W}$$

A heat sink with a thermal resistance of 5.01°C/W or better should be used. Thermal resistance of heat sinks is a function of airflow. The heat sink performance can be significantly improved with increased airflow.

Carefully estimating thermal resistance is important in the long-term reliability of an Actel FPGA. Design engineers should always correlate the power consumption of the device with the maximum allowable power dissipation of the package selected for that device.

Note: The junction-to-air and junction-to-board thermal resistances are based on JEDEC standard (JESD-51) and assumptions made in building the model. It may not be realized in actual application and therefore should be used with a degree of caution. Junction-to-case thermal resistance assumes that all power is dissipated through the case.

Temperature and Voltage Derating Factors

Table 2-7 • Temperature and Voltage Derating Factors for Timing Delays
(normalized to $T_J = 85^\circ\text{C}$, worst-case VCC = 1.425 V)

Array Voltage VCC (V)	Junction Temperature ($^\circ\text{C}$)					
	-40°C	0°C	25°C	70°C	85°C	100°C
1.425	0.86	0.91	0.93	0.98	1.00	1.03
1.500	0.81	0.86	0.88	0.93	0.95	0.97
1.575	0.78	0.83	0.85	0.90	0.91	0.94

Calculating Power Dissipation

Quiescent Supply Current

Table 2-8 • Quiescent Supply Current Characteristics

Power Supplies Configuration										
Modes and Power Supplies	VCCxxxIOBx VCCFPGAIOBx VCCMSSIOBx	VCC33A / VCC33ADCx VCC33AP / VCC33SDDx VCCMAINXTAL / VCCLPXTAL	VCC / VCC15A / VCC15ADCx VCCPLLx / VCOMPLAx VCCENVM	VDDBAT	VCCRCOSC	VJTAG	VPP	eNVM (reset/off)	LPXTAL (enable/disable)	MAINXTAL (enable/disable)
Power-down	0 V ¹	3.3 V	0 V	N/A	0 V	0 V	0 V	Off	Disable	Disable
Sleep	0 V ^{1,2}	3.3 V	0 V	N/A	0 V	0 V	0 V	Off	Enable	Disable
Time Keeping mode	0 V	0 V	0 V	3.3 V	0 V	0 V	0 V	Off	Enable	Disable
Standby mode	On ⁵	3.3 V	1.5 V	N/A	3.3 V	N/A	N/A	Reset	Enable	Disable
Parameter	Modes	A2F200				A2F500				
		1.5 V Domain		3.3 V Domain ³		1.5 V Domain		3.3 V Domain		
IDC1 ⁴	Power-down	N/A				N/A				
IDC2 ⁴	Sleep	N/A				N/A				
IDC3	Time Keeping mode	N/A		10 μA		N/A		10 μA		
IDC4	Standby mode	3 mA		1 mA		TBD		1 mA		

Notes:

1. When using PU_N, the I/O supplies can be turned off during Sleep and Power-Down modes. Power to the I/O should be restored as the device transitions to SoC Mode by the same control that triggers PU_N.
2. When using RTC_MATCH to trigger transition to SoC mode, I/O supply may be restored by using the 1.5 V as a trigger, or by maintaining at least one I/O bank supply ON during Sleep mode to restore the supply to all other IO banks.
3. Current monitors and temperature monitors should not be used when Power-down and/or Sleep mode are required by the application.
4. Power mode and Sleep mode are consuming higher current than expected in the current version of silicon. These specifications will be updated when a new version of the silicon is available.
5. On means proper voltage is applied. Refer to [Table 2-3 on page 2-3](#) for recommended operating conditions.

Power-Down and Sleep Mode Implementation

VCCRCOSC, VJTAG, and VPP should be connected to ground during Power-Down and Sleep modes. Note that when VJTAG is not powered, the 1.5 V voltage regulator cannot be enabled through TRSTB.

VCCRCOSC, VPP and VJTAG can be controlled through an external switch. Actel recommends ADG839, ADG849, or ADG841 as possible switches. Figure 2-2 shows the implementation for controlling VPP. The IN signal of the switch can be connected to PTBASE of the SmartFusion device. VCCRCOSC and VJTAG can be controlled in same manner.

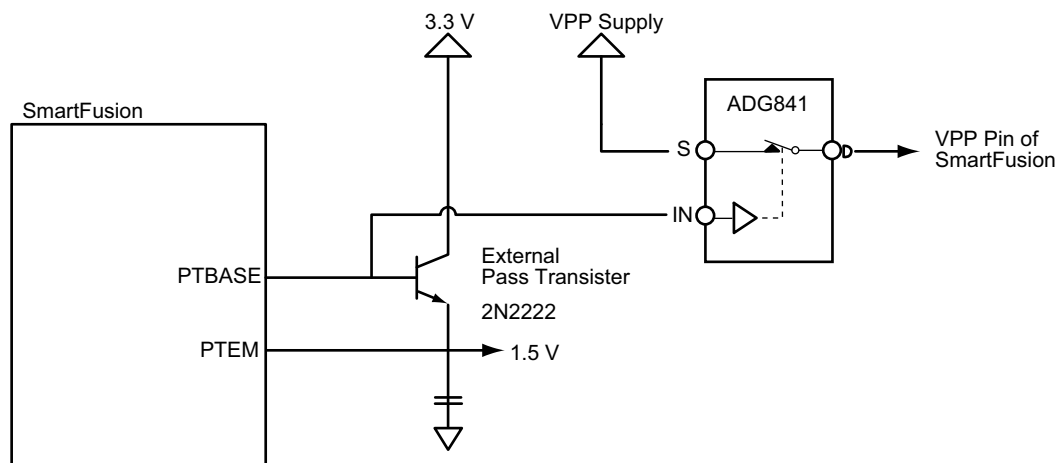


Figure 2-2 • Implementation to Control VPP

Power per I/O Pin

Table 2-9 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings
Applicable to FPGA I/O Banks

	VCCFPGAIOBx (V)	Static Power PDC7 (mW)	Dynamic Power PAC9 (μW/MHz)
Single-Ended			
3.3 V LVTTTL / 3.3 V LVCMOS	3.3	–	16.22
2.5 V LVCMOS	2.5	–	4.65
1.8 V LVCMOS	1.8	–	1.65
1.5 V LVCMOS (JESD8-11)	1.5	–	0.98
3.3 V PCI	3.3	–	17.64
3.3 V PCI-X	3.3	–	17.64
Differential			
LVDS	2.5	2.26	0.95
LVPECL	3.3	5.72	1.63

Table 2-10 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings
Applicable to MSS I/O Banks

	VCCMSSIOBx (V)	Static Power PDC7 (mW)	Dynamic Power PAC9 (μW/MHz)
Single-Ended			
3.3 V LVTTTL / 3.3 V LVCMOS	3.3	–	17.21
3.3 V LVCMOS / 3.3 V LVCMOS – Schmitt trigger	3.3	–	20.00
2.5 V LVCMOS	2.5	–	5.55
2.5 V LVCMOS – Schmitt trigger	2.5	–	7.03
1.8 V LVCMOS	1.8	–	2.61
1.8 V LVCMOS – Schmitt trigger	1.8	–	2.72
1.5 V LVCMOS (JESD8-11)	1.5	–	1.98
1.5 V LVCMOS (JESD8-11) – Schmitt trigger	1.5	–	1.93

Table 2-11 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings*
Applicable to FPGA I/O Banks

	C _{LOAD} (pF)	VCCFPGAIOBx (V)	Static Power PDC8 (mW)	Dynamic Power PAC10 (μW/MHz)
Single-Ended				
3.3 V LVTTTL / 3.3 V LVCMOS	35	3.3	–	468.67
2.5 V LVCMOS	35	2.5	–	267.48
1.8 V LVCMOS	35	1.8	–	149.46
1.5 V LVCMOS (JESD8-11)	35	1.5	–	103.12
3.3 V PCI	10	3.3	–	201.02
3.3 V PCI-X	10	3.3	–	201.02
Differential				
LVDS	–	2.5	7.74	89.71
LVPECL	–	3.3	19.54	167.54

Note: *Dynamic power consumption is given for standard load and software default drive strength and output slew.

Table 2-12 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings
Applicable to MSS I/O Banks

	C _{LOAD} (pF)	VCCMSSIOBx (V)	Static Power PDC8 (mW) ²	Dynamic Power PAC10 (μW/MHz) ³
Single-Ended				
3.3 V LVTTTL / 3.3 V LVCMOS	10	3.3	–	155.65
2.5 V LVCMOS	10	2.5	–	88.23
1.8 V LVCMOS	10	1.8	–	45.03
1.5 V LVCMOS (JESD8-11)	10	1.5	–	31.01

Power Consumption of Various Internal Resources

Table 2-13 • Different Components Contributing to Dynamic Power Consumption in SmartFusion Devices

Parameter	Definition	Power Supply		Device		Units
		Name	Domain	A2F200	A2F500	
PAC1	Clock contribution of a Global Rib	VCC	1.5 V	9.3		μW/MHz
PAC2	Clock contribution of a Global Spine	VCC	1.5 V	0.8		μW/MHz
PAC3	Clock contribution of a VersaTile row	VCC	1.5 V	0.81		μW/MHz
PAC4	Clock contribution of a VersaTile used as a sequential module	VCC	1.5 V	0.11		μW/MHz
PAC5	First contribution of a VersaTile used as a sequential module	VCC	1.5 V	0.07		μW/MHz
PAC6	Second contribution of a VersaTile used as a sequential module	VCC	1.5 V	0.29		μW/MHz
PAC7	Contribution of a VersaTile used as a combinatorial module	VCC	1.5 V	0.29		μW/MHz
PAC8	Average contribution of a routing net	VCC	1.5 V	0.70		μW/MHz
PAC9	Contribution of an I/O input pin (standard dependent)	VCCxxxxIOBx/VCC	See Table 2-9 and Table 2-10 on page 2-12			
PAC10	Contribution of an I/O output pin (standard dependent)	VCCxxxxIOBx/VCC	See Table 2-11 and Table 2-12 on page 2-12			
PAC11	Average contribution of a RAM block during a read operation	VCC	1.5 V	25.00		μW/MHz
PAC12	Average contribution of a RAM block during a write operation	VCC	1.5 V	30.00		μW/MHz
PAC13	Dynamic Contribution for PLL	VCC	1.5 V	2.60		μW/MHz
PAC15	Contribution of NVM block during a read operation (F < 33MHz)	VCC	1.5 V	358.00		μW/MHz
PAC16	1st contribution of NVM block during a read operation (F > 33MHz)	VCC	1.5 V	12.88		mW
PAC17	2nd contribution of NVM block during a read operation (F > 33MHz)	VCC	1.5 V	4.80		μW/MHz
PAC18	Main Crystal Oscillator contribution	VCCMAINXTAL	3.3 V	1.98		mW
PAC19a	RC Oscillator contribution	VCCRCOSC	3.3 V	3.30		mW
PAC19b	RC Oscillator contribution	VCC	1.5 V	3.00		mW
PAC20a	Analog Block Dynamic Power Contribution of the ADC	VCC33ADCx	3.3 V	8.25		mW
PAC20b	Analog Block Dynamic Power Contribution of the ADC	VCC15ADCx	1.5 V	3.00		mW
PAC21	Low Power Crystal Oscillator contribution	VCCLPXTAL	3.3 V	33.00		μW
PAC22	MSS Dynamic Power Contribution – Running Drystone at 100MHz ¹	VCC	1.5 V	67.50		mW
PAC23	Temperature Monitor Power Contribution	See Table 2-91 on page 2-80	–	1.23		mW

Table 2-13 • Different Components Contributing to Dynamic Power Consumption in SmartFusion Devices

Parameter	Definition	Power Supply		Device		Units
		Name	Domain	A2F200	A2F500	
PAC24	Current Monitor Power Contribution	See Table 2-90 on page 2-79	–	1.03		mW
PAC25	ABPS Power Contribution	See Table 2-93 on page 2-83	–	0.70		mW
PAC26	Sigma-Delta DAC Power Contribution ²	See Table 2-95 on page 2-85	–	0.59		mW
PAC27	Comparator Power Contribution	See Table 2-94 on page 2-84	–	0.96		mW
PAC28	Voltage Regulator Power Contribution ³	See Table 2-96 on page 2-87	–	36.30		mW

Notes:

1. For a different use of MSS peripherals and resources, refer to SmartPower.
2. Assumes Input = Half Scale Operation mode.
3. Assumes 100 mA load on 1.5 V domain.

Table 2-14 • Different Components Contributing to the Static Power Consumption in SmartFusion Devices

Parameter	Definition	Power Supply		Device		Units
		Name	Domain	A2F200	A2F500	
PDC1	Core static power contribution	VCC	1.5 V	1.50		mW
PDC2	Device static power contribution in Standby Mode	See Table 2-8 on page 2-10	–	1.50		mW
PDC3	Device static power contribution in Time Keeping mode	See Table 2-8 on page 2-10	3.3 V	0.00		mW
PDC4	eNVM static power contribution	See Table 2-8 on page 2-10	1.5 V	1.19		mW
PDC7	Static contribution per input pin (standard dependent contribution)	VCCxxxxIOBx/VCC	See Table 2-9 and Table 2-10 on page 2-12 .			
PDC8	Static contribution per input pin (standard dependent contribution)	VCCxxxxIOBx/VCC	See Table 2-11 and Table 2-12 on page 2-12 .			
PDC9	Static contribution per PLL	VCC	1.5 V	2.55		mW

Table 2-15 • eNVM Dynamic Power Consumption

Parameter	Description	Condition	Min.	Typ.	Max.	Units
eNVM System	eNVM array operating power					
		Idle		795		μA
		Read operation	See Table 2-13 on page 2-13 .			
		Erase		900		μA
		Write		900		μA
PNVMCTRL	eNVM controller operating power			20		μW/MHz

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in the Libero IDE software.

The power calculation methodology described below uses the following variables:

- The number of PLLs/CCCs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- The number of eNVM blocks used in the design
- The analog block used in the design, including the temperature monitor, current monitor, ABPS, sigma-delta DAC, comparator, low power crystal oscillator, RC oscillator and the main crystal oscillator
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in [Table 2-16 on page 2-20](#).
- Enable rates of output buffers—guidelines are provided for typical applications in [Table 2-17 on page 2-20](#).
- Read rate and write rate to the memory—guidelines are provided for typical applications in [Table 2-17 on page 2-20](#).
- Read rate to the eNVM blocks

The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption— P_{TOTAL}

SoC Mode, Standby Mode, and Time Keeping Mode.

$$P_{TOTAL} = P_{STAT} + P_{DYN}$$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption— P_{STAT}

SoC Mode

$$P_{STAT} = P_{DC1} + (N_{eNVM-BLOCKS} * P_{DC4}) + (N_{INPUTS} * P_{DC7}) + (N_{OUTPUTS} * P_{DC8}) + (N_{PLLS} * P_{DC9})$$

$N_{eNVM-BLOCKS}$ is the number of eNVM blocks available in the device.

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

N_{PLLS} is the number of PLLs available in the device.

Standby Mode

$$P_{STAT} = P_{DC2}$$

Time Keeping Mode

$$P_{STAT} = P_{DC3}$$

Total Dynamic Power Consumption— P_{DYN}

SoC Mode

$$P_{DYN} = P_{CLOCK} + P_{S-CELL} + P_{C-CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL} + P_{eNVM} + P_{XTAL-OSC} + P_{RC-OSC} + P_{AB} + P_{LPXTAL-OSC}$$

Standby Mode

$$P_{\text{DYN}} = P_{\text{RC-OSC}} + P_{\text{LPXTAL-OSC}}$$

Time Keeping Mode

$$P_{\text{DYN}} = P_{\text{LPXTAL-OSC}}$$

Global Clock Dynamic Contribution— P_{CLOCK}

SoC Mode

$$P_{\text{CLOCK}} = (P_{\text{AC1}} + N_{\text{SPINE}} * P_{\text{AC2}} + N_{\text{ROW}} * P_{\text{AC3}} + N_{\text{S-CELL}} * P_{\text{AC4}}) * F_{\text{CLK}}$$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in [Table 2-16 on page 2-20](#).

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in [Table 2-16 on page 2-20](#).

F_{CLK} is the global clock signal frequency.

$N_{\text{S-CELL}}$ is the number of VersaTiles used as sequential modules in the design.

Standby Mode and Time Keeping Mode

$$P_{\text{CLOCK}} = 0 \text{ W}$$

Sequential Cells Dynamic Contribution— $P_{\text{S-CELL}}$

SoC Mode

$$P_{\text{S-CELL}} = N_{\text{S-CELL}} * (P_{\text{AC5}} + (\alpha_1 / 2) * P_{\text{AC6}}) * F_{\text{CLK}}$$

$N_{\text{S-CELL}}$ is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in [Table 2-16 on page 2-20](#).

F_{CLK} is the global clock signal frequency.

Standby Mode and Time Keeping Mode

$$P_{\text{S-CELL}} = 0 \text{ W}$$

Combinatorial Cells Dynamic Contribution— $P_{\text{C-CELL}}$

SoC Mode

$$P_{\text{C-CELL}} = N_{\text{C-CELL}} * (\alpha_1 / 2) * P_{\text{AC7}} * F_{\text{CLK}}$$

$N_{\text{C-CELL}}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in [Table 2-16 on page 2-20](#).

F_{CLK} is the global clock signal frequency.

Standby Mode and Time Keeping Mode

$$P_{\text{C-CELL}} = 0 \text{ W}$$

Routing Net Dynamic Contribution— P_{NET}

SoC Mode

$$P_{\text{NET}} = (N_{\text{S-CELL}} + N_{\text{C-CELL}}) * (\alpha_1 / 2) * P_{\text{AC8}} * F_{\text{CLK}}$$

$N_{\text{S-CELL}}$ is the number VersaTiles used as sequential modules in the design.

$N_{\text{C-CELL}}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in [Table 2-16 on page 2-20](#).

F_{CLK} is the frequency of the clock driving the logic including these nets.

Standby Mode and Time Keeping Mode

$$P_{NET} = 0 \text{ W}$$

I/O Input Buffer Dynamic Contribution— P_{INPUTS}

SoC Mode

$$P_{INPUTS} = N_{INPUTS} * (\alpha_2 / 2) * P_{AC9} * F_{CLK}$$

Where:

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in [Table 2-16 on page 2-20](#).

F_{CLK} is the global clock signal frequency.

Standby Mode and Time Keeping Mode

$$P_{INPUTS} = 0 \text{ W}$$

I/O Output Buffer Dynamic Contribution— $P_{OUTPUTS}$

SoC Mode

$$P_{OUTPUTS} = N_{OUTPUTS} * (\alpha_2 / 2) * \beta_1 * P_{AC10} * F_{CLK}$$

Where:

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in [Table 2-16 on page 2-20](#).

β_1 is the I/O buffer enable rate—guidelines are provided in [Table 2-17 on page 2-20](#).

F_{CLK} is the global clock signal frequency.

Standby Mode and Time Keeping Mode

$$P_{OUTPUTS} = 0 \text{ W}$$

FPGA Fabric SRAM Dynamic Contribution— P_{MEMORY}

SoC Mode

$$P_{MEMORY} = (N_{BLOCKS} * P_{AC11} * \beta_2 * F_{READ-CLOCK}) + (N_{BLOCKS} * P_{AC12} * \beta_3 * F_{WRITE-CLOCK})$$

Where:

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ-CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations—guidelines are provided in [Table 2-17 on page 2-20](#).

β_3 the RAM enable rate for write operations—guidelines are provided in [Table 2-17 on page 2-20](#).

$F_{WRITE-CLOCK}$ is the memory write clock frequency.

Standby Mode and Time Keeping Mode

$$P_{MEMORY} = 0 \text{ W}$$

PLL/CCC Dynamic Contribution— P_{PLL}

SoC Mode

$$P_{PLL} = P_{AC13} * F_{CLKOUT}$$

F_{CLKIN} is the input clock frequency.

F_{CLKOUT} is the output clock frequency.¹

Standby Mode and Time Keeping Mode

1. The PLL dynamic contribution depends on the input clock frequency, the number of output clock signals generated by the PLL, and the frequency of each output clock. If a PLL is used to generate more than one output clock, include each output clock in the formula output clock by adding its corresponding contribution ($P_{AC14} * F_{CLKOUT}$ product) to the total PLL contribution.

$$P_{PLL} = 0 \text{ W}$$

Embedded Nonvolatile Memory Dynamic Contribution— P_{eNVM}

SoC Mode

The eNVM dynamic power consumption is a piecewise linear function of frequency.

$$P_{eNVM} = N_{eNVM-BLOCKS} * \beta_4 * P_{AC15} * F_{READ-eNVM} \text{ when } F_{READ-eNVM} \leq 33 \text{ MHz,}$$

$$P_{eNVM} = N_{eNVM-BLOCKS} * \beta_4 * (P_{AC16} + P_{AC17} * F_{READ-eNVM}) \text{ when } F_{READ-eNVM} > 33 \text{ MHz}$$

Where:

$N_{eNVM-BLOCKS}$ is the number of eNVM blocks used in the design.

β_4 is the eNVM enable rate for read operations. Default is 0 (eNVM mainly in idle state).

$F_{READ-eNVM}$ is the eNVM read clock frequency.

Standby Mode and Time Keeping Mode

$$P_{eNVM} = 0 \text{ W}$$

Main Crystal Oscillator Dynamic Contribution— $P_{XTL-OSC}$

SoC Mode

$$P_{XTL-OSC} = P_{AC18}$$

Standby Mode

$$P_{XTL-OSC} = 0 \text{ W}$$

Time Keeping Mode

$$P_{XTL-OSC} = 0 \text{ W}$$

Low Power Oscillator Crystal Dynamic Contribution— $P_{LPXTAL-OSC}$

Operating, Standby, and Time Keeping Mode

$$P_{LPXTAL-OSC} = P_{AC21}$$

RC Oscillator Dynamic Contribution— P_{RC-OSC}

SoC Mode

$$P_{RC-OSC} = P_{AC19A} + P_{AC19B}$$

Standby Mode and Time Keeping Mode

$$P_{RC-OSC} = 0 \text{ W}$$

Analog System Dynamic Contribution— P_{AB}

SoC Mode

$$P_{AB} = P_{AC23} * N_{TM} + P_{AC24} * N_{CM} + P_{AC25} * N_{ABPS} + P_{AC26} * N_{SDD} + P_{AC27} * N_{COMP} + P_{ADC} * N_{ADC} + P_{VR}$$

Where:

N_{CM} is the number of current monitor blocks

N_{TM} is the number of temperature monitor blocks

N_{SDD} is the number of sigma-delta DAC blocks

N_{ABPS} is the number of ABPS blocks

N_{ADC} is the number of ADC blocks

N_{COMP} is the number of comparator blocks

$$P_{VR} = P_{AC28}$$

$$P_{ADC} = P_{AC20A} + P_{AC20B}$$

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that the net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100%, as all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
 - Bit 0 (LSB) = 100%
 - Bit 1 = 50%
 - Bit 2 = 25%
 - ...
 - Bit 7 (MSB) = 0.78125%
 - Average toggle rate = (100% + 50% + 25% + 12.5% + . . . 0.78125%) / 8.

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When non-tristate output buffers are used, the enable rate should be 100%.

Table 2-16 • Toggle Rate Guidelines Recommended for Power Calculation

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

Table 2-17 • Enable Rate Guidelines Recommended for Power Calculation

Component	Definition	Guideline
β_1	I/O output buffer enable rate	Toggle rate of the logic driving the output buffer
β_2	FPGA fabric SRAM enable rate for read operations	12.5%
β_3	FPGA fabric SRAM enable rate for write operations	12.5%
β_4	eNVM enable rate for read operations	< 5%

User I/O Characteristics

Timing Model

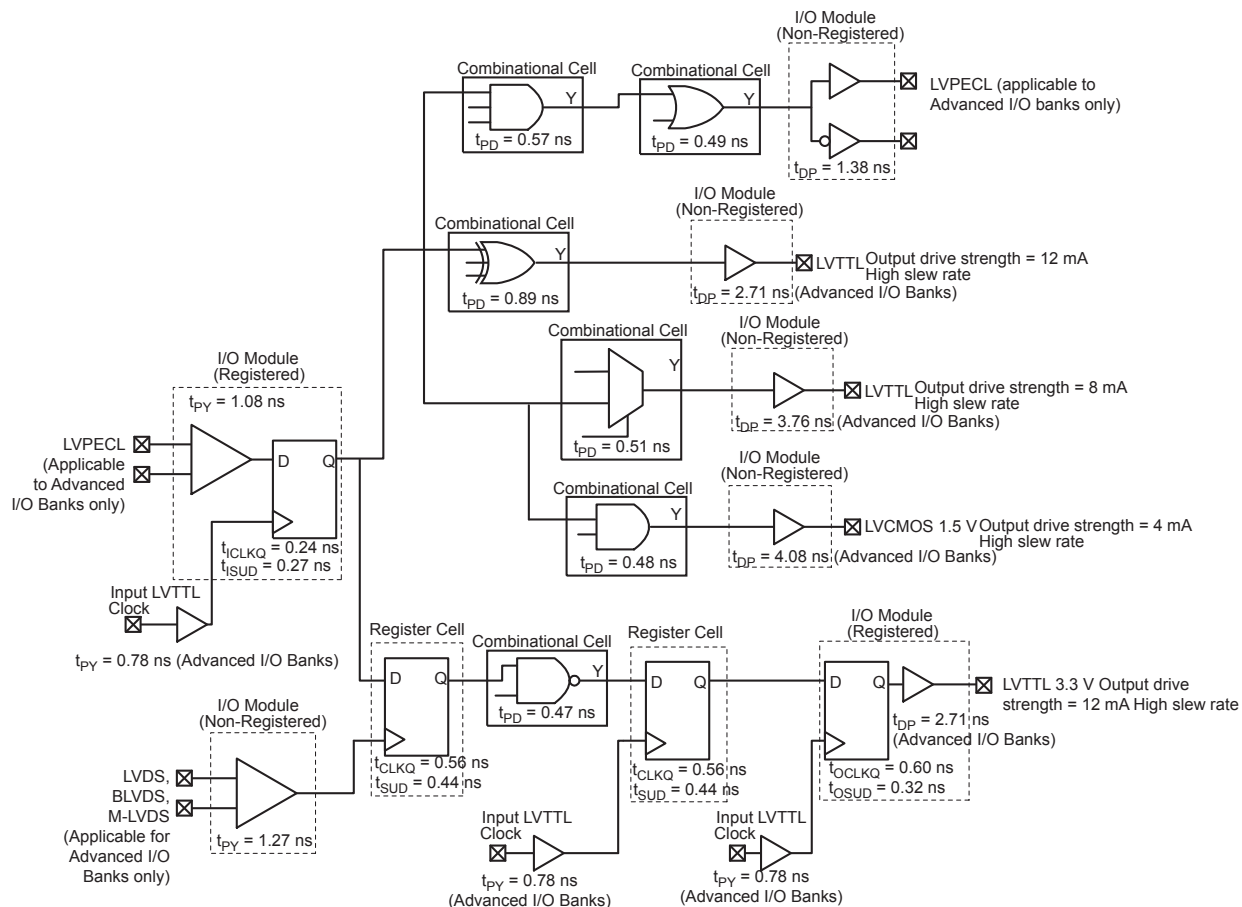


Figure 2-3 • Timing Model

Operating Conditions: –1 Speed, Commercial Temperature Range ($T_J = 85^\circ\text{C}$), Worst Case VCC = 1.425 V

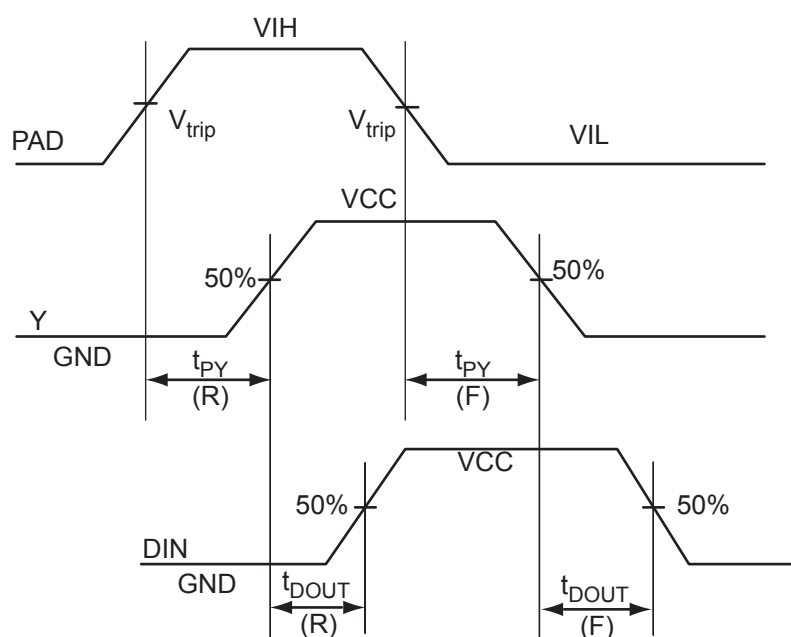
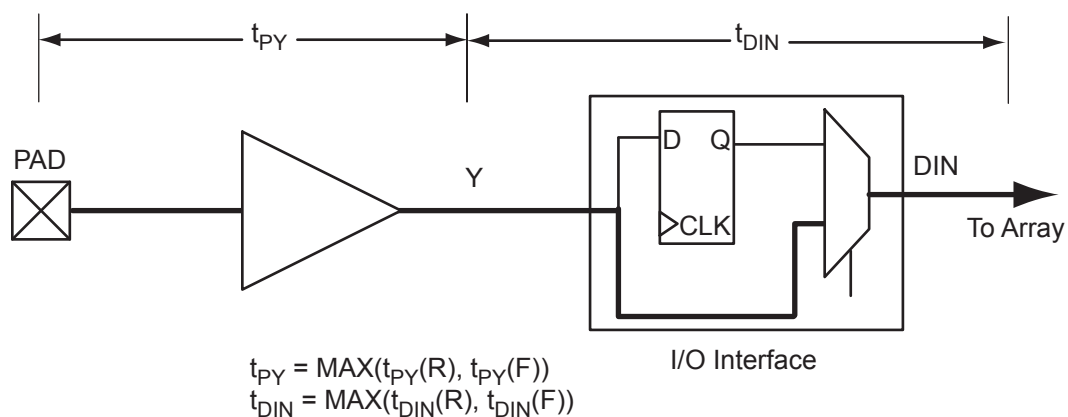


Figure 2-4 • Input Buffer Timing Model and Delays (example)

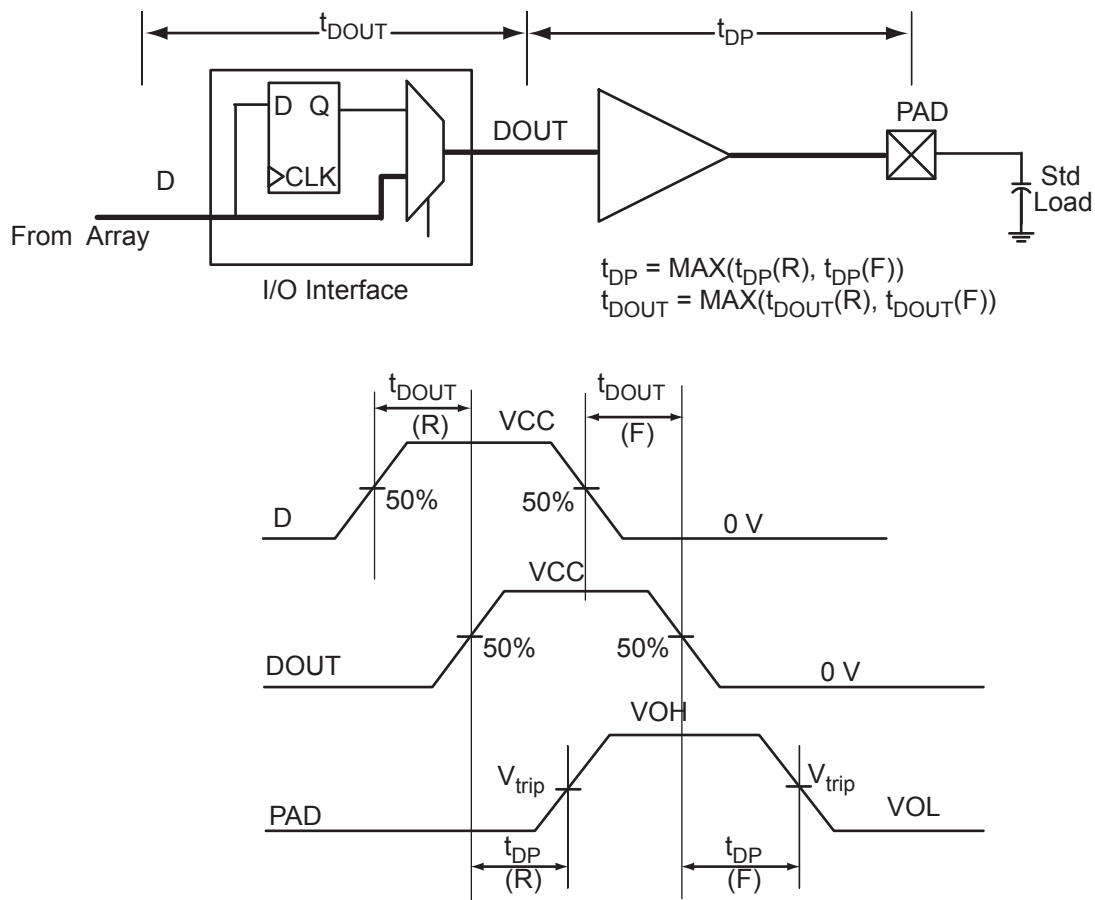


Figure 2-5 • Output Buffer Model and Delays (example)

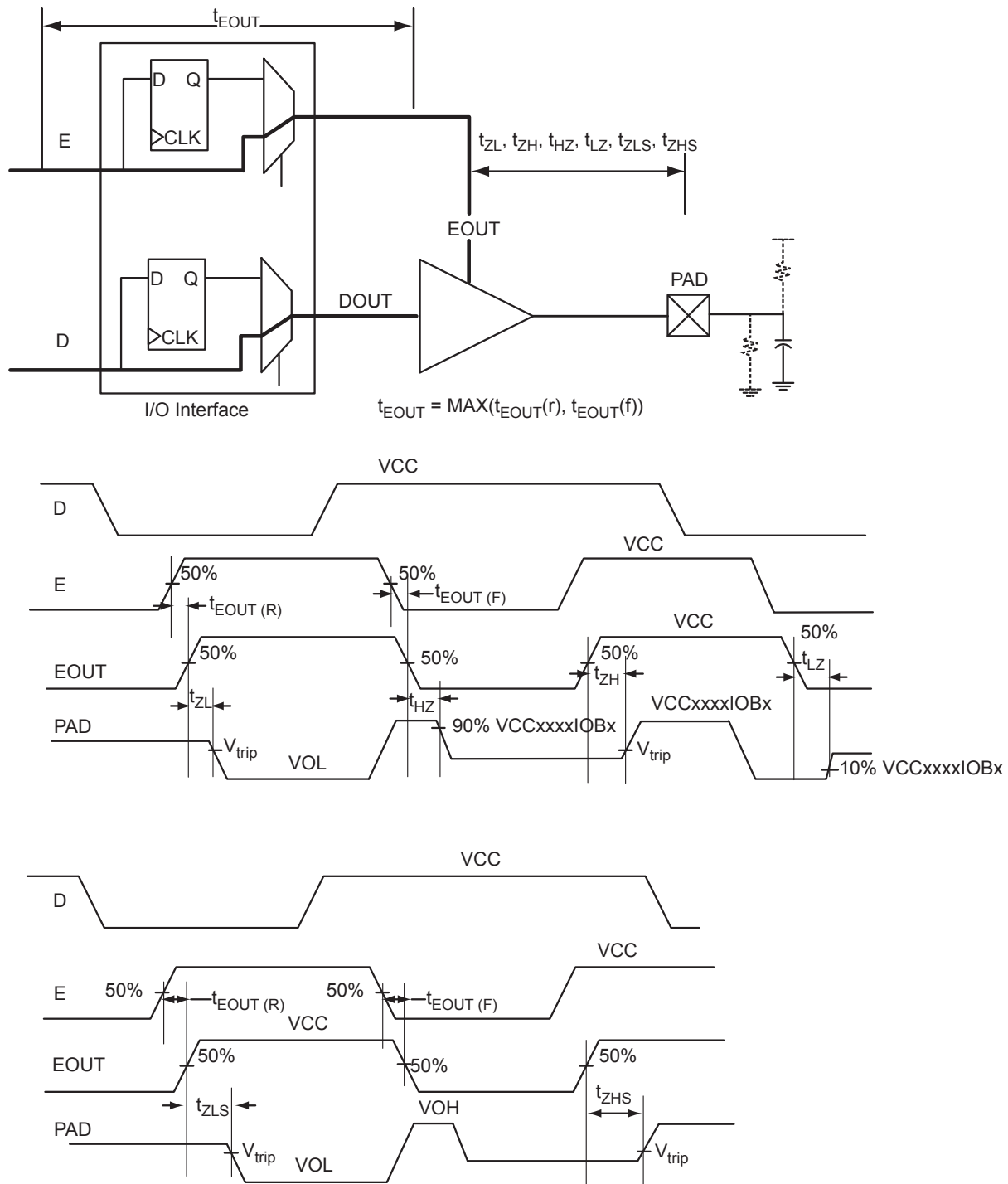


Figure 2-6 • Tristate Output Buffer Timing Model and Delays (example)

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 2-18 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial Conditions—Software Default Settings
Applicable to FPGA I/O Banks

I/O Standard	Drive Strgth.	Slew Rate	VIL		VIH		VOL	VOH	I _{OL} ¹	I _{OH} ¹
			Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
2.5 V LVCMOS	12 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	High	–0.3	0.35 * VCCxxxxIOBx	0.65* VCCxxxxIOBx	3.6	0.45	VCCxxxxIOBx – 0.45	12	12
1.5 V LVCMOS	12 mA	High	–0.3	0.35 * VCCxxxxIOBx	0.65* VCCxxxxIOBx	3.6	0.25 * VCCxxxxIOBx	0.75* VCCxxxxIOBx	12	12
3.3 V PCI	Per PCI specifications									
3.3 V PCI-X	Per PCI-X specifications									

Notes:

1. Currents are measured at 85°C junction temperature.
2. Output slew rate can be extracted by the IBIS Models.

Table 2-19 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial Conditions—Software Default Settings
Applicable to MSS I/O Banks

I/O Standard	Drive Strgth.	Slew Rate	VIL		VIH		VOL	VOH	I _{OL} ¹	I _{OH} ¹
			Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTTL / 3.3 V LVCMOS	8 mA	High	–0.3	0.8	2	3.6	0.4	2.4	8	8
2.5 V LVCMOS	8 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	8	8
1.8 V LVCMOS	4 mA	High	–0.3	0.35* VCCxxxxIOBx	0.65* VCCxxxxIOBx	3.6	0.45	VCCxxxxIOBx – 0.45	4	4
1.5 V LVCMOS	2 mA	High	–0.3	0.35* VCCxxxxIOBx	0.65* VCCxxxxIOBx	3.6	0.25* VCCxxxxIOBx	0.75* VCCxxxxIOBx	2	2

Notes:

1. Currents are measured at 85°C junction temperature.
2. Output slew rate can be extracted by the IBIS Models.

Table 2-20 • Summary of Maximum and Minimum DC Input Levels
Applicable to Commercial Conditions in all I/O Bank Types

DC I/O Standards	Commercial	
	I_{IL}	I_{IH}
	μA	μA
3.3 V LVTTTL / 3.3 V LVCMOS	15	15
2.5 V LVCMOS	15	15
1.8 V LVCMOS	15	15
1.5 V LVCMOS	15	15
3.3 V PCI	15	15
3.3 V PCI-X	15	15

Summary of I/O Timing Characteristics – Default I/O Software Settings

Table 2-21 • Summary of AC Measuring Points Applicable to All I/O Bank Types

Standard	Measuring Trip Point (V_{trip})
3.3 V LVTTTL / 3.3 V LVCMOS	1.4 V
2.5 V LVCMOS	1.2 V
1.8 V LVCMOS	0.90 V
1.5 V LVCMOS	0.75 V
3.3 V PCI	$0.285 * VCC_{xxxIOBx} (RR)$
	$0.615 * VCC_{xxxIOBx} (FF)$
3.3 V PCI-X	$0.285 * VCC_{xxxIOBx} (RR)$
	$0.615 * VCC_{xxxIOBx} (FF)$
LVDS	Cross point
LVPECL	Cross point

Table 2-22 • I/O AC Parameter Definitions

Parameter	Parameter Definition
t_{DP}	Data to pad delay through the output buffer
t_{PY}	Pad to data delay through the input buffer
t_{DOUT}	Data to output buffer delay through the I/O interface
t_{EOUT}	Enable to output buffer tristate control delay through the I/O interface
t_{DIN}	Input buffer to data delay through the I/O interface
t_{HZ}	Enable to pad delay through the output buffer—High to Z
t_{ZH}	Enable to pad delay through the output buffer—Z to High
t_{LZ}	Enable to pad delay through the output buffer—Low to Z
t_{ZL}	Enable to pad delay through the output buffer—Z to Low
t_{ZHS}	Enable to pad delay through the output buffer with delayed enable—Z to High
t_{ZLS}	Enable to pad delay through the output buffer with delayed enable—Z to Low

Table 2-23 • Summary of I/O Timing Characteristics—Software Default Settings

–1 Speed Grade, Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, Worst Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx (per standard)
Applicable to FPGA I/O Banks

I/O Standard	Drive Strength	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	High	35	–	0.50	2.56	0.03	0.90	0.32	2.60	1.97	2.50	2.82	4.32	3.68	ns
2.5 V LVCMOS	12 mA	High	35	–	0.50	2.57	0.03	1.01	0.32	2.62	2.35	2.58	2.72	4.33	4.06	ns
1.8 V LVCMOS	12 mA	High	35	–	0.50	3.01	0.03	0.93	0.32	3.01	3.01	2.76	2.70	4.73	4.73	ns
1.5 V LVCMOS	12 mA	High	35	–	0.50	3.58	0.03	1.10	0.32	3.49	3.58	2.93	2.73	5.20	5.30	ns
3.3 V PCI	Per PCI spec	High	10	25 ¹	0.50	2.06	0.03	0.66	0.32	2.09	1.50	2.46	2.75	3.81	3.21	ns
3.3 V PCI-X	Per PCI-X spec	High	10	25 ¹	0.50	2.06	0.03	0.64	0.32	2.09	1.50	2.46	2.75	3.81	3.21	ns
LVDS	24 mA	High	–	–	0.50	1.44	0.03	1.27	–	–	–	–	–	–	–	ns
LVPECL	24 mA	High	–	–	0.50	1.38	0.03	1.08	–	–	–	–	–	–	–	ns

Notes:

1. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See [Figure 2-11 on page 2-40](#) for connectivity. This resistor is not required during normal operation.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-9](#) for derating values.

Table 2-24 • Summary of I/O Timing Characteristics—Software Default Settings

–1 Speed Grade, Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, Worst Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx (per standard)
Applicable to MSS I/O Banks

I/O Standard	Drive Strength	Slew Rate	Capacitive Load (pF)	External Resistor	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{PVS} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	Units
3.3 V LVTTTL / 3.3 V LVCMOS	8 mA	High	10	–	0.50	1.92	0.03	0.78	1.09	0.37	1.96	1.55	1.83	2.04	ns
2.5 V LVCMOS	8 mA	High	10	–	0.50	1.96	0.03	0.99	1.16	0.37	2.00	1.82	1.82	1.93	ns
1.8 V LVCMOS	4 mA	High	10	–	0.50	2.31	0.03	0.91	1.37	0.37	2.35	2.27	1.84	1.87	ns
1.5 V LVCMOS	2 mA	High	10	–	0.50	2.70	0.03	1.07	1.55	0.37	2.75	2.67	1.87	1.85	ns

Notes:

1. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See [Figure 2-11 on page 2-40](#) for connectivity. This resistor is not required during normal operation.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-9](#) for derating values.

Detailed I/O DC Characteristics

Table 2-25 • Input Capacitance

Symbol	Definition	Conditions	Min.	Max.	Units
C_{IN}	Input capacitance	$V_{IN} = 0, f = 1.0 \text{ MHz}$		8	pF
C_{INCLK}	Input capacitance on the clock pin	$V_{IN} = 0, f = 1.0 \text{ MHz}$		8	pF

Table 2-26 • I/O Output Buffer Maximum Resistances¹
Applicable to FPGA I/O Banks

Standard	Drive Strength	$R_{PULL-DOWN}$ (Ω) ²	$R_{PULL-UP}$ (Ω) ³
3.3 V LVTTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
	24 mA	11	22
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
	12 mA	20	22
	16 mA	20	22
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

Notes:

1. These maximum values are provided for information only. Minimum output buffer resistance values depend on $V_{CCxxxIOBx}$, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website at <http://www.actel.com/download/ibis/default.aspx> (also generated by the Actel Libero IDE toolset).
2. $R_{(PULL-DOWN-MAX)} = (V_{OLspec}) / I_{OLspec}$
3. $R_{(PULL-UP-MAX)} = (V_{CCImax} - V_{OHspec}) / I_{OHspec}$

Table 2-27 • I/O Output Buffer Maximum Resistances¹
Applicable to MSS I/O Banks

Standard	Drive Strength	$R_{PULL-DOWN} (\Omega)^2$	$R_{PULL-UP} (\Omega)^3$
3.3 V LVTTTL / 3.3 V LVCMOS	8mA	50	150
2.5 V LVCMOS	8 mA	50	100
1.8 V LVCMOS	4 mA	100	112
1.5 V LVCMOS	2 mA	200	224

Notes:

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCxxxIOBx, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website at <http://www.actel.com/download/ibis/default.aspx>.
2. $R_{(PULL-DOWN-MAX)} = (V_{OLspec}) / I_{OLspec}$
3. $R_{(PULL-UP-MAX)} = (V_{CCI_{max}} - V_{OHspec}) / I_{OHspec}$

Table 2-28 • I/O Weak Pull-Up/Pull-Down Resistances
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values

VCCxxxIOBx	$R_{(WEAK PULL-UP)}^1 (\Omega)$		$R_{(WEAK PULL-DOWN)}^2 (\Omega)$	
	Min.	Max.	Min.	Max.
3.3 V	10 k	45 k	10 k	45 k
2.5 V	11 k	55 k	12 k	74 k
1.8 V	18 k	70 k	17 k	110 k
1.5 V	19 k	90 k	19 k	140 k

Notes:

1. $R_{(WEAK PULL-DOWN-MAX)} = (V_{OLspec}) / I_{(WEAK PULL-DOWN-MIN)}$
2. $R_{(WEAK PULL-UP-MAX)} = (V_{CCI_{max}} - V_{OHspec}) / I_{(WEAK PULL-UP-MIN)}$

Table 2-29 • I/O Short Currents I_{OSH}/I_{OSL}
Applicable to FPGA I/O Banks

	Drive Strength	I_{OSL} (mA)*	I_{OSH} (mA)*
3.3 V LVTTTL / 3.3 V LVCMOS	2 mA	27	25
	4 mA	27	25
	6 mA	54	51
	8 mA	54	51
	12 mA	109	103
	16 mA	127	132
	24 mA	181	268
2.5 V LVCMOS	2 mA	18	16
	4 mA	18	16
	6 mA	37	32
	8 mA	37	32
	12 mA	74	65
	16 mA	87	83
	24 mA	124	169
1.8 V LVCMOS	2 mA	11	9
	4 mA	22	17
	6 mA	44	35
	8 mA	51	45
	12 mA	74	91
	16 mA	74	91
1.5 V LVCMOS	2 mA	16	13
	4 mA	33	25
	6 mA	39	32
	8 mA	55	66
	12 mA	55	66
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	109	103

Note: * $T_J = 85^\circ\text{C}$.

Table 2-30 • I/O Short Currents I_{OSH}/I_{OSL}
Applicable to MSS I/O Banks

	Drive Strength	I_{OSL} (mA)*	I_{OSH} (mA)*
3.3 V LVTTTL / 3.3 V LVCMOS	8 mA	54	51
2.5 V LVCMOS	8 mA	37	32
1.8 V LVCMOS	4 mA	22	17
1.5 V LVCMOS	2 mA	16	13

Note: * $T_J = 85^\circ\text{C}$

The length of time an I/O can withstand I_{OSH}/I_{OSL} events depends on the junction temperature. The reliability data below is based on a 3.3 V, 12 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100°C, the short current condition would have to be sustained for more than 2200 operation hours to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 2-31 • Duration of Short Circuit Event before Failure

Temperature	Time before Failure
–40°C	> 20 years
0°C	> 20 years
25°C	> 20 years
70°C	5 years
85°C	2 years
100°C	6 months

Table 2-32 • Schmitt Trigger Input Hysteresis
Hysteresis Voltage Value (typical) for Schmitt Mode Input Buffers

Input Buffer Configuration	Hysteresis Value (typical)
3.3 V LVTTTL / LVCMOS / PCI / PCI-X (Schmitt trigger mode)	240 mV
2.5 V LVCMOS (Schmitt trigger mode)	140 mV
1.8 V LVCMOS (Schmitt trigger mode)	80 mV
1.5 V LVCMOS (Schmitt trigger mode)	60 mV

Table 2-33 • I/O Input Rise Time, Fall Time, and Related I/O Reliability

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)	Reliability
LVTTTL/LVCMOS	No requirement	10 ns *	20 years (100°C)
LVDS/B-LVDS/ M-LVDS/LVPEC L	No requirement	10 ns *	10 years (100°C)

* The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Actel recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.

Single-Ended I/O Characteristics

3.3 V LVTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic (LVTTL) is a general-purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTL input buffer and push-pull output buffer.

Table 2-34 • Minimum and Maximum DC Input and Output Levels
Applicable to FPGA I/O Banks

3.3 V LVTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA ²	μA ²
2 mA	−0.3	0.8	2	3.6	0.4	2.4	2	2	27	25	15	15
4 mA	−0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	15	15
6 mA	−0.3	0.8	2	3.6	0.4	2.4	6	6	54	51	15	15
8 mA	−0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	15	15
12 mA	−0.3	0.8	2	3.6	0.4	2.4	12	12	109	103	15	15
16 mA	−0.3	0.8	2	3.6	0.4	2.4	16	16	127	132	15	15
24 mA	−0.3	0.8	2	3.6	0.4	2.4	24	24	181	268	10	10

Notes:

1. Currents are measured at 100°C junction temperature and maximum voltage.
2. Currents are measured at 85°C junction temperature.
3. Software default selection highlighted in gray.

Table 2-35 • Minimum and Maximum DC Input and Output Levels
Applicable to MSS I/O Banks

3.3 V LVTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA ²	μA ²
8 mA	−0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	15	15

Notes:

1. Currents are measured at 100°C junction temperature and maximum voltage.
2. Currents are measured at 85°C junction temperature.
3. Software default selection highlighted in gray.

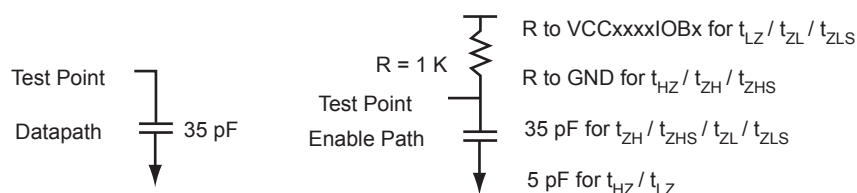


Figure 2-7 • AC Loading

Table 2-36 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	CLOAD (pF)
0	3.3	1.4	—	35

Note: *Measuring point = V_{trip} . See Table 2-21 on page 2-26 for a complete table of trip points.

Timing Characteristics

Table 2-37 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, Worst-Case VCC = 1.425 V,

Worst-Case VCCxxxxIOBx = 3.0 V

Applicable to FPGA I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	–1	0.50	5.87	0.03	0.90	0.32	5.98	5.05	2.03	2.00	7.70	6.77	ns
8 mA	–1	0.50	3.76	0.03	0.90	0.32	3.83	3.12	2.29	2.46	5.55	4.84	ns
12 mA	–1	0.5	2.71	0.03	0.90	0.32	2.76	2.17	2.463	2.75	4.48	3.88	ns
16 mA	–1	0.50	2.56	0.03	0.90	0.32	2.60	1.97	2.50	2.82	4.32	3.68	ns
24 mA	–1	0.50	2.36	0.03	0.90	0.32	2.40	1.63	2.55	3.11	4.12	3.34	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-9](#) for derating values.

Table 2-38 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, Worst-Case VCC = 1.425 V,

Worst-Case VCCxxxxIOBx = 3.0 V

Applicable to FPGA I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	–1	0.50	7.87	0.03	0.90	0.32	8.01	6.83	2.03	1.88	9.73	8.54	ns
8 mA	–1	0.50	5.58	0.03	0.90	0.32	5.68	4.82	2.29	2.33	7.40	6.54	ns
12 mA	–1	0.50	4.28	0.03	0.90	0.32	4.36	3.74	2.46	2.62	6.08	5.45	ns
16 mA	–1	0.50	3.99	0.03	0.90	0.32	4.07	3.50	2.50	2.69	5.78	5.22	ns
24 mA	–1	0.50	3.72	0.03	0.90	0.32	3.79	3.49	2.54	2.98	5.50	5.20	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-9](#) for derating values.

Table 2-39 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, Worst-Case VCC = 1.425 V,

Worst-Case VCCxxxxIOBx = 3.0 V

Applicable to MSS I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
8 mA	–1	0.50	1.924	0.033	0.781	1.09	0.37	1.96	1.55	1.83	2.04	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-9](#) for derating values.

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications. It uses a 5 V-tolerant input buffer and push-pull output buffer.

Table 2-40 • Minimum and Maximum DC Input and Output Levels
Applicable to FPGA I/O Banks

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA ²	μA ²
2 mA	−0.3	0.7	1.7	2.7	0.7	1.7	2	2	18	16	15	15
4 mA	−0.3	0.7	1.7	2.7	0.7	1.7	4	4	18	16	15	15
6 mA	−0.3	0.7	1.7	2.7	0.7	1.7	6	6	37	32	15	15
8 mA	−0.3	0.7	1.7	2.7	0.7	1.7	8	8	37	32	15	15
12 mA	−0.3	0.7	1.7	2.7	0.7	1.7	12	12	74	65	15	15
16 mA	−0.3	0.7	1.7	2.7	0.7	1.7	16	16	87	83	15	15
24 mA	−0.3	0.7	1.7	2.7	0.7	1.7	24	24	124	169	15	15

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.
3. Software default selection highlighted in gray.

Table 2-41 • Minimum and Maximum DC Input and Output Levels
Applicable to MSS I/O Banks

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA ²	μA ²
8 mA	−0.3	0.7	1.7	3.6	0.7	1.7	8	8	37	32	15	15

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.
3. Software default selection highlighted in gray.

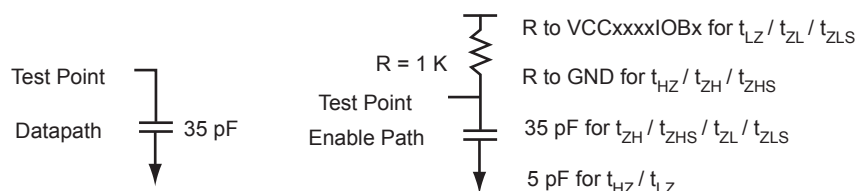


Figure 2-8 • AC Loading

Table 2-42 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	V _{REF} (typ.) (V)	C _{LOAD} (pF)
0	2.5	1.2	—	35

* Measuring point = V_{trip}. See Table 2-21 on page 2-26 for a complete table of trip points.

Timing Characteristics

Table 2-43 • 2.5 V LVCMOS High Slew

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxIOBx = 2.3 V
Applicable to FPGA I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	–1	0.46	6.65	0.03	1.01	0.32	6.01	6.65	2.05	1.77	7.72	8.36	ns
8 mA	–1	0.46	3.96	0.03	1.01	0.32	3.86	3.96	2.34	2.30	5.58	5.68	ns
12 mA	–1	0.50	2.73	0.03	1.01	0.32	2.78	2.63	2.53	2.64	4.50	4.35	ns
16 mA	–1	0.50	2.57	0.03	1.01	0.32	2.62	2.35	2.58	2.72	4.33	4.06	ns
24 mA	–1	0.50	2.37	0.03	1.01	0.32	2.41	1.87	2.64	3.07	4.13	3.59	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-9](#) for derating values.

Table 2-44 • 2.5 V LVCMOS Low Slew

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxIOBx = 2.3 V
Applicable to FPGA I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	–1	0.46	8.74	0.03	1.01	0.32	8.61	8.74	2.05	1.69	10.32	10.46	ns
8 mA	–1	0.46	6.11	0.03	1.01	0.32	6.22	5.99	2.34	2.22	7.93	7.71	ns
12 mA	–1	0.50	4.74	0.03	1.01	0.32	4.83	4.54	2.53	2.55	6.54	6.26	ns
16 mA	–1	0.50	4.42	0.03	1.01	0.32	4.50	4.24	2.58	2.64	6.22	5.95	ns
24 mA	–1	0.50	4.22	0.03	1.01	0.32	4.22	4.22	2.63	2.97	5.94	5.94	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-9](#) for derating values.

Table 2-45 • 2.5 V LVCMOS High Slew

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxIOBx = 3.0 V
Applicable to MSS I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
8 mA	–1	0.50	1.96	0.03	0.99	1.16	0.37	2.00	1.82	1.82	1.93	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-9](#) for derating values.

1.8 V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

Table 2-46 • Minimum and Maximum DC Input and Output Levels
Applicable to FPGA I/O Banks

1.8 V LVCMOS	VIL		VIH		VOL	VOH	I _{OL}	I _{OH}	I _{OSL}	I _{OSH}	I _{IL}	I _{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA ²	μA ²
2 mA	−0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx − 0.45	2	2	11	9	15	15
4 mA	−0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx − 0.45	4	4	22	17	15	15
6 mA	−0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx − 0.45	6	6	44	35	15	15
8 mA	−0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx − 0.45	8	8	51	45	15	15
12 mA	−0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx − 0.45	12	12	74	91	15	15
16 mA	−0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx − 0.45	16	16	74	91	15	15

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.
3. Software default selection highlighted in gray.

Table 2-47 • Minimum and Maximum DC Input and Output Levels
Applicable to MSS I/O Banks

1.8 V LVCMOS	VIL		VIH		VOL	VOH	I _{OL}	I _{OH}	I _{OSL}	I _{OSH}	I _{IL}	I _{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA ²	μA ²
4 mA	−0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	3.6	0.45	VCCxxxxIOBx − 0.45	4	4	22	17	15	15

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.
3. Software default selection highlighted in gray.

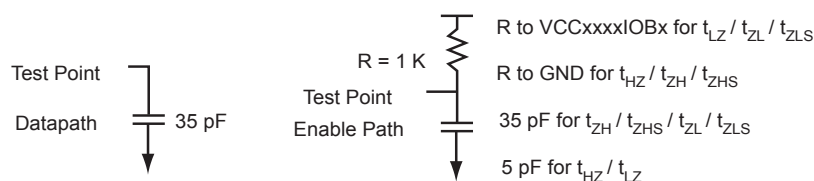


Figure 2-9 • AC Loading

Table 2-48 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	V _{REF} (typ.) (V)	C _{LOAD} (pF)
0	1.8	0.9	—	35

* Measuring point = V_{trip}. See Table 2-21 on page 2-26 for a complete table of trip points.

Timing Characteristics

Table 2-49 • 1.8 V LVCMOS High Slew

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,
Worst-Case $V_{CC} \times \text{I/OBx} = 1.7\text{ V}$
Applicable to FPGA I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	–1	0.50	9.10	0.03	0.93	0.32	7.01	9.10	2.13	1.27	8.72	10.82	ns
4 mA	–1	0.50	5.30	0.03	0.93	0.32	4.50	5.30	2.47	2.18	6.21	7.02	ns
6 mA	–1	0.50	3.41	0.03	0.93	0.32	3.21	3.41	2.71	2.59	4.92	5.13	ns
8 mA	–1	0.50	3.01	0.03	0.93	0.32	3.01	3.01	2.76	2.70	4.73	4.73	ns
12 mA	–1	0.50	2.71	0.03	0.93	0.324	2.76	2.33	2.84	3.13	4.48	4.05	ns
16 mA	–1	0.50	2.71	0.03	0.93	0.32	2.76	2.33	2.84	3.13	4.48	4.05	ns

Notes:

- Software default selection highlighted in gray.
- For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-9](#) for derating values.

Table 2-50 • 1.8 V LVCMOS Low Slew

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,
Worst-Case $V_{CC} \times \text{I/OBx} = 1.7\text{ V}$
Applicable to FPGA I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	–1	0.50	11.91	0.03	1.01	0.32	10.83	11.91	2.13	1.23	12.54	13.63	ns
4 mA	–1	0.50	8.04	0.03	1.01	0.32	7.99	8.04	2.48	2.10	9.70	9.75	ns
6 mA	–1	0.50	6.17	0.03	1.01	0.32	6.29	6.02	2.71	2.51	8.00	7.73	ns
8 mA	–1	0.50	5.76	0.03	1.01	0.32	5.86	5.60	2.77	2.62	7.58	7.31	ns
12 mA	–1	0.50	5.59	0.03	1.01	0.32	5.55	5.59	2.84	3.03	7.27	7.31	ns
16 mA	–1	0.50	5.59	0.03	1.01	0.32	5.55	5.59	2.84	3.03	7.27	7.31	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-9](#) for derating values.

Table 2-51 • 1.8 V LVCMOS High Slew

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,
Worst-Case $V_{CC} \times \text{I/OBx} = 1.7\text{ V}$
Applicable to MSS I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
4 mA	–1	0.50	2.31	0.03	0.91	1.37	0.37	2.35	2.27	1.84	1.87	ns

Notes:

- Software default selection highlighted in gray.
- For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-9](#) for derating values.

1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

Table 2-52 • Minimum and Maximum DC Input and Output Levels
Applicable to FPGA I/O Banks

1.5 V LVCMOS	VIL		VIH		VOL	VOH	I _{OL}	I _{OH}	I _{OSL}	I _{OSH}	I _{IL}	I _{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA ²	μA ²
2 mA	−0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.575	0.25* VCCxxxxIOBx	0.75 * VCCxxxxIOBx	2	2	16	13	15	15
4 mA	−0.3	0.35* VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.575	0.25* VCCxxxxIOBx	0.75 * VCCxxxxIOBx	4	4	33	25	15	15
6 mA	−0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.575	0.25* VCCxxxxIOBx	0.75 * VCCxxxxIOBx	6	6	39	32	15	15
8 mA	−0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.575	0.25* VCC	0.75 * VCCxxxxIOBx	8	8	55	66	15	15
12 mA	−0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.575	0.25 * VCCxxxxIOBx	0.75 * VCCxxxxIOBx	12	12	55	66	15	15

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.
3. Software default selection highlighted in gray.

Table 2-53 • Minimum and Maximum DC Input and Output Levels
Applicable to MSS I/O Banks

1.5 V LVCMOS	VIL		VIH		VOL	VOH	I _{OL}	I _{OH}	I _{OSL}	I _{OSH}	I _{IL}	I _{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA ²	μA ²
2 mA	−0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.575	0.25 * VCCxxxxIOBx	0.75 * VCCxxxxIOBx	2	2	16	13	15	15

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.
3. Software default selection highlighted in gray.

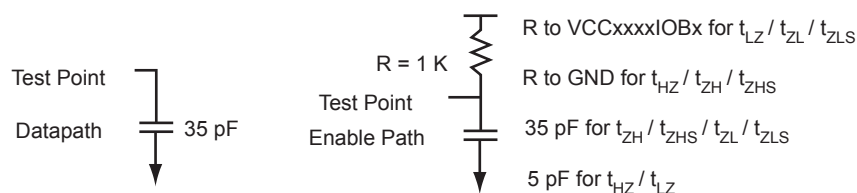


Figure 2-10 • AC Loading

Table 2-54 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	V _{REF} (typ.) (V)	C _{LOAD} (pF)
0	1.5	0.75	–	35

* Measuring point = V_{trip}. See Table 2-21 on page 2-26 for a complete table of trip points.

Timing Characteristics

Table 2-55 • 1.5 V LVCMOS High Slew

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 1.425 V
Applicable to FPGA I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 m	–1	0.50	6.42	0.03	1.10	0.32	5.23	6.42	2.60	2.12	6.95	8.13	ns
4 mA	–1	0.50	4.08	0.03	1.10	0.32	3.72	4.08	2.87	2.61	5.44	5.79	ns
6 mA	–1	0.50	3.58	0.03	1.10	0.32	3.49	3.58	2.93	2.73	5.20	5.30	ns
8 mA	–1	0.50	3.13	0.03	1.10	0.32	3.19	2.74	3.03	3.22	4.90	4.46	ns
12 mA	–1	0.50	3.13	0.03	1.10	0.32	3.19	2.74	3.03	3.22	4.90	4.46	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-9](#) for derating values.

Table 2-56 • 1.5 V LVCMOS Low Slew

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 1.4 V
Applicable to FPGA I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	–1	0.50	9.81	0.03	1.01	0.32	9.83	9.81	2.61	2.03	11.54	11.52	ns
4 mA	–1	0.50	7.68	0.03	1.01	0.32	7.82	7.32	2.88	2.51	9.54	9.04	ns
6 mA	–1	0.50	7.16	0.03	1.01	0.32	7.29	6.82	2.94	2.63	9.01	8.54	ns
8 mA	–1	0.50	6.83	0.03	1.01	0.32	6.96	6.82	3.03	3.11	8.68	8.54	ns
12 mA	–1	0.50	6.83	0.03	1.01	0.32	6.96	6.82	3.03	3.11	8.68	8.54	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-9](#) for derating values.

Table 2-57 • 1.5 V LVCMOS High Slew

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 3.0 V
Applicable to MSS I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	–1	0.50	2.70	0.03	1.07	1.55	0.37	2.75	2.67	1.87	1.85	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-9](#) for derating values.

3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

Table 2-58 • Minimum and Maximum DC Input and Output Levels

3.3 V PCI/PCI-X	VIL		VIH		VOL	VOH	IO _L	IO _H	IOS _L	IOS _H	II _L	II _H
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA ²	μA ²
Per PCI specification	Per PCI curves										15	15

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.

AC loadings are defined per the PCI/PCI-X specifications for the datapath; Actel loadings for enable path characterization are described in [Figure 2-11](#).

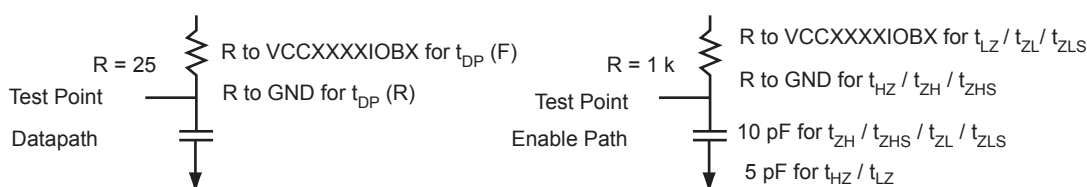


Figure 2-11 • AC Loading

AC loadings are defined per PCI/PCI-X specifications for the datapath; Actel loading for tristate is described in [Table 2-59](#).

Table 2-59 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	V _{REF} (typ.) (V)	C _{LOAD} (pF)
0	3.3	0.285 * VCCxxxIOBx for t _{DP(R)} 0.615 * VCCxxxIOBx for t _{DP(F)}	–	10

* Measuring point = V_{trip}. See [Table 2-21](#) on [page 2-26](#) for a complete table of trip points.

Timing Characteristics

Table 2-60 • 3.3 V PCI

Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxIOBx = 3.0 V
Applicable to FPGA I/O Banks

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
–1	0.50	2.06	0.03	0.66	0.32	2.09	1.50	2.46	2.75	3.81	3.21	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7](#) on [page 2-9](#) for derating values.

Table 2-61 • 3.3 V PCI-X

Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxIOBx = 3.0 V
Applicable to Standard Plus I/O Banks

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
–1	0.50	2.06	0.03	0.64	0.32	2.09	1.50	2.46	2.75	3.81	3.21	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7](#) on [page 2-9](#) for derating values.

Differential I/O Characteristics

Physical Implementation

Configuration of the I/O modules as a differential pair is handled by Actel Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in [Figure 2-12](#). The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

Along with LVDS I/O, SmartFusion also supports Bus LVDS structure and Multipoint LVDS (M-LVDS) configuration (up to 40 nodes).

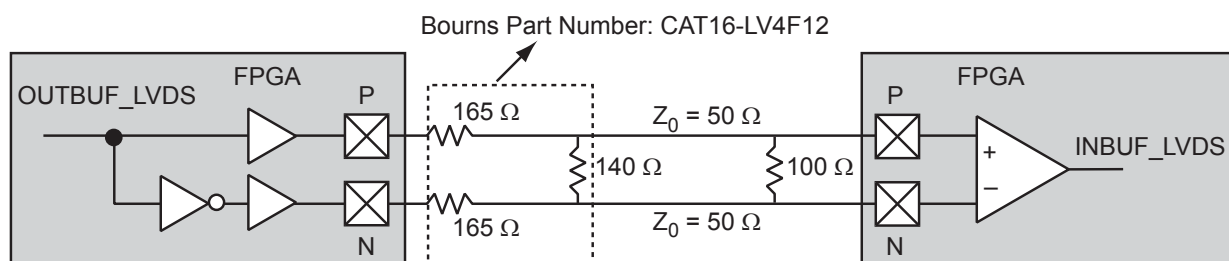


Figure 2-12 • LVDS Circuit Diagram and Board-Level Implementation

Table 2-62 • LVDS Minimum and Maximum DC Input and Output Levels

DC Parameter	Description	Min.	Typ.	Max.	Units
VCCFPGAIOBx	Supply voltage	2.375	2.5	2.625	V
VOL	Output low voltage	0.9	1.075	1.25	V
VOH	Output high voltage	1.25	1.425	1.6	V
I_{OL}^1	Output lower current	0.65	0.91	1.16	mA
I_{OH}^1	Output high current	0.65	0.91	1.16	mA
VI	Input voltage	0		2.925	V
I_{IH}^2	Input high leakage current			15	μ A
I_{IL}^2	Input low leakage current			15	μ A
V _{ODIFF}	Differential output voltage	250	350	450	mV
V _{OCM}	Output common mode voltage	1.125	1.25	1.375	V
V _{ICM}	Input common mode voltage	0.05	1.25	2.35	V
V _{IDIFF}	Input differential voltage	100	350		mV

Notes:

1. I_{OL}/I_{OH} defined by $V_{ODIFF}/(\text{resistor network})$.
2. Currents are measured at 85°C junction temperature.

Table 2-63 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	V _{REF} (typ.) (V)
1.075	1.325	Cross point	–

* Measuring point = V_{trip} . See Table 2-21 on page 2-26 for a complete table of trip points.

Timing Characteristics**Table 2-64 • LVDS**

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, Worst-Case VCC = 1.425 V,
Worst-Case VCCFPGAIOBx = 2.3 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
–1	0.50	1.44	0.03	1.27	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

B-LVDS/M-LVDS

Bus LVDS (B-LVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers. Actel LVDS drivers provide the higher drive current required by B-LVDS and M-LVDS to accommodate the loading. The drivers require series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus since the driver can be located anywhere on the bus. These configurations can be implemented using the TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multipoint designs using Actel LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in Figure 2-13. The input and output buffer delays are available in the LVDS section in Table 2-64.

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst-case commercial operating conditions, at the farthest receiver: $R_S = 60 \Omega$ and $R_T = 70 \Omega$, given $Z_0 = 50 \Omega$ (2") and $Z_{stub} = 50 \Omega$ (~1.5").

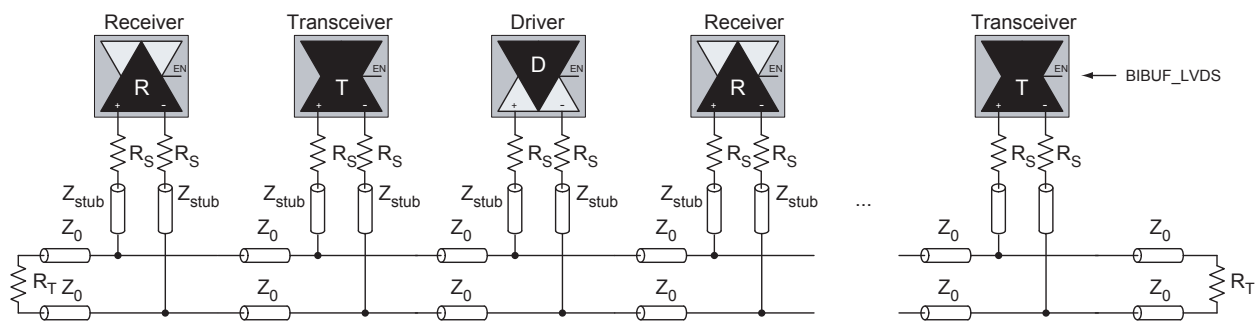


Figure 2-13 • B-LVDS/M-LVDS Multipoint Application Using LVDS I/O Buffers

LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in [Figure 2-14](#). The building blocks of the LVPECL transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation because the output standard specifications are different.

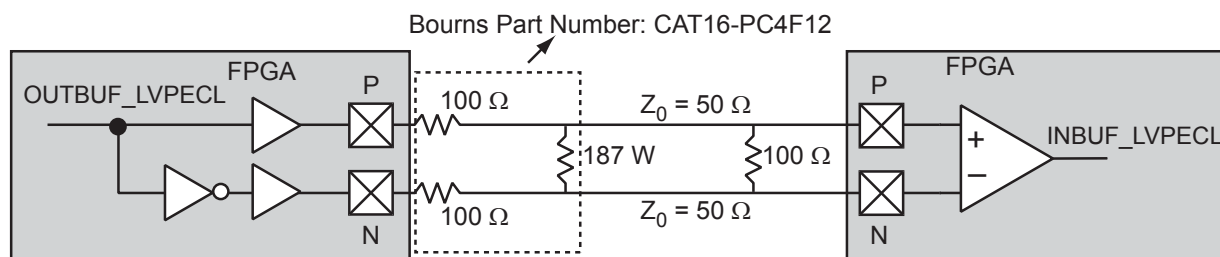


Figure 2-14 • LVPECL Circuit Diagram and Board-Level Implementation

Table 2-65 • Minimum and Maximum DC Input and Output Levels

DC Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
VCCFPGAIOBx	Supply Voltage	3.0	3.3	3.6				V
VOL	Output Low Voltage	0.96	1.27	1.06	1.43	1.30	1.57	V
VOH	Output High Voltage	1.8	2.11	1.92	2.28	2.13	2.41	V
V _{IL} , V _{IH}	Input Low, Input High Voltages	0	3.3	0	3.6	0	3.9	V
V _{ODIFF}	Differential Output Voltage	0.625	0.97	0.625	0.97	0.625	0.97	V
V _{OCM}	Output Common-Mode Voltage	1.762	1.98	1.762	1.98	1.762	1.98	V
V _{ICM}	Input Common-Mode Voltage	1.01	2.57	1.01	2.57	1.01	2.57	V
V _{IDIFF}	Input Differential Voltage	300		300		300		mV

Table 2-66 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	V _{REF} (typ.) (V)
1.64	1.94	Cross point	—

* Measuring point = V_{trip}. See [Table 2-21 on page 2-26](#) for a complete table of trip points.

Timing Characteristics

Table 2-67 • LVPECL

Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCFPGAIOBx = 3.0 V

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{py}	Units
–1	0.50	1.38	0.03	1.08	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-9](#) for derating values.

I/O Register Specifications

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

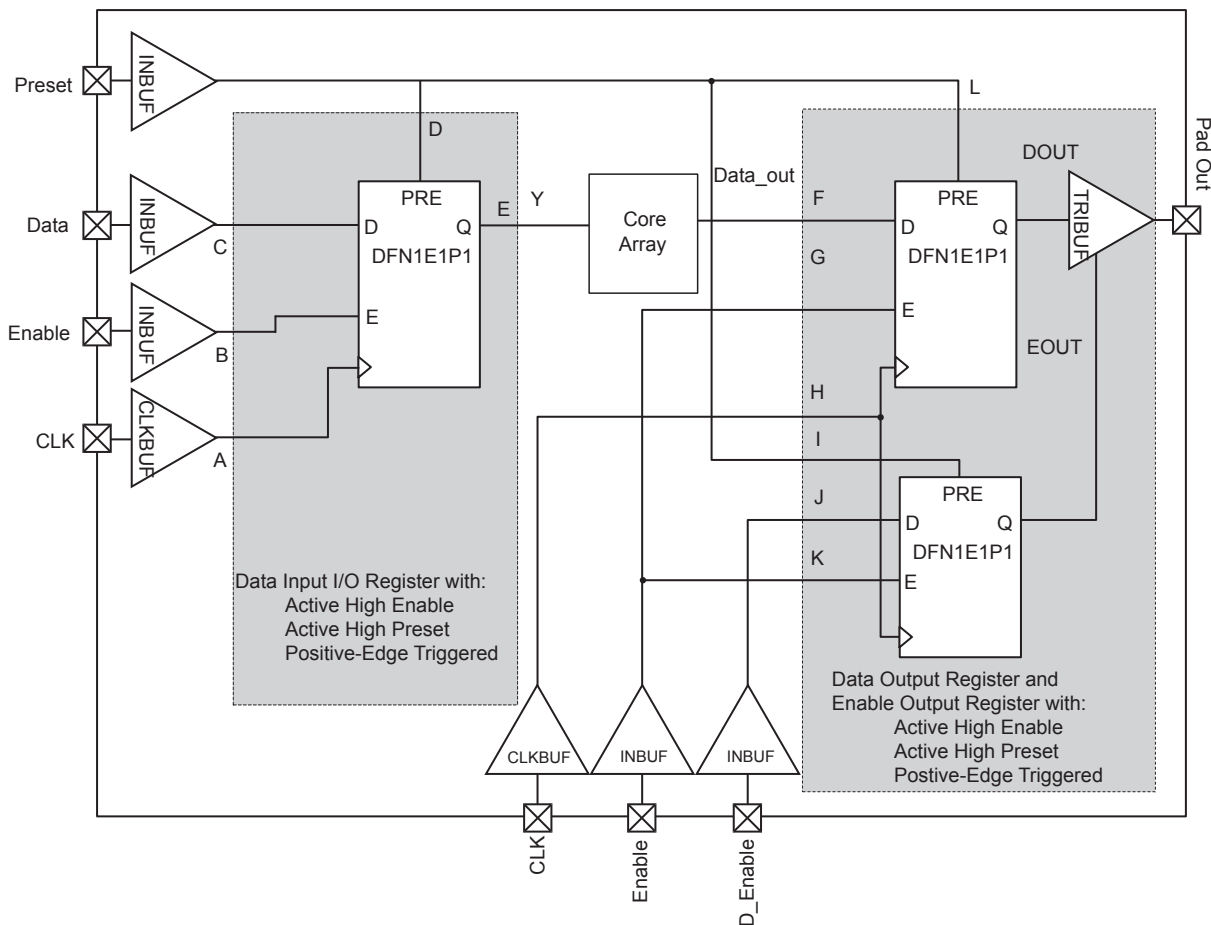


Figure 2-15 • Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

Table 2-68 • Parameter Definition and Measuring Nodes

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OSUE}	Enable Setup Time for the Output Data Register	G, H
t_{OHE}	Enable Hold Time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold Time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{ISUD}	Data Setup Time for the Input Data Register	C, A
t_{IHD}	Data Hold Time for the Input Data Register	C, A
t_{ISUE}	Enable Setup Time for the Input Data Register	B, A
t_{IHE}	Enable Hold Time for the Input Data Register	B, A
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

* See [Figure 2-15 on page 2-45](#) for more information.

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

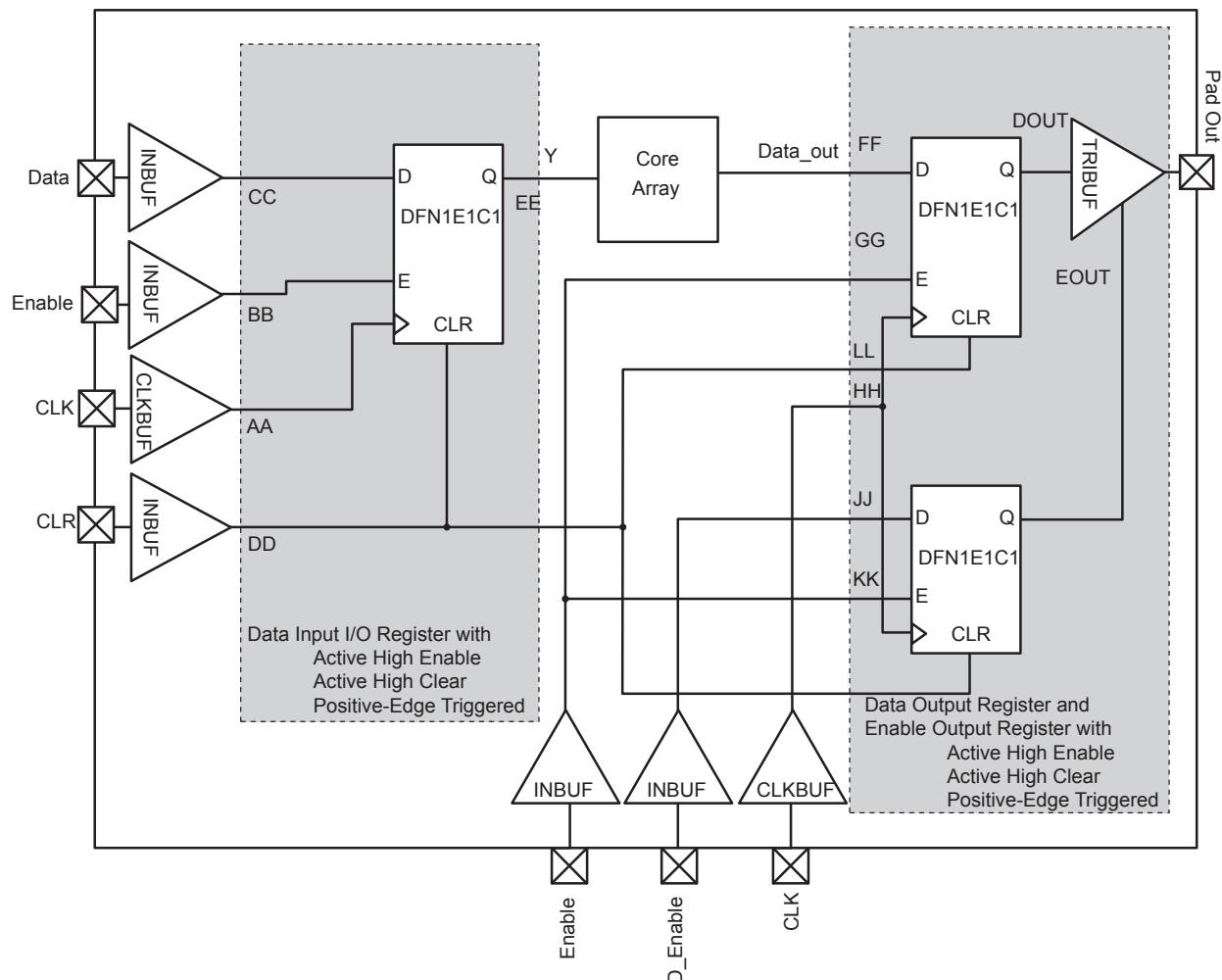


Figure 2-16 • Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

Table 2-69 • Parameter Definition and Measuring Nodes

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	HH, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	FF, HH
t_{OHD}	Data Hold Time for the Output Data Register	FF, HH
t_{OSUE}	Enable Setup Time for the Output Data Register	GG, HH
t_{OHE}	Enable Hold Time for the Output Data Register	GG, HH
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	LL, DOUT
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	LL, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	LL, HH
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	HH, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	JJ, HH
t_{OEHD}	Data Hold Time for the Output Enable Register	JJ, HH
t_{OESUE}	Enable Setup Time for the Output Enable Register	KK, HH
t_{OEHE}	Enable Hold Time for the Output Enable Register	KK, HH
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	II, EOUT
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	II, HH
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	II, HH
t_{ICLKQ}	Clock-to-Q of the Input Data Register	AA, EE
t_{ISUD}	Data Setup Time for the Input Data Register	CC, AA
t_{IHD}	Data Hold Time for the Input Data Register	CC, AA
t_{ISUE}	Enable Setup Time for the Input Data Register	BB, AA
t_{IHE}	Enable Hold Time for the Input Data Register	BB, AA
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	DD, EE
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	DD, AA
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	DD, AA

* See [Figure 2-16 on page 2-47](#) for more information.

[illegible]

Timing Characteristics

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	–1	Units
t _{1CLKQ}	Clock-to-Q of the Input Data Register	0.24	ns
t _{1SUD}	Data Setup Time for the Input Data Register	0.27	ns
t _{1HD}	Data Hold Time for the Input Data Register	0.00	ns
t _{1SUE}	Enable Setup Time for the Input Data Register	0.38	ns
t _{1HE}	Enable Hold Time for the Input Data Register	0.00	ns
t _{1CLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.46	ns
t _{1PRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.46	ns
t _{1REMCLR}	Asynchronous Clear Removal Time for the Input Data Register	0.00	ns
t _{1RECCLR}	Asynchronous Clear Recovery Time for the Input Data Register	0.23	ns
t _{1REMPRE}	Asynchronous Preset Removal Time for the Input Data Register	0.00	ns
t _{1RECPRE}	Asynchronous Preset Recovery Time for the Input Data Register	0.23	ns
t _{1WCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.22	ns
t _{1WPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.22	ns
t _{1CKMPWH}	Clock Minimum Pulse Width High for the Input Data Register	0.36	ns
t _{1CKMPWL}	Clock Minimum Pulse Width Low for the Input Data Register	0.32	ns

2-49

Output Register

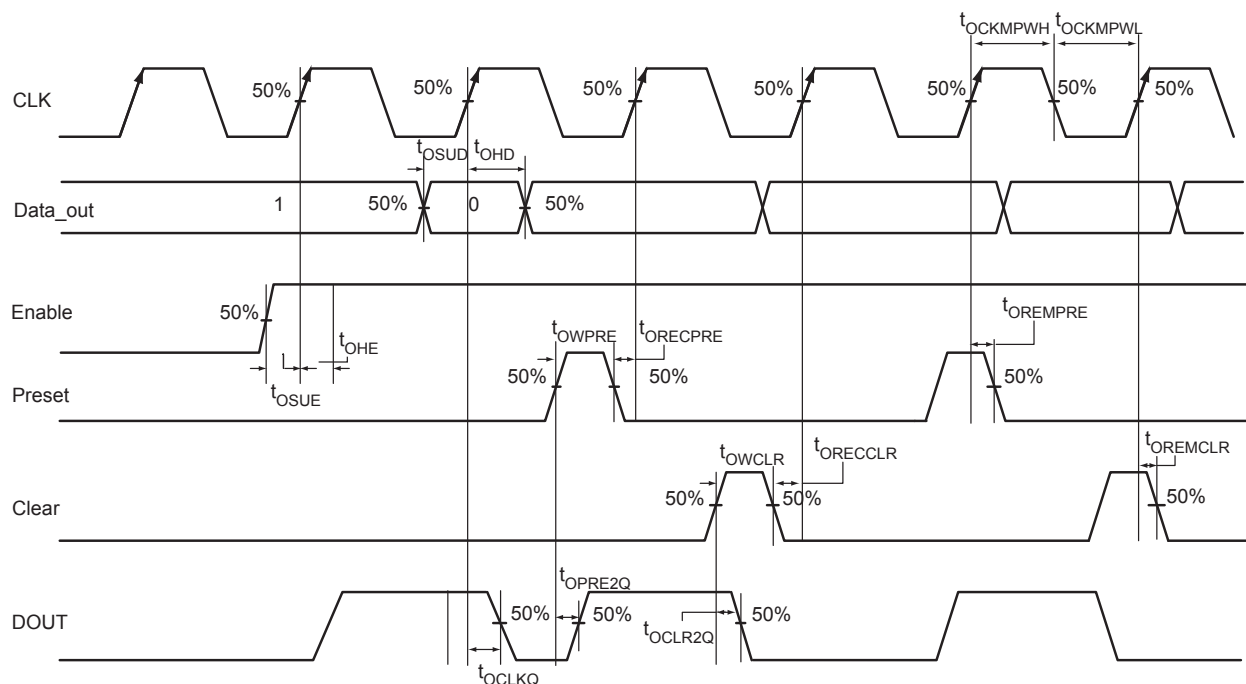


Figure 2-18 • Output Register Timing Diagram

Timing Characteristics

Table 2-71 • Output Data Register Propagation Delays

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	-1	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.60	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.32	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	0.44	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.82	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.82	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.23	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.23	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.22	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.22	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output Data Register	0.36	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output Data Register	0.32	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-9](#) for derating values.

Output Enable Register

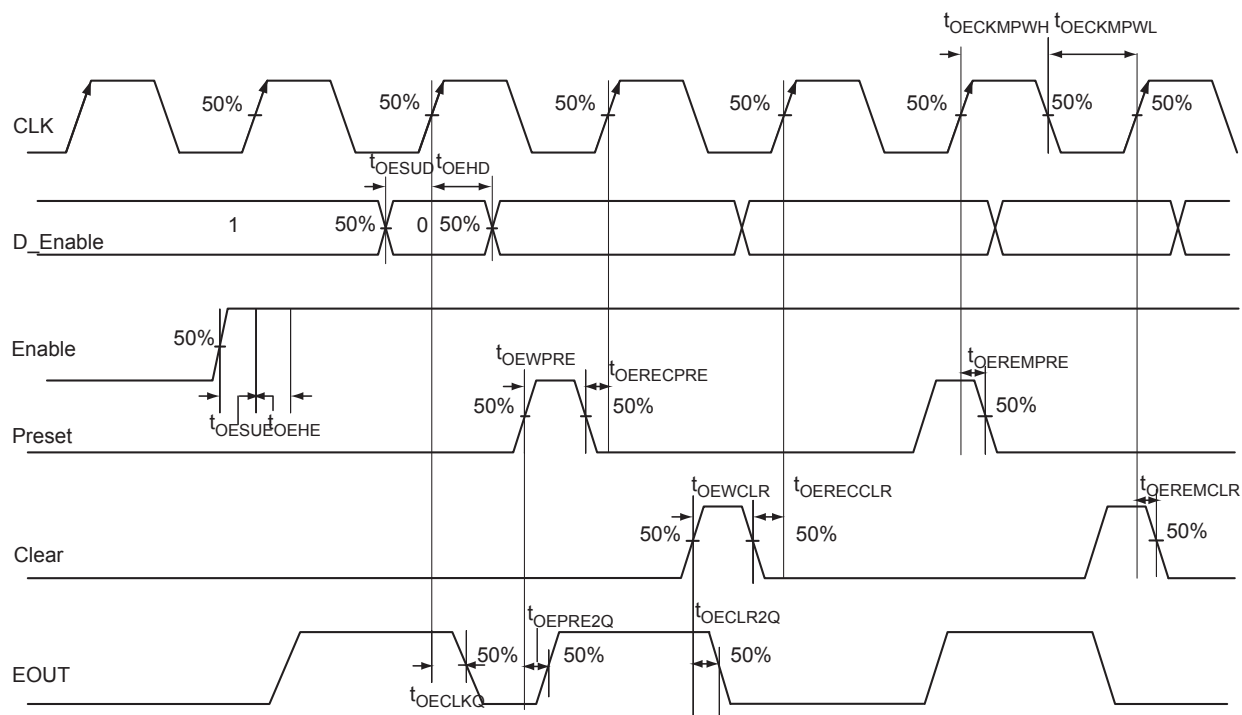


Figure 2-19 • Output Enable Register Timing Diagram

Timing Characteristics

Table 2-72 • Output Enable Register Propagation Delays
Worst Commercial-Case Conditions: $T_J = 85^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	–1	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.45	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.32	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	0.44	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.68	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.68	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	ns
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.23	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	ns
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.23	ns
$t_{OEWCCLR}$	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.22	ns
t_{OEWPPE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.22	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width High for the Output Enable Register	0.36	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width Low for the Output Enable Register	0.32	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-9](#) for derating values.

DDR Module Specifications

Input DDR Module

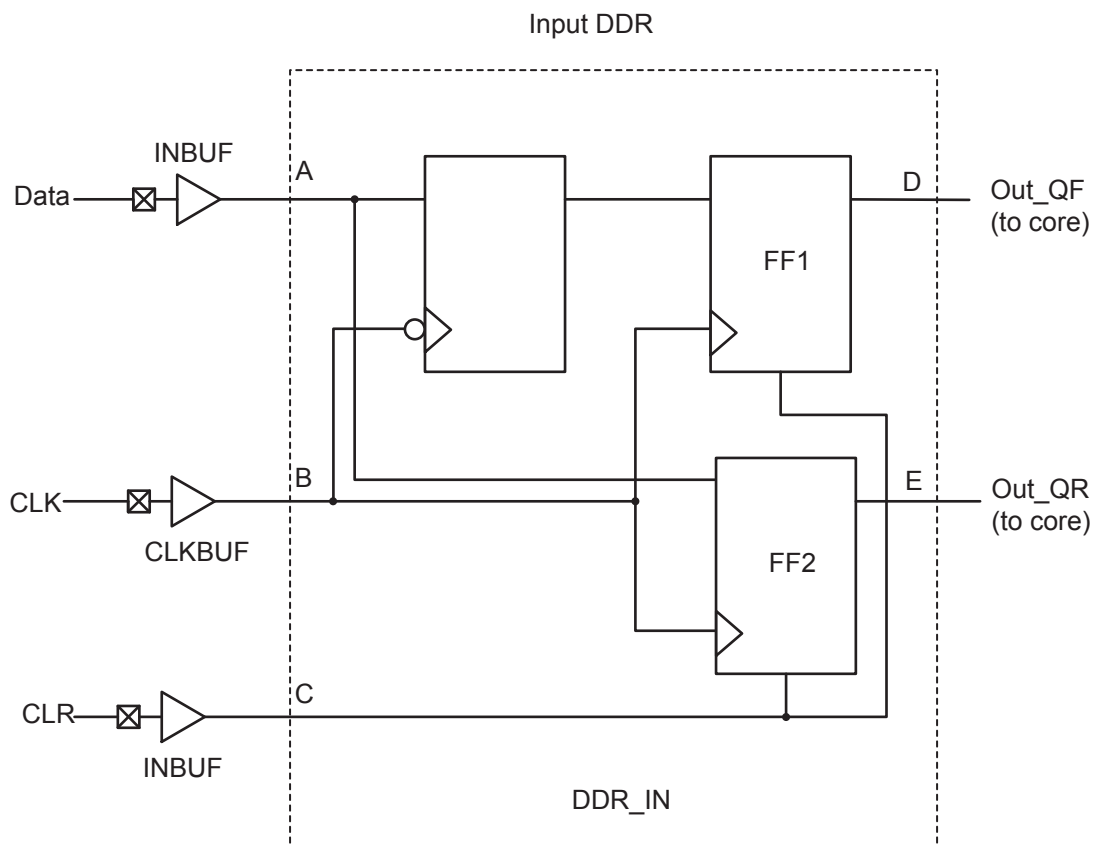
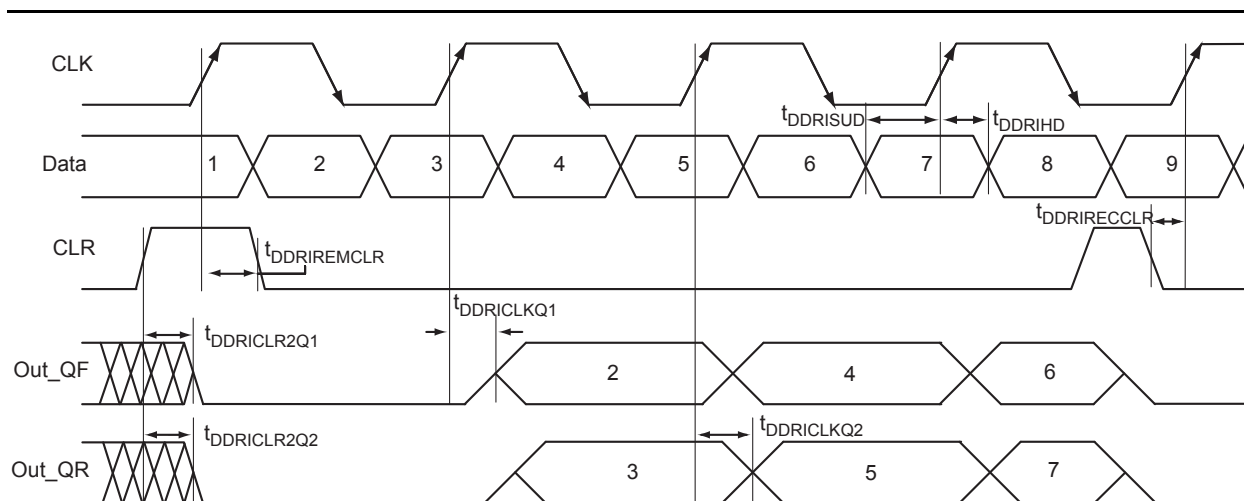


Figure 2-20 • Input DDR Timing Model

Table 2-73 • Parameter Definitions

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDRICKQ1}$	Clock-to-Out Out_QR	B, D
$t_{DDRICKQ2}$	Clock-to-Out Out_QF	B, E
$t_{DDRISUD}$	Data Setup Time of DDR input	A, B
t_{DDRILD}	Data Hold Time of DDR input	A, B
$t_{DDRICLR2Q1}$	Clear-to-Out Out_QR	C, D
$t_{DDRICLR2Q2}$	Clear-to-Out Out_QF	C, E
$t_{DDRIREMCLR}$	Clear Removal	C, B
$t_{DDRIRECCLR}$	Clear Recovery	C, B


Figure 2-21 • Input DDR Timing Diagram

Timing Characteristics

Table 2-74 • Input DDR Propagation Delays

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	-1	Units
t_{DDRCLKQ1}	Clock-to-Out Out_QR for Input DDR	0.39	ns
t_{DDRCLKQ2}	Clock-to-Out Out_QF for Input DDR	0.28	ns
t_{DDRISUD}	Data Setup for Input DDR	0.29	ns
t_{DDRHD}	Data Hold for Input DDR	0.00	ns
$t_{\text{DDRCLR2Q1}}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.58	ns
$t_{\text{DDRCLR2Q2}}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.47	ns
t_{DDRRECLR}	Asynchronous Clear Removal time for Input DDR	0.00	ns
$t_{\text{DDRRECCLR}}$	Asynchronous Clear Recovery time for Input DDR	0.23	ns
t_{DDRWCCLR}	Asynchronous Clear Minimum Pulse Width for Input DDR	0.22	ns
$t_{\text{DDRICKMPWH}}$	Clock Minimum Pulse Width High for Input DDR	0.36	ns
$t_{\text{DDRICKMPWL}}$	Clock Minimum Pulse Width Low for Input DDR	0.32	ns
F_{DDRIMAX}	Maximum Frequency for Input DDR	350	MHz

Note: For derating values at specific junction temperature and voltage-supply levels, refer to [Table 2-7 on page 2-9](#) for derating values.

Output DDR Module

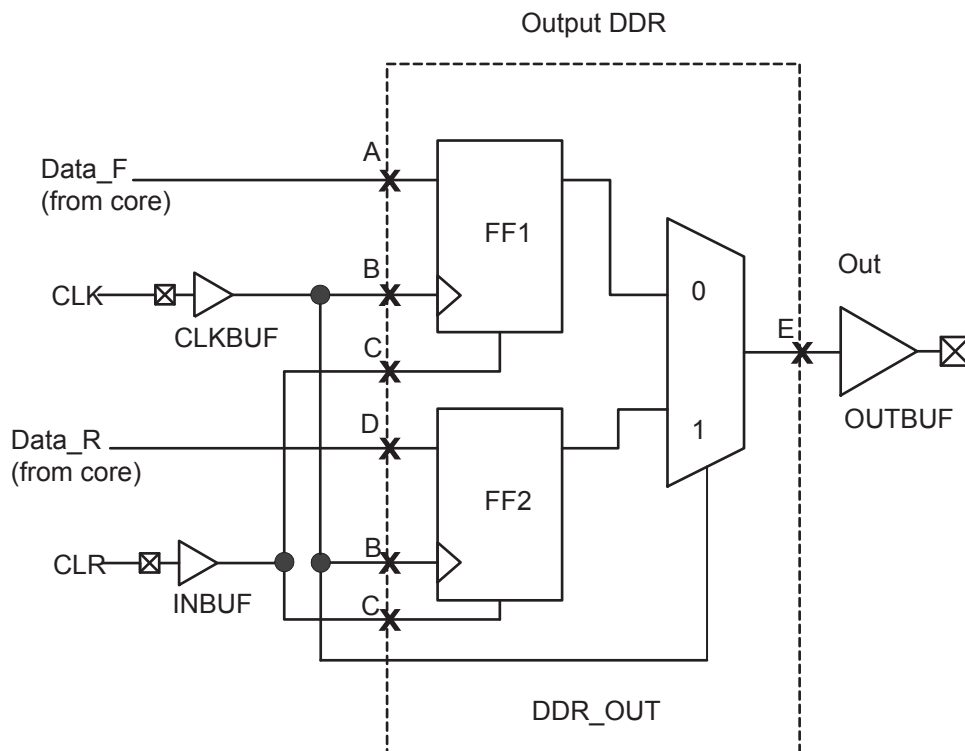
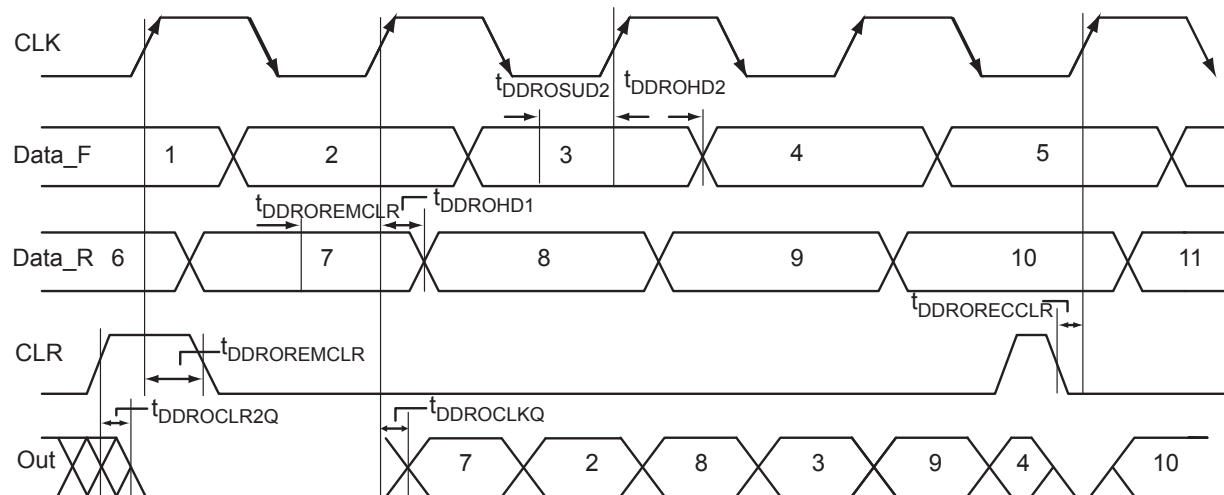


Figure 2-22 • Output DDR Timing Model

Table 2-75 • Parameter Definitions

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B


Figure 2-23 • Output DDR Timing Diagram

Timing Characteristics

Table 2-76 • Output DDR Propagation Delays

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	-1	Units
t_{DDROCLKQ}	Clock-to-Out of DDR for Output DDR	0.71	ns
t_{DDROSUD1}	Data_F Data Setup for Output DDR	0.38	ns
t_{DDROSUD2}	Data_R Data Setup for Output DDR	0.38	ns
t_{DDROHD1}	Data_F Data Hold for Output DDR	0.00	ns
t_{DDROHD2}	Data_R Data Hold for Output DDR	0.00	ns
$t_{\text{DDROCLR2Q}}$	Asynchronous Clear-to-Out for Output DDR	0.81	ns
$t_{\text{DDROEMCLR}}$	Asynchronous Clear Removal Time for Output DDR	0.00	ns
$t_{\text{DDROECCLR}}$	Asynchronous Clear Recovery Time for Output DDR	0.23	ns
$t_{\text{DDROWCLR1}}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.22	ns
$t_{\text{DDROCKMPWH}}$	Clock Minimum Pulse Width High for the Output DDR	0.36	ns
$t_{\text{DDROCKMPWL}}$	Clock Minimum Pulse Width Low for the Output DDR	0.32	ns
F_{DDOMAX}	Maximum Frequency for the Output DDR	350	MHz

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-9](#) for derating values.

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The SmartFusion library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *IGLOO/e*, *Fusion*, *ProASIC3/E*, and *SmartFusion Macro Library Guide*.

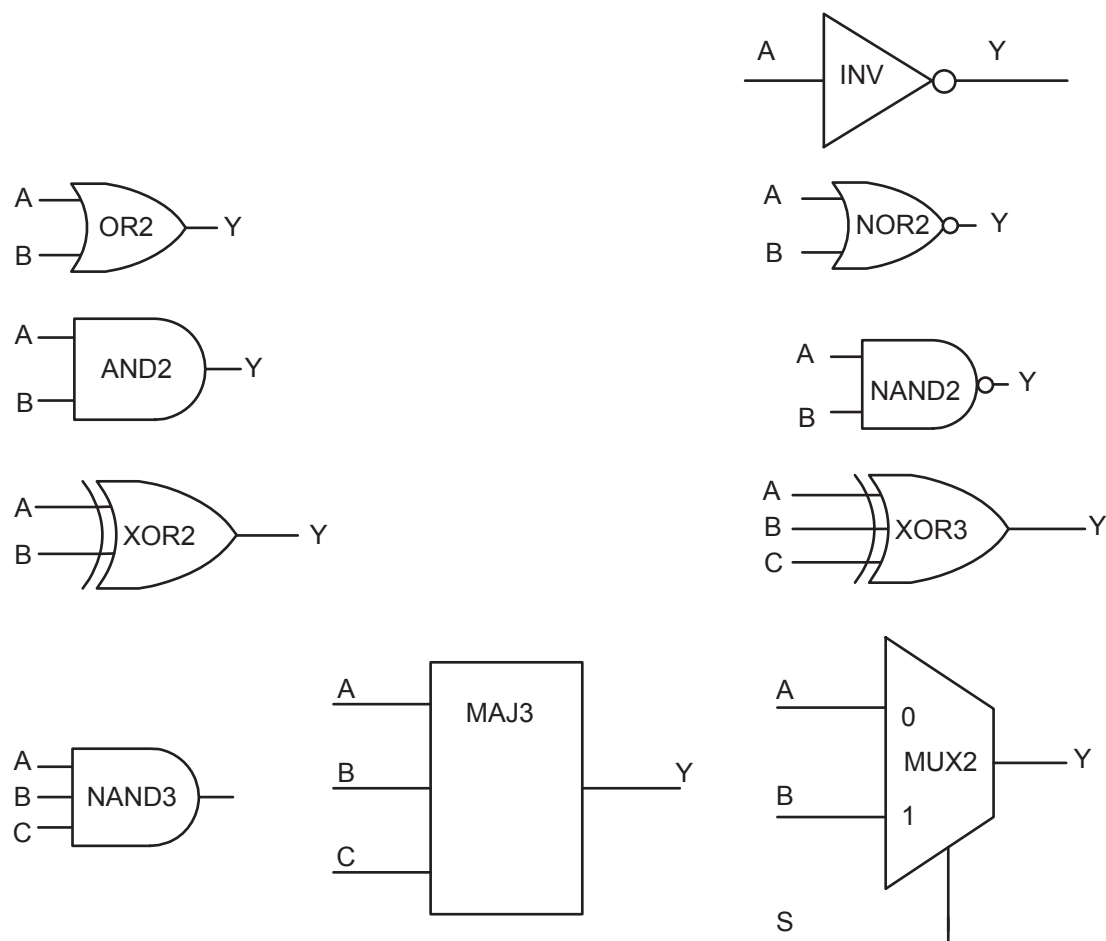


Figure 2-24 • Sample of Combinatorial Cells

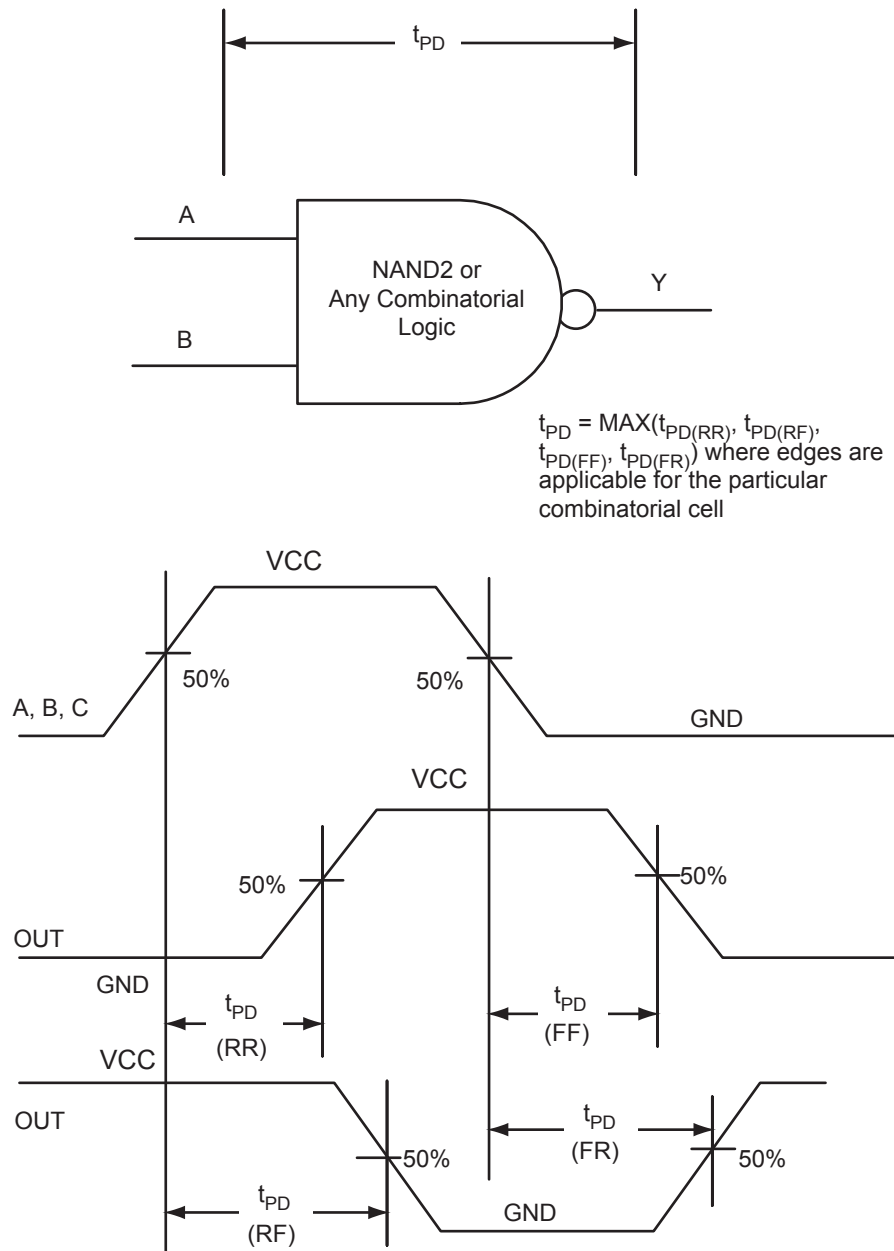


Figure 2-25 • Timing Model and Waveforms

Timing Characteristics

Table 2-77 • Combinatorial Cell Propagation Delays

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Combinatorial Cell	Equation	Parameter	-1	Units
INV	$Y = !A$	t_{PD}	0.39	ns
AND2	$Y = A \cdot B$	t_{PD}	0.48	ns
NAND2	$Y = !(A \cdot B)$	t_{PD}	0.48	ns
OR2	$Y = A + B$	t_{PD}	0.49	ns
NOR2	$Y = !(A + B)$	t_{PD}	0.49	ns
XOR2	$Y = A \oplus B$	t_{PD}	0.75	ns
MAJ3	$Y = \text{MAJ}(A, B, C)$	t_{PD}	0.71	ns
XOR3	$Y = A \oplus B \oplus C$	t_{PD}	0.89	ns
MUX2	$Y = A !S + B S$	t_{PD}	0.51	ns
AND3	$Y = A \cdot B \cdot C$	t_{PD}	0.57	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-9](#) for derating values.

VersaTile Specifications as a Sequential Module

The SmartFusion library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the [IGLOO/e](#), [Fusion](#), [ProASIC3/E](#), and [SmartFusion Macro Library Guide](#).

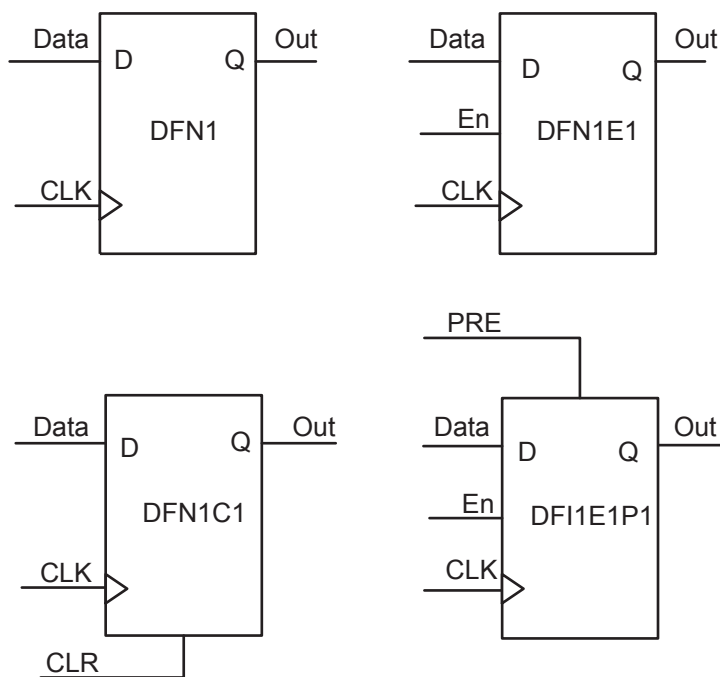
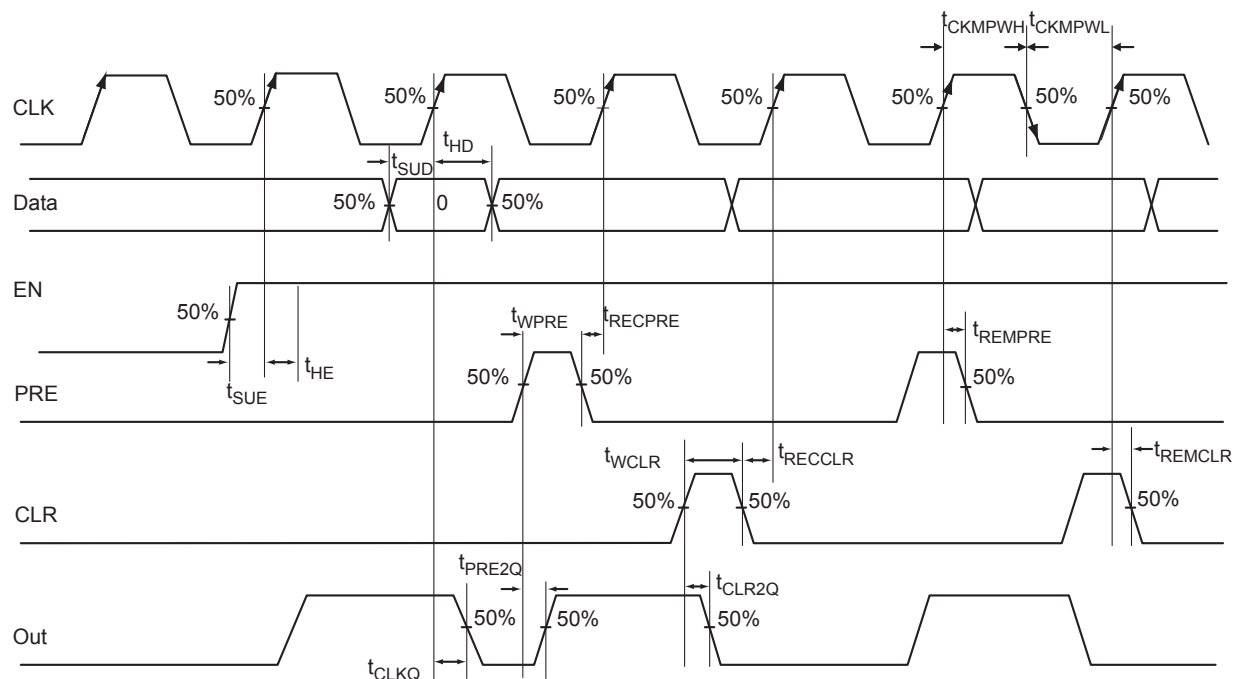


Figure 2-26 • Sample of Sequential Cells


Figure 2-27 • Timing Model and Waveforms

Timing Characteristics

Table 2-78 • Register Delays

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	-1	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.56	ns
t_{SUD}	Data Setup Time for the Core Register	0.44	ns
t_{HD}	Data Hold Time for the Core Register	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	0.46	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.41	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.41	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.23	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.23	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.22	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.22	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core Register	0.32	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core Register	0.36	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-9](#) for derating values.

Global Resource Characteristics

A2F200 Clock Tree Topology

Clock delays are device-specific. Figure 2-28 is an example of a global tree used for clock routing. The global tree presented in Figure 2-28 is driven by a CCC located on the west side of the A2F200 device. It is used to drive all D-flip-flops in the device.

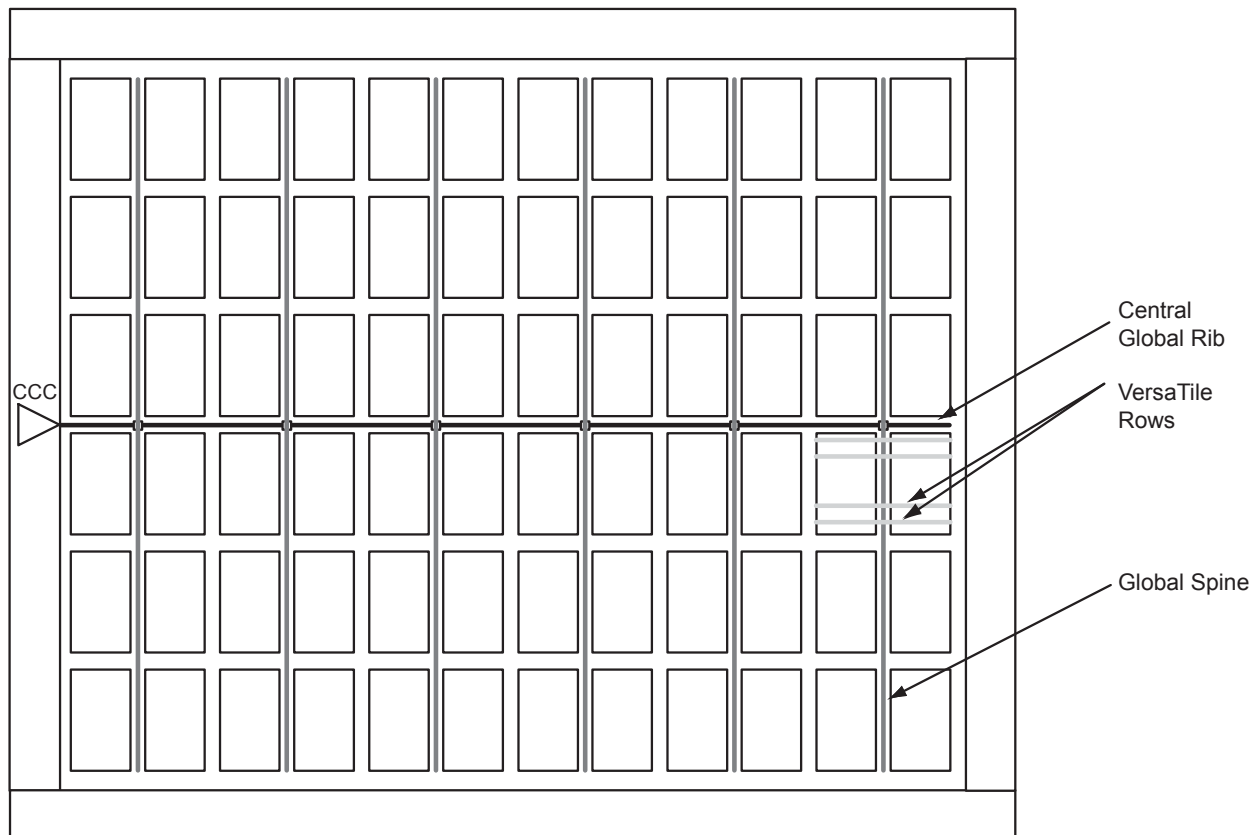


Figure 2-28 • Example of Global Tree Use in an A2F200 Device for Clock Routing

Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard-dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the ["Clock Conditioning Circuits" section on page 2-65](#). [Table 2-79](#) presents minimum and maximum global clock delays for the A2F200 device. Minimum and maximum delays are measured with minimum and maximum loading.

Timing Characteristics

Table 2-79 • A2F200 Global Resource

Worst Commercial-Case Conditions: $T_J = 85^{\circ}\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	–1		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	0.51	0.76	ns
t_{RCKH}	Input High Delay for Global Clock	0.51	0.80	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock			ns
t_{RCKSW}	Maximum Skew for Global Clock		0.29	ns
F_{RMAX}	Maximum Frequency for Global Clock			MHz

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage-supply levels, refer to [Table 2-7 on page 2-9](#) for derating values.

RC Oscillator

The table below describes the electrical characteristics of the RC oscillator.

RC Oscillator Characteristics

Table 2-80 • Electrical Characteristics of the RC Oscillator

Parameter	Description	Condition	Min.	Typ.	Max.	Units
FRC	Operating frequency			100		MHz
	Accuracy	Temperature: 0°C to 85°C Voltage: 3.3 V \pm 5%		1		%
	Output jitter	Period jitter (at 5 K cycles)		100		ps
		Cycle-to-cycle jitter (at 5 K cycles)		100		ps
		Period jitter (at 5 K cycles) with 1 KHz / 300 mV peak-to-peak noise on power supply		150		ps
		Cycle-to-cycle jitter (at 5 K cycles) with 1 KHz / 300 mV peak-to-peak noise on power supply		150		ps
	Output duty cycle	3.3 V domain		1		%
IDYNRC	Operating current	1.5 V domain		2		mA

Main and Lower Power Crystal Oscillator

The tables below describes the electrical characteristics of the main and low power crystal oscillator.

Table 2-81 • Electrical Characteristics of the Main Crystal Oscillator

Parameter	Description	Condition	Min.	Typ.	Max.	Units
	Operating frequency	Using external crystal	0.032		20	MHz
		Using ceramic resonator	0.5		8	MHz
		Using RC Network	0.032		4	MHz
	Output duty cycle			50		%
	Output jitter	With 10 MHz crystal		50		ps RMS
IDYNXTAL	Operating current	RC		0.6		mA
		0.032–0.2		0.6		mA
		0.2–2.0		0.6		mA
		2.0–20.0		0.6		mA
ISTBXTAL	Standby current of crystal oscillator			10		μA
PSRRXTAL	Power supply noise tolerance			0.5		Vp-p
VIHXTAL	Input logic level High		90% of VCC			V
VILXTAL	Input logic level Low				10% of VCC	V
	Startup time	RC				μs
		0.032–0.2				μs
		0.2–2.0				μs
		2.0–20.0				μs

Table 2-82 • Electrical Characteristics of the Low Power Oscillator

Parameter	Description	Condition	Min.	Typ.	Max.	Units
	Operating frequency			32		KHz
	Output duty cycle			50		%
	Output jitter			50		ps RMS
IDYNXTAL	Operating current	32 KHz		10		μA
ISTBXTAL	Standby current of crystal oscillator					μA
PSRRXTAL	Power supply noise tolerance			0.5		Vp-p
VIHXTAL	Input logic level High		90% of VCC			V
VILXTAL	Input logic level Low				10% of VCC	V
	Startup time	Test load used: 20 pF		2.5		s

Clock Conditioning Circuits

CCC Electrical Specifications

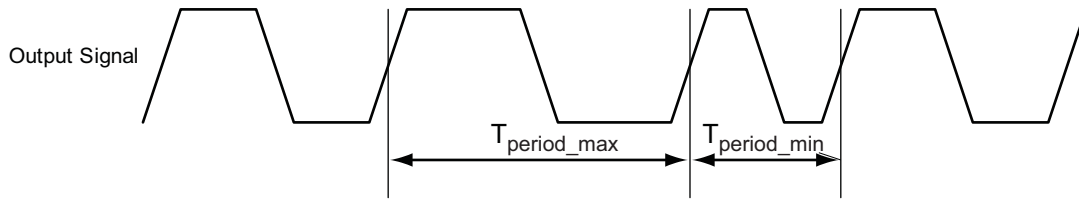
Timing Characteristics

Table 2-83 • SmartFusion CCC/PLL Specification

Parameter	Minimum	Typical	Maximum	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		350	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		350 ¹	MHz
Delay Increments in Programmable Delay Blocks ^{2, 3}		160		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Input Period Jitter			1.5	ns
CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT}	Max Peak-to-Peak Period Jitter			
	1 Global Network Used		3 Global Networks Used	
0.75 MHz to 24 MHz	0.50%		0.70%	
24 MHz to 100 MHz	1.00%		1.20%	
100 MHz to 250 MHz	1.75%		2.00%	
250 MHz to 350 MHz	2.50%		5.60%	
Acquisition Time				
LockControl = 0			300	μs
LockControl = 1			6.0	ms
Tracking Jitter ⁴				
LockControl = 0			1.6	ns
LockControl = 1			0.8	ns
Output Duty Cycle	48.5		5.15	%
Delay Range in Block: Programmable Delay ^{12,3}	0.6		5.56	ns
Delay Range in Block: Programmable Delay ^{22,3}	0.025		5.56	ns
Delay Range in Block: Fixed Delay ^{2,3}		2.2		ns

Notes:

1. One of the CCC outputs (GLA0) is used as an MSS clock and is limited to 100 MHz (maximum) by software. Details regarding CCC/PLL are in the "PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators" chapter of the SmartFusion Microcontroller Subsystem User's Guide.
2. This delay is a function of voltage and temperature. See Table 2-7 on page 2-9 for deratings.
3. $T_J = 25^\circ\text{C}$, $V_{CC} = 1.5\text{ V}$
4. Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.



Note: Peak-to-peak jitter measurements are defined by $T_{\text{peak-to-peak}} = T_{\text{period_max}} - T_{\text{period_min}}$.

Figure 2-29 • Peak-to-Peak Jitter Definition

FPGA Fabric SRAM and FIFO Characteristics

FPGA Fabric SRAM

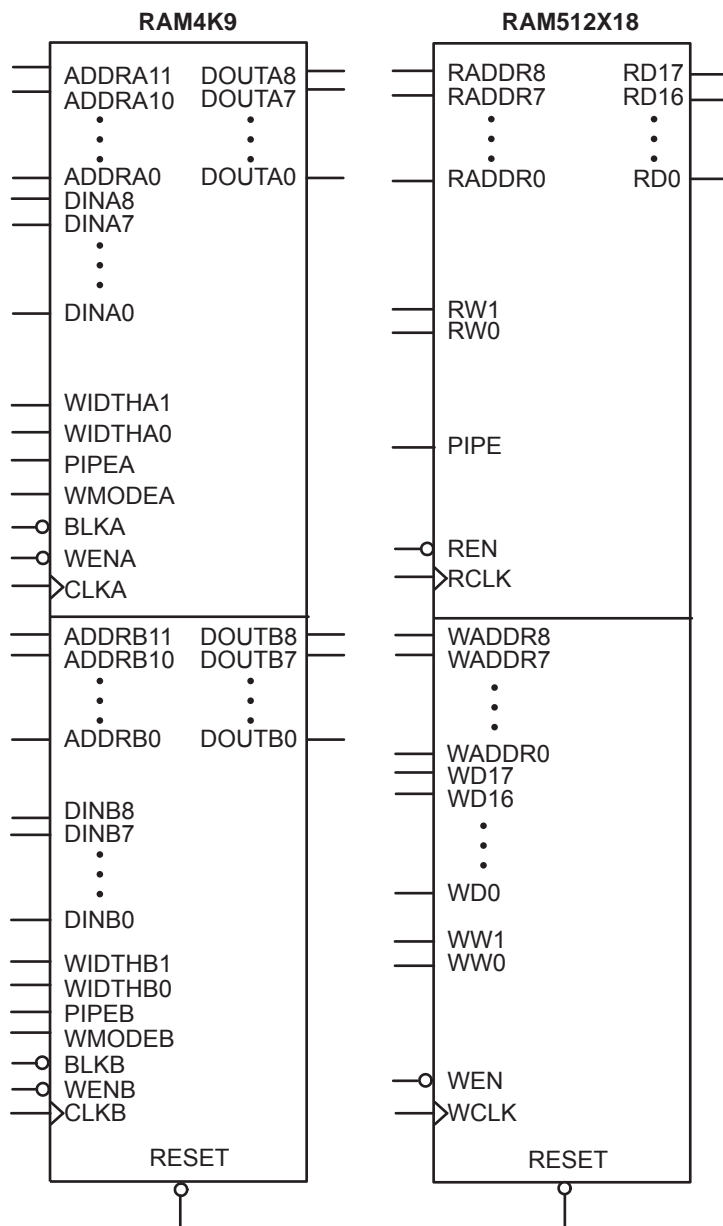


Figure 2-30 • RAM Models

Timing Waveforms

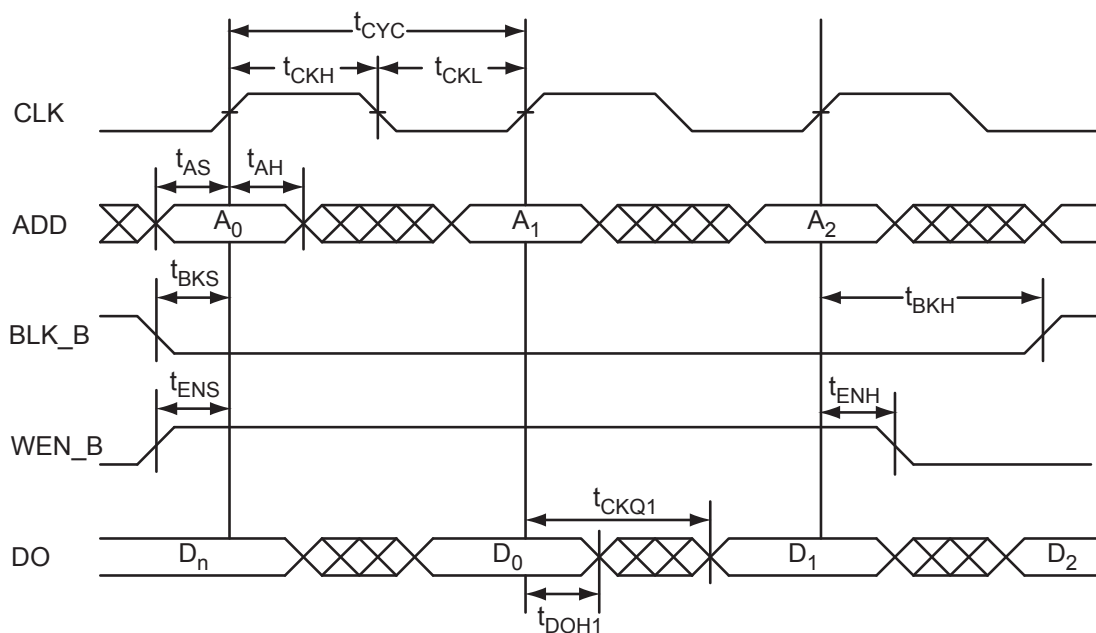


Figure 2-31 • RAM Read for Pass-Through Output

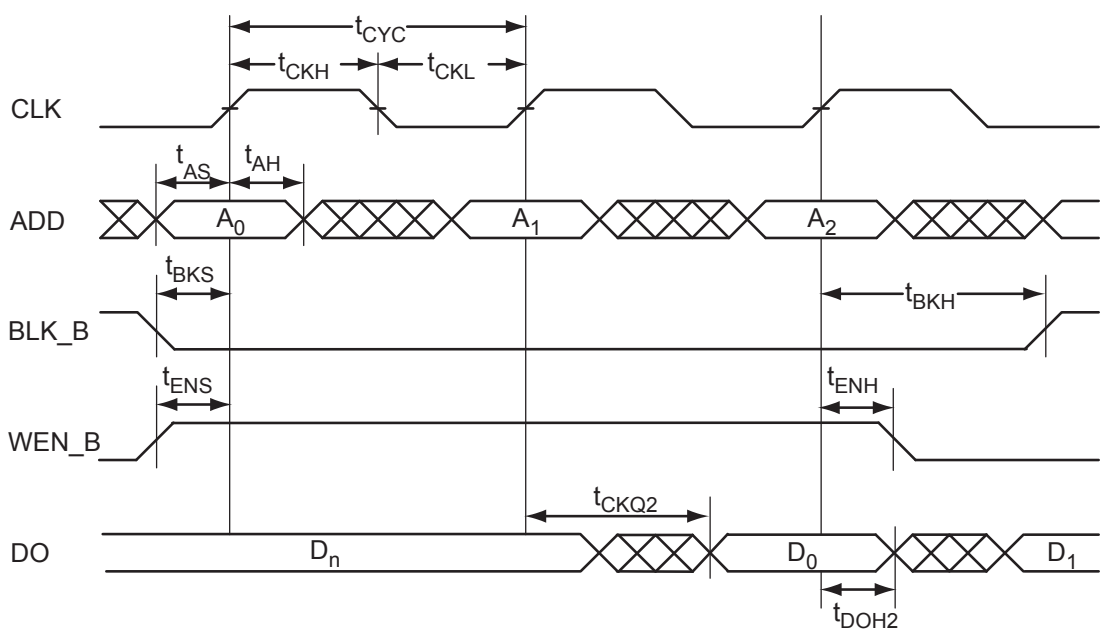


Figure 2-32 • RAM Read for Pipelined Output

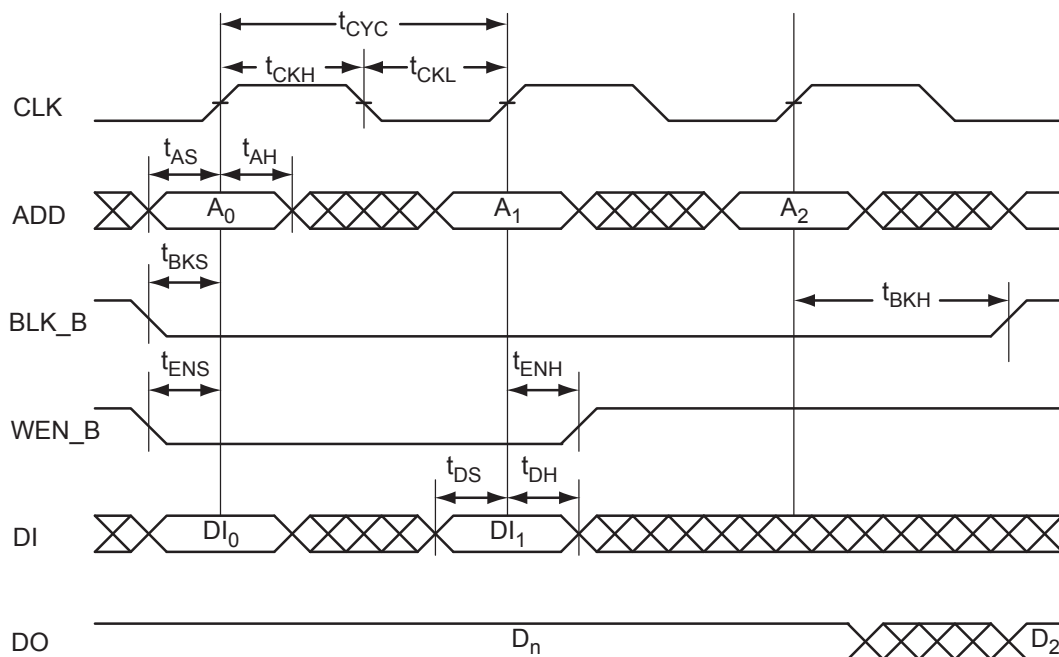


Figure 2-33 • RAM Write, Output Retained (WMODE = 0)

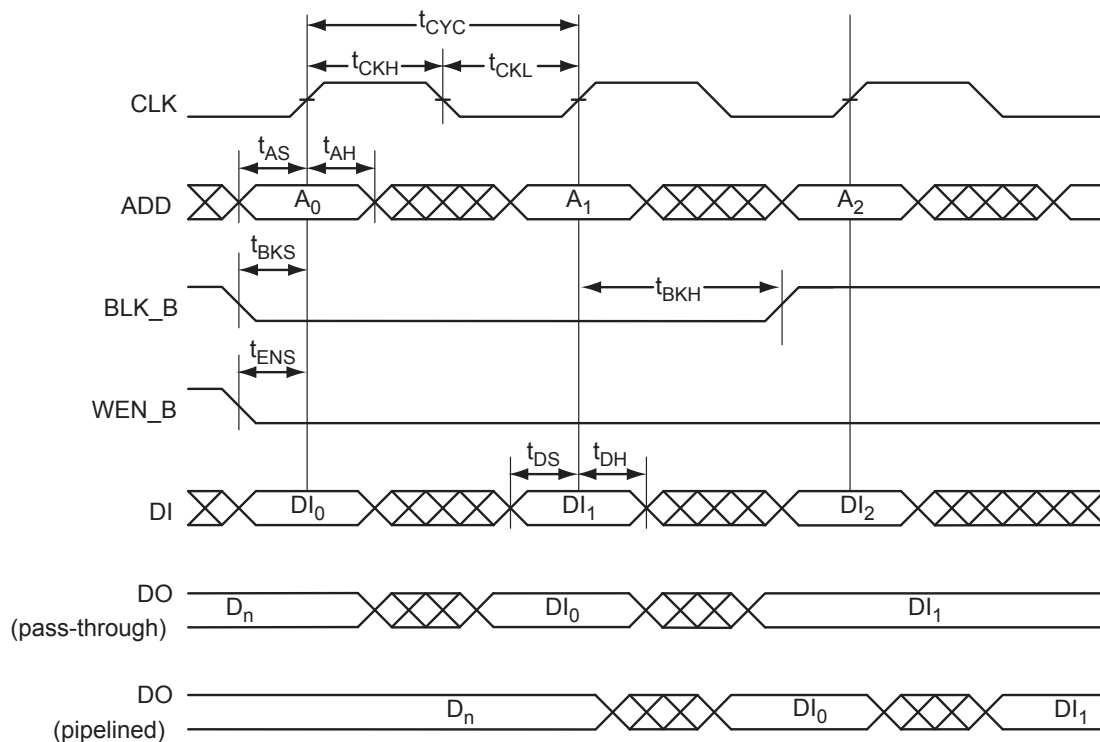


Figure 2-34 • RAM Write, Output as Write Data (WMODE = 1)

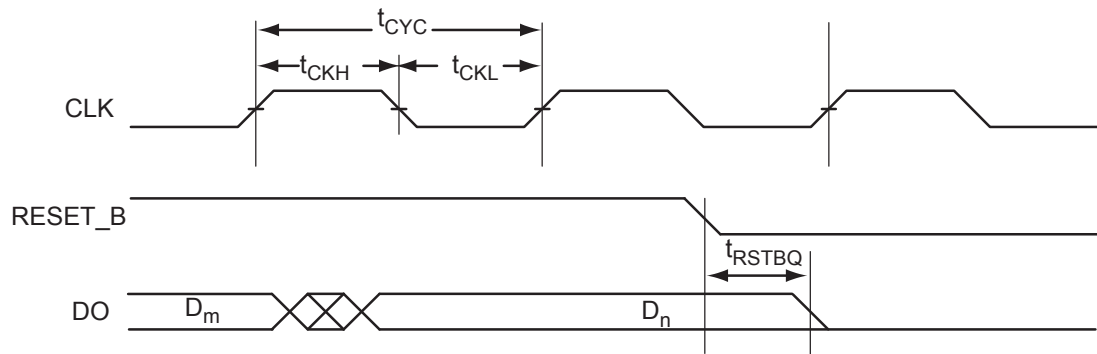


Figure 2-35 • RAM Reset

Timing Characteristics

Table 2-84 • RAM4K9
Worst Commercial-Case Conditions: $T_J = 85^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	–1	Units
t_{AS}	Address setup time	0.25	ns
t_{AH}	Address hold time	0.00	ns
t_{ENS}	REN_B, WEN_B setup time	0.15	ns
t_{ENH}	REN_B, WEN_B hold time	0.10	ns
t_{BKS}	BLK_B setup time	0.24	ns
t_{BKH}	BLK_B hold time	0.02	ns
t_{DS}	Input data (DI) setup time	0.19	ns
t_{DH}	Input data (DI) hold time	0.00	ns
t_{CKQ1}	Clock High to new data valid on DO (output retained, WMODE = 0)	1.81	ns
	Clock High to new data valid on DO (flow-through, WMODE = 1)	2.39	ns
t_{CKQ2}	Clock High to new data valid on DO (pipelined)	0.91	ns
t_{C2CWWH}	Address collision clk-to-clk delay for reliable write after write on same address—applicable to rising edge	0.30	ns
t_{C2CRWH}	Address collision clk-to-clk delay for reliable read access after write on same address—applicable to opening edge	0.45	ns
t_{C2CWRH}	Address collision clk-to-clk delay for reliable write access after read on same address—applicable to opening edge	0.49	ns
t_{RSTBQ}	RESET_B Low to data out Low on DO (flow-through)	0.94	ns
	RESET_B Low to Data Out Low on DO (pipelined)	0.94	ns
$t_{REMRSTB}$	RESET_B removal	0.29	ns
$t_{RECRSTB}$	RESET_B recovery	1.52	ns
$t_{MPWRSTB}$	RESET_B minimum pulse width	0.22	ns
t_{CYC}	Clock cycle time	3.28	ns
F_{MAX}	Maximum clock frequency	305	MHz

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 2-7](#) on [page 2-9](#) for derating values.

Table 2-85 • RAM512X18
Worst Commercial-Case Conditions: $T_J = 85^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	–1	Units
t_{AS}	Address setup time	0.25	ns
t_{AH}	Address hold time	0.00	ns
t_{ENS}	REN_B, WEN_B setup time	0.09	ns
t_{ENH}	REN_B, WEN_B hold time	0.06	ns
t_{DS}	Input data (DI) setup time	0.19	ns
t_{DH}	Input data (DI) hold time	0.00	ns
t_{CKQ1}	Clock High to new data valid on DO (output retained, WMODE = 0)	2.19	ns
t_{CKQ2}	Clock High to new data valid on DO (pipelined)	0.91	ns
t_{C2CRWH}	Address collision clk-to-clk delay for reliable read access after write on same address—applicable to opening edge	0.50	ns
t_{C2CWRH}	Address collision clk-to-clk delay for reliable write access after read on same address—applicable to opening edge	0.59	ns
t_{RSTBQ}	RESET_B Low to data out Low on DO (flow-through)	0.94	ns
	RESET_B Low to data out Low on DO (pipelined)	0.94	ns
$t_{REMRSTB}$	RESET_B removal	0.29	ns
$t_{RECRSTB}$	RESET_B recovery	1.52	ns
$t_{MPWRSTB}$	RESET_B minimum pulse width	0.22	ns
t_{CYC}	Clock cycle time	3.28	ns
F_{MAX}	Maximum clock frequency	305	MHz

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 2-7](#) on [page 2-9](#) for derating values.

Timing Waveforms

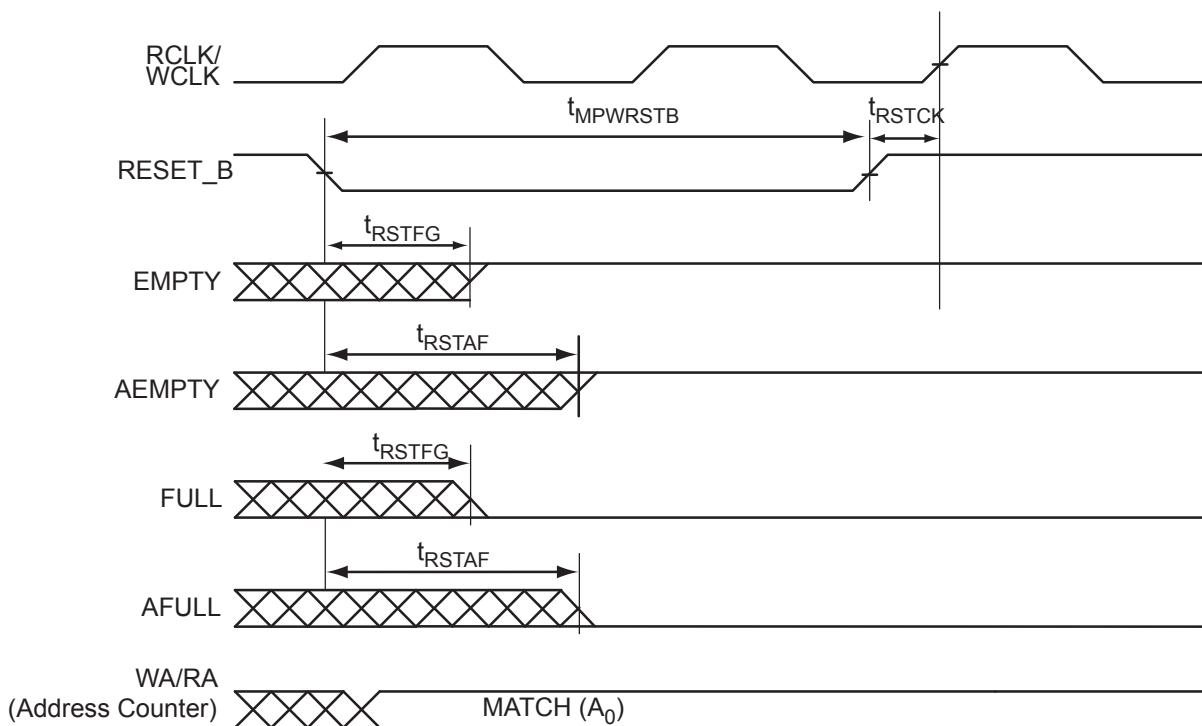


Figure 2-37 • FIFO Reset

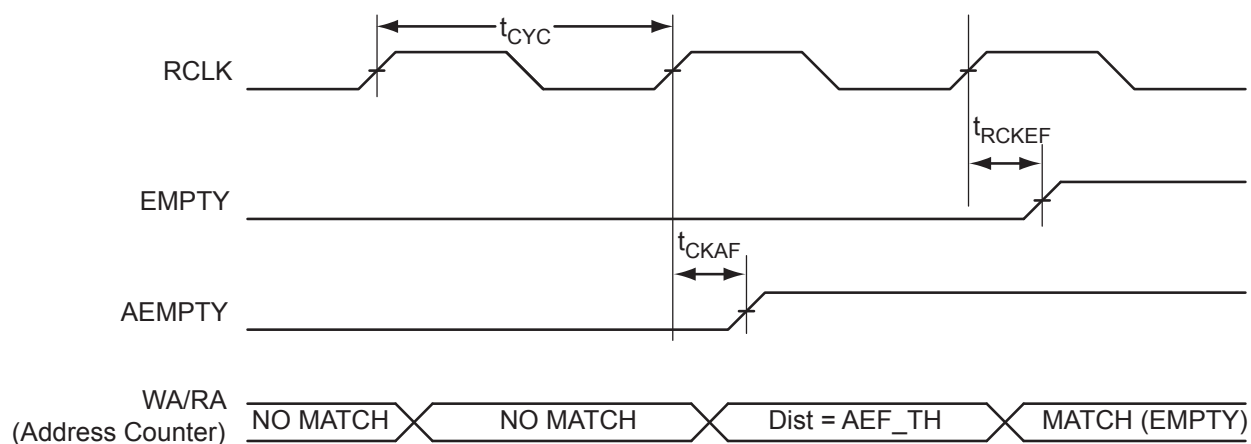
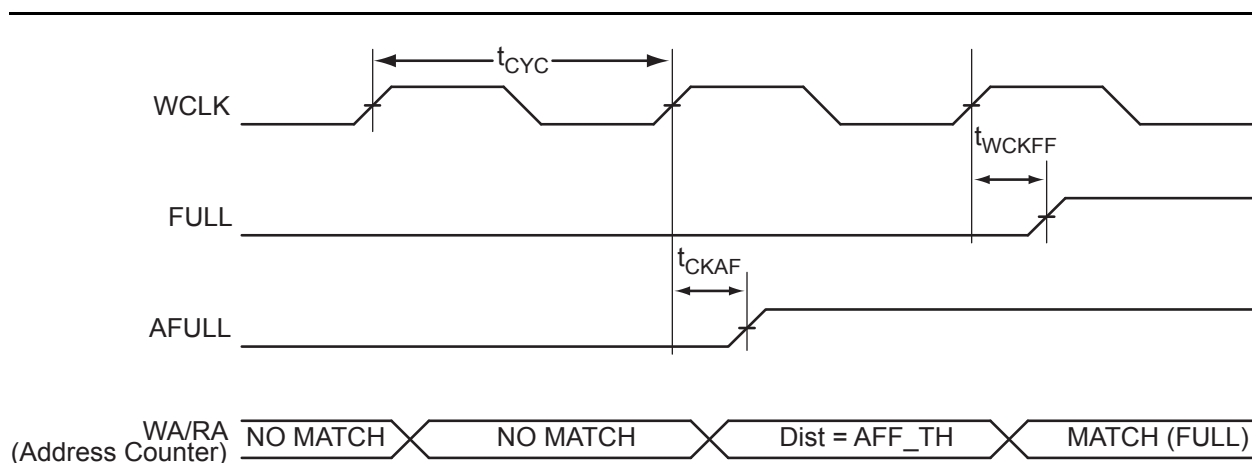
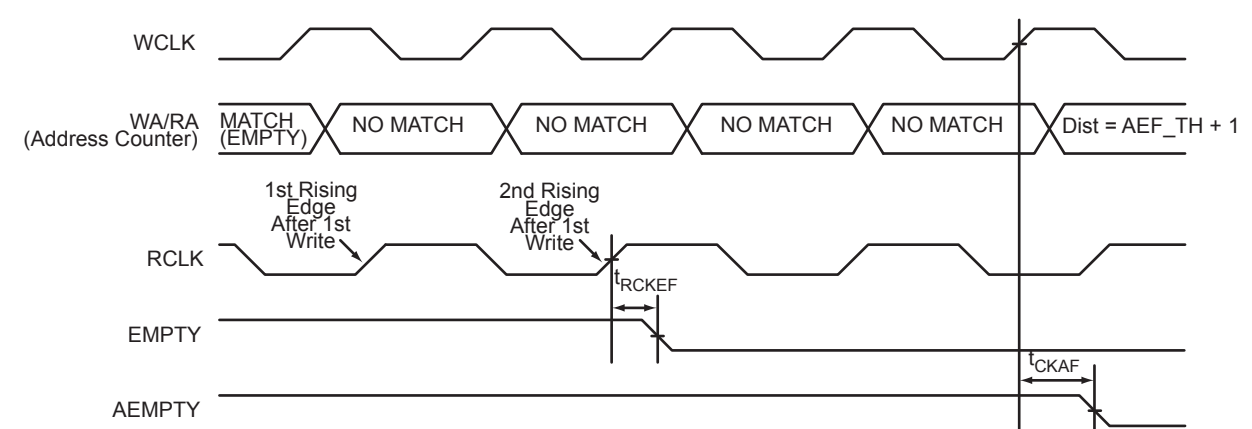
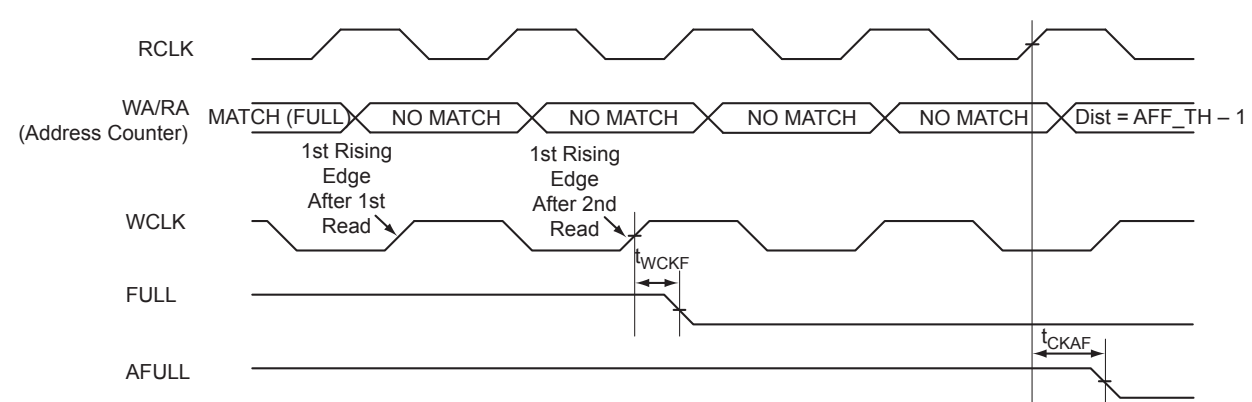


Figure 2-38 • FIFO EMPTY Flag and AEMPTY Flag Assertion


Figure 2-39 • FIFO FULL Flag and AFULL Flag Assertion

Figure 2-40 • FIFO EMPTY Flag and AEMPTY Flag Deassertion

Figure 2-41 • FIFO FULL Flag and AFULL Flag Deassertion

Timing Characteristics

Table 2-86 • FIFO
Worst Commercial-Case Conditions: $T_J = 85^{\circ}\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	–1	Units
t_{ENS}	REN_B, WEN_B Setup Time	1.40	ns
t_{ENH}	REN_B, WEN_B Hold Time	0.02	ns
t_{BKS}	BLK_B Setup Time	0.19	ns
t_{BKH}	BLK_B Hold Time	0.00	ns
t_{DS}	Input Data (DI) Setup Time	0.19	ns
t_{DH}	Input Data (DI) Hold Time	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on DO (flow-through)	2.39	ns
t_{CKQ2}	Clock High to New Data Valid on DO (pipelined)	0.91	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	1.74	ns
t_{WCKFF}	WCLK High to Full Flag Valid	1.66	ns
t_{CKAF}	Clock HIGH to Almost Empty/Full Flag Valid	6.29	ns
t_{RSTFG}	RESET_B Low to Empty/Full Flag Valid	1.72	ns
t_{RSTAF}	RESET_B Low to Almost Empty/Full Flag Valid	6.22	ns
t_{RSTBQ}	RESET_B Low to Data Out Low on DO (flow-through)	0.94	ns
	RESET_B Low to Data Out Low on DO (pipelined)	0.94	ns
t_{REMRSTB}	RESET_B Removal	0.29	ns
t_{RECRSTB}	RESET_B Recovery	1.52	ns
t_{MPWRSTB}	RESET_B Minimum Pulse Width	0.22	ns
t_{CYC}	Clock Cycle Time	3.28	ns
F_{MAX}	Maximum Frequency for FIFO	305	MHz

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-9](#) for derating values.

Embedded Nonvolatile Memory Block (eNVM)

Electrical Characteristics

Table 2-87 describes the eNVM maximum performance.

Table 2-87 • eNVM Block Timing, Worst Commercial Case Conditions: $T_J = 85^{\circ}\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	A2F200		A2F500		Units
		–1	Std.	–1	Std.	
$t_{FMAXCLKeNVM}$	Maximum frequency for clock for the control logic – 6 cycles (6:1:1:1*)	100	N/A	100	80	MHz
$t_{FMAXCLKeNVM}$	Maximum frequency for clock for the control logic – 5 cycles (5:1:1:1*)	80	80	50	50	MHz

Note: *6:1:1:1 indicates 6 cycles for the first access and 1 each for the next three accesses. 5:1:1:1 indicates 5 cycles for the first access and 1 each for the next three accesses.

Embedded FlashROM (eFROM)

Electrical Characteristics

Table 2-88 describes the eFROM maximum performance

Table 2-88 • FlashROM Access Time, Worst Commercial Case Conditions: $T_J = 85^{\circ}\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	–1	Units
t_{CK2Q}	Clock to out	28.68	ns
F_{max}	Maximum Clock frequency	15.00	MHz

JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/O Characteristics" section on page 2-21 for more details.

Timing Characteristics

Table 2-89 • JTAG 1532

Worst Commercial-Case Conditions: $T_J = 85^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	–1	Units
t_{DISU}	Test Data Input Setup Time	0.67	ns
t_{DIHD}	Test Data Input Hold Time	1.33	ns
t_{TMSSU}	Test Mode Select Setup Time	0.67	ns
t_{TMDHD}	Test Mode Select Hold Time	1.33	ns
t_{TCK2Q}	Clock to Q (data out)	8.00	ns
t_{RSTB2Q}	Reset to Q (data out)	26.67	ns
F_{TCKMAX}	TCK Maximum Frequency	19.00	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Table 2-89 • JTAG 1532
Worst Commercial-Case Conditions: $T_J = 85^{\circ}\text{C}$, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Units
t_{TRSTREM}	ResetB Removal Time	0.00	ns
t_{TRSTREC}	ResetB Recovery Time	0.27	ns
t_{TRSTMPW}	ResetB Minimum Pulse		ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-9](#) for derating values.

Programmable Analog Specifications

Current Monitor

Unless otherwise noted, current monitor performance is specified at 25°C with nominal power supply voltages, with the output measured using the internal voltage reference with the internal ADC in 12-bit mode and 91 Ksps, after digital compensation. All results are based on averaging over 16 samples.

Table 2-90 • Current Monitor Performance Specification

Specification	Test Conditions	Min.	Typical	Max.	Units
Input voltage range (for driving ADC over full range)*		0 – 48	0 – 50	1 – 51	mV
Analog gain	From the differential voltage across the input pads to the ADC input		50		V/V
Input referred offset voltage			–2.3		mV
Gain error	Slope of BFSL vs. 50 V/V		±0.5		% nom.
Overall Accuracy	Peak error from ideal transfer function, 25°C		±(0.4 + 1.5%)		mV plus % reading
Input referred noise	0 VDC input (no output averaging)		0.6		mVrms
Common-mode rejection ratio	0 V to 12 VDC common-mode voltage		84		dB
Analog settling time	To 0.1% of final value (with ADC load)				
	From CM_STB (High)	5			µs
	From ADC_START (High)	5		200	µs
Input capacitance			8		pF
Input biased current	CM[n] or TM[n] pad, –40°C to +100°C over maximum input voltage range (plus is into pad)				
	Strobe = 0; IBIAS on CM[n]		0		µA
	Strobe = 1; IBIAS on CM[n]		1		µA
	Strobe = 0; IBIAS on TM[n]		2		µA
	Strobe = 1; IBIAS on TM[n]		1		µA
Power supply rejection ratio	DC (0 – 10 KHz)		48		dB
Incremental operational current monitor power supply current requirements (per current monitor instance, not including ADC or VAREF _x)	VCC33A		150		µA
	VCC33AP		140		µA
	VCC15A		50		µA

Note: Under no condition should the TM pad ever be greater than 10 mV above than the CM pad.

Temperature Monitor

Unless otherwise noted, temperature monitor performance is specified with a 2N3904 diode-connected bipolar transistor from National Semiconductor or Infineon Technologies, nominal power supply voltages, with the output measured using the internal voltage reference with the internal ADC in 12-bit mode and 62.5 Ksps. After digital compensation. Unless otherwise noted, the specifications pertain to conditions where the SmartFusion device and the sensing diode are at the same temperature.

Table 2-91 • Temperature Monitor Performance Specifications

Specification	Test Conditions	Min.	Typical	Max.	Units
Input diode temperature range		–55		150	°C
		233.2		378.15	K
Temperature sensitivity			2.5		mV/K
Intercept	Extrapolated to 0K		0		V
Input referred temperature offset error	At 25°C (298.15K)		±1		°C
Gain error	Slope of BFSL vs. 2.5 mV/K		±1		% nom.
Overall accuracy	Peak error from ideal transfer function		±2		°C
Input referred noise	At 25°C (298.15K) – no output averaging		4		°C rms
Output current	Idle mode		100		µA
	Final measurement phases		10		µA
Analog settling time	Measured to 0.1% of final value, (with ADC load)				
	From TM_STB (High)	5			µs
	From ADC_START (High)	5		105	µs
AT parasitic capacitance				500	pF
Power supply rejection ratio	DC (0–10 KHz)		48		°C/V
Input referred temperature sensitivity error	Variation due to device temperature (–40°C to +100°C). External temperature sensor held constant.		0.0075		°C/°C
Temperature monitor (TM) operational power supply current requirements (per temperature monitor instance, not including ADC or VAREF _x)	VCC33A		200		µA
	VCC33AP		150		µA
	VCC15A		50		µA

Note: All results are based on averaging over 64 samples.

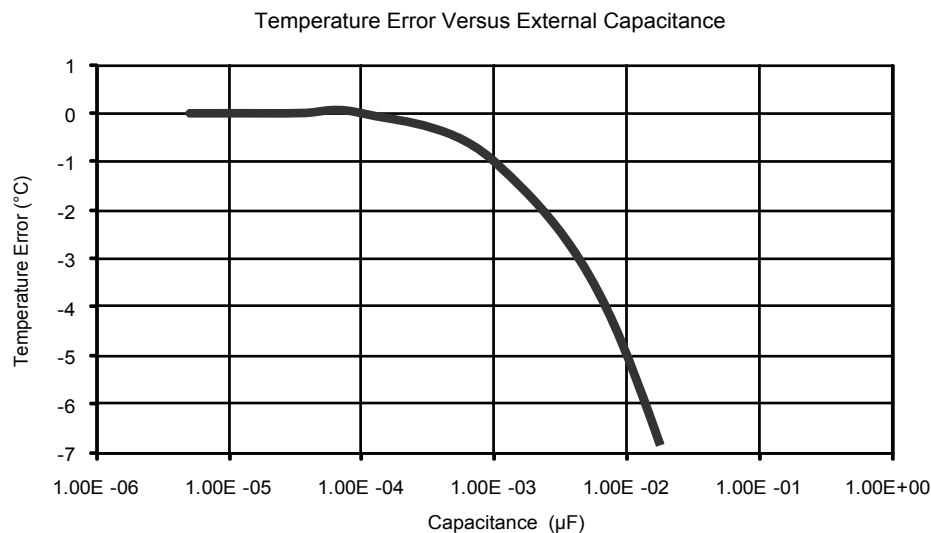


Figure 2-42 • Temperature Error Versus External Capacitance

Analog-to-Digital Converter (ADC)

Unless otherwise noted, ADC direct input performance is specified at 25°C with nominal power supply voltages, with the output measured using the external voltage reference with the internal ADC in 12-bit mode and 500 KHz sampling frequency, after trimming and digital compensation.

Table 2-92 • ADC Specifications

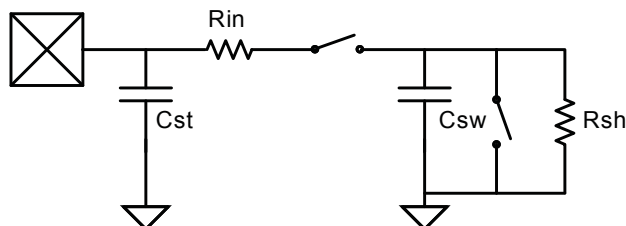
Specification	Test Conditions	Min.	Typ.	Max.	Units
Input voltage range (for driving ADC over its full range)			2.56		V
Gain error			±0.1	±0.2	%
Input referred offset voltage			±1	±2	mV
Integral non-linearity (INL)	RMS deviation from BFUL				
	10-bit mode		0.8		LSB
	8-bit mode		0.2		LSB
Differential non-linearity (DNL)	12-bit mode		2.4		LSB
	10-bit mode		0.6		LSB
	8-bit mode		0.2		LSB
Signal to noise ratio			64		dB
Effective number of bits (ENOB) $\text{ENOB} = \frac{\text{SINAD} - 1.76 \text{ dB}}{6.02 \text{ dB/bit}}$ EQ 10	–1 dBFS input				
	12-bit mode 10 KHz		10.4		Bits
	12-bit mode 100 KHz		10		Bits
	10-bit mode 10 KHz		9.6		Bits
	10-bit mode 100 KHz		9.5		Bits
	8-bit mode 10 KHz		7.9		Bits
	8-bit mode 100 KHz		7.9		Bits

Note: All 3.3 V supplies are tied together and varied from 3.0 V to 3.6 V. 1.5 V supplies are held constant.

Table 2-92 • ADC Specifications (continued)

Specification	Test Conditions	Min.	Typ.	Max.	Units
Full power bandwidth	At –3 dB; –1 dBFS input	300			KHz
Analog settling time	To 0.1% of final value (with 1 Kohm source impedance and with ADC load)		2		μs
Input capacitance	Switched capacitance (ADC sample capacitor)		12	15	pF
	Cs: Static capacitance (Figure 2-43)				
	CM[n] input		3		pF
	TM[n] input		3		pF
Input resistance	ADC[n] input		3		pF
	Rin: Series resistance (Figure 2-43)		2		KΩ
Input leakage current	Rsh: Shunt resistance, exclusive of switched capacitance effects (Figure 2-43)	10			MΩ
	–40°C to +100°C		1		μA
Power supply rejection ratio ²	DC		52		dB
ADC power supply operational current requirements	VCC33ADCx			2.5	mA
	VCC15A			2	mA

Note: All 3.3 V supplies are tied together and varied from 3.0 V to 3.6 V. 1.5 V supplies are held constant.


Figure 2-43 • ADC Input Model

Analog Bipolar Prescaler (ABPS)

With the ABPS set to its high range setting (GDEC = 00), a hypothetical input voltage in the range –15.36 V to +15.36 V is scaled and offset by the ABPS input amplifier to match the ADC full range of 0 V to 2.56 V using a nominal gain of –0.08333 V/V. However, due to reliability considerations, the voltage applied to the ABPS input should never be outside the range of –11.5 V to +14.4 V, restricting the usable ADC input voltage to 2.238 V to 0.080 V and the corresponding 12-bit output codes to the range of 3581 to 128 (decimal), respectively.

Unless otherwise noted, ABPS performance is specified at 25°C with nominal power supply voltages, with the output measured using the internal voltage reference with the internal ADC in 12-bit mode and 100 KHz sampling frequency, after trimming and digital compensation; and applies to all ranges.

Table 2-93 • ABPS Performance Specifications

Specification	Test Conditions	Min.	Typ.	Max.	Units
Input voltage range (for driving ADC over its full range)	GDEC[1:0] = 11		±2.56		V
	GDEC[1:0] = 10		±5.12		V
	GDEC[1:0] = 01		±10.24		V
	GDEC[1:0] = 00 (limited by maximum rating)		See note 1		V
Analog gain (from input pad to ADC input)	GDEC[1:0] = 11		–0.5		V/V
	GDEC[1:0] = 10		–0.25		V/V
	GDEC[1:0] = 01		–0.125		V/V
	GDEC[1:0] = 00		–0.0833		V/V
Gain error			±1		%
Input referred offset voltage					
	GDEC[1:0] = 11		–3.8		mV
	GDEC[1:0] = 10		–7.5		mV
	GDEC[1:0] = 01		–15		mV
	GDEC[1:0] = 00		–22		mV
SINAD			60		dB
Non-linearity	RMS deviation from BFSL			0.5	% FR
Effective number of bits (ENOB) $\text{ENOB} = \frac{\text{SINAD} - 1.76 \text{ dB}}{6.02 \text{ dB/bit}}$ EQ 11	GDEC[1:0] = 11 (±2.56 range), –1 dBFS input				
	12-bit mode 10 KHz		9.8		Bits
	12-bit mode 100 KHz		9.8		Bits
	10-bit mode 10 KHz		9.2		Bits
	10-bit mode 100 KHz		9.2		Bits
	8-bit mode 10 KHz		7.8		Bits
	8-bit mode 100 KHz		7.8		Bits
Large-signal bandwidth	–1 dBFS input		1		MHz
Analog settling time	To 0.1% of final value (with ADC load)			10	µs
Input resistance			1		MΩ

Table 2-93 • ABPS Performance Specifications (continued)

Specification	Test Conditions	Min.	Typ.	Max.	Units
Power supply rejection ratio	DC (0–1 KHz)		85		dB
ABPS power supply current requirements (not including ADC or VAREF _x)	ABPS_EN = 1 (operational mode)				
	VCC33A		130		μA
	VCC33AP		81		μA
	VCC15A		1		μA

Comparator

Unless otherwise specified, performance is specified at 25°C with nominal power supply voltages.

Table 2-94 • Comparator Performance Specifications

Specification	Test Conditions	Min.	Typ.	Max.	Units
Input voltage range	Minimum		0		V
	Maximum		2.56		V
Input offset voltage	HYS[1:0] = 00 (no hysteresis)		±1	±3	mV
Input bias current	Measured at 2.56 V		40		nA
Input resistance			10		MΩ
Power supply rejection ratio	DC (0 – 10 KHz)		60		dB
Propagation delay	100 mV overdrive HYS[1:0] = 00 (no hysteresis)		15		ns
	100 mV overdrive HYS[1:0] = 10 (with hysteresis)		25		ns
Hysteresis (± refers to rising and falling threshold shifts, respectively)	HYS[1:0] = 00		0		mV
	HYS[1:0] = 01		± 10		mV
	HYS[1:0] = 10		± 30		mV
	HYS[1:0] = 11		± 100		mV
Comparator current requirements	VCC33A = 3.3 V (operational mode); COMP_EN = 1				
	VCC33A		150		μA
	VCC33AP		140		μA
	VCC15A		1		μA

Analog Sigma-Delta Digital to Analog Converter (DAC)

Unless otherwise noted, sigma-delta DAC performance is specified at 25°C with nominal power supply voltages, using the internal sigma-delta modulators with 16-bit inputs, HCLK = 100 MHz, modulator inputs updated at a 100 KHz rate, in voltage output mode with an external 160 pF capacitor to ground, after trimming and digital [pre-]compensation.

Table 2-95 • Analog Sigma-Delta DAC

Specification	Test Conditions	Min.	Typ.	Max.	Units
Resolution		8	16	24	bits
Output range			0 to 2.56		V
	Current output mode		0 to 256		μA
Output Impedance			10		KΩ
	Current output mode	10	80		MΩ
Output voltage compliance	Current output mode		0–3.0		V
Gain error			1		%
	Current output mode		1		%
Output referred offset	With respect to GNDSDDX			1	mV
	Current output mode			1	μA
Integral non-linearity	RMS deviation from BFSL		0.5		%FR
Differential non-linearity			0.1		%FR
Analog settling time			Refer to Figure 2-44 on page 2-86		μs
Power supply rejection ratio	DC, full scale output		67		dB
Sigma-delta DAC power supply current requirements (not including VAREFx)	Input = 0, EN = 1 (operational mode)				
	VCC33SDDx		30		μA
	VCC15A		40		μA
	Input = Half scale, EN = 1 (operational mode)				
	VCC33SDDx		160		μA
	VCC15A		40		μA
	Input = Full scale, EN = 1 (operational mode)				
	VCC33SDDx		290		μA
	VCC15A		40		μA

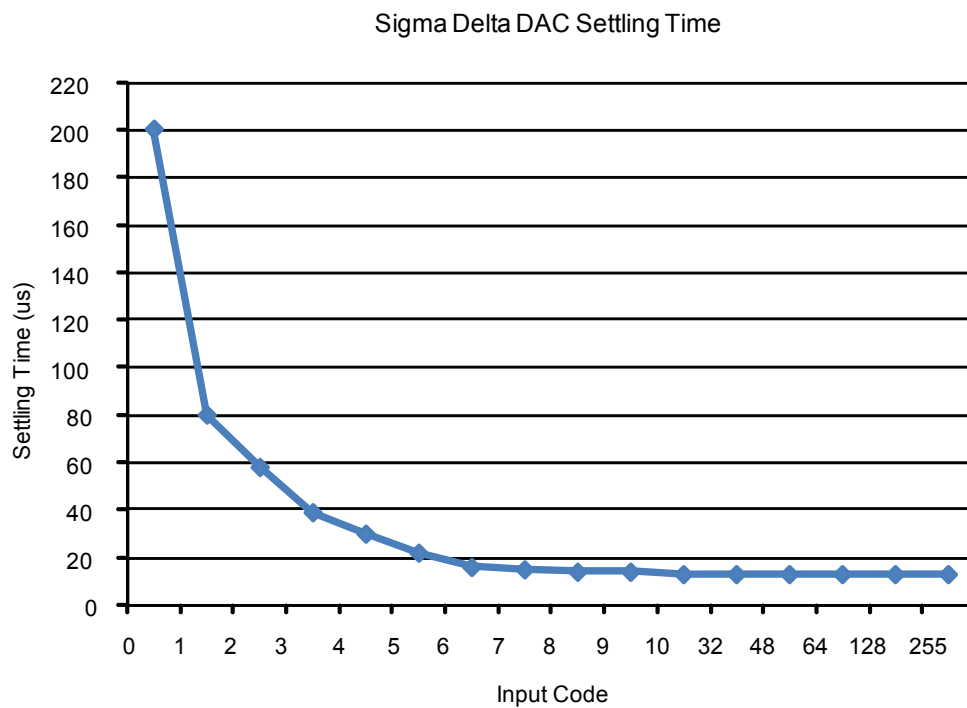


Figure 2-44 • Sigma-Delta DAC Settling Time

Voltage Regulator

Table 2-96 • Voltage Regulator

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V _{OUT}	Output voltage	T _J = 25°C		1.425	1.5	1.575	V
V _{OS}	Output offset voltage	T _J = 25°C			11		mV
I _{CC33A}	Operation current	T _J = 25°C	I _{LOAD} = 1 mA		3.4		mA
			I _{LOAD} = 100 mA		11		mA
			I _{LOAD} = 0.5 A		21		mA
ΔV _{OUT}	Load regulation	T _J = 25°C	I _{LOAD} = 1mA to 0.5 A		5.8		mV
ΔV _{OUT}	Line regulation	T _J = 25°C	V _{CC33A} = 2.97 V to 3.63 V I _{LOAD} = 1 mA		5.3		mV/V
			V _{CC33A} = 2.97 V to 3.63 V I _{LOAD} = 100 mA		5.3		mV/V
			V _{CC33A} = 2.97 V to 3.63 V I _{LOAD} = 500mA		5.3		mV/V
	Dropout voltage ¹	T _J = 25°C	I _{LOAD} = 1 mA		0.63		V
			I _{LOAD} = 100 mA		0.84		V
			I _{LOAD} = 0.5 A		1.35		V
I _{PTBASE}	PTBase current	T _J = 25°C	I _{LOAD} = 1 mA		48		μA
			I _{LOAD} = 100 mA		736		μA
			I _{LOAD} = 0.5 A		12		mA
	Startup time ²	T _J = 25°C			200		ms

Notes:

- *Dropout voltage is defined as the minimum V_{CC33A} voltage. The parameter is specified with respect to the output voltage. The specification represents the minimum input-to-output differential voltage required to maintain regulation.
- Assumes 10 μf.

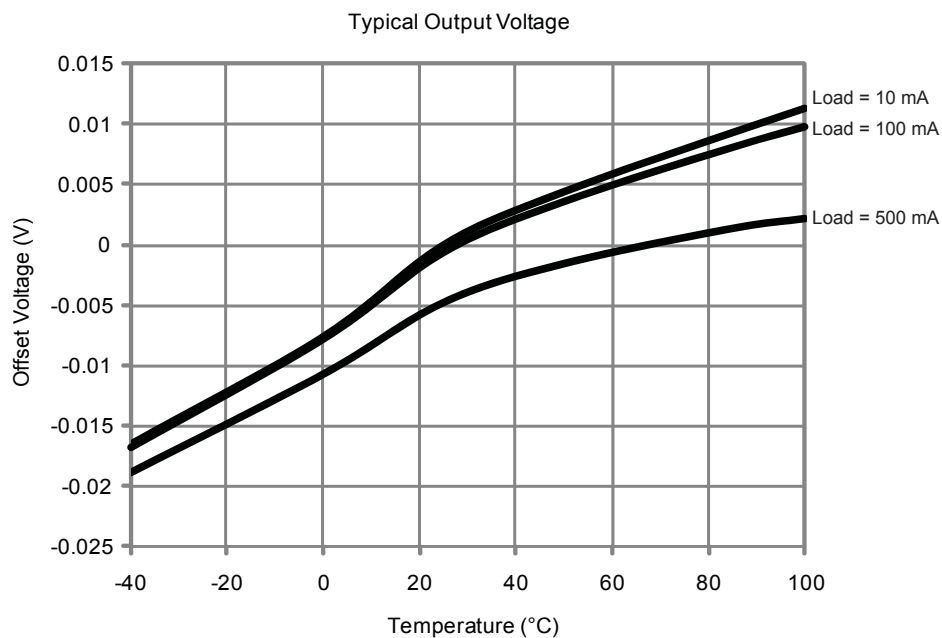


Figure 2-45 • Typical Output Voltage

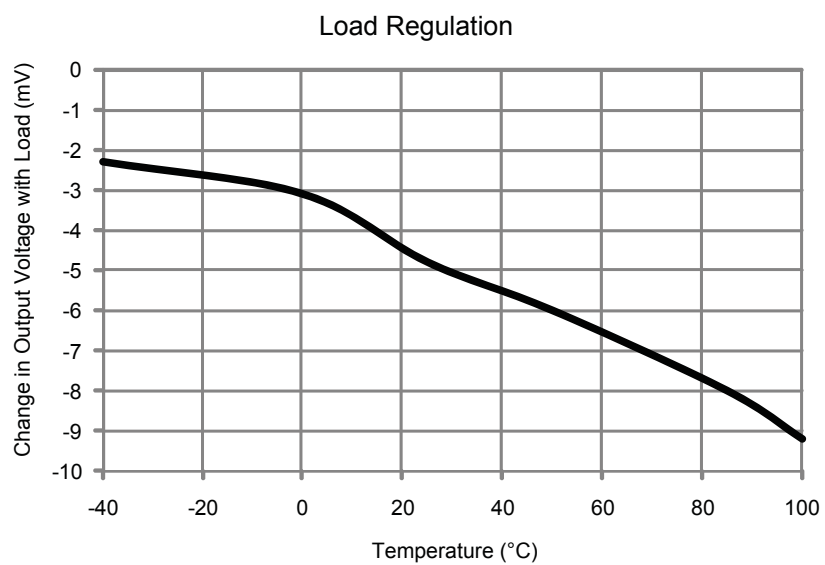


Figure 2-46 • Load Regulation

Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_x_CLK. For timing parameter definitions, refer to [Figure 2-47 on page 2-90](#).

Table 2-97 • SPI Characteristics

Commercial Case Conditions: T_J = 85°C, VDD = 1.425 V, –1 Speed Grade

Symbol	Description and Condition	A2F200	A2F500	Unit
sp1	SPI_x_CLK minimum period			
	SPI_x_CLK = PCLK/2	NA	20	ns
	SPI_x_CLK = PCLK/4	40	40	ns
	SPI_x_CLK = PCLK/8	80	80	ns
	SPI_x_CLK = PCLK/16	0.16	0.16	µs
	SPI_x_CLK = PCLK/32	0.32	0.32	µs
	SPI_x_CLK = PCLK/64	0.64	0.64	µs
	SPI_x_CLK = PCLK/128	1.28	1.28	µs
	SPI_x_CLK = PCLK/256	2.56	2.56	µs
sp2	SPI_x_CLK minimum pulse width high			
	SPI_x_CLK = PCLK/2	NA	10	ns
	SPI_x_CLK = PCLK/4	20	20	ns
	SPI_x_CLK = PCLK/8	40	40	ns
	SPI_x_CLK = PCLK/16	0.08	0.08	µs
	SPI_x_CLK = PCLK/32	0.16	0.16	µs
	SPI_x_CLK = PCLK/64	0.32	0.32	µs
	SPI_x_CLK = PCLK/128	0.64	0.64	µs
	SPI_x_CLK = PCLK/256	1.28	1.28	us
sp3	SPI_x_CLK minimum pulse width low			
	SPI_x_CLK = PCLK/2	NA	10	ns
	SPI_x_CLK = PCLK/4	20	20	ns
	SPI_x_CLK = PCLK/8	40	40	ns
	SPI_x_CLK = PCLK/16	0.08	0.08	µs
	SPI_x_CLK = PCLK/32	0.16	0.16	µs
	SPI_x_CLK = PCLK/64	0.32	0.32	µs
	SPI_x_CLK = PCLK/128	0.64	0.64	µs
	SPI_x_CLK = PCLK/256	1.28	1.28	µs
sp4	SPI_x_CLK, SPI_x_DO, SPI_x_SS rise time (10%-90%) ¹	4.7	4.7	ns
sp5	SPI_x_CLK, SPI_x_DO, SPI_x_SS fall time (10%-90%) ¹	3.4	3.4	ns

Notes:

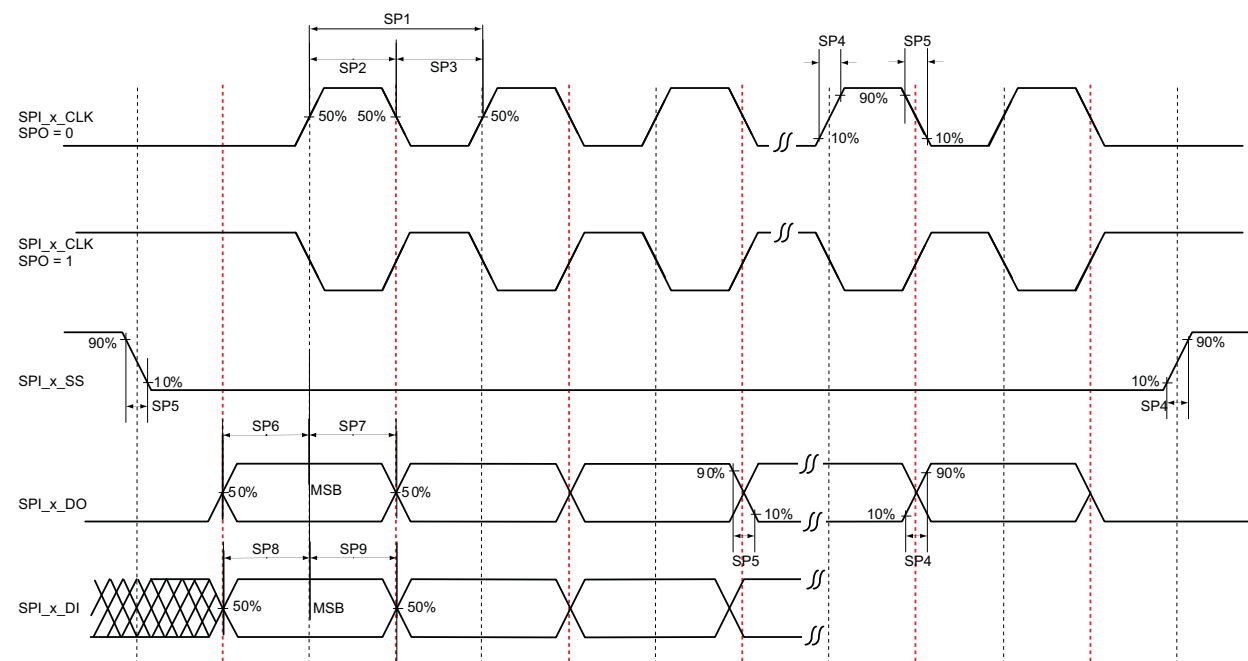
1. These values are provided for a load of 35 pF. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website:
<http://www.actel.com/download/ibis/default.aspx>.
2. For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the [SmartFusion Microcontroller Subsystem User's Guide](#).

Table 2-97 • SPI Characteristics
Commercial Case Conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.425\text{ V}$, -1 Speed Grade (continued)

Symbol	Description and Condition	A2F200	A2F500	Unit
sp6	Data from master (SPI_x_DO) setup time ²	1	1	pclk cycles
sp7	Data from master (SPI_x_DO) hold time ²	1	1	pclk cycles
sp8	SPI_x_DI setup time ²	1	1	pclk cycles
sp9	SPI_x_DI hold time ²	1	1	pclk cycles

Notes:

- These values are provided for a load of 35 pF. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website:
<http://www.actel.com/download/ibis/default.aspx>.
- For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the *SmartFusion Microcontroller Subsystem User's Guide*.


Figure 2-47 • SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)

Inter-Integrated Circuit (I²C) Characteristics

This section describes the DC and switching of the I²C interface. Unless otherwise noted, all output characteristics given are for a 100 pF load on the pins. For timing parameter definitions, refer to [Figure 2-48 on page 2-92](#).

Table 2-98 • I²C Characteristics

Commercial Case Conditions: T_J = 85°C, V_{DD} = 1.425 V, –1 Speed Grade

Parameter	Definition	Condition	Value	Unit
V _{IL}	Minimum input low voltage	–	See Table 2-35 on page 2-32	–
	Maximum input low voltage	–	See Table 2-35	–
V _{IH}	Minimum input high voltage	–	See Table 2-35	–
	Maximum input high voltage	–	See Table 2-35	–
V _{OL}	Maximum output voltage low	I _{OL} = 8 mA	See Table 2-35	–
I _{IL}	Input current high	–	See Table 2-35	–
I _{IH}	Input current low	–	See Table 2-35	–
V _{hyst}	Hysteresis of Schmitt trigger inputs	–	See Table 2-32 on page 2-31	V
T _{FALL}	Fall time ²	VIHmin to VILMax, C _{load} = 400 pF	15.0	ns
		VIHmin to VILMax, C _{load} = 100 pF	4.0	ns
T _{RISE}	Rise time ²	VILMax to VIHmin, C _{load} = 400pF	19.5	ns
		VILMax to VIHmin, C _{load} = 100pF	5.2	ns
C _{in}	Pin capacitance	VIN = 0, f = 1.0 MHz	8.0	pF
R _{pull-up}	Output buffer maximum pull-down Resistance ¹	–	50	Ω
R _{pull-down}	Output buffer maximum pull-up Resistance ¹	–	150	Ω
D _{max}	Maximum data rate	Fast mode	400	Kbps
t _{LOW}	Low period of I2C_x_SCL ³	–	1	clk cycles
t _{HIGH}	High period of I2C_x_SCL ³	–	1	clk cycles
t _{HD;STA}	START hold time ³	–	1	clk cycles
t _{SU;STA}	START setup time ³	–	1	clk cycles
t _{HD;DAT}	DATA hold time ³	–	1	clk cycles
t _{SU;DAT}	DATA setup time ³	–	1	clk cycles

Notes:

1. These maximum values are provided for information only. Minimum output buffer resistance values depend on VCCxxxIOBx, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website at <http://www.actel.com/download/ibis/default.aspx>.
2. These values are provided for a load of 100 pF and 400 pF. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website at <http://www.actel.com/download/ibis/default.aspx>.
3. For allowable Pclk configurations, refer to the Inter-Integrated Circuit (I²C) Peripherals section in the [SmartFusion Microcontroller Subsystem User's Guide](#).

Table 2-98 • I²C Characteristics

Commercial Case Conditions: T_J = 85°C, V_{DD} = 1.425 V, –1 Speed Grade (continued)

Parameter	Definition	Condition	Value	Unit
t _{SU;STO}	STOP setup time ³	–	1	pclk cycles
t _{FILT}	Maximum spike width filtered	–	50	ns

Notes:

1. These maximum values are provided for information only. Minimum output buffer resistance values depend on VCCxxxxIOBx, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website at <http://www.actel.com/download/ibis/default.aspx>.
2. These values are provided for a load of 100 pF and 400 pF. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website at <http://www.actel.com/download/ibis/default.aspx>.
3. For allowable Pclk configurations, refer to the Inter-Integrated Circuit (I²C) Peripherals section in the [SmartFusion Microcontroller Subsystem User's Guide](#).

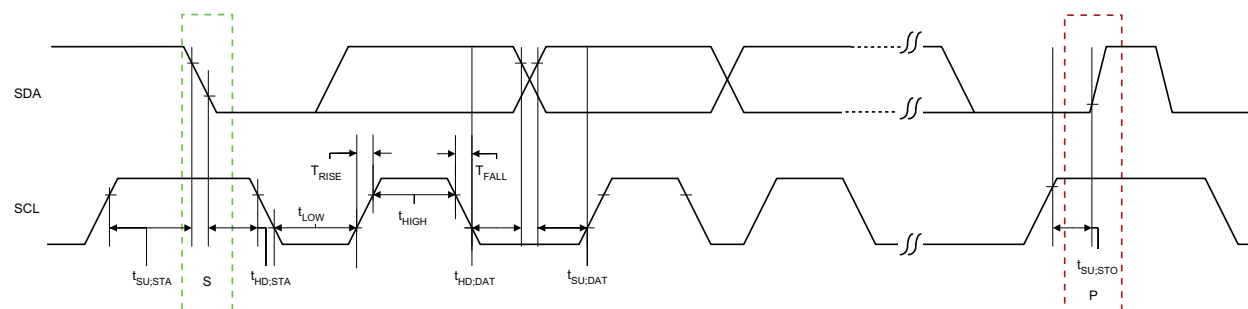


Figure 2-48 • I2C Timing Parameter Definition

3 – SmartFusion Development Tools

SmartFusion™ applications will be developed by a multi-discipline team of designers working on one project or one designer acting in several roles. Actel has developed design tools and flows to meet the needs of three different skilled designers that can work smoothly together in a single project (Figure 3-1).

- FPGA designers
- Embedded software designers
- Analog designers

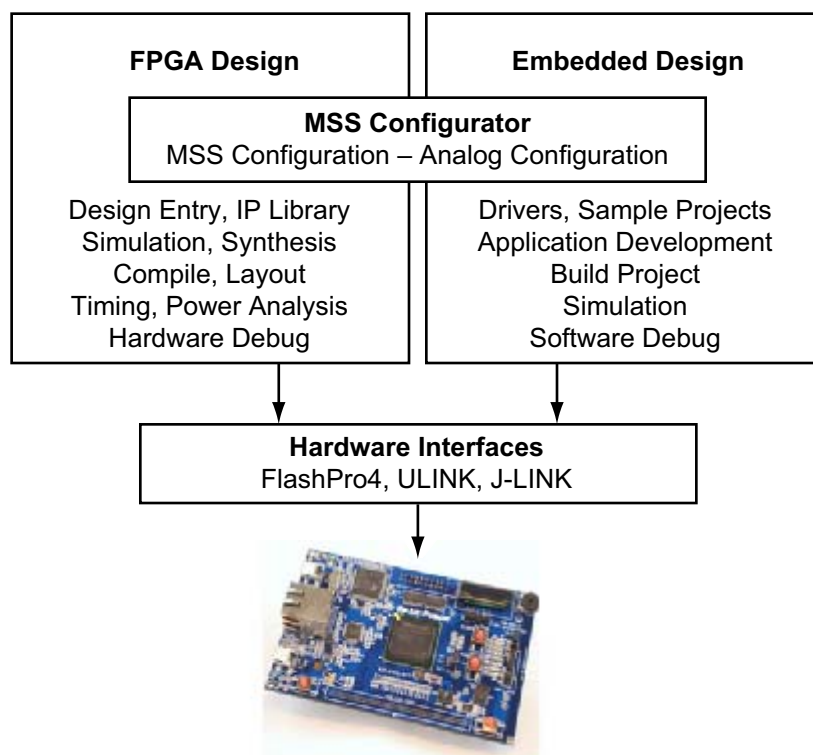


Figure 3-1 • Three Design Roles

For FPGA designers, Libero® Integrated Design Environment (IDE) is Actel's comprehensive toolset for designing with all Actel FPGAs. Libero IDE includes industry leading synthesis, simulation, and place-and-route debug tools, including Synplicity® and ModelSim®, as well as innovative timing, power optimization, and power analysis.

For embedded designers, Actel offers FREE SoftConsole Eclipse-based IDE, as well as evaluation versions from Keil™ and IAR Systems. Full versions of the latter are available from the respective suppliers.

For analog designers, the microcontroller subsystem (MSS) configurator provides graphical setup for current, voltage, and temperature monitors, sample sequencing setup and post processing configuration, and DAC output.

The MSS configurator creates a bridge between the FPGA and embedded designers so device configuration can be easily shared between multiple developers.

The MSS configurator includes the following:

- A simple configurator for the embedded designer to control the MSS peripherals and I/Os
- A method to import and view a hardware configuration from the FPGA flow into the embedded flow containing the memory map
- Automatic generation of drivers for any peripherals or soft IP used in the system configuration
- Comprehensive analog configuration for the programmable analog components
- Creation of a standard MSS block to be used in SmartDesign for connection of FPGA fabric designs and IP

SmartFusion Ecosystem

Actel has a long history of supplying comprehensive FPGA development tools and recognizes the benefit of partnering with industry leaders to deliver the optimum usability and productivity to users. Taking the same approach to processor development, Actel has partnered with key industry leaders in the microcontroller space to provide a robust solution that can be easily adopted by existing embedded developers and has an easy learning path for FPGA designers. Actel is partnering with Keil and IAR to provide software IDE support to SmartFusion Designers. In addition, Micrium provides support for SmartFusion with its new μ C/OS-III,™ TCP/IP,™ and μ C/Probe™ products (Table 3-1 on page 3-3).

Support for the Actel device and ecosystem resources is represented in Figure 3-2.

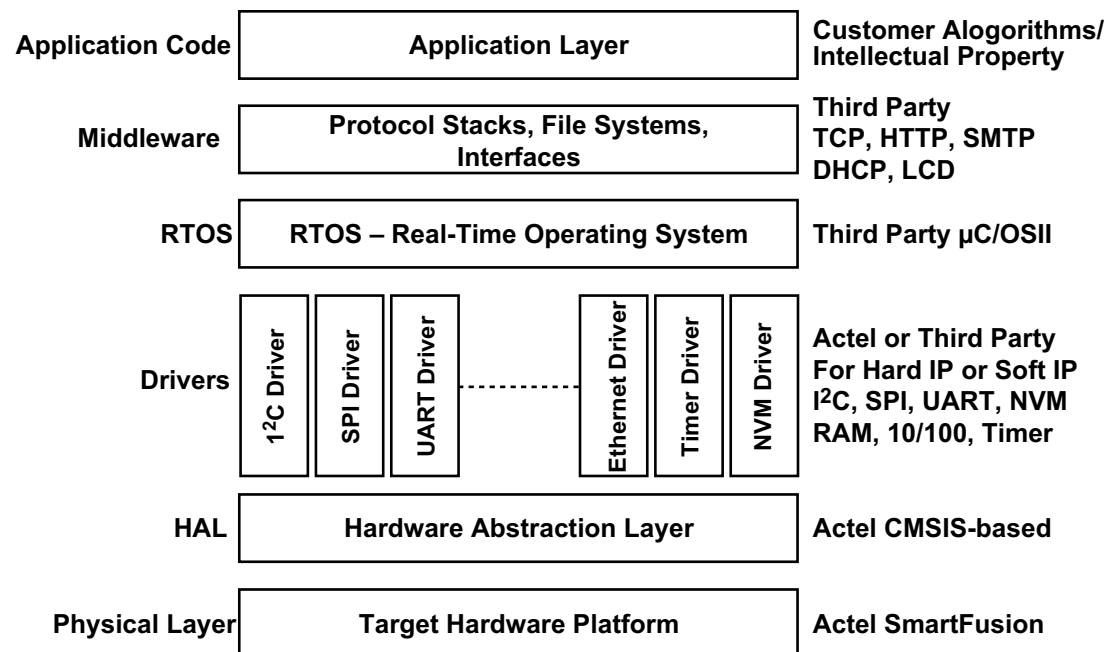






Figure 3-2 • SmartFusion Ecosystem

Starting from the base up, the ARM® Cortex™ Microcontroller Software Interface Standard (CMSIS) hardware abstraction layer (HAL) is built on top of the SmartFusion hardware platform. Each of the peripherals has its own driver, whether it is hard IP or soft IP added in the FPGA fabric. Then on top of that we will work with third party real-time operating system (RTOS) vendors for OS, protocol stacks, and interfaces. A designer can add a custom application with all, some, or none of the layers below.




Software Integrated Design Environment (IDE) Choices

			
Software IDE	SoftConsole	Vision IDE	Embedded Workbench
Website	www.actel.com	www.keil.com	www.iar.com
Free versions from Actel	Free with Libero IDE	32 K code limited	32 K code limited
Available from Vendor	N/A	Full version	Full version
Compiler	GNU GCC	RealView C/C++	IAR ARM Compiler
Debugger	GDB debug	Vision Debugger	C-SPY Debugger
Instruction Set Simulator	No	Vision Simulator	Yes
Debug Hardware	FlashPro4	ULINK2 or ULINK-ME	J-LINK or J-LINK Lite

Operating System and Middleware Support

Micrium is recognized as a leader in embedded software components. The company's flagship μ C/OS family is recognized for a variety of features and benefits, including unparalleled reliability, performance, dependability, impeccable source code, and vast documentation, available from www.micrium.com

Table 3-1 • Micrium Embedded Software Components

		
μ C/OS-III,™ Micrium's newest RTOS, is designed to save time on your next embedded project and puts greater control of the software in your hands, yet maintains Micrium's ease-of-use, ease-of-integration, short learning curve, unsurpassed documentation, and clean code.	μ C/TCP-IP™ is a compact, reliable, and high-performance stack built from the ground up by Micrium and has the quality, scalability, and reliability that translates into a rapid configuration of network options, remarkable ease-of-use, and rapid time-to-market.	μ C/Probe™ is one of the most useful tools in embedded systems design and puts you in the driver's seat, allowing you to take charge of virtually any variable, memory location, and I/O port in your embedded product, while your system is running—there's no need to stop.

4 – SmartFusion Programming

SmartFusion devices have three separate flash areas that can be programmed:

1. The FPGA fabric
2. The embedded nonvolatile memories (eNVMs)
3. The embedded flash ROM (eFROM)

There are essentially three methodologies for programming these areas:

1. In-system programming (ISP)
2. In-application programming (IAP)—only the FPGA Fabric and the eNVM
3. Pre-programming (non-ISP)

Programming, whether ISP or IAP methodologies are employed, can be done in two ways:

1. Securely using the on chip AES decryption logic
2. In plain text

In-System Programming

In-System Programming is performed with the aid of external JTAG programming hardware. [Table 4-1](#) describes the JTAG programming hardware that will program a SmartFusion device and [Table 4-2](#) defines the JTAG pins that provide the interface for the programming hardware.

Table 4-1 • Supported JTAG Programming Hardware

Dongle	Source	JTAG	SWD ¹	SWV ²	Program FPGA	Program eFROM	Program eNVM
FlashPro3/4	Actel	Yes	No	No	Yes	Yes	Yes
ULINK Pro	Keil	Yes	Yes	Yes	Yes	Yes	Yes
ULINK2	Keil	Yes	Yes	Yes	Yes	Yes	Yes
IAR J-Link	IAR	Yes	Yes	Yes	Yes	Yes	Yes

Notes:

1. SWD = ARM Serial Wire Debug
2. SWV = ARM Serial Wire Viewer

Table 4-2 • SmartFusion JTAG Pin Descriptions

Pin Name	Description
JTAGSEL	ARM Cortex-M3 or FPGA test access port (TAP) controller selection
TRSTB	Test reset bar
TCK	Test clock
TMS	Test mode select
TDI	Test data input
TDO	Test data output

The JTAGSEL pin selects the FPGA TAP controller or the Cortex-M3 debug logic. When JTAG SEL is asserted, the FPGA TAP controller is selected and the TRSTB input into the Cortex-M3 is held in a reset state (logic 0), as depicted in [Figure 4-1](#). Users should tie the JTAGSEL pin high externally.

Note: Standard ARM JTAG connectors do not have access to the JTAGSEL pin. Actel's free Eclipse-based IDE, Soft Console, automatically sets JTAGSEL via FlashPro4 to the appropriate state for programming all memory regions.

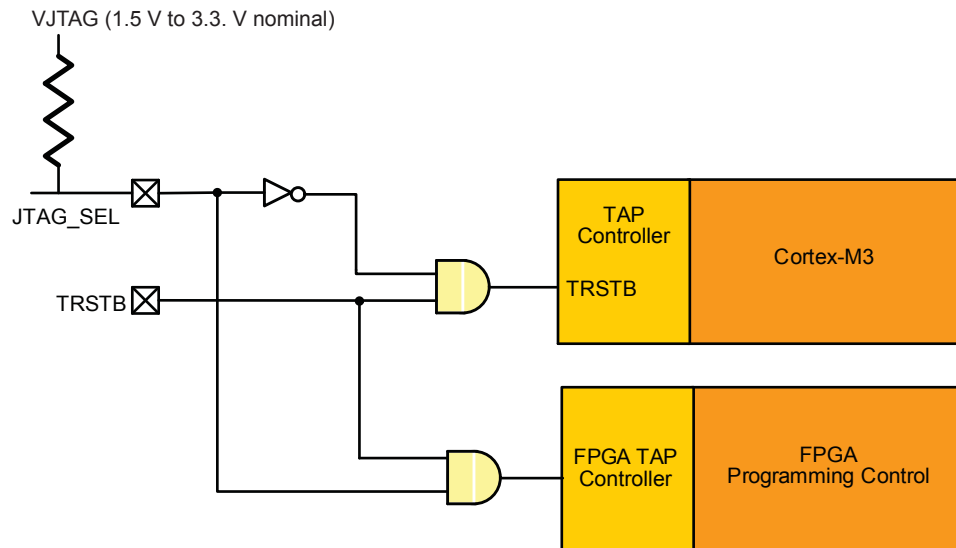


Figure 4-1 • TRSTB Logic

In-Application Programming

In-application programming refers to the ability to reprogram the various flash areas under direct supervision of the Cortex-M3.

Reprogramming the FPGA Fabric Using the Cortex-M3

In this mode, the Cortex-M3 is executing the programming algorithm on-chip. The IAP driver can be incorporated into the design project and executed from eNVM or eSRAM. Actel provides working example projects for SoftConsole, IAR, and Keil development environments. These can be downloaded via the Actel Firmware Catalog. The new bitstream to be programmed into the FPGA can reside on the user's printed circuit board (PCB) in a separate SPI flash memory. Alternately, the user can modify the existing projects supplied by Actel and, via custom handshaking software, throttle the download of the new image and program the FPGA a piece at a time in real time. A cost-effective and reliable approach would be to store the bitstream in an external SPI flash. Another option is storing a redundant bitstream image in an external SPI flash and loading the newest version into the FPGA only when receiving an IAP command. Since the FPGA I/Os are tristated or held at predefined or last known state during FPGA programming, the user must use MSS I/Os to interface to external memories. Since there are two SPI controllers in the MSS, the user can dedicate one to an SPI flash and the other to the particulars of an application. The amount of flash memory required to program the FPGA always exceeds the size of the eNVM block that is on-chip. The external memory controller (EMC) cannot be used as an interface to a memory device for storage of a bitstream because its I/O pads are FPGA I/Os; hence they are tristated when the FPGA is in a programming state.

Re-Programming the eNVM Blocks Using the Cortex-M3

In this mode the Cortex-M3 is executing the eNVM programming algorithm from eSRAM. Since individual pages (132 bytes) of the eNVM can be write-protected, the programming algorithm software can be protected from inadvertent erasure. When reprogramming the eNVM, both MSS I/Os and FPGA I/Os are available as interfaces for sourcing the new eNVM image. Actel provides working example projects for SoftConsole, IAR, and Keil development environments. These can be downloaded via the Actel Firmware Catalog.

Alternately, the eNVM can be reprogrammed by the Cortex-M3 via the IAP driver. This is necessary when using an encrypted image.

Secure Programming

For background, refer to the *Security in Low Power Flash Devices* application note on the Actel website. SmartFusion Secure ISP behaves identically to Fusion Secure ISP. Secure IAP of SmartFusion devices is accomplished by using the IAP driver. Only the FPGA fabric and the eNVM can be reprogrammed securely by using the IAP driver.

Typical Programming and Erase Times

Table 4-3 documents the typical programming and erase times for two components of SmartFusion devices, FPGA fabric and eNVM, using Actel's FlashPro hardware and software. These times will be different for other ISP and IAP methods. The **Program** action in FlashPro software includes erase, program, and verify to complete.

The typical programming (including erase) time per page of the eNVM is 8 ms.

Table 4-3 • Typical Programming and Erase Times

	FPGA Fabric (seconds)		eNVM (seconds)	
	A2F200	A2F500	A2F200	A2F500
Erase	21	21	N/A	N/A
Program	8	15	18	26
Verify	9	16	26	42

References

Application Notes

In-System Programming (ISP) of Actel's Low-Power Flash Devices Using FlashPro3

http://www.actel.com/documents/LPD_ISP_HBs.pdf

Security in Low Power Flash Devices

http://www.actel.com/documents/LPD_Security_HBs.pdf

Programming Flash Devices

http://www.actel.com/documents/Flash_Program_HBs.pdf

Microprocessor Programming of Actel's Low-Power Flash Devices

http://www.actel.com/documents/LPD_Microprocessor_HBs.pdf

User's Guides

DirectC User's Guide

http://www.actel.com/documents/DirectC_UG.pdf

5 – Pin Descriptions

Supply Pins

Name	Type	Description
GND	Ground	Digital ground to the FPGA fabric, microcontroller subsystem and GPIOs
GND15ADC0	Ground	Quiet analog ground to the 1.5 V circuitry of the first analog-to-digital converter (ADC)
GND15ADC1	Ground	Quiet analog ground to the 1.5 V circuitry of the second ADC
GND15ADC2	Ground	Quiet analog ground to the 1.5 V circuitry of the third ADC
GND33ADC0	Ground	Quiet analog ground to the 3.3 V circuitry of the first ADC
GND33ADC1	Ground	Quiet analog ground to the 3.3 V circuitry of the second ADC
GND33ADC2	Ground	Quiet analog ground to the 3.3 V circuitry of the third ADC
GND _A	Ground	Quiet analog ground to the analog front-end
GND _{AQ}	Ground	Quiet analog ground to the analog I/O of Actel SmartFusion™ devices
GND _{ENVM}	Ground	Digital ground to the embedded nonvolatile memory (eNVM)
GND _{LPXTAL}	Ground	Analog ground to the low power 32 KHz crystal oscillator circuitry
GND _{MAINXTAL}	Ground	Analog ground to the main crystal oscillator circuitry
GND _Q	Ground	Quiet digital ground supply voltage to input buffers of I/O banks. Within the package, the GND _Q plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GND _Q needs to always be connected on the board to GND.
GND _{RCOSC}	Ground	Analog ground to the integrated RC oscillator circuit
GND _{SDD0}	Ground	Analog ground to the first sigma-delta DAC
GND _{SDD1}	Ground	Common analog ground to the second and third sigma-delta DACs
GND _{TM0}	Ground	Analog temperature monitor common ground for signal conditioning blocks SCB 0 and SCB 1 (see information for pins "TM0" and "TM1" in the "Analog Front-End (AFE)" section on page 5-12).
GND _{TM1}	Ground	Analog temperature monitor common ground for signal conditioning block SCB 2 and SBCB 3 (see information for pins "TM2" and "TM3" in the "Analog Front-End (AFE)" section on page 5-12).
GND _{TM2}	Ground	Analog temperature monitor common ground for signal conditioning block SCB4
GND _{VAREF}	Ground	Analog ground reference used by the ADC. This pad should be connected to a quiet analog ground.
VCC	Supply	Digital supply to the FPGA fabric and MSS, nominally 1.5 V. VCC is also required for powering the JTAG state machine, in addition to V _{JTAG} . Even when a SmartFusion device is in bypass mode in a JTAG chain of interconnected devices, both VCC and V _{JTAG} must remain powered to allow JTAG signals to pass through the SmartFusion device.

Notes:

1. The following 3.3 V supplies should be connected together while following proper noise filtering practices: VCC33A, VCC33ADCx, VCC33AP, VCC33SDDx, VCCMAINXTAL, and VCCLPXTAL.
2. The following 1.5 V supplies should be connected together while following proper noise filtering practices: VCC, VCC15A, and VCC15ADCx.

Name	Type	Description
VCC15A	Supply	Clean analog 1.5 V supply to the analog circuitry
VCC15ADC0	Supply	Analog 1.5 V supply to the first ADC
VCC15ADC1	Supply	Analog 1.5 V supply to the second ADC
VCC15ADC2	Supply	Analog 1.5 V supply to the third ADC
VCC33A	Supply	Clean 3.3 V analog supply to the analog circuitry. VCC33A is also used to feed the 1.5 V voltage regulator for designs that do not provide an external supply to VCC. Refer to the Voltage Regulator (VR), Power Supply Monitor (PSM), and Power Modes section in the <i>SmartFusion Microcontroller Subsystem User's Guide</i> for more information.
VCC33ADC0	Supply	Analog 3.3 V supply to the first ADC.
VCC33ADC1	Supply	Analog 3.3 V supply to the second ADC
VCC33ADC2	Supply	Analog 3.3 V supply to the third ADC
VCC33AP	Supply	Analog clean 3.3 V supply to the charge pump. To avoid high current draw, VCC33AP should be powered up simultaneously with or after VCC33A.
VCC33N	Supply	–3.3 V output from the voltage converter. A 2.2 μ F capacitor must be connected from this pin to GND. Analog charge pump capacitors are not needed if none of the analog SCB features are used and none of the SDDs are used. In that case it should be left unconnected.
VCC33SDD0	Supply	Analog 3.3 V supply to the first sigma-delta DAC
VCC33SDD1	Supply	Common analog 3.3 V supply to the second and third sigma-delta DACs
VCCENVM	Supply	Digital 1.5 V power supply to the embedded nonvolatile memory blocks. To avoid high current draw, VCC should be powered up before or simultaneously with VCCENVM.
VCCFPGAIOB0	Supply	Digital supply to the FPGA fabric I/O bank 0 (north FPGA I/O bank) for the output buffers and I/O logic. Each bank can have a separate VCCFPGAIO connection. All I/Os in a bank will run off the same VCCFPGAIO supply. VCCFPGAIO can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCFPGAIO pins tied to GND.
VCCFPGAIOB1	Supply	Digital supply to the FPGA fabric I/O bank 1 (east FPGA I/O bank) for the output buffers and I/O logic.
VCCFPGAIOB5	Supply	Digital supply to the FPGA fabric I/O bank 5 (west FPGA I/O bank) for the output buffers and I/O logic. Each bank can have a separate VCCFPGAIO connection. All I/Os in a bank will run off the same VCCFPGAIO supply. VCCFPGAIO can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCFPGAIO pins tied to GND. Each bank can have a separate VCCFPGAIO connection. All I/Os in a bank will run off the same VCCFPGAIO supply. VCCFPGAIO can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCFPGAIO pins tied to GND.
VCCLPXTAL	Supply	Analog supply to the low power 32 KHz crystal oscillator
VCCMAINXTAL	Supply	Analog supply to the main crystal oscillator circuit

Notes:

1. The following 3.3 V supplies should be connected together while following proper noise filtering practices: VCC33A, VCC33ADCx, VCC33AP, VCC33SDDx, VCCMAINXTAL, and VCCLPXTAL.
2. The following 1.5 V supplies should be connected together while following proper noise filtering practices: VCC, VCC15A, and VCC15ADCx.

Name	Type	Description
VCCMSSIOB2	Supply	Supply voltage to the microcontroller subsystem I/O bank 2 (east MSS I/O bank) for the output buffers and I/O logic
VCCMSSIOB4	Supply	Supply voltage to the microcontroller subsystem I/O bank 4 (west MSS I/O bank) for the output buffers and I/O logic. Each bank can have a separate VCCMSSIO connection. All I/Os in a bank will run off the same VCCMSSIO supply. VCCMSSIO can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCMSSIO pins tied to GND. Each bank can have a separate VCCMSSIO connection. All I/Os in a bank will run off the same VCCMSSIO supply. VCCMSSIO can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCMSSIO pins tied to GND.
VCCPLLx	Supply	Analog 1.5 V supply to the PLL
VCCRCOSC	Supply	Analog supply to the integrated RC oscillator circuit
VCOMPLAx	Supply	Analog ground for the PLL
VDDBAT	Supply	External battery connection to the low power 32 KHz crystal oscillator (along with VCCLPXTAL), RTC, and battery switchover circuit
VJTAG	Supply	Digital supply to the JTAG controller SmartFusion devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned to be used, the V _{JTAG} pin together with the TRSTB pin could be tied to GND. Note that VCC is required to be powered for JTAG operation; VJTAG alone is insufficient. If a SmartFusion device is in a JTAG chain of interconnected boards and it is desired to power down the board containing the device, this can be done provided both VJTAG and VCC to the device remain powered; otherwise, JTAG signals will not be able to transition the device, even in bypass mode. See "JTAG Pins" section on page 5-8 .
VPP	Supply	Digital programming circuitry supply SmartFusion devices support single-voltage in-system programming (ISP) of the configuration flash, embedded FlashROM (eFROM), and embedded nonvolatile memory (eNVM). For programming, VPP should be in the 3.3 V \pm 5% range. During normal device operation, VPP can be left floating or can be tied to any voltage between 0 V and 3.6 V. When the VPP pin is tied to ground, it shuts off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry. For proper programming, 0.01 μ F and 0.33 μ F capacitors (both rated at 16 V) are to be connected in parallel across VPP and GND, and positioned as close to the FPGA pins as possible.

Notes:

1. The following 3.3 V supplies should be connected together while following proper noise filtering practices: VCC33A, VCC33ADCx, VCC33AP, VCC33SDDx, VCCMAINXTAL, and VCCLPXTAL.
2. The following 1.5 V supplies should be connected together while following proper noise filtering practices: VCC, VCC15A, and VCC15ADCx.

User-Defined Supply Pins

Name	Type	Polarity/Bus Size	Description
VAREF0	Input	1	<p>Analog reference voltage for first ADC</p> <p>The SmartFusion device can be configured to generate a 2.56 V internal reference that can be used by the ADC. While using the internal reference, the reference voltage is output on the VAREFOUT pin for use as a system reference. If a different reference voltage is required, it can be supplied by an external source and applied to this pin. The valid range of values that can be supplied to the ADC is 1.0 V to 3.3 V. When VAREF0 is internally generated, a bypass capacitor must be connected from this pin to ground. The value of the bypass capacitor should be between 3.3 μF and 22 μF, which is based on the needs of the individual designs. The choice of the capacitor value has an impact on the settling time it takes the VAREF0 signal to reach the required specification of 2.56 V to initiate valid conversions by the ADC. If the lower capacitor value is chosen, the settling time required for VAREF0 to achieve 2.56 V will be shorter than when selecting the larger capacitor value. The above range of capacitor values supports the accuracy specification of the ADC, which is detailed in the datasheet. Designers choosing the smaller capacitor value will not obtain as much margin in the accuracy as that achieved with a larger capacitor value. See the Analog-to-Digital Converter (ADC) section in the SmartFusion Programmable Analog User's Guide for more information. Actel recommends customers use 10 μF as the value of the bypass capacitor. Designers choosing to use an external VAREF0 need to ensure that a stable and clean VAREF0 source is supplied to the VAREF0 pin before initiating conversions by the ADC. To use the internal voltage reference, you must connect the VAREFOUT pin to the appropriate ADC VAREFx input—either the VAREF0 or VAREF1 pin—on the PCB.</p>
VAREF1	Input	1	<p>Analog reference voltage for second ADC</p> <p>See "VAREF0" above for more information.</p>
VAREF2	Input	1	<p>Analog reference voltage for third ADC</p> <p>See "VAREF0" above for more.</p>
VAREFOUT	Out	1	<p>Internal 2.56 V voltage reference output. Can be used to provide the two ADCs with a unique voltage reference externally by connecting VAREFOUT to both VAREF0 and VAREF1. To use the internal voltage reference, you must connect the VAREFOUT pin to the appropriate ADC VAREFx input—either the VAREF0 or VAREF1 pin—on the PCB.</p>

User Pins

Name	Type	Polarity/Bus Size	Description
GPIO_x	In/out	32	<p>Microcontroller Subsystem (MSS)</p> <p>General Purpose I/O (GPIO).</p> <p>The MSS GPIO pin functions as an input, output, tristate, or bidirectional buffer with configurable interrupt generation and Schmitt trigger support. Input and output signal levels are compatible with the I/O standard selected.</p> <p>Unused GPIO pins are tristated and do not include pull-up or pull-down resistors.</p> <p>During power-up, the used GPIO pins are tristated with no pull-up or pull-down resistors until Sys boot configures them.</p> <p>Some of these pins are also multiplexed with integrated peripherals in the MSS (SPI, I²C, and UART).</p> <p>GPIOs can be routed to dedicated I/O buffers (MSSIOBUF) or in some cases to the FPGA fabric interface through an IOMUX. This allows GPIO pins to be multiplexed as either I/Os for the FPGA fabric, the ARM[®] Cortex[™]-M3 or for given integrated MSS peripherals. The MSS peripherals are not multiplexed with each other; they are multiplexed only with the GPIO block. For more information General Purpose I/O Block (GPIO) section in the SmartFusion Microcontroller Subsystem User's Guide.</p>
IO	In/out		<p>FPGA user I/O</p> <p>The FPGA user I/O pin functions as an input, output, tristate or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected. Unused I/O pins are disabled by Libero IDE software and include a weak pull-up resistor. During power-up, the used I/O pins are tristated with no pull-up or pull-down resistors until I/O enable (there is a delay after voltage stabilizes, and different I/O banks power up sequentially to avoid a surge of ICCI).</p> <p>Some of these pins are also multiplexed with integrated peripherals in the MSS (Ethernet MAC and external memory controller).</p> <p>During programming, I/Os become tristated and weakly pulled up to VCCI. With the VCCI and VCC supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os are instantly configured to the desired user configuration. For more information see the SmartFusion FPGA User I/Os section in the SmartFusion FPGA Fabric User's Guide.</p> <p>The naming convention used for each FPGA user I/O is:</p> <p>IOuxwByVz where:</p> <p>u = I/O pair number in bank, starting at 00 from the northwest I/O bank and incrementing clockwise.</p> <p>x = P (positive) or N (negative) or S (single-ended) or R (regular, single-ended).</p> <p>w = D (differential pair) or P (pair) or S (single-ended) or R (regular, single-ended).</p> <p>y = Bank number starting at 0 from northwest I/O bank and incrementing clockwise.</p> <p>z = V_{REF} mini bank number.</p>

Special Function Pins

Name	Type	Polarity/Bus Size	Description
NC			No connect This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.
DC			Do not connect. This pin should not be connected to any signals on the PCB. These pins should be left unconnected.
LPXIN	In	1	Low power 32 KHz crystal oscillator. Input from the 32 KHz oscillator. Pin for connecting a low power 32 KHz watch crystal. If not used, the LPXIN pin can be left floating. For more information, see the PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators section in the SmartFusion Microcontroller Subsystem User's Guide .
LPXOUT	In	1	Low power 32 KHz crystal oscillator. Output to the 32 KHz oscillator. Pin for connecting a low power 32 KHz watch crystal. If not used, the LPXOUT pin can be left floating. For more information, see the PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators section in the SmartFusion Microcontroller Subsystem User's Guide .
MAINXIN	In	1	Main crystal oscillator circuit. Input to the crystal oscillator circuit. Pin for connecting an external crystal, ceramic resonator, or RC network. When using an external crystal or ceramic oscillator, external capacitors are also recommended. Refer to documentation from the crystal oscillator manufacturer for proper capacitor value. If using an external RC network or clock input, MAINXIN should be used and MAINXOUT left unconnected. For more information, see the PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators section in the SmartFusion Microcontroller Subsystem User's Guide .
MAINXOUT	Out	1	Main crystal oscillator circuit. Output from the crystal oscillator circuit. Pin for connecting external crystal or ceramic resonator. When using an external crystal or ceramic oscillator, external capacitors are also recommended. Refer to documentation from the crystal oscillator manufacturer for proper capacitor value. If using external RC network or clock input, MAINXIN should be used and MAINXOUT left unconnected. For more information, see the PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators section in the SmartFusion Microcontroller Subsystem User's Guide .
NCAP		1	Negative capacitor connection. This is the negative terminal of the charge pump. A capacitor, with a 2.2 μ F recommended value, is required to connect between PCAP and NCAP. Analog charge pump capacitors are not needed if none of the analog SCB features are used and none of the SDDs are used. In that case it should be left unconnected.

Name	Type	Polarity/Bus Size	Description
PCAP		1	Positive Capacitor connection. This is the positive terminal of the charge pump. A capacitor, with a 2.2 μ F recommended value, is required to connect between PCAP and NCAP. If this pin is not used, it must be left unconnected/floating. In this case, no capacitor is needed. Analog charge pump capacitors are not needed if none of the analog SCB features are used, and none of the SDDs are used.
PTBASE		1	Pass transistor base connection This is the control signal of the voltage regulator. This pin should be connected to the base of an external pass transistor used with the 1.5 V internal voltage regulator and can be floating if not used.
PTEM		1	Pass transistor emitter connection. This is the feedback input of the voltage regulator. This pin should be connected to the emitter of an external pass transistor used with the 1.5 V internal voltage regulator and can be floating if not used.
MSS_RESET_N	In	Low	Reset signal for the microcontroller subsystem.
PU_N	In	Low	Push-button is the connection for the external momentary switch used to turn on the 1.5 V voltage regulator and can be floating if not used.

JTAG Pins

SmartFusion devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the SmartFusion part must be supplied to allow JTAG signals to transition the SmartFusion device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility with supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned to be used, the V_{JTAG} pin together with the TRSTB pin could be tied to GND.

Name	Type	Polarity/ Bus Size	Description
JTAGSEL	In	1	<p>JTAG controller selection</p> <p>Depending on the state of the JTAGSEL pin, an external JTAG controller will either see the FPGA fabric TAP/auxiliary TAP (High) or the Cortex-M3 JTAG debug interface (Low).</p> <p>The JTAGSEL pin should be connected to an external pull-up resistor such that the default configuration selects the FPGA fabric TAP.</p>
TCK	In	1	<p>Test clock</p> <p>Serial input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/-down resistor. If JTAG is not used, it is recommended to tie off TCK to GND or V_{JTAG} through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.</p> <p>Note that to operate at all V_{JTAG} voltages, 500 Ω to 1 kΩ will satisfy the requirements. Refer to Table 5-1 on page 5-9 for more information.</p>
TDI	In	1	<p>Test data</p> <p>Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.</p>
TDO	Out	1	<p>Test data</p> <p>Serial output for JTAG boundary scan, ISP, and UJTAG usage.</p>
TMS		HIGH	<p>Test mode select</p> <p>The TMS pin controls the use of the IEEE1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.</p>
TRSTB		HIGH	<p>Boundary scan reset pin</p> <p>The TRST pin functions as an active low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the TAP is held in reset mode. The resistor values must be chosen from Table 5-1 on page 5-9 and must satisfy the parallel resistance value requirement. The values in Table 5-1 on page 5-9 correspond to the resistor recommended when a single device is used. The values correspond to the equivalent parallel resistor when multiple devices are connected via a JTAG chain.</p> <p>In critical applications, an upset in the JTAG circuit could allow entering an undesired JTAG state. In such cases, it is recommended that you tie off TRST to GND through a resistor placed close to the FPGA pin.</p> <p>The TRSTB pin also resets the serial wire JTAG – debug port (SWJ-DP) circuitry within the Cortex-M3.</p>

Table 5-1 • Recommended Tie-Off Values for the TCK and TRST Pins

V_{JTAG}	Tie-Off Resistance^{1, 2}
V _{JTAG} at 3.3 V	200 Ω to 1 k Ω
V _{JTAG} at 2.5 V	200 Ω to 1 k Ω
V _{JTAG} at 1.8 V	500 Ω to 1 k Ω
V _{JTAG} at 1.5 V	500 Ω to 1 k Ω

Notes:

1. The TCK pin can be pulled up/down.
2. The TRST pin can only be pulled down.
1. Equivalent parallel resistance if more than one device is on JTAG chain.

Microcontroller Subsystem (MSS)

Name	Type	Polarity/ Bus Size	Description
External Memory Controller			
EMC_ABx	Out	26	External memory controller address bus Can also be used as an FPGA user I/O (see "IO" on page 5-5).
EMC_BYTENx	Out	LOW/2	External memory controller byte enable Can also be used as an FPGA user I/O (see "IO" on page 5-5).
EMC_CLK	Out	Rise	External memory controller clock Can also be used as an FPGA user I/O (see "IO" on page 5-5).
EMC_CSx_N	Out	LOW/2	External memory controller chip selects Can also be used as an FPGA User IO (see "IO" on page 5-5).
EMC_DBx	In/out	16	External memory controller data bus Can also be used as an FPGA user I/O (see "IO" on page 5-5).
EMC_OENx_N	Out	LOW/2	External memory controller output enables Can also be used as an FPGA User IO (see "IO" on page 5-5).
EMC_RW_N	Out	Level	External memory controller read/write. Read = High, write = Low. Can also be used as an FPGA user I/O (see "IO" on page 5-5).
Inter-Integrated Circuit (I²C) Peripherals			
I2C_0_SCL	In/out	1	I ² C bus serial clock output. First I ² C. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-5).
I2C_0_SDA	In/out	1	I ² C bus serial data input/output. First I ² C. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-5).
I2C_1_SCL	In/out	1	I ² C bus serial clock output. Second I ² C. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-5).
I2C_1_SDA	In/out	1	I ² C bus serial data input/output. Second I ² C. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-5).
Serial Peripheral Interface (SPI) Controllers			
SPI_0_CLK	Out	1	Clock. First SPI. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-5).
SPI_0_DI	In	1	Data input. First SPI. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-5).
SPI_0_DO	Out	1	Data output. First SPI. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-5).
SPI_0_SS	Out	1	Slave select (chip select). First SPI. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-5).
SPI_1_CLK	Out	1	Clock. Second SPI. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-5).
SPI_1_DI	In	1	Data input. Second SPI. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-5).

Name	Type	Polarity/ Bus Size	Description
SPI_1_DO	Out	1	Data output. Second SPI. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-5).
SPI_1_SS	Out	1	Slave select (chip select). Second SPI. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-5).
Universal Asynchronous Receiver/Transmitter (UART) Peripherals			
UART_0_RXD	In	1	Receive data. First UART. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-5).
UART_0_TXD	Out	1	Transmit data. First UART. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-5).
UART_1_RXD	In	1	Receive data. Second UART. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-5).
UART_1_TXD	Out	1	Transmit data. Second UART. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-5).
Ethernet MAC			
MAC_CLK	In	Rise	Receive clock. 50 MHz \pm 50 ppm clock source received from RMII PHY.
MAC_CRSDV	In	High	Carrier sense/receive data valid for RMII PHY Can also be used as an FPGA User IO (see "IO" on page 5-5).
MAC_MDC	Out	Rise	RMII management clock Can also be used as an FPGA User IO (see "IO" on page 5-5).
MAC_MDIO	In/Out	1	RMII management data input/output Can also be used as an FPGA User IO (see "IO" on page 5-5).
MAC_RXDx	In	2	Ethernet MAC receive data. Data recovered and decoded by PHY. The RXD[0] signal is the least significant bit. Can also be used as an FPGA User I/O (see "IO" on page 5-5).
MAC_RXER	In	HIGH	Ethernet MAC receive error. If MACRX_ER is asserted during reception, the frame is received and status of the frame is updated with MACRX_ER. Can also be used as an FPGA user I/O (see "IO" on page 5-5).
MAC_TXDx	Out	2	Ethernet MAC transmit data. The TXD[0] signal is the least significant bit. Can also be used as an FPGA user I/O (see "IO" on page 5-5).
MAC_TXEN	Out	HIGH	Ethernet MAC transmit enable. When asserted, indicates valid data for the PHY on the TXD port. Can also be used as an FPGA User I/O (see "IO" on page 5-5).

Analog Front-End (AFE)

Name	Type	Description	Associated With	
			ADC/SDD	SCB
ABPS0	In	SCB 0 / active bipolar prescaler input 1. See the Active Bipolar Prescaler (ABPS) section in the SmartFusion Programmable Analog User's Guide .	ADC0	SCB0
ABPS1	In	SCB 0 / active bipolar prescaler Input 2	ADC0	SCB0
ABPS2	In	SCB 1 / active bipolar prescaler Input 1	ADC0	SCB1
ABPS3	In	SCB 1 / active bipolar prescaler Input 2	ADC0	SCB1
ABPS4	In	SCB 2 / active bipolar prescaler Input 1	ADC1	SCB2
ABPS5	In	SCB 2 / active bipolar prescaler Input 2	ADC1	SCB2
ABPS6	In	SCB 3 / active bipolar prescaler Input 1	ADC1	SCB3
ABPS7	In	SCB 3 / active bipolar prescaler input 2	ADC1	SCB3
ABPS8	In	SCB 4 / active bipolar prescaler input 1	ADC2	SCB4
ABPS9	In	SCB 4 / active bipolar prescaler input 2	ADC2	SCB4
ADC0	In	ADC 0 direct input 0 / FPGA Input.	ADC0	SCB0
ADC1	In	ADC 0 direct input 1 / FPGA input	ADC0	SCB0
ADC2	In	ADC 0 direct input 2 / FPGA input	ADC0	SCB1
ADC3	In	ADC 0 direct input 3 / FPGA input	ADC0	SCB1
ADC4	In	ADC 1 direct input 0 / FPGA input	ADC1	SCB2
ADC5	In	ADC 1 direct input 1 / FPGA input	ADC1	SCB2
ADC6	In	ADC 1 direct input 2 / FPGA input	ADC1	SCB3
ADC7	In	ADC 1 direct input 3 / FPGA input	ADC1	SCB3
ADC8	In	ADC 2 direct input 0 / FPGA input	ADC2	SCB4
ADC9	In	ADC 2 direct input 1 / FPGA input	ADC2	SCB4
ADC10	In	ADC 2 direct input 2 / FPGA input	ADC2	N/A
ADC11	In	ADC 2 direct input 3 / FPGA input	ADC2	N/A
CM0	In	SCB 0 / high side of current monitor / comparator Positive input. See the Current Monitor section in the SmartFusion Programmable Analog User's Guide .	ADC0	SCB0
CM1	In	SCB 1 / high side of current monitor / comparator. Positive input.	ADC0	SCB1
CM2	In	SCB 2 / high side of current monitor / comparator. Positive input.	ADC1	SCB2
CM3	In	SCB 3 / high side of current monitor / comparator. Positive input.	ADC1	SCB3
CM4	In	SCB 4 / high side of current monitor / comparator. Positive input.	ADC2	SCB4
TM0	In	SCB 0 / low side of current monitor / comparator Negative input / high side of temperature monitor. See the Temperature Monitor section.	ADC0	SCB0

Note: Unused analog inputs should be grounded. This aids in shielding and prevents an undesired coupling path.

Name	Type	Description	Associated With	
			ADC/SDD	SCB
TM1	In	SCB 1 / low side of current monitor / comparator. Negative input / high side of temperature monitor.	ADC0	SCB1
TM2	In	SCB 2 / low side of current monitor / comparator. Negative input / high side of temperature monitor.	ADC1	SCB2
TM3	In	SCB 3 low side of current monitor / comparator. Negative input / high side of temperature monitor.	ADC1	SCB3
TM4	In	SCB 4 low side of current monitor / comparator. Negative input / high side of temperature monitor.	ADC2	SCB4
SDD0	Out	Output of SDD0	SDD0	N/A
SDD1	Out	Output of SDD1	SDD1	N/A
SDD2	Out	Output of SDD2	SDD2	N/A

Note: Unused analog inputs should be grounded. This aids in shielding and prevents an undesired coupling path.

Analog Front-End Pin-Level Function Multiplexing

Table 5-2 describes the relationships between the various internal signals found in the analog front-end (AFE) and how they are multiplexed onto the external package pins. Note that, in general, only one function is available for those pads that have numerous functions listed. The exclusion to this rule is when a comparator is used; the ADC can still convert either input side of the comparator.

Table 5-2 • Relationships Between Signals in the Analog Front-End

Pin	ADC Channel	Dir.-In Option	Prescaler	Current Mon.	Temp. Mon.	Compar.	LVTTTL	SDD MUX	SDD
ABPS0	ADC0_CH1		ABPS0_IN						
ABPS1	ADC0_CH2		ABPS1_IN						
ABPS2	ADC0_CH5		ABPS2_IN						
ABPS3	ADC0_CH6		ABPS3_IN						
ABPS4	ADC1_CH1		ABPS4_IN						
ABPS5	ADC1_CH2		ABPS5_IN						
ABPS6	ADC1_CH5		ABPS6_IN						
ABPS7	ADC1_CH6		ABPS7_IN						
ABPS8	ADC2_CH1		ABPS8_IN						
ABPS9	ADC2_CH2		ABPS9_IN						
ADC0	ADC0_CH9	Yes				CMP1_P	LVTTTL0_IN		
ADC1	ADC0_CH10	Yes				CMP1_N	LVTTTL1_IN	SDDM0_OUT	
ADC2	ADC0_CH11	Yes				CMP3_P	LVTTTL2_IN		
ADC3	ADC0_CH12	Yes				CMP3_N	LVTTTL3_IN	SDDM1_OUT	
ADC4	ADC1_CH9	Yes				CMP5_P	LVTTTL4_IN		
ADC5	ADC1_CH10	Yes				CMP5_N	LVTTTL5_IN	SDDM2_OUT	
ADC6	ADC1_CH11	Yes				CMP7_P	LVTTTL6_IN		
ADC7	ADC1_CH12	Yes				CMP7_N	LVTTTL7_IN	SDDM3_OUT	
ADC8	ADC2_CH9	Yes				CMP9_P	LVTTTL8_IN		
ADC9	ADC2_CH10	Yes				CMP9_N	LVTTTL9_IN	SDDM4_OUT	
ADC10	ADC2_CH11	Yes					LVTTTL10_IN		
ADC11	ADC2_CH12	Yes					LVTTTL11_IN		
CM0	ADC0_CH3	Yes		CM0_H		CMP0_P			
CM1	ADC0_CH7	Yes		CM1_H		CMP2_P			
CM2	ADC1_CH3	Yes		CM2_H		CMP4_P			
CM3	ADC1_CH7	Yes		CM3_H		CMP6_P			
CM4	ADC2_CH3	Yes		CM4_H		CMP8_P			
SDD0	ADC0_CH15								SDD0_OUT
SDD1	ADC1_CH15								SDD1_OUT

Notes:

1. ABPSx_IN: Input to active bipolar prescaler channel x.
2. CMx_H/L: Current monitor channel x, high/low side.
3. TMx_IO: Temperature monitor channel x.
4. CMPx_P/N: Comparator channel x, positive/negative input.
5. LVTTTLx_IN: LVTTTL I/O channel x.
6. SDDMx_OUT: Output from sigma-delta DAC MUX channel x.
7. SDDx_OUT: Direct output from sigma-delta DAC channel x.

Table 5-2 • Relationships Between Signals in the Analog Front-End

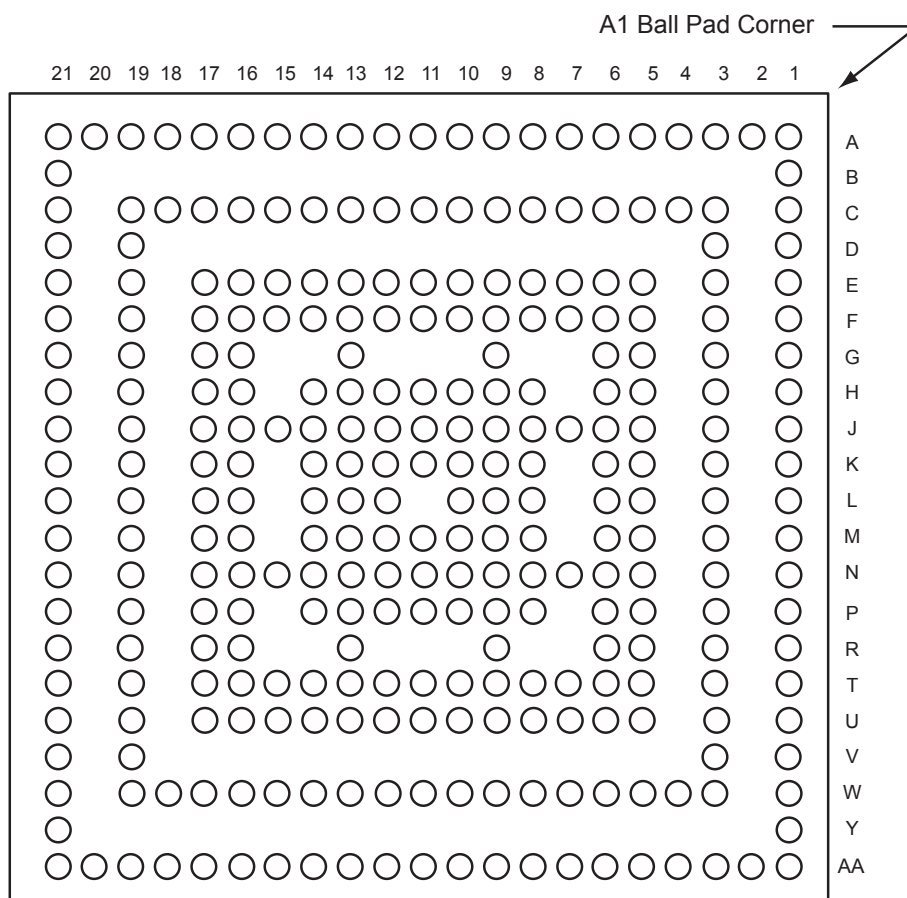
Pin	ADC Channel	Dir.-In Option	Prescaler	Current Mon.	Temp. Mon.	Compar.	LVTTTL	SDD MUX	SDD
SDD2	ADC2_CH15								SDD2_OUT
TM0	ADC0_CH4	Yes		CM0_L	TM0_IO	CMP0_N			
TM1	ADC0_CH8	Yes		CM1_L	TM1_IO	CMP2_N			
TM2	ADC1_CH4	Yes		CM2_L	TM2_IO	CMP4_N			
TM3	ADC1_CH8	Yes		CM3_L	TM3_IO	CMP6_N			
TM4	ADC2_CH4	Yes		CM4_L	TM4_IO	CMP8_N			

Notes:

1. *ABPSx_IN*: Input to active bipolar prescaler channel *x*.
2. *CMx_H/L*: Current monitor channel *x*, high/low side.
3. *TMx_IO*: Temperature monitor channel *x*.
4. *CMPx_P/N*: Comparator channel *x*, positive/negative input.
5. *LVTTTLx_IN*: LVTTTL I/O channel *x*.
6. *SDDMx_OUT*: Output from sigma-delta DAC MUX channel *x*.
7. *SDDx_OUT*: Direct output from sigma-delta DAC channel *x*.

Pin Assignment Tables

288-Pin CSP



Note: Bottom view

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.actel.com/products/solutions/package/docs.aspx>.

Pin Number	288-Pin CSP	
	A2F200 Function	A2F500 Function
A1	VCCFPGAIOB0	VCCFPGAIOB0
A2	GNDQ	GNDQ
A3	EMC_CLK/GAA0/IO00NDB0V0	EMC_CLK/GAA0/IO02NDB0V0
A4	EMC_RW_N/GAA1/IO00PDB0V0	EMC_RW_N/GAA1/IO02PDB0V0
A5	GND	GND
A6	EMC_CS1_N/GAB1/IO01PDB0V0	EMC_CS1_N/GAB1/IO05PDB0V0
A7	EMC_CS0_N/GAB0/IO01NDB0V0	EMC_CS0_N/GAB0/IO05NDB0V0
A8	EMC_AB[0]/IO04NPB0V0	EMC_AB[0]/IO06NPB0V0
A9	VCCFPGAIOB0	VCCFPGAIOB0
A10	EMC_AB[4]/IO06NDB0V0	EMC_AB[4]/IO10NDB0V0
A11	EMC_AB[8]/IO08NPB0V0	EMC_AB[8]/IO13NPB0V0
A12	EMC_AB[14]/IO11NPB0V0	EMC_AB[14]/IO15NPB0V0
A13	GND	GND
A14	EMC_AB[18]/IO13NDB0V0	EMC_AB[18]/IO18NDB0V0
A15	EMC_AB[24]/IO16NDB0V0	EMC_AB[24]/IO20NDB0V0
A16	EMC_AB[25]/IO16PDB0V0	EMC_AB[25]/IO20PDB0V0
A17	VCCFPGAIOB0	VCCFPGAIOB0
A18	EMC_AB[20]/IO14NDB0V0	EMC_AB[20]/IO21NDB0V0
A19	EMC_AB[21]/IO14PDB0V0	EMC_AB[21]/IO21PDB0V0
A20	GNDQ	GNDQ
A21	GND	GND
AA1	ABPS1	ABPS1
AA2	GNDQA	GNDQA
AA3	GND	GND
AA4	VCC33N	VCC33N
AA5	SDD0	SDD0
AA6	ABPS0	ABPS0
AA7	GNDTM0	GNDTM0
AA8	ABPS2	ABPS2
AA9	VAREF0	VAREF0
AA10	GND15ADC0	GND15ADC0
AA11	ADC6	ADC6
AA12	ABPS7	ABPS7
AA13	TM2	TM2
AA14	ABPS4	ABPS4
AA15	SDD1	SDD1

Note: Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.

Pin Number	288-Pin CSP	
	A2F200 Function	A2F500 Function
AA16	GNDVAREF	GNDVAREF
AA17	VAREFOUT	VAREFOUT
AA18	PU_N	PU_N
AA19	VCC33A	VCC33A
AA20	PTEM	PTEM
AA21	GND	GND
B1	GND	GND
B21	GBB2/IO20NDB1V0	GBB2/IO27NDB1V0
C1	EMC_DB[15]/GAA2/IO71PDB5V0	EMC_DB[15]/GAA2/IO88PDB5V0
C3	VCOMPLA	VCOMPLA0
C4	VCCPLL	VCCPLL0
C5	VCCFPGAIOB0	VCCFPGAIOB0
C6	EMC_AB[1]/IO04PPB0V0	EMC_AB[1]/IO06PPB0V0
C7	GND	GND
C8	EMC_OEN0_N/IO03NDB0V0	EMC_OEN0_N/IO08NDB0V0
C9	EMC_AB[2]/IO05NDB0V0	EMC_AB[2]/IO09NDB0V0
C10	EMC_AB[5]/IO06PDB0V0	EMC_AB[5]/IO10PDB0V0
C11	VCCFPGAIOB0	VCCFPGAIOB0
C12	EMC_AB[9]/IO08PPB0V0	EMC_AB[9]/IO13PPB0V0
C13	EMC_AB[15]/IO11PPB0V0	EMC_AB[15]/IO15PPB0V0
C14	EMC_AB[19]/IO13PDB0V0	EMC_AB[19]/IO18PDB0V0
C15	GND	GND
C16	EMC_AB[22]/IO15NDB0V0	EMC_AB[22]/IO19NDB0V0
C17	EMC_AB[23]/IO15PDB0V0	EMC_AB[23]/IO19PDB0V0
C18	NC	VCCPLL1
C19	NC	VCOMPLA1
C21	GBA2/IO20PDB1V0	GBA2/IO27PDB1V0
D1	EMC_DB[14]/GAB2/IO71NDB5V0	EMC_DB[14]/GAB2/IO88NDB5V0
D3	VCCFPGAIOB5	VCCFPGAIOB5
D19	GND	GND
D21	VCCFPGAIOB1	VCCFPGAIOB1
E1	EMC_DB[13]/GAC2/IO70PDB5V0	EMC_DB[13]/GAC2/IO87PDB5V0
E3	EMC_DB[12]/IO70NDB5V0	EMC_DB[12]/IO87NDB5V0
E5	GNDQ	GNDQ
E6	EMC_BYTEN[0]/GAC0/IO02NDB0V0	EMC_BYTEN[0]/GAC0/IO07NDB0V0
E7	EMC_BYTEN[1]/GAC1/IO02PDB0V0	EMC_BYTEN[1]/GAC1/IO07PDB0V0

Note: Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.

Pin Number	288-Pin CSP	
	A2F200 Function	A2F500 Function
E8	EMC_OEN1_N/IO03PDB0V0	EMC_OEN1_N/IO08PDB0V0
E9	EMC_AB[3]/IO05PDB0V0	EMC_AB[3]/IO09PDB0V0
E10	EMC_AB[10]/IO09NDB0V0	EMC_AB[10]/IO11NDB0V0
E11	EMC_AB[7]/IO07PDB0V0	EMC_AB[7]/IO12PDB0V0
E12	EMC_AB[13]/IO10PDB0V0	EMC_AB[13]/IO14PDB0V0
E13	EMC_AB[16]/IO12NDB0V0	EMC_AB[16]/IO17NDB0V0
E14	EMC_AB[17]/IO12PDB0V0	EMC_AB[17]/IO17PDB0V0
E15	GCB0/IO27NDB1V0	GCB0/IO34NDB1V0
E16	GCB1/IO27PDB1V0	GCB1/IO34PDB1V0
E17	GCB2/IO24PDB1V0	GCB2/IO33PDB1V0
E19	GCA0/IO28NDB1V0	GCA0/IO36NDB1V0
E21	GCA1/IO28PDB1V0	GCA1/IO36PDB1V0
F1	VCCFPGAIOB5	VCCFPGAIOB5
F3	GFB2/IO68NDB5V0	GFB2/IO85NDB5V0
F5	GFA2/IO68PDB5V0	GFA2/IO85PDB5V0
F6	EMC_DB[11]/IO69PDB5V0	EMC_DB[11]/IO86PDB5V0
F7	GND	GND
F8	GFC1/IO66PPB5V0	GFC1/IO83PPB5V0
F9	VCCFPGAIOB0	VCCFPGAIOB0
F10	EMC_AB[11]/IO09PDB0V0	EMC_AB[11]/IO11PDB0V0
F11	EMC_AB[6]/IO07NDB0V0	EMC_AB[6]/IO12NDB0V0
F12	EMC_AB[12]/IO10NDB0V0	EMC_AB[12]/IO14NDB0V0
F13	GND	GND
F14	GCC1/IO26PPB1V0	GCC1/IO35PPB1V0
F15	GNDQ	GNDQ
F16	VCCFPGAIOB1	VCCFPGAIOB1
F17	IO24NDB1V0	IO33NDB1V0
F19	GDB1/IO30PDB1V0	GDB1/IO39PDB1V0
F21	GDB0/IO30NDB1V0	GDB0/IO39NDB1V0
G1	IO67NDB5V0	IO84NDB5V0
G3	GFC2/IO67PDB5V0	GFC2/IO84PDB5V0
G5	GFB1/IO65PDB5V0	GFB1/IO82PDB5V0
G6	EMC_DB[10]/IO69NDB5V0	EMC_DB[10]/IO86NDB5V0
G9	GFC0/IO66NPB5V0	GFC0/IO83NPB5V0
G13	GCC0/IO26NPB1V0	GCC0/IO35NPB1V0
G16	GDA0/IO31NDB1V0	GDA0/IO40NDB1V0

Note: Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.

Pin Number	288-Pin CSP	
	A2F200 Function	A2F500 Function
G17	GDC1/IO29PDB1V0	GDC1/IO38PDB1V0
G19	GDC0/IO29NDB1V0	GDC0/IO38NDB1V0
G21	GND	GND
H1	EMC_DB[9]/GEC1/IO63PPB5V0	EMC_DB[9]/GEC1/IO80PPB5V0
H3	GND	GND
H5	GFB0/IO65NDB5V0	GFB0/IO82NDB5V0
H6	EMC_DB[7]/GEB1/IO62PDB5V0	EMC_DB[7]/GEB1/IO79PDB5V0
H8	GND	GND
H9	VCC	VCC
H10	GND	GND
H11	VCC	VCC
H12	GND	GND
H13	VCC	VCC
H14	GND	GND
H16	GDA1/IO31PDB1V0	GDA1/IO40PDB1V0
H17	GDC2/IO32PPB1V0	GDC2/IO41PPB1V0
H19	VCCFPGAIOB1	VCCFPGAIOB1
H21	GDB2/IO33PDB1V0	GDB2/IO42PDB1V0
J1	EMC_DB[4]/GEA0/IO61NPB5V0	EMC_DB[4]/GEA0/IO78NPB5V0
J3	EMC_DB[8]/GEC0/IO63NPB5V0	EMC_DB[8]/GEC0/IO80NPB5V0
J5	EMC_DB[1]/GEB2/IO59PDB5V0	EMC_DB[1]/GEB2/IO76PDB5V0
J6	EMC_DB[6]/GEB0/IO62NDB5V0	EMC_DB[6]/GEB0/IO79NDB5V0
J7	VCCFPGAIOB5	VCCFPGAIOB5
J8	VCC	VCC
J9	GND	GND
J10	VCC	VCC
J11	GND	GND
J12	VCC	VCC
J13	GND	GND
J14	VCC	VCC
J15	VPP	VPP
J16	IO32NPB1V0	IO41NPB1V0
J17	GNDQ	GNDQ
J19	VCCMAINXTAL	VCCMAINXTAL
J21	GDA2/IO33NDB1V0	GDA2/IO42NDB1V0
K1	GND	GND

Note: Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.

Pin Number	288-Pin CSP	
	A2F200 Function	A2F500 Function
K3	EMC_DB[5]/GEA1/IO61PPB5V0	EMC_DB[5]/GEA1/IO78PPB5V0
K5	EMC_DB[0]/GEA2/IO59NDB5V0	EMC_DB[0]/GEA2/IO76NDB5V0
K6	EMC_DB[3]/GEC2/IO60PPB5V0	EMC_DB[3]/GEC2/IO77PPB5V0
K8	GND	GND
K9	VCC	VCC
K10	GND	GND
K11	VCC	VCC
K12	GND	GND
K13	VCC	VCC
K14	GND	GND
K16	LPXOUT	LPXOUT
K17	GNDLPXTAL	GNDLPXTAL
K19	GNDMAINXTAL	GNDMAINXTAL
K21	MAINXIN	MAINXIN
L1	GNDRCOSC	GNDRCOSC
L3	VCCFPGAIOB5	VCCFPGAIOB5
L5	EMC_DB[2]/IO60NPB5V0	EMC_DB[2]/IO77NPB5V0
L6	GNDQ	GNDQ
L8	VCC	VCC
L9	GND	GND
L10	VCC	VCC
L12	VCC	VCC
L13	GND	GND
L14	VCC	VCC
L16	VCCLPXTAL	VCCLPXTAL
L17	VDDBAT	VDDBAT
L19	LPXIN	LPXIN
L21	MAINXOUT	MAINXOUT
M1	VCCRCOSC	VCCRCOSC
M3	MSS_RESET_N	MSS_RESET_N
M5	GPIO_5/IO42RSB4V0	GPIO_5/IO51RSB4V0
M6	GND	GND
M8	GND	GND
M9	VCC	VCC
M10	GND	GND
M11	VCC	VCC

Note: Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.

Pin Number	288-Pin CSP	
	A2F200 Function	A2F500 Function
M12	GND	GND
M13	VCC	VCC
M14	GND	GND
M16	TMS	TMS
M17	VJTAG	VJTAG
M19	TDO	TDO
M21	TRSTB	TRSTB
N1	VCCMSSIOB4	VCCMSSIOB4
N3	GND	GND
N5	GPIO_4/IO43RSB4V0	GPIO_4/IO52RSB4V0
N6	GPIO_8/IO39RSB4V0	GPIO_8/IO48RSB4V0
N7	GPIO_9/IO38RSB4V0	GPIO_9/IO47RSB4V0
N8	VCC	VCC
N9	GND	GND
N10	VCC	VCC
N11	GND	GND
N12	VCC	VCC
N13	GND	GND
N14	VCC	VCC
N15	GND	GND
N16	TCK	TCK
N17	TDI	TDI
N19	GNDENV	GNDENV
N21	VCCENV	VCCENV
P1	MAC_MDC/IO48RSB4V0	MAC_MDC/IO57RSB4V0
P3	GPIO_7/IO40RSB4V0	GPIO_7/IO49RSB4V0
P5	GPIO_6/IO41RSB4V0	GPIO_6/IO50RSB4V0
P6	VCCMSSIOB4	VCCMSSIOB4
P8	GND	GND
P9	VCC	VCC
P10	GND	GND
P11	VCC	VCC
P12	GND	GND
P13	VCC	VCC
P14	GND	GND
P16	JTAGSEL	JTAGSEL

Note: Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.

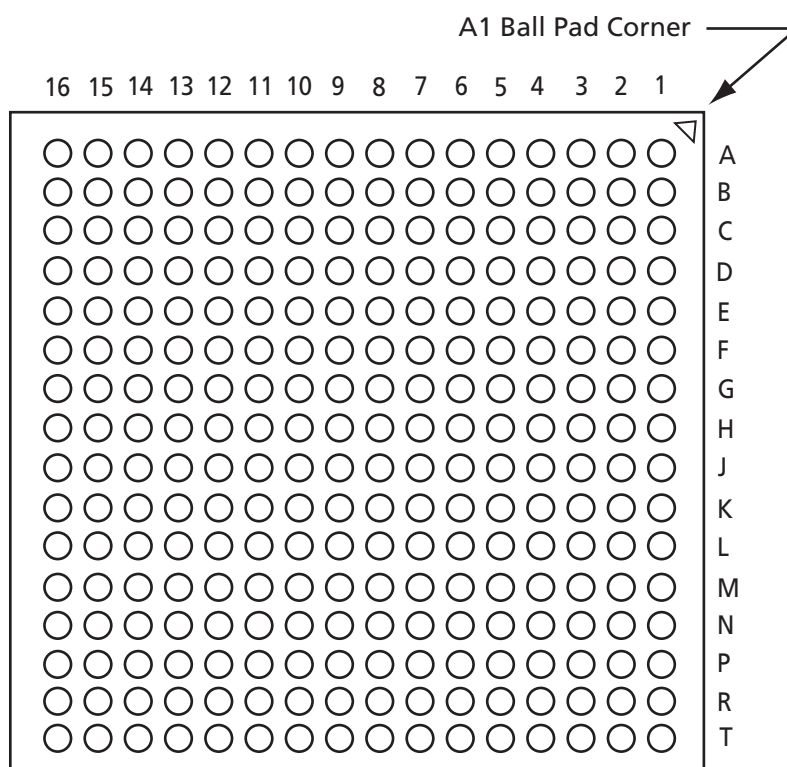
Pin Number	288-Pin CSP	
	A2F200 Function	A2F500 Function
P17	I2C_0_SCL/GPIO_23	I2C_0_SCL/GPIO_23
P19	VCCMSSIOB2	VCCMSSIOB2
P21	GND	GND
R1	MAC_MDIO/IO49RSB4V0	MAC_MDIO/IO58RSB4V0
R3	MAC_TXEN/IO52RSB4V0	MAC_TXEN/IO61RSB4V0
R5	MAC_TXD[0]/IO56RSB4V0	MAC_TXD[0]/IO65RSB4V0
R6	MAC_CRSDV/IO51RSB4V0	MAC_CRSDV/IO60RSB4V0
R9	GNDA	GNDA
R13	GNDA	GNDA
R16	UART_1_RXD/GPIO_29	UART_1_RXD/GPIO_29
R17	UART_1_TXD/GPIO_28	UART_1_TXD/GPIO_28
R19	I2C_0_SDA/GPIO_22	I2C_0_SDA/GPIO_22
R21	I2C_1_SDA/GPIO_30	I2C_1_SDA/GPIO_30
T1	GND	GND
T3	MAC_TXD[1]/IO55RSB4V0	MAC_TXD[1]/IO64RSB4V0
T5	MAC_RXD[1]/IO53RSB4V0	MAC_RXD[1]/IO62RSB4V0
T6	MAC_RXER/IO50RSB4V0	MAC_RXER/IO59RSB4V0
T7	CM1	CM1
T8	ADC1	ADC1
T9	GND33ADC0	GND33ADC0
T10	VCC15ADC0	VCC15ADC0
T11	GND33ADC1	GND33ADC1
T12	VAREF1	VAREF1
T13	ADC4	ADC4
T14	TM3	TM3
T15	SPI_1_SS/GPIO_27	SPI_1_SS/GPIO_27
T16	VCCMSSIOB2	VCCMSSIOB2
T17	UART_0_RXD/GPIO_21	UART_0_RXD/GPIO_21
T19	UART_0_TXD/GPIO_20	UART_0_TXD/GPIO_20
T21	I2C_1_SCL/GPIO_31	I2C_1_SCL/GPIO_31
U1	MAC_RXD[0]/IO54RSB4V0	MAC_RXD[0]/IO63RSB4V0
U3	VCCMSSIOB4	VCCMSSIOB4
U5	VCC33SDD0	VCC33SDD0
U6	VCC15A	VCC15A
U7	ABPS3	ABPS3
U8	ADC2	ADC2

Note: Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.

Pin Number	288-Pin CSP	
	A2F200 Function	A2F500 Function
U9	VCC33ADC0	VCC33ADC0
U10	GND15ADC1	GND15ADC1
U11	VCC33ADC1	VCC33ADC1
U12	ADC7	ADC7
U13	ABPS6	ABPS6
U14	GNDTM1	GNDTM1
U15	SPI_1_CLK/GPIO_26	SPI_1_CLK/GPIO_26
U16	SPI_0_CLK/GPIO_18	SPI_0_CLK/GPIO_18
U17	SPI_0_SS/GPIO_19	SPI_0_SS/GPIO_19
U19	GND	GND
U21	SPI_1_DO/GPIO_24	SPI_1_DO/GPIO_24
V1	MAC_CLK	MAC_CLK
V3	GNDSDD0	GNDSDD0
V19	SPI_1_DI/GPIO_25	SPI_1_DI/GPIO_25
V21	VCCMSSIOB2	VCCMSSIOB2
W1	PCAP	PCAP
W3	NCAP	NCAP
W4	CM0	CM0
W5	TM0	TM0
W6	TM1	TM1
W7	ADC0	ADC0
W8	ADC3	ADC3
W9	GND33ADC0	GND33ADC0
W10	VCC15ADC1	VCC15ADC1
W11	GND33ADC1	GND33ADC1
W12	ADC5	ADC5
W13	CM3	CM3
W14	CM2	CM2
W15	ABPS5	ABPS5
W16	GND AQ	GND AQ
W17	VCC33SDD1	VCC33SDD1
W18	GNDSDD1	GNDSDD1
W19	PTBASE	PTBASE
W21	SPI_0_DI/GPIO_17	SPI_0_DI/GPIO_17
Y1	VCC33AP	VCC33AP
Y21	SPI_0_DO/GPIO_16	SPI_0_DO/GPIO_16

Note: Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.

256-Pin FBGA



Note

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Pin Number	256-Pin FBGA		
	A2F200 Function	A2F500 Function	Handling When Unused
A1	GND	GND	
A2	VCCFPGAIOB0	VCCFPGAIOB0	Can be grounded if I/O Bank0 is unused.
A3	EMC_AB[0]/IO04NDB0V0	EMC_AB[0]/IO06NDB0V0	
A4	EMC_AB[1]/IO04PDB0V0	EMC_AB[1]/IO06PDB0V0	
A5	GND	GND	
A6	EMC_AB[3]/IO05PDB0V0	EMC_AB[3]/IO09PDB0V0	
A7	EMC_AB[5]/IO06PDB0V0	EMC_AB[5]/IO10PDB0V0	
A8	VCCFPGAIOB0	VCCFPGAIOB0	Can be grounded if I/O Bank0 is unused.
A9	GND	GND	
A10	EMC_AB[14]/IO11NDB0V0	EMC_AB[14]/IO15NDB0V0	
A11	EMC_AB[15]/IO11PDB0V0	EMC_AB[15]/IO15PDB0V0	
A12	GND	GND	
A13	EMC_AB[20]/IO14NDB0V0	EMC_AB[20]/IO21NDB0V0	
A14	EMC_AB[24]/IO16NDB0V0	EMC_AB[24]/IO20NDB0V0	
A15	VCCFPGAIOB0	VCCFPGAIOB0	Can be grounded if I/O Bank0 is unused.
A16	GND	GND	
B1	EMC_DB[15]/GAA2/IO71PDB5V0	EMC_DB[15]/GAA2/IO88PDB5V0	
B2	GND	GND	
B3	EMC_BYTEN[1]/GAC1/IO02PDB0V0	EMC_BYTEN[1]/GAC1/IO07PDB0V0	
B4	EMC_OEN0_N/IO03NDB0V0	EMC_OEN0_N/IO08NDB0V0	
B5	EMC_OEN1_N/IO03PDB0V0	EMC_OEN1_N/IO08PDB0V0	
B6	EMC_AB[2]/IO05NDB0V0	EMC_AB[2]/IO09NDB0V0	
B7	EMC_AB[4]/IO06NDB0V0	EMC_AB[4]/IO10NDB0V0	
B8	EMC_AB[9]/IO08PDB0V0	EMC_AB[9]/IO13PDB0V0	
B9	EMC_AB[12]/IO10NDB0V0	EMC_AB[12]/IO14NDB0V0	
B10	EMC_AB[13]/IO10PDB0V0	EMC_AB[13]/IO14PDB0V0	
B11	EMC_AB[16]/IO12NDB0V0	EMC_AB[16]/IO17NDB0V0	
B12	EMC_AB[18]/IO13NDB0V0	EMC_AB[18]/IO18NDB0V0	
B13	EMC_AB[21]/IO14PDB0V0	EMC_AB[21]/IO21PDB0V0	
B14	EMC_AB[25]/IO16PDB0V0	EMC_AB[25]/IO20PDB0V0	
B15	GND	GND	
B16	GNDQ	GNDQ	

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Pin Number	256-Pin FBGA		
	A2F200 Function	A2F500 Function	Handling When Unused
C1	EMC_DB[14]/GAB2/IO71NDB0V0	EMC_DB[14]/GAB2/IO88NDB0V0	
C2	VCCPLL	VCCPLL0	Always power this pin.
C3	EMC_BYTEN[0]/GAC0/IO02NDB0V0	EMC_BYTEN[0]/GAC0/IO07NDB0V0	
C4	VCCFPGAIOB0	VCCFPGAIOB0	Can be grounded if I/O Bank0 is unused.
C5	EMC_CS0_N/GAB0/IO01NDB0V0	EMC_CS0_N/GAB0/IO05NDB0V0	
C6	EMC_CS1_N/GAB1/IO01PDB0V0	EMC_CS1_N/GAB1/IO05PDB0V0	
C7	GND	GND	
C8	EMC_AB[8]/IO08NDB0V0	EMC_AB[8]/IO13NDB0V0	
C9	EMC_AB[11]/IO09PDB0V0	EMC_AB[11]/IO11PDB0V0	
C10	VCCFPGAIOB0	VCCFPGAIOB0	Can be grounded if I/O Bank0 is unused.
C11	EMC_AB[17]/IO12PDB0V0	EMC_AB[17]/IO17PDB0V0	
C12	EMC_AB[19]/IO13PDB0V0	EMC_AB[19]/IO18PDB0V0	
C13	GND	GND	
C14	GBA2/IO20PPB1V0	GBA2/IO27PPB1V0	
C15	GCA2/IO23PDB1V0	GCA2/IO28PDB1V0	
C16	IO23NDB1V0	IO28NDB1V0	
D1	VCCFPGAIOB5	VCCFPGAIOB5	Can be grounded if I/O Bank5 is unused.
D2	VCOMPLA	VCOMPLA0	Always ground this pin.
D3	GND	GND	
D4	GNDQ	GNDQ	
D5	EMC_CLK/GAA0/IO00NDB0V0	EMC_CLK/GAA0/IO02NDB0V0	
D6	EMC_RW_N/GAA1/IO00PDB0V0	EMC_RW_N/GAA1/IO02PDB0V0	
D7	EMC_AB[6]/IO07NDB0V0	EMC_AB[6]/IO12NDB0V0	
D8	EMC_AB[7]/IO07PDB0V0	EMC_AB[7]/IO12PDB0V0	
D9	EMC_AB[10]/IO09NDB0V0	EMC_AB[10]/IO11NDB0V0	
D10	EMC_AB[22]/IO15NDB0V0	EMC_AB[22]/IO19NDB0V0	
D11	EMC_AB[23]/IO15PDB0V0	EMC_AB[23]/IO19PDB0V0	
D12	GNDQ	GNDQ	
D13	GBB2/IO20NPB1V0	GBB2/IO27NPB1V0	
D14	GCB2/IO24PDB1V0	GCB2/IO33PDB1V0	
D15	IO24NDB1V0	IO33NDB1V0	

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Pin Number	256-Pin FBGA		
	A2F200 Function	A2F500 Function	Handling When Unused
D16	VCCFPGAIOB1	VCCFPGAIOB1	Can be grounded if I/O Bank1 is unused.
E1	EMC_DB[13]/GAC2/IO70PDB5V0	EMC_DB[13]/GAC2/IO87PDB5V0	
E2	EMC_DB[12]/IO70NDB5V0	EMC_DB[12]/IO87NDB5V0	
E3	GFA2/IO68PDB5V0	GFA2/IO85PDB5V0	
E4	EMC_DB[10]/IO69NPB5V0	EMC_DB[10]/IO86NPB5V0	
E5	GNDQ	GNDQ	
E6	GND	GND	
E7	VCCFPGAIOB0	VCCFPGAIOB0	Can be grounded if I/O Bank0 is unused.
E8	GND	GND	
E9	VCCFPGAIOB0	VCCFPGAIOB0	Can be grounded if I/O Bank0 is unused.
E10	GND	GND	
E11	VCCFPGAIOB0	VCCFPGAIOB0	Can be grounded if I/O Bank0 is unused.
E12	GCA1/IO28PDB1V0	GCA1/IO36PDB1V0	
E13	VCCFPGAIOB1	VCCFPGAIOB1	Can be grounded if I/O Bank1 is unused.
E14	GCB1/IO27PDB1V0	GCB1/IO34PDB1V0	
E15	GDC1/IO29PDB1V0	GDC1/IO38PDB1V0	
E16	GDC0/IO29NDB1V0	GDC0/IO38NDB1V0	
F1	EMC_DB[9]/GEC1/IO63PDB5V0	EMC_DB[9]/GEC1/IO80PDB5V0	
F2	GND	GND	
F3	GFB2/IO68NDB5V0	GFB2/IO85NDB5V0	
F4	VCCFPGAIOB5	VCCFPGAIOB5	Can be grounded if I/O Bank5 is unused.
F5	EMC_DB[11]/IO69PPB5V0	EMC_DB[11]/IO86PPB5V0	
F6	VCCFPGAIOB5	VCCFPGAIOB5	Can be grounded if I/O Bank5 is unused.
F7	GND	GND	
F8	VCC	VCC	
F9	GND	GND	
F10	VCC	VCC	
F11	GND	GND	
F12	GCA0/IO28NDB1V0	GCA0/IO36NDB1V0	

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Pin Number	256-Pin FBGA		
	A2F200 Function	A2F500 Function	Handling When Unused
F13	GNDQ	GNDQ	
F14	GCB0/IO27NDB1V0	GCB0/IO34NDB1V0	
F15	GND	GND	
F16	VCCENV	VCCENV	Must be powered all the time.
G1	EMC_DB[8]/GEC0/IO63NDB5V0	EMC_DB[8]/GEC0/IO80NDB5V0	
G2	EMC_DB[7]/GEB1/IO62PDB5V0	EMC_DB[7]/GEB1/IO79PDB5V0	
G3	EMC_DB[6]/GEB0/IO62NDB5V0	EMC_DB[6]/GEB0/IO79NDB5V0	
G4	GFC2/IO67PDB5V0	GFC2/IO84PDB5V0	
G5	IO67NDB5V0	IO84NDB5V0	
G6	GND	GND	
G7	VCC	VCC	
G8	GND	GND	
G9	VCC	VCC	
G10	GND	GND	
G11	VCCFPGAIOB1	VCCFPGAIOB1	Can be grounded if I/O Bank1 is unused.
G12	VPP	VPP	
G13	TRSTB	TRSTB	Can be left floating as it has internal pull-down.
G14	TMS	TMS	Can be left floating.
G15	TCK	TCK	Can be left floating.
G16	GNDENV	GNDENV	
H1	GND	GND	
H2	EMC_DB[5]/GEA1/IO61PPB5V0	EMC_DB[5]/GEA1/IO78PPB5V0	
H3	VCCFPGAIOB5	VCCFPGAIOB5	Can be grounded if I/O Bank5 is unused.
H4	EMC_DB[1]/GEB2/IO59PDB5V0	EMC_DB[1]/GEB2/IO76PDB5V0	
H5	EMC_DB[0]/GEA2/IO59NDB5V0	EMC_DB[0]/GEA2/IO76NDB5V0	
H6	VCCFPGAIOB5	VCCFPGAIOB5	Can be grounded if I/O Bank5 is unused.
H7	GND	GND	
H8	VCC	VCC	
H9	GND	GND	
H10	VCC	VCC	
H11	GND	GND	

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Pin Number	256-Pin FBGA		
	A2F200 Function	A2F500 Function	Handling When Unused
H12	VJTAG	VJTAG	
H13	TDO	TDO	Can be left floating.
H14	TDI	TDI	Can be left floating.
H15	JTAGSEL	JTAGSEL	Can be left floating as internal pull-up is there.
H16	GND	GND	
J1	EMC_DB[4]/GEA0/IO61NPB5V0	EMC_DB[4]/GEA0/IO78NPB5V0	
J2	EMC_DB[3]/GEC2/IO60PDB5V0	EMC_DB[3]/GEC2/IO77PDB5V0	
J3	EMC_DB[2]/IO60NDB5V0	EMC_DB[2]/IO77NDB5V0	
J4	GNDRCOS	GNDRCOS	
J5	GNDQ	GNDQ	
J6	GND	GND	
J7	VCC	VCC	
J8	GND	GND	
J9	VCC	VCC	
J10	GND	GND	
J11	VCCMSSIOB2	VCCMSSIOB2	Can be grounded if I/O Bank2 is unused.
J12	I2C_0_SCL/GPIO_23	I2C_0_SCL/GPIO_23	
J13	I2C_0_SDA/GPIO_22	I2C_0_SDA/GPIO_22	
J14	I2C_1_SCL/GPIO_31	I2C_1_SCL/GPIO_31	
J15	VCCMSSIOB2	VCCMSSIOB2	Can be grounded if I/O Bank2 is unused.
J16	I2C_1_SDA/GPIO_30	I2C_1_SDA/GPIO_30	
K1	MAC_MDIO/IO49RSB4V0	MAC_MDIO/IO58RSB4V0	
K2	MAC_MDC/IO48RSB4V0	MAC_MDC/IO57RSB4V0	
K3	VCCMSSIOB4	VCCMSSIOB4	Can be grounded if I/O Bank4 is unused.
K4	MSS_RESET_N	MSS_RESET_N	Can be left floating as internal pull-up is there.
K5	VCCRCOSC	VCCRCOSC	Must be powered all the time.
K6	VCCMSSIOB4	VCCMSSIOB4	Can be grounded if I/O Bank4 is unused.
K7	GND	GND	
K8	VCC	VCC	
K9	GND	GND	

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Pin Number	256-Pin FBGA		
	A2F200 Function	A2F500 Function	Handling When Unused
K10	VCC	VCC	
K11	GND	GND	
K12	UART_0_RXD/GPIO_21	UART_0_RXD/GPIO_21	
K13	GND	GND	
K14	UART_1_TXD/GPIO_28	UART_1_TXD/GPIO_28	
K15	UART_1_RXD/GPIO_29	UART_1_RXD/GPIO_29	
K16	UART_0_TXD/GPIO_20	UART_0_TXD/GPIO_20	
L1	GND	GND	
L2	MAC_TXEN/IO52RSB4V0	MAC_TXEN/IO61RSB4V0	
L3	MAC_CRSDV/IO51RSB4V0	MAC_CRSDV/IO60RSB4V0	
L4	MAC_RXER/IO50RSB4V0	MAC_RXER/IO59RSB4V0	
L5	MAC_CLK	MAC_CLK	Can be left floating.
L6	GND	GND	
L7	VCC	VCC	
L8	GND	GND	
L9	VCC	VCC	
L10	GND	GND	
L11	VCCMSSIOB2	VCCMSSIOB2	Can be grounded if I/O Bank2 is unused.
L12	SPI_1_DO/GPIO_24	SPI_1_DO/GPIO_24	
L13	SPI_1_SS/GPIO_27	SPI_1_SS/GPIO_27	
L14	SPI_1_CLK/GPIO_26	SPI_1_CLK/GPIO_26	
L15	SPI_1_DI/GPIO_25	SPI_1_DI/GPIO_25	
L16	GND	GND	
M1	MAC_TXD[0]/IO56RSB4V0	MAC_TXD[0]/IO65RSB4V0	
M2	MAC_TXD[1]/IO55RSB4V0	MAC_TXD[1]/IO64RSB4V0	
M3	MAC_RXD[0]/IO54RSB4V0	MAC_RXD[0]/IO63RSB4V0	
M4	GND	GND	
M5	ADC3	ADC3	Can be left floating if unused.
M6	GND15ADC0	GND15ADC0	
M7	GND33ADC1	GND33ADC1	
M8	GND33ADC1	GND33ADC1	
M9	ADC4	ADC4	Can be left floating if unused.
M10	GNDTM1	GNDTM1	

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Pin Number	256-Pin FBGA		
	A2F200 Function	A2F500 Function	Handling When Unused
M11	TM2	TM2	Can be left floating if unused.
M12	CM2	CM2	Can be left floating if unused.
M13	SPI_0_SS/GPIO_19	SPI_0_SS/GPIO_19	
M14	VCCMSSIOB2	VCCMSSIOB2	Can be grounded if IO Bank2 is unused.
M15	SPI_0_CLK/GPIO_18	SPI_0_CLK/GPIO_18	
M16	SPI_0_DI/GPIO_17	SPI_0_DI/GPIO_17	
N1	MAC_RXD[1]/IO53RSB4V0	MAC_RXD[1]/IO62RSB4V0	
N2	VCCMSSIOB4	VCCMSSIOB4	Can be grounded if IO Bank4 is unused.
N3	VCC15A	VCC15A	Must be powered all the time.
N4	VCC33AP	VCC33AP	Either pull-down or connect to VCC33A.
N5	ABPS3	ABPS3	Can be left floating if unused.
N6	TM1	TM1	Can be left floating if unused.
N7	GND33ADC0	GND33ADC0	
N8	VCC33ADC1	VCC33ADC1	NEVER ground it. Can be left floating if unused.
N9	ADC5	ADC5	Can be left floating if unused.
N10	CM3	CM3	Can be left floating if unused.
N11	GNDAQ	GNDAQ	
N12	VAREFOUT	VAREFOUT	Can be left floating if unused.
N13	GNDSDD1	GNDSDD1	
N14	VCC33SDD1	VCC33SDD1	Can be floated or grounded if second and third DACs unused.
N15	GND	GND	
N16	SPI_0_DO/GPIO_16	SPI_0_DO/GPIO_16	
P1	GNDSDD0	GNDSDD0	
P2	VCC33SDD0	VCC33SDD0	Can be left floating or pulled down if DAC0 is unused.
P3	VCC33N	VCC33N	Must have 2.2 μ F CAP to ground.
P4	GNDA	GNDA	
P5	GNDAQ	GNDAQ	
P6	CM1	CM1	Can be left floating if unused.
P7	ADC2	ADC2	Can be left floating if unused.

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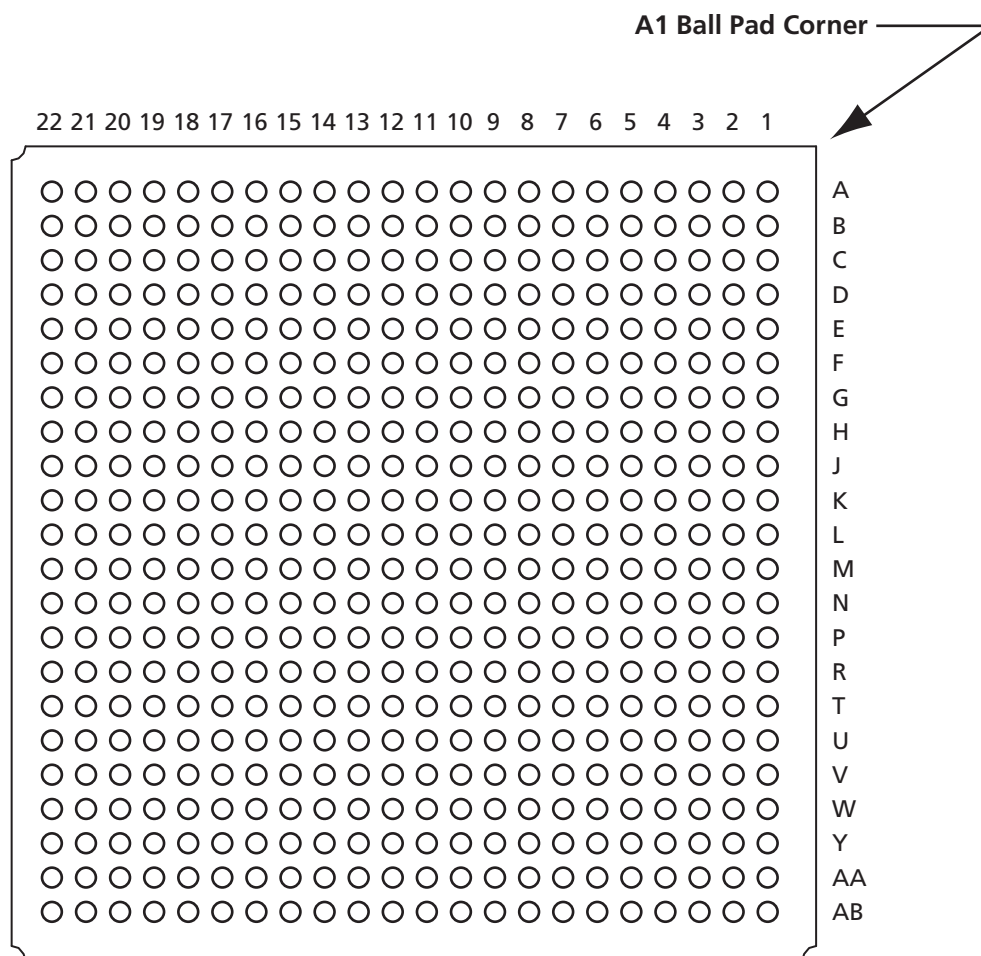
Pin Number	256-Pin FBGA		
	A2F200 Function	A2F500 Function	Handling When Unused
P8	VCC15ADC0	VCC15ADC0	Must be powered all the time.
P9	ADC6	ADC6	Can be left floating if unused.
P10	TM3	TM3	Can be left floating if unused.
P11	GNDA	GNDA	
P12	VCCMAINXTAL	VCCMAINXTAL	Pull-down to GND if unused.
P13	GNDLPXTAL	GNDLPXTAL	
P14	VDDBAT	VDDBAT	Pull-down to GND if unused.
P15	PTEM	PTEM	
P16	PTBASE	PTBASE	Can be left floating if unused.
R1	PCAP	PCAP	Connect 2.2 μ F CAP between PCAP and NCAP.
R2	SDD0	SDD0	Can be left floating if unused.
R3	ABPS0	ABPS0	Can be left floating if unused.
R4	TM0	TM0	Can be left floating if unused.
R5	ABPS2	ABPS2	Can be left floating if unused.
R6	ADC1	ADC1	Can be left floating if unused.
R7	VCC33ADC0	VCC33ADC0	
R8	VCC15ADC1	VCC15ADC1	Must be powered all the time.
R9	ADC7	ADC7	Can be left floating if unused.
R10	ABPS7	ABPS7	Can be left floating if unused.
R11	ABPS4	ABPS4	Can be left floating if unused.
R12	MAINXIN	MAINXIN	Can be pulled-down if unused.
R13	MAINXOUT	MAINXOUT	Must be left floating if unused.
R14	LPXIN	LPXIN	Can be pulled-down if unused.
R15	LPXOUT	LPXOUT	Must be left floating if unused.
R16	VCC33A	VCC33A	
T1	NCAP	NCAP	Connect 2.2uF CAP between PCAP and NCAP.
T2	ABPS1	ABPS1	Can be left floating if unused.
T3	CM0	CM0	Can be left floating if unused.
T4	GNDTM0	GNDTM0	
T5	ADC0	ADC0	Can be left floating if unused.
T6	VAREF0	VAREF0	Can be left floating if unused.
T7	GND33ADC0	GND33ADC0	
T8	GND15ADC1	GND15ADC1	

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Pin Number	256-Pin FBGA		
	A2F200 Function	A2F500 Function	Handling When Unused
T9	VAREF1	VAREF1	Can be left floating if unused.
T10	ABPS6	ABPS6	Can be left floating if unused.
T11	ABPS5	ABPS5	Can be left floating if unused.
T12	SDD1	SDD1	Can be left floating if unused.
T13	GNDVAREF	GNDVAREF	
T14	GNDMAINXTAL	GNDMAINXTAL	
T15	VCCLPXTAL	VCCLPXTAL	Pull-down to GND if unused.
T16	PU_N	PU_N	

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484-Pin FBGA



Note

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Pin Number	484-Pin FBGA	
	A2F200 Function	A2F500 Function
A1	GND	GND
A2	NC	NC
A3	NC	NC
A4	GND	GND
A5	EMC_CS0_N/GAB0/IO01NDB0V0	EMC_CS0_N/GAB0/IO05NDB0V0
A6	EMC_CS1_N/GAB1/IO01PDB0V0	EMC_CS1_N/GAB1/IO05PDB0V0
A7	GND	GND
A8	EMC_AB[0]/IO04NDB0V0	EMC_AB[0]/IO06NDB0V0
A9	EMC_AB[1]/IO04PDB0V0	EMC_AB[1]/IO06PDB0V0
A10	GND	GND
A11	NC	NC
A12	EMC_AB[7]/IO07PDB0V0	EMC_AB[7]/IO12PDB0V0
A13	GND	GND
A14	EMC_AB[12]/IO10NDB0V0	EMC_AB[12]/IO14NDB0V0
A15	EMC_AB[13]/IO10PDB0V0	EMC_AB[13]/IO14PDB0V0
A16	GND	GND
A17	NC	IO16NDB0V0
A18	NC	IO16PDB0V0
A19	GND	GND
A20	NC	NC
A21	NC	NC
A22	GND	GND
AA1	GPIO_4/IO43RSB4V0	GPIO_4/IO52RSB4V0
AA2	GPIO_12/IO37RSB4V0	GPIO_12/IO46RSB4V0
AA3	MAC_MDC/IO48RSB4V0	MAC_MDC/IO57RSB4V0
AA4	MAC_RXER/IO50RSB4V0	MAC_RXER/IO59RSB4V0
AA5	MAC_TXD[0]/IO56RSB4V0	MAC_TXD[0]/IO65RSB4V0
AA6	ABPS0	ABPS0
AA7	TM1	TM1
AA8	ADC1	ADC1
AA9	GND15ADC1	GND15ADC1
AA10	GND33ADC1	GND33ADC1
AA11	CM3	CM3
AA12	GNDTM1	GNDTM1
AA13	NC	ADC10
AA14	NC	ADC9

Note: Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.

Pin Number	484-Pin FBGA	
	A2F200 Function	A2F500 Function
AA15	NC	GND15ADC2
AA16	MAINXIN	MAINXIN
AA17	MAINXOUT	MAINXOUT
AA18	LPXIN	LPXIN
AA19	LPXOUT	LPXOUT
AA20	NC	NC
AA21	NC	NC
AA22	SPI_1_CLK/GPIO_26	SPI_1_CLK/GPIO_26
AB1	GND	GND
AB2	GPIO_13/IO36RSB4V0	GPIO_13/IO45RSB4V0
AB3	GPIO_14/IO35RSB4V0	GPIO_14/IO44RSB4V0
AB4	GND	GND
AB5	PCAP	PCAP
AB6	NCAP	NCAP
AB7	ABPS3	ABPS3
AB8	ADC3	ADC3
AB9	GND15ADC0	GND15ADC0
AB10	VCC33ADC1	VCC33ADC1
AB11	VAREF1	VAREF1
AB12	TM2	TM2
AB13	CM2	CM2
AB14	ABPS4	ABPS4
AB15	GND4Q	GND4Q
AB16	GNDMAINXTAL	GNDMAINXTAL
AB17	GNDLPXTAL	GNDLPXTAL
AB18	VCCLPXTAL	VCCLPXTAL
AB19	VDDBAT	VDDBAT
AB20	PTBASE	PTBASE
AB21	NC	NC
AB22	GND	GND
B1	EMC_DB[15]/GAA2/IO71PDB5V0	EMC_DB[15]/GAA2/IO88PDB5V0
B2	GND	GND
B3	NC	NC
B4	NC	NC
B5	VCCFPGAIOB0	VCCFPGAIOB0
B6	EMC_RW_N/GAA1/IO00PDB0V0	EMC_RW_N/GAA1/IO02PDB0V0

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Pin Number	484-Pin FBGA	
	A2F200 Function	A2F500 Function
B7	NC	IO04PPB0V0
B8	VCCFPGAIOB0	VCCFPGAIOB0
B9	EMC_BYTEN[0]/GAC0/IO02NDB0V0	EMC_BYTEN[0]/GAC0/IO07NDB0V0
B10	EMC_AB[2]/IO05NDB0V0	EMC_AB[2]/IO09NDB0V0
B11	EMC_AB[3]/IO05PDB0V0	EMC_AB[3]/IO09PDB0V0
B12	EMC_AB[6]/IO07NDB0V0	EMC_AB[6]/IO12NDB0V0
B13	EMC_AB[14]/IO11NDB0V0	EMC_AB[14]/IO15NDB0V0
B14	EMC_AB[15]/IO11PDB0V0	EMC_AB[15]/IO15PDB0V0
B15	VCCFPGAIOB0	VCCFPGAIOB0
B16	EMC_AB[18]/IO13NDB0V0	EMC_AB[18]/IO18NDB0V0
B17	EMC_AB[19]/IO13PDB0V0	EMC_AB[19]/IO18PDB0V0
B18	VCCFPGAIOB0	VCCFPGAIOB0
B19	GBB0/IO18NDB0V0	GBB0/IO24NDB0V0
B20	GBB1/IO18PDB0V0	GBB1/IO24PDB0V0
B21	GND	GND
B22	GBA2/IO20PDB1V0	GBA2/IO27PDB1V0
C1	EMC_DB[14]/GAB2/IO71NDB5V0	EMC_DB[14]/GAB2/IO88NDB5V0
C2	NC	NC
C3	NC	NC
C4	NC	IO01NDB0V0
C5	NC	IO01PDB0V0
C6	EMC_CLK/GAA0/IO00NDB0V0	EMC_CLK/GAA0/IO02NDB0V0
C7	NC	IO03PPB0V0
C8	NC	IO04NPB0V0
C9	EMC_BYTEN[1]/GAC1/IO02PDB0V0	EMC_BYTEN[1]/GAC1/IO07PDB0V0
C10	EMC_OEN1_N/IO03PDB0V0	EMC_OEN1_N/IO08PDB0V0
C11	GND	GND
C12	VCCFPGAIOB0	VCCFPGAIOB0
C13	EMC_AB[8]/IO08NDB0V0	EMC_AB[8]/IO13NDB0V0
C14	EMC_AB[16]/IO12NDB0V0	EMC_AB[16]/IO17NDB0V0
C15	EMC_AB[17]/IO12PDB0V0	EMC_AB[17]/IO17PDB0V0
C16	EMC_AB[24]/IO16NDB0V0	EMC_AB[24]/IO20NDB0V0
C17	EMC_AB[22]/IO15NDB0V0	EMC_AB[22]/IO19NDB0V0
C18	EMC_AB[23]/IO15PDB0V0	EMC_AB[23]/IO19PDB0V0
C19	GBA0/IO19NPB0V0	GBA0/IO23NPB0V0
C20	NC	NC

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Pin Number	484-Pin FBGA	
	A2F200 Function	A2F500 Function
C21	GBC2/IO21PDB1V0	GBC2/IO30PDB1V0
C22	GBB2/IO20NDB1V0	GBB2/IO27NDB1V0
D1	GND	GND
D2	EMC_DB[12]/IO70NDB5V0	EMC_DB[12]/IO87NDB5V0
D3	EMC_DB[13]/GAC2/IO70PDB5V0	EMC_DB[13]/GAC2/IO87PDB5V0
D4	NC	NC
D5	NC	NC
D6	GND	GND
D7	NC	IO00NPB0V0
D8	NC	IO03NPB0V0
D9	GND	GND
D10	EMC_OEN0_N/IO03NDB0V0	EMC_OEN0_N/IO08NDB0V0
D11	EMC_AB[10]/IO09NDB0V0	EMC_AB[10]/IO11NDB0V0
D12	EMC_AB[11]/IO09PDB0V0	EMC_AB[11]/IO11PDB0V0
D13	EMC_AB[9]/IO08PDB0V0	EMC_AB[9]/IO13PDB0V0
D14	GND	GND
D15	GBC1/IO17PPB0V0	GBC1/IO22PPB0V0
D16	EMC_AB[25]/IO16PDB0V0	EMC_AB[25]/IO20PDB0V0
D17	GND	GND
D18	GBA1/IO19PPB0V0	GBA1/IO23PPB0V0
D19	NC	NC
D20	NC	NC
D21	IO21NDB1V0	IO30NDB1V0
D22	GND	GND
E1	GFC2/IO67PPB5V0	GFC2/IO84PPB5V0
E2	VCCFPGAIOB5	VCCFPGAIOB5
E3	GFA2/IO68PDB5V0	GFA2/IO85PDB5V0
E4	GND	GND
E5	NC	NC
E6	GNDQ	GNDQ
E7	VCCFPGAIOB0	VCCFPGAIOB0
E8	NC	IO00PPB0V0
E9	NC	NC
E10	VCCFPGAIOB0	VCCFPGAIOB0
E11	EMC_AB[4]/IO06NDB0V0	EMC_AB[4]/IO10NDB0V0
E12	EMC_AB[5]/IO06PDB0V0	EMC_AB[5]/IO10PDB0V0

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Pin Number	484-Pin FBGA	
	A2F200 Function	A2F500 Function
E13	VCCFPGAIOB0	VCCFPGAIOB0
E14	GBC0/IO17NPB0V0	GBC0/IO22NPB0V0
E15	NC	NC
E16	VCCFPGAIOB0	VCCFPGAIOB0
E17	NC	VCOMPLA1
E18	NC	IO25NPB1V0
E19	GND	GND
E20	NC	NC
E21	VCCFPGAIOB1	VCCFPGAIOB1
E22	IO22NDB1V0	IO32NDB1V0
F1	GFB1/IO65PPB5V0	GFB1/IO82PPB5V0
F2	IO67NPB5V0	IO84NPB5V0
F3	GFB2/IO68NDB5V0	GFB2/IO85NDB5V0
F4	EMC_DB[10]/IO69NPB5V0	EMC_DB[10]/IO86NPB5V0
F5	VCCFPGAIOB5	VCCFPGAIOB5
F6	VCCPLL	VCCPLL0
F7	VCOMPLA	VCOMPLA0
F8	NC	NC
F9	NC	NC
F10	NC	NC
F11	NC	NC
F12	NC	NC
F13	EMC_AB[20]/IO14NDB0V0	EMC_AB[20]/IO21NDB0V0
F14	EMC_AB[21]/IO14PDB0V0	EMC_AB[21]/IO21PDB0V0
F15	GNDQ	GNDQ
F16	NC	VCCPLL1
F17	NC	IO25PPB1V0
F18	VCCFPGAIOB1	VCCFPGAIOB1
F19	IO23NDB1V0	IO28NDB1V0
F20	NC	IO31PDB1V0
F21	NC	IO31NDB1V0
F22	IO22PDB1V0	IO32PDB1V0
G1	GND	GND
G2	GFB0/IO65NPB5V0	GFB0/IO82NPB5V0
G3	EMC_DB[9]/GEC1/IO63PDB5V0	EMC_DB[9]/GEC1/IO80PDB5V0
G4	GFC1/IO66PPB5V0	GFC1/IO83PPB5V0

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Pin Number	484-Pin FBGA	
	A2F200 Function	A2F500 Function
G5	EMC_DB[11]/IO69PPB5V0	EMC_DB[11]/IO86PPB5V0
G6	GNDQ	GNDQ
G7	NC	NC
G8	GND	GND
G9	VCCFPGAIOB0	VCCFPGAIOB0
G10	GND	GND
G11	VCCFPGAIOB0	VCCFPGAIOB0
G12	GND	GND
G13	VCCFPGAIOB0	VCCFPGAIOB0
G14	GND	GND
G15	VCCFPGAIOB0	VCCFPGAIOB0
G16	GNDQ	GNDQ
G17	NC	IO26PDB1V0
G18	NC	IO26NDB1V0
G19	GCA2/IO23PDB1V0	GCA2/IO28PDB1V0
G20	IO24NDB1V0	IO33NDB1V0
G21	GCB2/IO24PDB1V0	GCB2/IO33PDB1V0
G22	GND	GND
H1	EMC_DB[7]/GEB1/IO62PDB5V0	EMC_DB[7]/GEB1/IO79PDB5V0
H2	VCCFPGAIOB5	VCCFPGAIOB5
H3	EMC_DB[8]/GEC0/IO63NDB5V0	EMC_DB[8]/GEC0/IO80NDB5V0
H4	GND	GND
H5	GFC0/IO66NPB5V0	GFC0/IO83NPB5V0
H6	GFA1/IO64PDB5V0	GFA1/IO81PDB5V0
H7	GND	GND
H8	VCC	VCC
H9	GND	GND
H10	VCC	VCC
H11	GND	GND
H12	VCC	VCC
H13	GND	GND
H14	VCC	VCC
H15	GND	GND
H16	VCCFPGAIOB1	VCCFPGAIOB1
H17	IO25NDB1V0	IO29NDB1V0
H18	GCC2/IO25PDB1V0	GCC2/IO29PDB1V0

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Pin Number	484-Pin FBGA	
	A2F200 Function	A2F500 Function
H19	GND	GND
H20	GCC0/IO26NPB1V0	GCC0/IO35NPB1V0
H21	VCCFPGAIOB1	VCCFPGAIOB1
H22	GCB0/IO27NDB1V0	GCB0/IO34NDB1V0
J1	EMC_DB[6]/GEB0/IO62NDB5V0	EMC_DB[6]/GEB0/IO79NDB5V0
J2	EMC_DB[5]/GEA1/IO61PDB5V0	EMC_DB[5]/GEA1/IO78PDB5V0
J3	EMC_DB[4]/GEA0/IO61NDB5V0	EMC_DB[4]/GEA0/IO78NDB5V0
J4	EMC_DB[3]/GEC2/IO60PPB5V0	EMC_DB[3]/GEC2/IO77PPB5V0
J5	VCCFPGAIOB5	VCCFPGAIOB5
J6	GFA0/IO64NDB5V0	GFA0/IO81NDB5V0
J7	VCCFPGAIOB5	VCCFPGAIOB5
J8	GND	GND
J9	VCC	VCC
J10	GND	GND
J11	VCC	VCC
J12	GND	GND
J13	VCC	VCC
J14	GND	GND
J15	VCC	VCC
J16	GND	GND
J17	NC	IO37PDB1V0
J18	VCCFPGAIOB1	VCCFPGAIOB1
J19	GCA0/IO28NDB1V0	GCA0/IO36NDB1V0
J20	GCA1/IO28PDB1V0	GCA1/IO36PDB1V0
J21	GCC1/IO26PPB1V0	GCC1/IO35PPB1V0
J22	GCB1/IO27PDB1V0	GCB1/IO34PDB1V0
K1	GND	GND
K2	EMC_DB[0]/GEA2/IO59NDB5V0	EMC_DB[0]/GEA2/IO76NDB5V0
K3	EMC_DB[1]/GEB2/IO59PDB5V0	EMC_DB[1]/GEB2/IO76PDB5V0
K4	NC	IO74PPB5V0
K5	EMC_DB[2]/IO60NPB5V0	EMC_DB[2]/IO77NPB5V0
K6	NC	IO75PDB5V0
K7	GND	GND
K8	VCC	VCC
K9	GND	GND
K10	VCC	VCC

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Pin Number	484-Pin FBGA	
	A2F200 Function	A2F500 Function
K11	GND	GND
K12	VCC	VCC
K13	GND	GND
K14	VCC	VCC
K15	GND	GND
K16	VCCFPGAIOB1	VCCFPGAIOB1
K17	NC	IO37NDB1V0
K18	GDA1/IO31PDB1V0	GDA1/IO40PDB1V0
K19	GDA0/IO31NDB1V0	GDA0/IO40NDB1V0
K20	GDC1/IO29PDB1V0	GDC1/IO38PDB1V0
K21	GDC0/IO29NDB1V0	GDC0/IO38NDB1V0
K22	GND	GND
L1	NC	IO73PDB5V0
L2	NC	IO73NDB5V0
L3	NC	IO72PPB5V0
L4	GND	GND
L5	NC	IO74NPB5V0
L6	NC	IO75NDB5V0
L7	VCCFPGAIOB5	VCCFPGAIOB5
L8	GND	GND
L9	VCC	VCC
L10	GND	GND
L11	VCC	VCC
L12	GND	GND
L13	VCC	VCC
L14	GND	GND
L15	VCC	VCC
L16	GND	GND
L17	GNDQ	GNDQ
L18	GDA2/IO33NDB1V0	GDA2/IO42NDB1V0
L19	VCCFPGAIOB1	VCCFPGAIOB1
L20	GDB1/IO30PDB1V0	GDB1/IO39PDB1V0
L21	GDB0/IO30NDB1V0	GDB0/IO39NDB1V0
L22	GDC2/IO32PDB1V0	GDC2/IO41PDB1V0
M1	NC	IO71PDB5V0
M2	NC	IO71NDB5V0

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Pin Number	484-Pin FBGA	
	A2F200 Function	A2F500 Function
M3	VCCFPGAIOB5	VCCFPGAIOB5
M4	NC	IO72NPB5V0
M5	GNDQ	GNDQ
M6	NC	IO68PDB5V0
M7	GND	GND
M8	VCC	VCC
M9	GND	GND
M10	VCC	VCC
M11	GND	GND
M12	VCC	VCC
M13	GND	GND
M14	VCC	VCC
M15	GND	GND
M16	VCCFPGAIOB1	VCCFPGAIOB1
M17	NC	NC
M18	GDB2/IO33PDB1V0	GDB2/IO42PDB1V0
M19	VJTAG	VJTAG
M20	GND	GND
M21	VPP	VPP
M22	IO32NDB1V0	IO41NDB1V0
N1	GND	GND
N2	NC	IO70PDB5V0
N3	NC	IO70NDB5V0
N4	VCCRCOSC	VCCRCOSC
N5	VCCFPGAIOB5	VCCFPGAIOB5
N6	NC	IO68NDB5V0
N7	VCCFPGAIOB5	VCCFPGAIOB5
N8	GND	GND
N9	VCC	VCC
N10	GND	GND
N11	VCC	VCC
N12	GND	GND
N13	VCC	VCC
N14	GND	GND
N15	VCC	VCC
N16	NC	GND

Note: Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.

Pin Number	484-Pin FBGA	
	A2F200 Function	A2F500 Function
N17	NC	NC
N18	VCCFPGAIOB1	VCCFPGAIOB1
N19	VCCENVM	VCCENVM
N20	GNDENVM	GNDENVM
N21	NC	NC
N22	GND	GND
P1	NC	IO69NDB5V0
P2	NC	IO69PDB5V0
P3	GNDRCOSC	GNDRCOSC
P4	GND	GND
P5	NC	NC
P6	NC	NC
P7	GND	GND
P8	VCC	VCC
P9	GND	GND
P10	VCC	VCC
P11	GND	GND
P12	VCC	VCC
P13	GND	GND
P14	VCC	VCC
P15	GND	GND
P16	VCCFPGAIOB1	VCCFPGAIOB1
P17	TDI	TDI
P18	TCK	TCK
P19	GND	GND
P20	TMS	TMS
P21	TDO	TDO
P22	TRSTB	TRSTB
R1	MSS_RESET_N	MSS_RESET_N
R2	VCCFPGAIOB5	VCCFPGAIOB5
R3	GPIO_1/IO46RSB4V0	GPIO_1/IO55RSB4V0
R4	NC	NC
R5	NC	NC
R6	NC	NC
R7	NC	NC
R8	GND	GND

Note: Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.

Pin Number	484-Pin FBGA	
	A2F200 Function	A2F500 Function
R9	VCC	VCC
R10	GND	GND
R11	VCC	VCC
R12	GND	GND
R13	VCC	VCC
R14	GND	GND
R15	VCC	VCC
R16	JTAGSEL	JTAGSEL
R17	NC	NC
R18	NC	NC
R19	NC	NC
R20	NC	NC
R21	VCCFPGAIOB1	VCCFPGAIOB1
R22	NC	NC
T1	GND	GND
T2	VCCMSSIOB4	VCCMSSIOB4
T3	GPIO_8/IO39RSB4V0	GPIO_8/IO48RSB4V0
T4	GPIO_11/IO57RSB4V0	GPIO_11/IO66RSB4V0
T5	GND	GND
T6	MAC_CLK	MAC_CLK
T7	VCCMSSIOB4	VCCMSSIOB4
T8	VCC33SDD0	VCC33SDD0
T9	VCC15A	VCC15A
T10	GND4Q	GND4Q
T11	GND33ADC0	GND33ADC0
T12	ADC7	ADC7
T13	NC	TM4
T14	NC	VAREF2
T15	VAREFOUT	VAREFOUT
T16	VCCMSSIOB2	VCCMSSIOB2
T17	SPI_1_DO/GPIO_24	SPI_1_DO/GPIO_24
T18	GND	GND
T19	NC	NC
T20	NC	NC
T21	VCCMSSIOB2	VCCMSSIOB2
T22	GND	GND

Note: Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.

Pin Number	484-Pin FBGA	
	A2F200 Function	A2F500 Function
U1	GND	GND
U2	GPIO_5/IO42RSB4V0	GPIO_5/IO51RSB4V0
U3	GPIO_10/IO58RSB4V0	GPIO_10/IO67RSB4V0
U4	VCCMSSIOB4	VCCMSSIOB4
U5	MAC_RXD[1]/IO53RSB4V0	MAC_RXD[1]/IO62RSB4V0
U6	NC	NC
U7	VCC33AP	VCC33AP
U8	VCC33N	VCC33N
U9	CM1	CM1
U10	VAREF0	VAREF0
U11	GND33ADC1	GND33ADC1
U12	ADC4	ADC4
U13	NC	GNDTM2
U14	NC	ADC11
U15	GNDVAREF	GNDVAREF
U16	VCC33SDD1	VCC33SDD1
U17	SPI_0_DO/GPIO_16	SPI_0_DO/GPIO_16
U18	UART_0_RXD/GPIO_21	UART_0_RXD/GPIO_21
U19	VCCMSSIOB2	VCCMSSIOB2
U20	I2C_1_SCL/GPIO_31	I2C_1_SCL/GPIO_31
U21	I2C_0_SCL/GPIO_23	I2C_0_SCL/GPIO_23
U22	GND	GND
V1	GPIO_0/IO47RSB4V0	GPIO_0/IO56RSB4V0
V2	GPIO_6/IO41RSB4V0	GPIO_6/IO50RSB4V0
V3	GPIO_9/IO38RSB4V0	GPIO_9/IO47RSB4V0
V4	MAC_MDIO/IO49RSB4V0	MAC_MDIO/IO58RSB4V0
V5	MAC_RXD[0]/IO54RSB4V0	MAC_RXD[0]/IO63RSB4V0
V6	GND	GND
V7	SDD0	SDD0
V8	ABPS1	ABPS1
V9	ADC2	ADC2
V10	VCC33ADC0	VCC33ADC0
V11	ADC6	ADC6
V12	ADC5	ADC5
V13	ABPS5	ABPS5
V14	NC	ADC8

Note: Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.

Pin Number	484-Pin FBGA	
	A2F200 Function	A2F500 Function
V15	NC	GND33ADC2
V16	NC	NC
V17	GND	GND
V18	SPI_0_DI/GPIO_17	SPI_0_DI/GPIO_17
V19	SPI_1_DI/GPIO_25	SPI_1_DI/GPIO_25
V20	UART_1_TXD/GPIO_28	UART_1_TXD/GPIO_28
V21	I2C_0_SDA/GPIO_22	I2C_0_SDA/GPIO_22
V22	I2C_1_SDA/GPIO_30	I2C_1_SDA/GPIO_30
W1	GPIO_2/IO45RSB4V0	GPIO_2/IO54RSB4V0
W2	GPIO_7/IO40RSB4V0	GPIO_7/IO49RSB4V0
W3	GND	GND
W4	MAC_CRSDV/IO51RSB4V0	MAC_CRSDV/IO60RSB4V0
W5	MAC_TXD[1]/IO55RSB4V0	MAC_TXD[1]/IO64RSB4V0
W6	NC	SDD2
W7	GND	GND
W8	TM0	TM0
W9	ABPS2	ABPS2
W10	GND33ADC0	GND33ADC0
W11	VCC15ADC1	VCC15ADC1
W12	ABPS6	ABPS6
W13	NC	CM4
W14	NC	ABPS9
W15	NC	VCC33ADC2
W16	GND	GND
W17	PU_N	PU_N
W18	GNDSD1	GNDSD1
W19	SPI_0_CLK/GPIO_18	SPI_0_CLK/GPIO_18
W20	GND	GND
W21	SPI_1_SS/GPIO_27	SPI_1_SS/GPIO_27
W22	UART_1_RXD/GPIO_29	UART_1_RXD/GPIO_29
Y1	GPIO_3/IO44RSB4V0	GPIO_3/IO53RSB4V0
Y2	VCCMSSIOB4	VCCMSSIOB4
Y3	GPIO_15/IO34RSB4V0	GPIO_15/IO43RSB4V0
Y4	MAC_TXEN/IO52RSB4V0	MAC_TXEN/IO61RSB4V0
Y5	VCCMSSIOB4	VCCMSSIOB4
Y6	GNDSD0	GNDSD0

Note: Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.

Pin Number	484-Pin FBGA	
	A2F200 Function	A2F500 Function
Y7	CM0	CM0
Y8	GNDTM0	GNDTM0
Y9	ADC0	ADC0
Y10	VCC15ADC0	VCC15ADC0
Y11	ABPS7	ABPS7
Y12	TM3	TM3
Y13	NC	ABPS8
Y14	NC	GND33ADC2
Y15	NC	VCC15ADC2
Y16	VCCMAINXTAL	VCCMAINXTAL
Y17	SDD1	SDD1
Y18	PTEM	PTEM
Y19	VCC33A	VCC33A
Y20	SPI_0_SS/GPIO_19	SPI_0_SS/GPIO_19
Y21	VCCMSSIOB2	VCCMSSIOB2
Y22	UART_0_TXD/GPIO_20	UART_0_TXD/GPIO_20

Note: Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.

6 – Datasheet Information

List of Changes

The following table lists critical changes that were made in each revision of the SmartFusion datasheet.

Revision	Changes	Page
Revision 4 (September 2010)	Table 2-8 • Quiescent Supply Current Characteristics was revised. VCCRCOSC was moved to a column of its own with new values. VCCENVM was added to the table. Standby mode for VJTAG and VPP was changed from 0 V to N/A. "Disable" was changed to "Off" in the eNVM column. The column for RCOSC was deleted.	2-10
	The "Power-Down and Sleep Mode Implementation" section was revised to include VCCROSC.	2-11
Revision 3 (September 2010)	The "I/Os and Operating Voltage" section was revised to list "single 3.3 V power supply with on-chip 1.5 V regulator" and "external 1.5 V is allowed" (SAR 27663).	I
	The CS288 package was added to the "Package I/Os: MSS + FPGA I/Os" table (SAR 27101), "Product Ordering Codes" table, and "Temperature Grade Offerings" table (SAR 27044). The number of direct analog inputs for the FG256 package in A2F060 was changed from 8 to 6.	III, VI, VI
	Two notes were added to the "SmartFusion Family Product Table" indicating limitations for features of the A2F500 device: <i>Two PLLs are available in CS288 and FG484 (one PLL in FG256).</i> <i>[ADCs, DACs, SCBs, comparators, current monitors, and bipolar high voltage monitors are] Available on FG484 only. FG256 and CS288 packages offer the same programmable analog capabilities as A2F200.</i> Table cells were merged in rows containing the same values for easier reading (SAR 24748).	II
	The security feature option was added to the "Product Ordering Codes" table.	VI
	In Table 2-3 • Recommended Operating Conditions, the VDDBAT recommended operating range was changed from "2.97 to 3.63" to "2.7 to 3.63" (SAR 25246). Recommended operating range was changed to "3.15 to 3.45" for the following voltages: VCC33A VCC33ADCx VCC33AP VCC33SDDx VCCMAINXTAL VCCLPXTAL Two notes were added to the table (SAR 27109): 1. The following 3.3 V supplies should be connected together while following proper noise filtering practices: VCC33A, VCC33ADCx, VCC33AP, VCC33SDDx, VCCMAINXTAL, and VCCLPXTAL. 2. The following 1.5 V supplies should be connected together while following proper noise filtering practices: VCC, VCC15A, and VCC15ADCx.	2-3
	In Table 2-3 • Recommended Operating Conditions, the description for VCCLPXTAL was corrected to change "32 Hz" to "32 KHz" (SAR 27110).	2-3
	The "Power Supply Sequencing Requirement" section is new (SAR 27178).	2-4

Revision	Changes	Page
Revision 3 (continued)	Table 2-8 • Quiescent Supply Current Characteristics was revised to change most on/off entries to voltages. Note 5 was added, stating that "on" means proper voltage is applied. The values of 6 μ A and 16 μ A were removed for IDC1 and IDC2 for 3.3 V. A note was added for IDC1 and IDC2: "Power mode and Sleep mode are consuming higher current than expected in the current version of silicon. These specifications will be updated when new version of the silicon is available" (SAR 27926).	2-10
	The "Power-Down and Sleep Mode Implementation" section is new (SAR 27178).	2-11
	A note was added to Table 2-83 • SmartFusion CCC/PLL Specification, pertaining to f_{out_CCC} , stating that "one of the CCC outputs (GLA0) is used as an MSS clock and is limited to 100 MHz (maximum) by software" (SAR 26388).	2-65
	Table 2-87 • eNVM Block Timing, Worst Commercial Case Conditions: $T_J = 85^{\circ}\text{C}$, $V_{CC} = 1.425\text{ V}$ was revised. Values were included for A2F200 and A2F500, for -1 and Std. speed grades. A note was added to define 6:1:1:1 and 5:1:1:1 (SAR 26166).	2-77
	The units were corrected (mV instead of V) for input referred offset voltage, $GDEC[1:0] = 00$ in Table 2-93 • ABPS Performance Specifications (SAR 25381).	2-83
	The test condition values for operating current ($ICC33A$, typical) were changed in Table 2-96 • Voltage Regulator (SAR 26465).	2-87
	Figure 2-45 • Typical Output Voltage was revised to add legends for the three curves, stating the load represented by each (SAR 25247).	2-88
	The "SmartFusion Programming" chapter was moved to this document from the SmartFusion Subsystem Microcontroller User's Guide (SAR 26542). The "Typical Programming and Erase Times" section was added to this chapter.	4-5
	Figure 4-1 • TRSTB Logic was revised to change 1.5 V to "VJTAG (1.5 V to 3.3 V nominal)" (SAR 24694).	4-6
	Two notes were added to the "Supply Pins" table (SAR 27109): 1. The following supplies should be connected together while following proper noise filtering practices: V_{CC33A} , $V_{CC33ADCx}$, V_{CC33AP} , $V_{CC33SDDx}$, $V_{CCMAINXTAL}$, and $V_{CCLPXTAL}$. 2. The following 1.5 V supplies should be connected together while following proper noise filtering practices: V_{CC} , V_{CC15A} , and $V_{CC15ADCx}$.	5-1
	The descriptions for the " V_{CC33N} ", " $NCAP$ ", and " $PCAP$ " pins were revised to include information on what to do if analog SCB features and SDDs are not used (SAR 26744).	5-2, 5-6, 5-7
	Information was added to the "User Pins" table regarding tristating of used and unused GPIO pins. The IO portion of the table was revised to state that unused I/O pins are disabled by Libero IDE software and include a weak pull-up resistor (SAR 26890). Information was added regarding behavior of used I/O pins during power-up.	5-5
	The type for " EMC_RW_N " was changed from In/out to Out (SAR 25113).	5-10
	A note was added to the "Analog Front-End (AFE)" table stating that unused analog inputs should be grounded (SAR 26744).	5-12
	The "288-Pin CSP" section is new, with pin tables for A2F200 and A2F500 (SAR 27044).	5-16
	The "256-Pin FBGA" pin table was replaced and now includes "Handling When Unused" information (SAR 27709).	5-25

Revision	Changes	Page
Revision 2 (May 2010)	Embedded nonvolatile flash memory (eNVM) was changed from "64 to 512 Kbytes" to "128 to 512 Kbytes" in the "Microcontroller Subsystem (MSS)" section and "SmartFusion Family Product Table" (SAR 26005).	I, II
	The main oscillator range of values was changed to "32 KHz to 20 MHz" in the "Microcontroller Subsystem (MSS)" section and the "SmartFusion Family Product Table" (SAR 24906).	I, II
	The value for t_{PD} was changed from 50 ns to 15 ns for the high-speed voltage comparators listed in the "Analog Front-End (AFE)" section (SAR 26005).	I
	The number of PLLs for A2F200 was changed from 2 to 1 in the "SmartFusion Family Product Table" (SAR 25093).	II
	Values for direct analog input, total analog input, and total I/Os were updated for the FG256 package, A2F060, in the "Package I/Os: MSS + FPGA I/Os" table. The Max. column was removed from the table (SAR 26005).	III
	The Speed Grade section of the "Product Ordering Codes" table was revised (SAR 25257).	VI
Revision 1 (March 2010)	The "Product Ordering Codes" table was revised to add "blank" as an option for lead-free packaging and application (junction temperature range).	VI
	Table 2-3 • Recommended Operating Conditions was revised. T_a (ambient temperature) was replaced with T_j (junction temperature).	2-3
	PDC5 was deleted from Table 2-14 • Different Components Contributing to the Static Power Consumption in SmartFusion Devices.	2-15
	The formulas in the footnotes for Table 2-28 • I/O Weak Pull-Up/Pull-Down Resistances were revised.	2-29
	The values for input biased current were revised in Table 2-90 • Current Monitor Performance Specification.	2-79
Revision 0 (March 2010)	The "Analog Front-End (AFE)" section was updated to change the throughput for 10-bit mode from 600 Ksps to 550 Ksps.	I
	The A2F060 device was added to product information tables.	N/A
	The "Product Ordering Codes" table was updated to removed STD speed and add speed grade 1. Pre-production was removed from the application ordering code category.	VI
	The "SmartFusion Block Diagram" was revised.	IV
	The "Datasheet Categories" section was updated, referencing the "SmartFusion Block Diagram" table, which is new.	1-4, IV
	The "VCCI" parameter was renamed to "VCCxxxIOBx." "Advanced I/Os" were renamed to "FPGA I/Os." Generic pin names that represent multiple pins were standardized with a lower case x as a placeholder. For example, VAREF _x designates VAREF0, VAREF1, and VAREF2. Modes were renamed as follows: Operating mode was renamed to SoC mode. 32KHz Active mode was renamed to Standby mode. Battery mode was renamed to Time Keeping mode. Table entries have been filled with values as data has become available.	N/A

Revision	Changes	Page
Revision 0 (continued)	Table 2-1 • Absolute Maximum Ratings, Table 2-2 • Analog Maximum Ratings, and Table 2-3 • Recommended Operating Conditions were revised extensively.	2-1 through 2-3
	Device names were updated in Table 2-6 • Package Thermal Resistance.	2-7
	Table 2-8 • Quiescent Supply Current Characteristics was revised extensively.	2-10
	Table 2-10 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings was revised extensively.	2-12
	Removed "Example of Power Calculation."	N/A
	Table 2-13 • Different Components Contributing to Dynamic Power Consumption in SmartFusion Devices was revised extensively.	2-13
	Table 2-14 • Different Components Contributing to the Static Power Consumption in SmartFusion Devices was revised extensively.	2-15
	The "Power Calculation Methodology" section was revised.	2-16
	Table 2-80 • Electrical Characteristics of the RC Oscillator was revised extensively.	2-63
	Table 2-82 • Electrical Characteristics of the Low Power Oscillator was revised extensively.	2-64
	The parameter t_{RSTBQ} was changed to T_{C2CWRH} in Table 2-84 • RAM4K9.	2-71
	The 12-bit mode row for integral non-linearity was removed from Table 2-92 • ADC Specifications. The typical value for 10-bit mode was revised. The table note was punctuated correctly to make it clear.	2-81
	Figure 37-34 • Write Access after Write onto Same Address, Figure 37-34 • Read Access after Write onto Same Address, and Figure 37-34 • Write Access after Read onto Same Address were deleted.	N/A
	Table 2-96 • Voltage Regulator was revised extensively.	2-87
	The "Serial Peripheral Interface (SPI) Characteristics" section and "Inter-Integrated Circuit (I ² C) Characteristics" section are new.	2-89, 2-91
	"SmartFusion Development Tools" section was replaced with new content.	3-1
	The pin description tables were revised by adding additional pins to reflect the pinout for A2F500.	5-1 through 5-14
	The descriptions for "GNDSDD1" and "VCC33SDD1" were revised.	5-1, 5-2
	The description for "VCC33A" was revised.	5-2
	The pin tables for the "256-Pin FBGA" and "484-Pin FBGA" were replaced with tables that compare pin functions across densities for each package.	5-25
Draft B (December 2009)	The "Digital I/Os" section was renamed to the "I/Os and Operating Voltage" section and information was added regarding digital and analog VCC.	I
	The "SmartFusion Family Product Table" and "Package I/Os: MSS + FPGA I/Os" section were revised.	II
	The terminology for the analog blocks was changed to "programmable analog," consisting of two blocks: the analog front-end and analog compute engine. This is reflected throughout the text and in the "SmartFusion Block Diagram".	IV
	The "Product Ordering Codes" table was revised to add G as an ordering code for eNVM size.	VI

Revision	Changes	Page
Draft B (continued)	Timing tables were populated with information that has become available for speed grade –1.	N/A
	All occurrences of the VMV parameter were removed.	N/A
	The SDD[n] voltage parameter was removed from Table 2-2 • Analog Maximum Ratings .	2-2
	Table 36-4 • Flash Programming Limits – Retention, Storage and Operating Temperature was replaced with Table 2-4 • FPGA and Embedded Flash Programming, Storage and Operating Limits .	2-4
	The "Thermal Characteristics" section was revised extensively.	2-7
	Table 2-8 • Quiescent Supply Current Characteristics was revised significantly.	2-10
	Table 2-13 • Different Components Contributing to Dynamic Power Consumption in SmartFusion Devices and Table 2-14 • Different Components Contributing to the Static Power Consumption in SmartFusion Devices were updated.	2-13
	Figure 2-3 • Timing Model was updated.	2-21
	The temperature associated with the reliability for LVTTL/LVCMOS in Table 2-33 • I/O Input Rise Time, Fall Time, and Related I/O Reliability was changed from 110° to 100°.	2-31
	The values in Table 2-77 • Combinatorial Cell Propagation Delays were updated.	2-59
	Table 2-82 • Electrical Characteristics of the Low Power Oscillator is new. Table 2-81 • Electrical Characteristics of the Main Crystal Oscillator was revised.	2-64
	Table 2-87 • eNVM Block Timing, Worst Commercial Case Conditions: T_J = 85°C, VCC = 1.425 V and Table 2-88 • FlashROM Access Time, Worst Commercial Case Conditions: T_J = 85°C, VCC = 1.425 V are new.	2-77
	The performance tables in the "Programmable Analog Specifications" section were revised, including new data available. Table 2-95 • Analog Sigma-Delta DAC is new.	2-79
	The "256-Pin FBGA" table for A2F200 is new.	4-15

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "SmartFusion Device Status" table on page III, is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Production

This version contains information that is considered to be final.

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