

Low Voltage Adjustable Precision Shunt Regulator

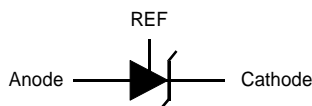
Features

- Precise Reference Voltage to 1.24V
- Guaranteed 0.5%, 1% or 1.5% Reference Voltage Tolerance
- Sink Current Capability, 80uA to 100mA
- Quick Turn-on
- Adjustable Output Voltage, $V_O = V_{REF}$ to 20V
- Low Operational Cathode Current, 80µA Typical
- 0.1Ω Typical Output Impedance
- SOT-23-3, SOT-23-5, TO-92 and SOT-89 Packages
- Lead Free and Green Devices Available (RoHS Compliant)

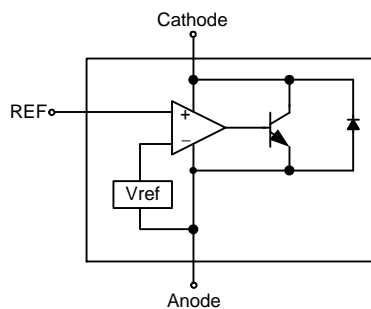
Applications

- Linear Regulators
- Adjustable Power Supply
- Switching Power Supply

Symbol



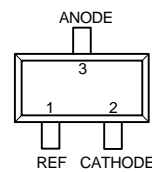
Functional Diagram



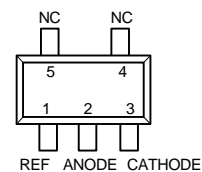
General Description

The APL431L is a 3-terminal low voltage adjustable precision reference with specified thermal stability over applicable commercial temperature ranges. Output voltage may be set to any value between V_{REF} (1.24 V) and 20 V with two external resistors (see Figure 2). When used with a photocoupler, the APL431L is an ideal voltage reference in isolated feedback circuits for 3V to 12V switching-mode power supplies. This device has a typical output impedance of 0.1W. Active output circuitry provides a very sharp turn-on characteristic, making the APL431L excellent replacements for zener diodes in many applications, including on-board regulation and adjustable power supplies.

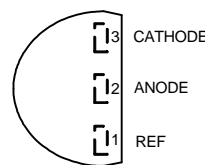
Pin Configuration



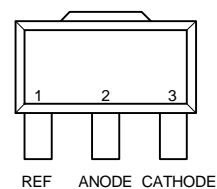
SOT-23-3 (Top View)



SOT-23-5 (Top View)



TO-92 (Top View)



SOT-89 (Top View)

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Electrical Characteristics $T_A = 25^\circ\text{C}$ (unless otherwise noted)

Symbol	Parameter	Test Conditions	APL431L			Unit	
			Min.	Typ.	Max.		
V_{REF}	Reference Voltage	$V_{KA}=V_{REF}, I_K=10\text{mA}$ $T_A = 25^\circ\text{C}$, (Fig. 1)	APL431LA	1.234	1.240	1.246	V
			APL431LB	1.228	1.240	1.252	
			APL431LC	1.223	1.240	1.258	
		$T_A = \text{full range}$ (see Note1), (Fig. 1)	APL431LA	1.222	1.240	1.258	
			APL431LB	1.215	1.240	1.265	
			APL431LC	1.212	1.240	1.262	
V_{DEF}	V_{DEF} Temp Deviation	$T_A = \text{full range}$ (see Note1) $V_{KA}=V_{REF}, I_K=10\text{mA}$ (Fig. 1)		5	15	mV	
$\frac{\Delta V_{REF}}{\Delta V_{KA}}$	Ratio of Change in V_{REF} to Change in Cathode Voltage	$I_K=10\text{mA}, V_{KA}=16\text{V}$ to V_{REF} (Fig. 2)		-0.2	-1.0	mV/V	
I_{REF}	Reference Input Current	$I_K=10\text{mA}, R_1=10\text{k}\Omega, R_2=\infty$ (Fig. 2)		0.15	0.5	μA	
$I_{REF(DEV)}$	I_{REF} Temp Deviation	$T_K = \text{full range}$ ^(Note 1) , $R_1=10\text{k}\Omega, R_2=\infty, I_K=10\text{mA}$, (Fig. 2)		0.05	0.3	μA	
$I_{K(off)}$	Off-State Cathode Current	$V_{REF}=0\text{V}$, (Fig. 3)	$V_{KA}=6\text{V}$		0.01	0.1	μA
			$V_{KA}=16\text{V}$		0.01	0.5	
Z_{KA}	Dynamic Output Impedance	$V_{KA}=V_{REF}, I_K=1\text{mA}$ to 100mA , $f \leq 1\text{kHz}$ (Fig. 1)		0.1	0.4	Ω	
$I_{K(MIN)}$	Minimum Operating Current	$V_{KA}=V_{REF}$ (Fig. 1)		80	100	μA	

Note 1 : Full temperature range is 0°C to 70°C for APL431LXXC, and -40°C to 85°C for APL431LXXI.

Test Figures

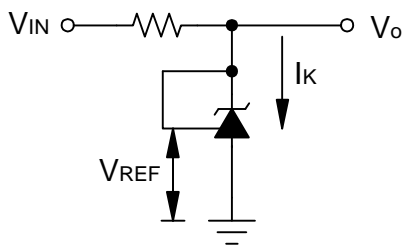


Figure 1. Test Circuit for $V_{KA}=V_{REF}, V_O=V_{KA}=V_{REF}$

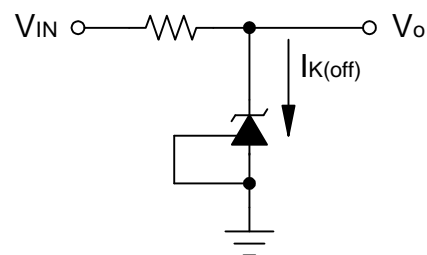


Figure 2. Test Circuit for $I_{K(off)}$

Test Figures (Cont.)

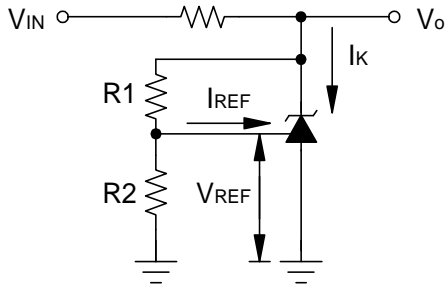
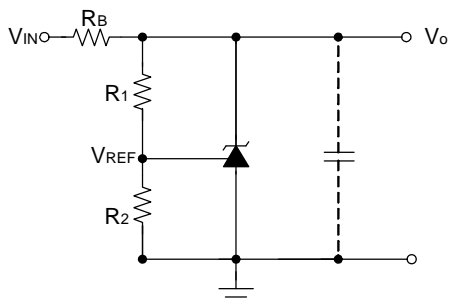
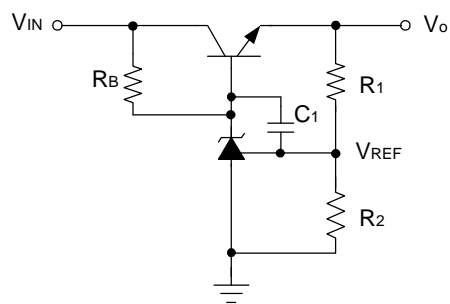


Figure 3. Test Circuit for $V_{KA} > V_{REF}$
 $V_O = V_{KA} = V_{REF} \times (1 + R_1/R_2) + I_{REF} \times R_1$

Application Circuits



Precision Voltage Reference



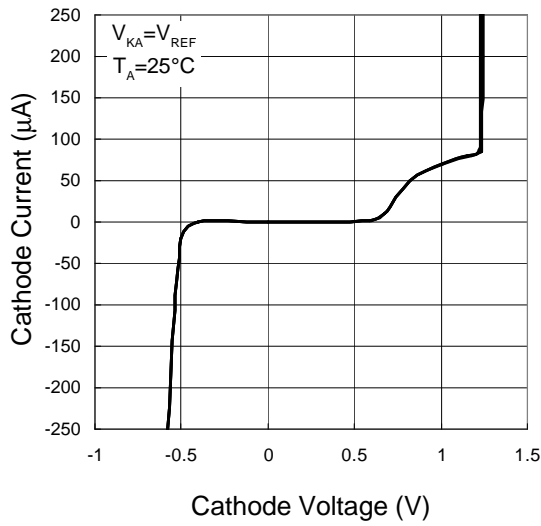
Precision High-Current Series Regulator

Notes for Application Circuits:

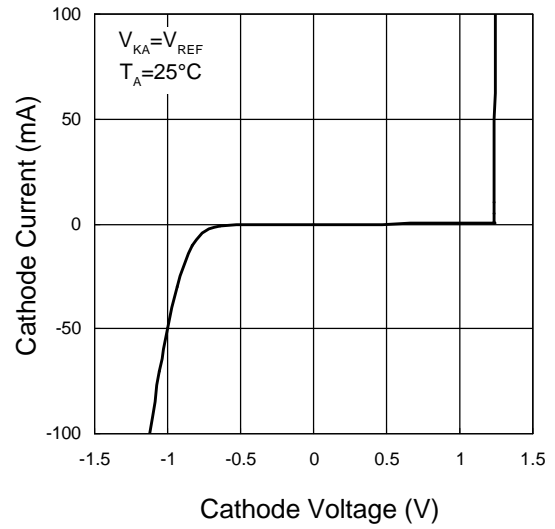
- 1) For the series regulator applications, add a compensation capacitor C1 between CATHODE and REF is strongly recommended to improve the stability of output voltage .
- 2) Set V_O according to the following equation: $V_O = V_{REF}(1 + R_1/R_2) + I_{REF} \times R_1$
- 3) Choose the value for R_B as follows:
 - A) The maximum limit for R_B should be such that the cathode current (I_k) is greater than the minimum operating current (80µA) at $V_{IN(MIN)}$.
 - B) The minimum limit for R_B should be such that the cathode current (I_k) does not exceed 100mA under all load conditions, and the instantaneous turn-on value for I_k does not exceed 150mA.

Typical Characteristics

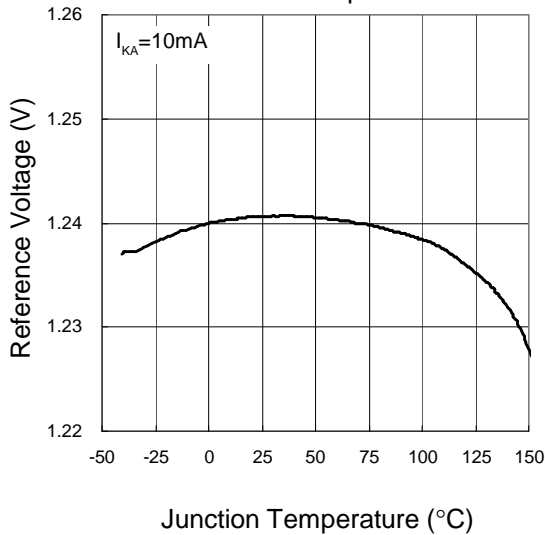
Cathode Current vs. Cathode Voltage



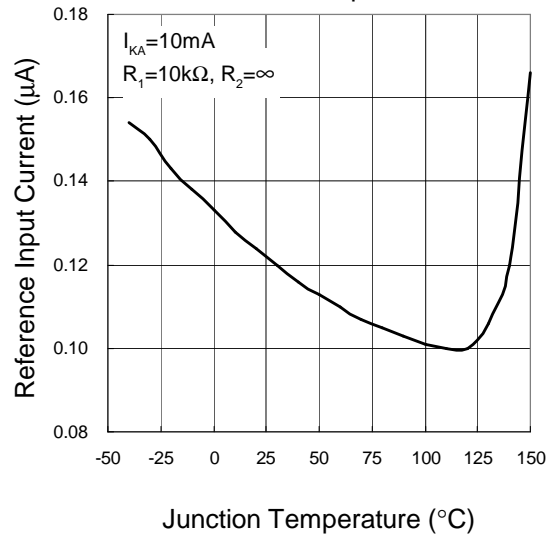
Cathode Current vs. Cathode Voltage



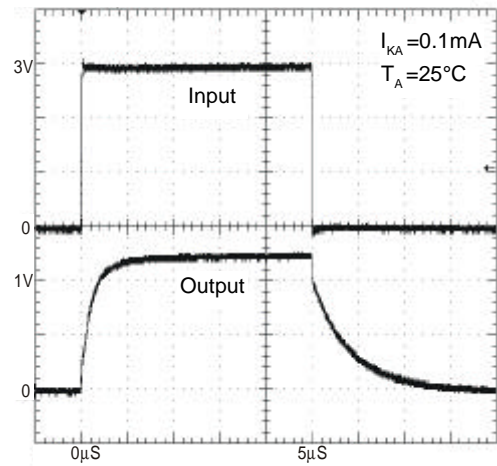
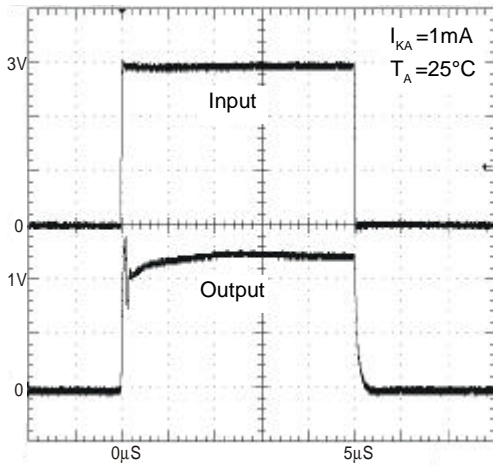
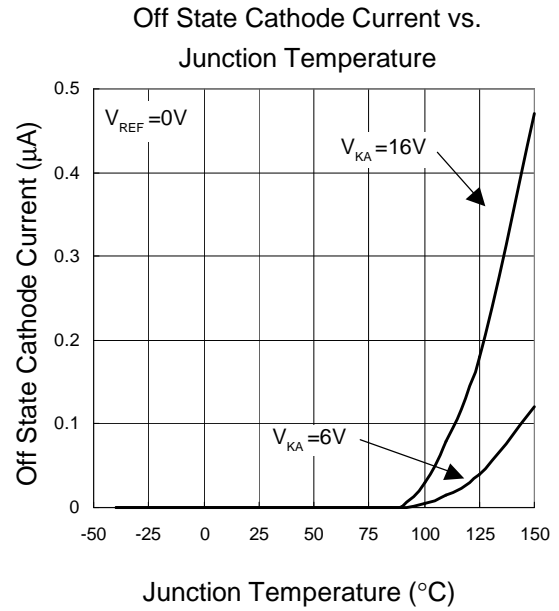
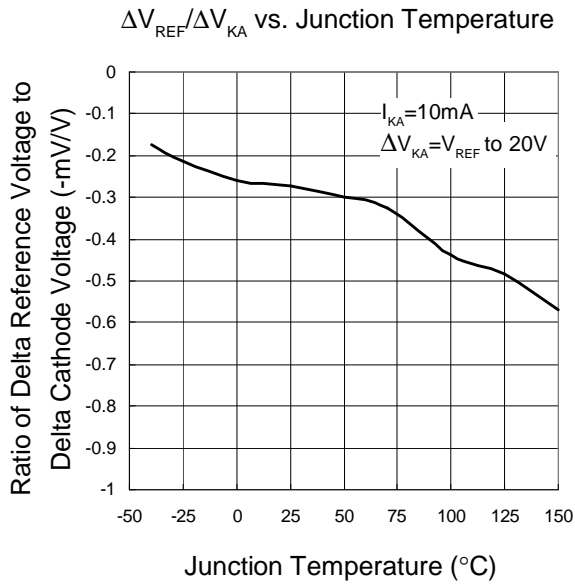
Reference Voltage vs. Junction Temperature



Reference Input Current vs. Junction Temperature

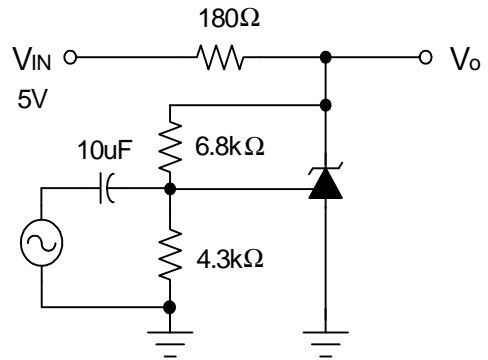
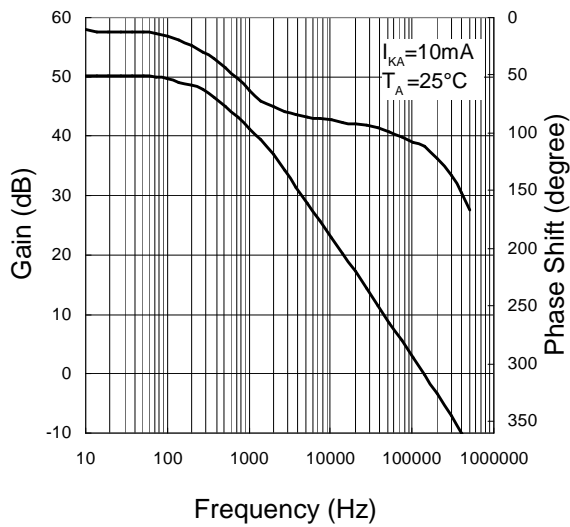


Typical Characteristics



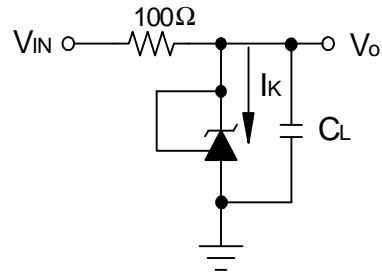
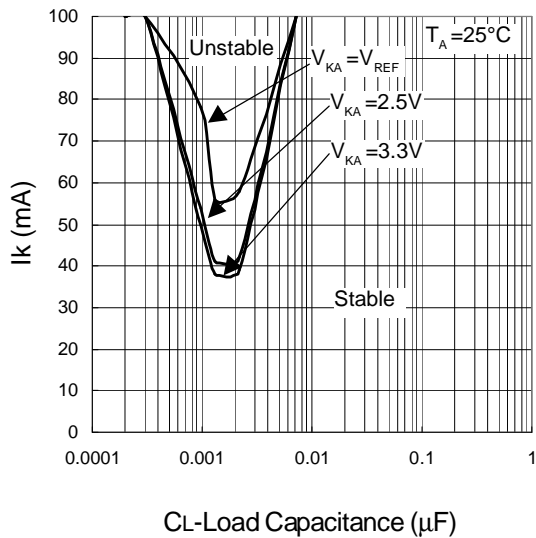
Typical Characteristics

Gain vs. Phase Shift vs. Frequency

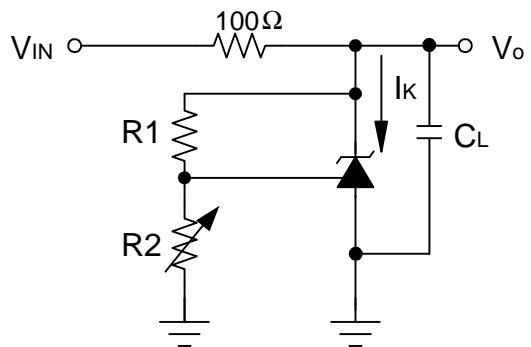


Gain & Phase Test Circuit

Stability Boundary Conditions

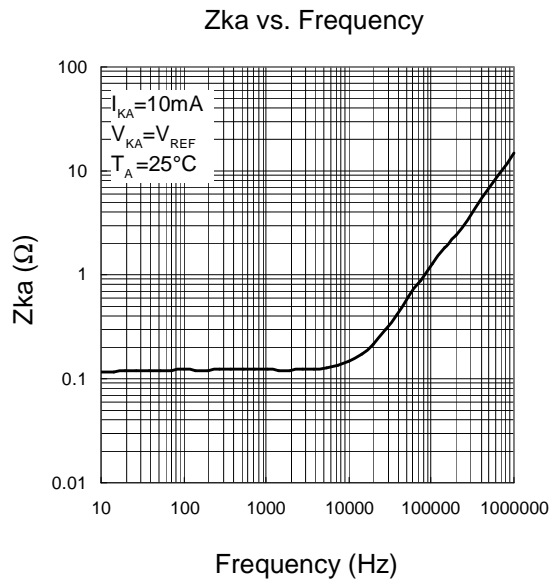


Stability Test Circuit for $V_{KA} = V_{REF}$



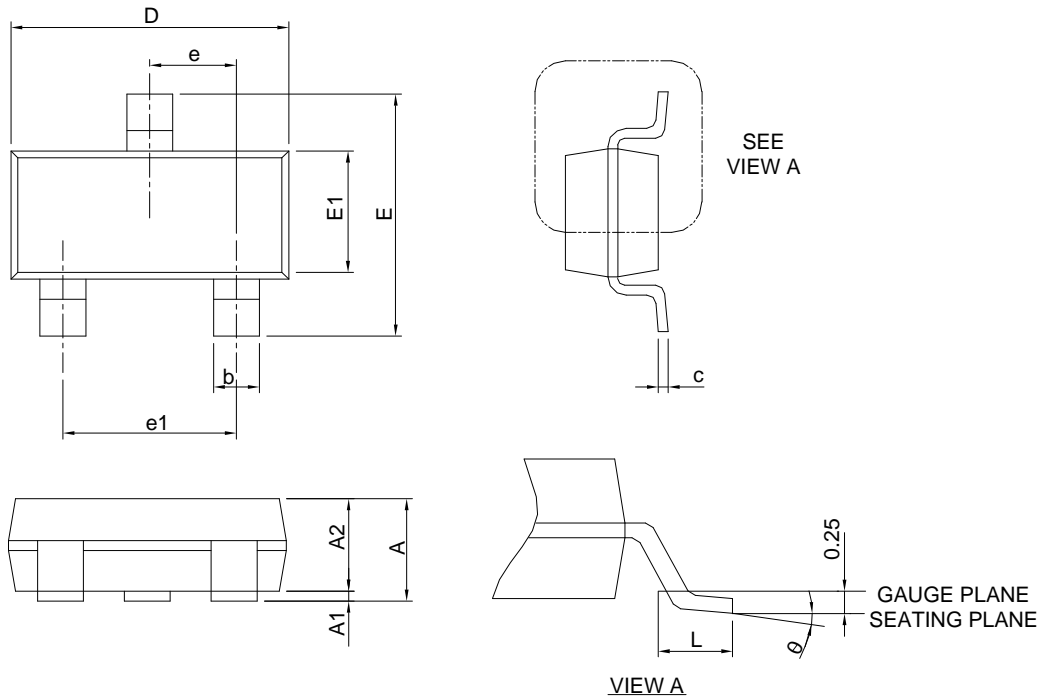
Stability Test Circuit for $V_{KA} > V_{REF}$
 $V_O = V_{KA} = V_{REF} \times (1 + R_1/R_2) + I_{REF} \times R_1$
 Use the MLCC for CL

Typical Characteristics



Package Information

SOT-23-3

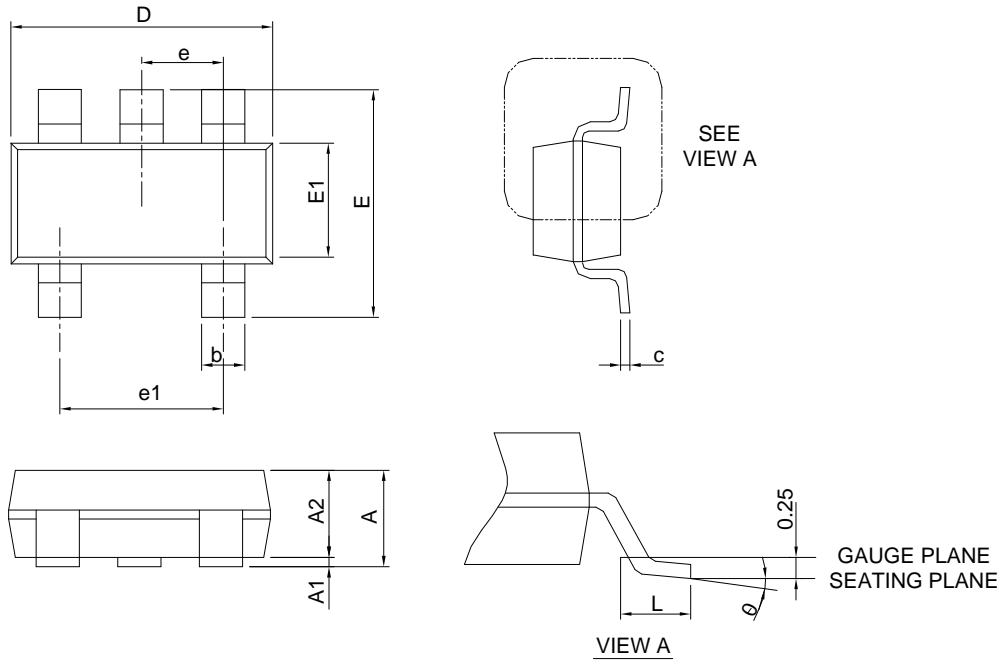


SYMBOL	SOT-23			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.45		0.057
A1	0.00	0.15	0.000	0.006
A2	0.90	1.30	0.035	0.051
b	0.30	0.50	0.012	0.020
c	0.08	0.22	0.003	0.009
D	2.70	3.10	0.106	0.122
E	2.60	3.00	0.102	0.118
E1	1.40	1.80	0.055	0.071
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.30	0.60	0.012	0.024
theta	0°	8°	0°	8°

Note : Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.

Package Information

SOT-23-5

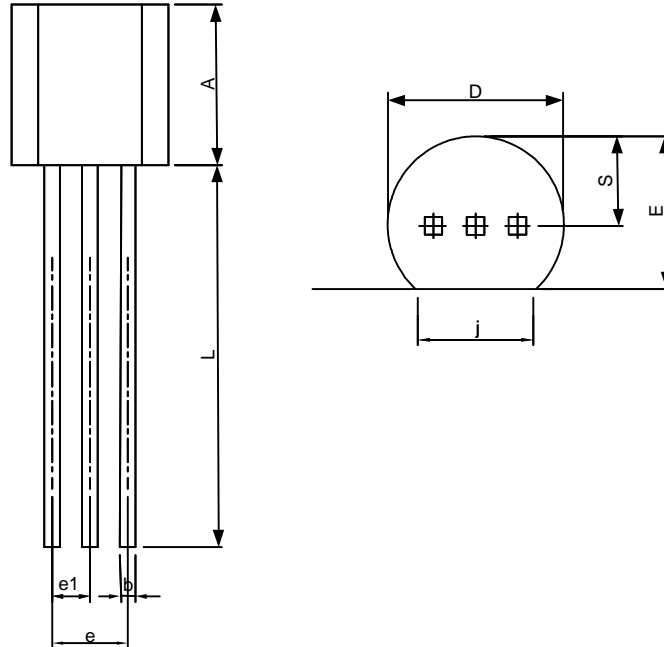


SYMBOL	SOT-23-5			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.45		0.057
A1	0.00	0.15	0.000	0.006
A2	0.90	1.30	0.035	0.051
b	0.30	0.50	0.012	0.020
c	0.08	0.22	0.003	0.009
D	2.70	3.10	0.016	0.122
E	2.60	3.00	0.102	0.118
E1	1.40	1.80	0.055	0.071
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

Note : 1. Follow JEDEC TO-178 AA.
 2. Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.

Package Information

TO-92

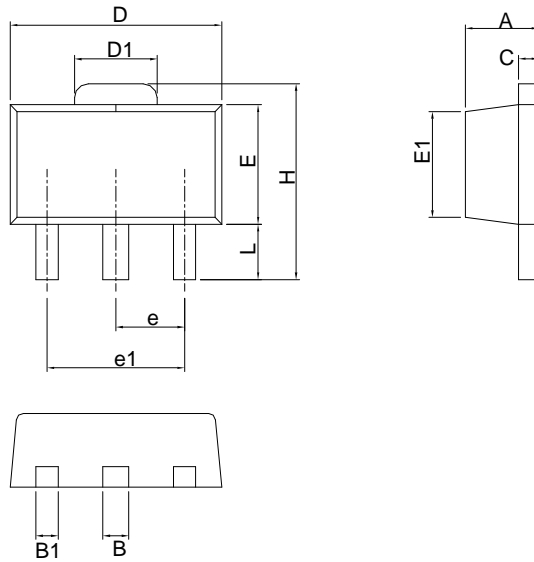


SYMBOL	TO-92			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.32	5.33	0.170	0.210
b	0.41	0.53	0.016	0.021
D	4.45	5.20	0.175	0.205
E	3.18	4.19	0.125	0.165
e	2.42	2.66	0.095	0.105
e1	1.15	1.39	0.045	0.055
j	3.43	4.00	0.135	0.157
L	12.70	15.00	0.500	0.591
S	2.03	2.66	0.080	0.105

Note : Follow JEDEC TO-92.

Package Information

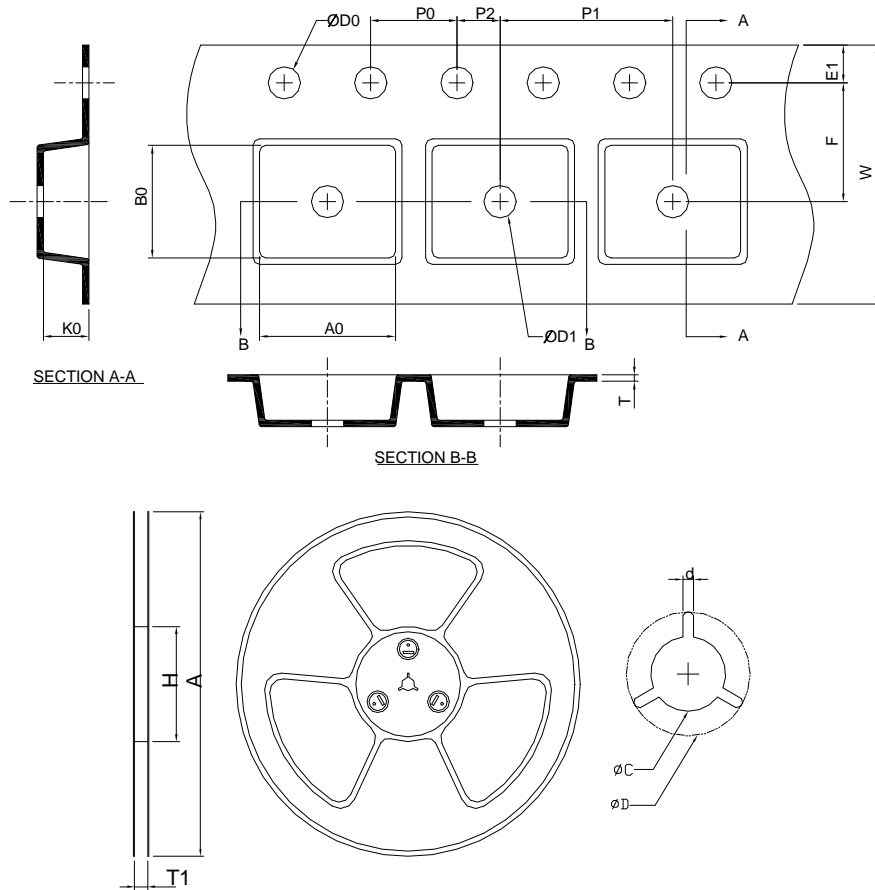
SOT-89



SYMBOL	SOT-89			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	1.40	1.60	0.055	0.063
B	0.44	0.56	0.017	0.022
B1	0.36	0.48	0.014	0.019
C	0.35	0.44	0.014	0.017
D	4.40	4.60	0.173	0.181
D1	1.62	1.83	0.064	0.072
E	2.29	2.60	0.090	0.102
E1	2.13	2.29	0.084	0.090
e	1.50 BSC		0.059 BSC	
e1	3.00 BSC		0.118 BSC	
H	3.94	4.25	0.155	0.167
L	0.89	1.20	0.035	0.047

Note : Follow JEDEC TO-243 AA.

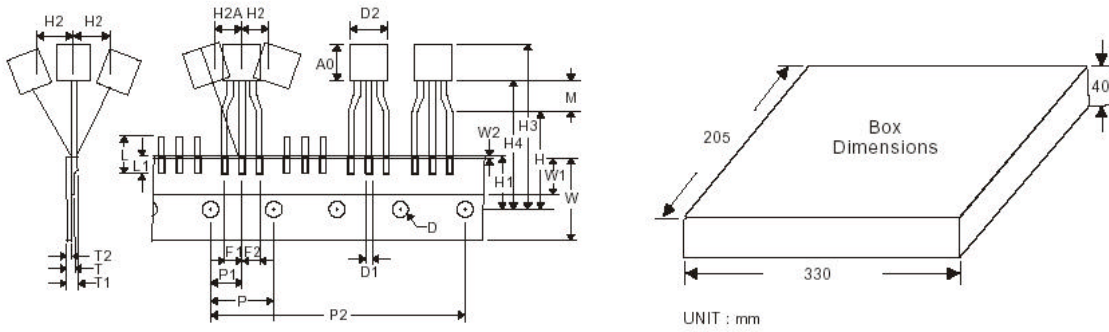
Carrier Tape & Reel Dimensions



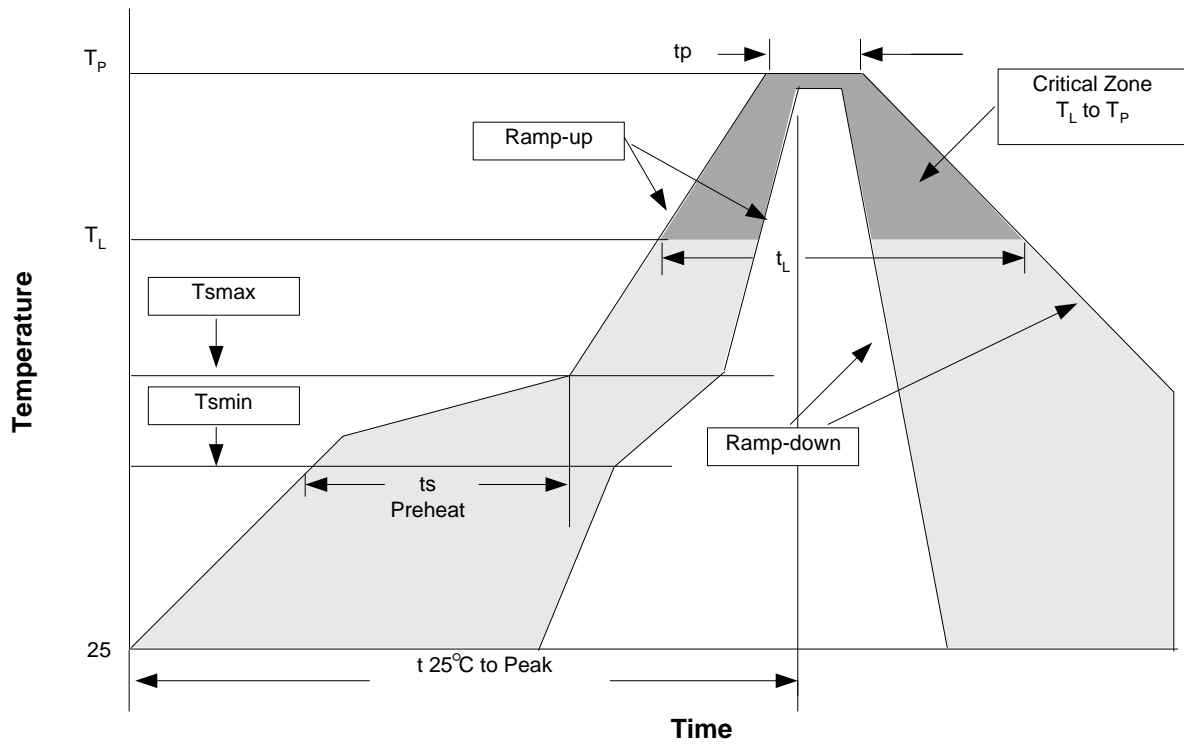
Application	A	H	T1	C	d	D	W	E1	F
SOT-23-3	178.0 ±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0 ±0.30	1.75 ±0.10	3.5 ±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0 ±0.10	4.0 ±0.10	2.0 ±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.20 ±0.20	3.10 ±0.20	1.50 ±0.20
Application	A	H	T1	C	d	D	W	E1	F
SOT-89	178.0 ±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0 ±0.30	1.75 ±0.10	5.50 ±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0 ±0.10	8.0 ±0.10	2.0 ±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	4.80 ±0.20	4.50 ±0.20	1.80 ±0.20
Application	A	H	T1	C	d	D	W	E1	F
SOT-23-5	178.0 ±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0 ±0.30	1.75 ±0.10	3.5 ±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0 ±0.10	4.0 ±0.10	2.0 ±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.20 ±0.20	3.10 ±0.20	1.50 ±0.20

(mm)

Carrier Tape & Box Dimensions



Reflow Condition (IR/Convection or VPR Reflow)



Devices Per Unit

Package Type	Unit	Quantity
SOT-23-3	Tape & Reel	3000
SOT-89	Tape & Reel	1000
SOT-23-5	Tape & Reel	3000
TO-92	Tape & Box	2000

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C, 5 sec
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @125°C
PCT	JESD-22-B, A102	168 Hrs, 100%RH, 121°C
TST	MIL-STD-883D-1011.9	-65°C~150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms, 1 _{tr} > 100mA

Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T _L to T _P)	3°C/second max.	3°C/second max.
Preheat	100°C	150°C
- Temperature Min (T _{smin})	150°C	200°C
- Temperature Max (T _{smax})	60-120 seconds	60-180 seconds
- Time (min to max) (t _s)		
Time maintained above:	183°C	217°C
- Temperature (T _L)	60-150 seconds	60-150 seconds
- Time (t _L)		
Peak/Classification Temperature (T _p)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (t _p)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Note: All temperatures refer to topside of the package. Measured on the body surface.

Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm ³ <350	Volume mm ³ ≥350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm ³ <350	Volume mm ³ 350-2000	Volume mm ³ >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*

* Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.

Customer Service

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