ADVANCE INFORMATION

CYM9291

1M x 36 Pipelined NoBL™ SRAM Module

Features

- **Operates at 133 MHz**
- **Uses 512K x 18 high-performance Pipelined NoBL™ synchronous SRAMs**
- **2.5V data inputs/outputs**

Functional Description

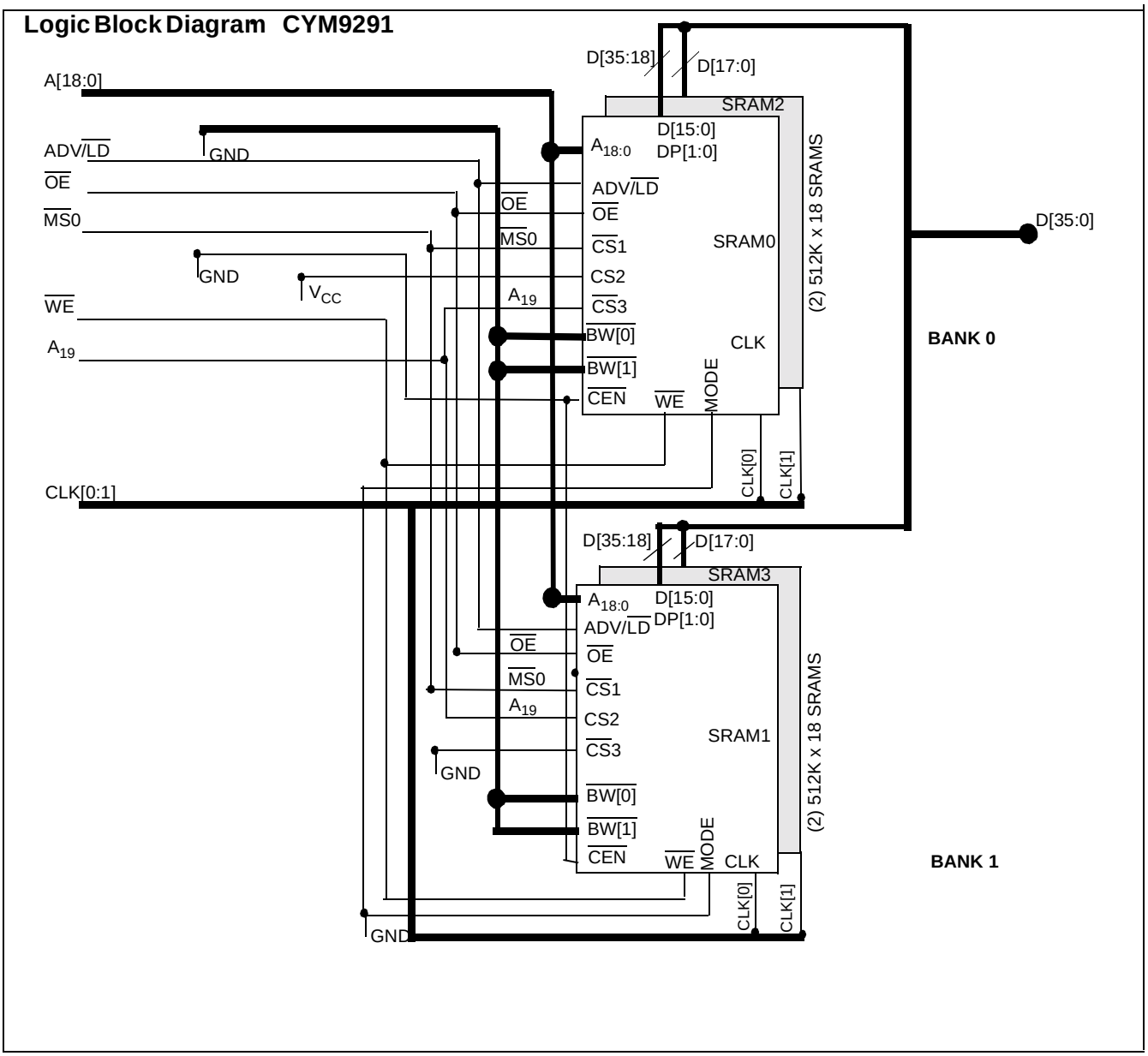
The CYM9291 is a high-performance synchronous pipelined NoBL memory module organized as 1M by 36 bits. These modules are constructed from 512K x 18 NoBL SRAMs in plastic surface mount packages on an epoxy laminate board with pins. The modules are designed to be incorporated into large memory arrays.

The module is configured as two banks, where each bank has separate chip select controls. Separate clocks are provided for every pair of SRAMs.

Multiple ground pins and on-board decoupling capacitors ensure high performance with maximum noise immunity.

All components on the modules are surface mounted on a multi-layer epoxy laminate (FR-4) substrate.

Logic Block Diagram CYM9291



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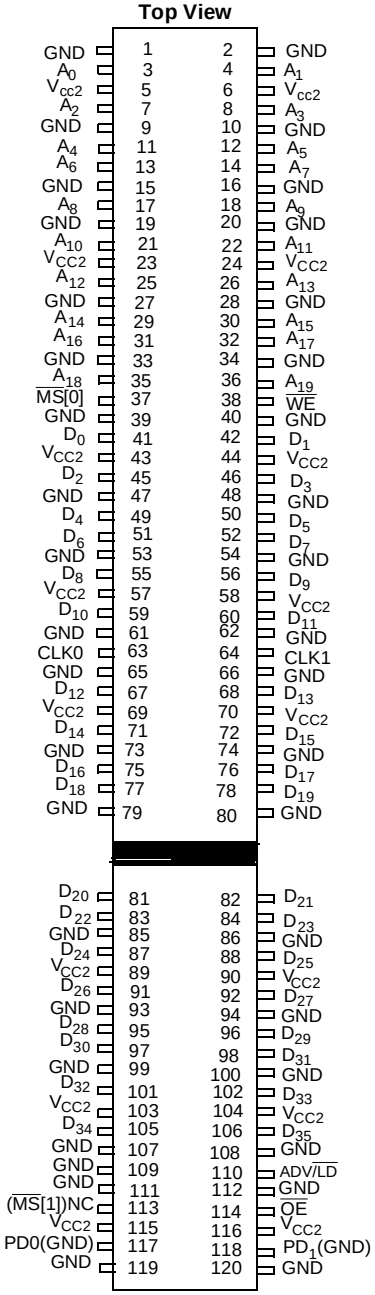
Selection Guide

NoBL Pipelined Module				
Part Number	**Cache Size**	**SRAM's Used**	**System Clock (MHz)**	**Data t_{CDV}**
CYM9291PZ-133	1M x 36	4 of 512K x 18(TQFP)	133	4.4 ns
CYM9291PZ-117	1M x 36	4 of 512K x 18(TQFP)	117	4.8ns

Pin Configuration

Dual Read-Out ZIP
Top View



Pin Definitions

Signal	Description
V_{CC2}	2.5V Supply
GND	Ground
A[19:0]	Addresses from processor
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{MS}$[0]	Chip Select for the module
PD_0–PD_1	Presence Detect output pins
D[35:0]	Data lines from processor
CLK[0:1]	Clock lines to the module
ADV/$\overline{LD}$	Advance Load Signal from processor
NC	Signal not connected on module
NC(Pin 113)	Reserved for Depth expansion
RSVD	Reserved

Presence Detect Pins

	PD_1	PD_0
CYM9291PZ - 1M x 36	GND	GND

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –55°C to +125°C

Ambient Temperature with Power Applied..... 0°C to +70°C

Supply Voltage to Ground Potential ..... –0.3V to +3.6V

DC Voltage Applied to Outputs in High Z State ..... –0.3V to +3.6V

DC Input Voltage ..... –0.5V to +3.6V

Output Current into Outputs (LOW)..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	2.5V ± 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Condition	Min.	Max.	Unit
V_{IH}	Input HIGH Voltage		1.7	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage		–0.3	0.7	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min. I_{OH} = –1 mA	2.0		V
V_{OL}	Output LOW Voltage	V_{CC} = Min. I_{OL} = 1 mA		0.2	V
I_{CC} (9291)	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT}=0 mA, f=f_{MAX}=1/t_{RC}		1680	mA

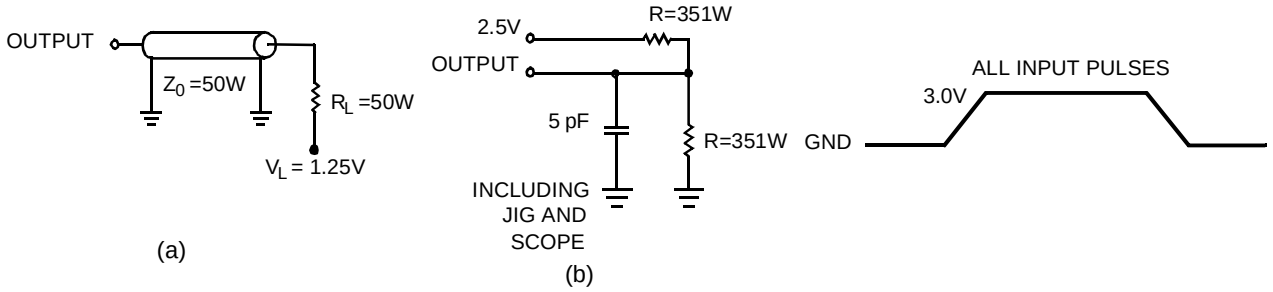
Capacitance[1]

Parameter	Description	Test Conditions	Max.	Unit
C_A	Address Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 2.5 V	24	pF
C_I	Control Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 2.5 V	24	pF
C_O	Input/Output Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 2.5 V	16	pF
C_{CLK}	Clock Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 2.5 V	6	pF

Note:

1. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Switching Characteristics Over the Operating Range[2]

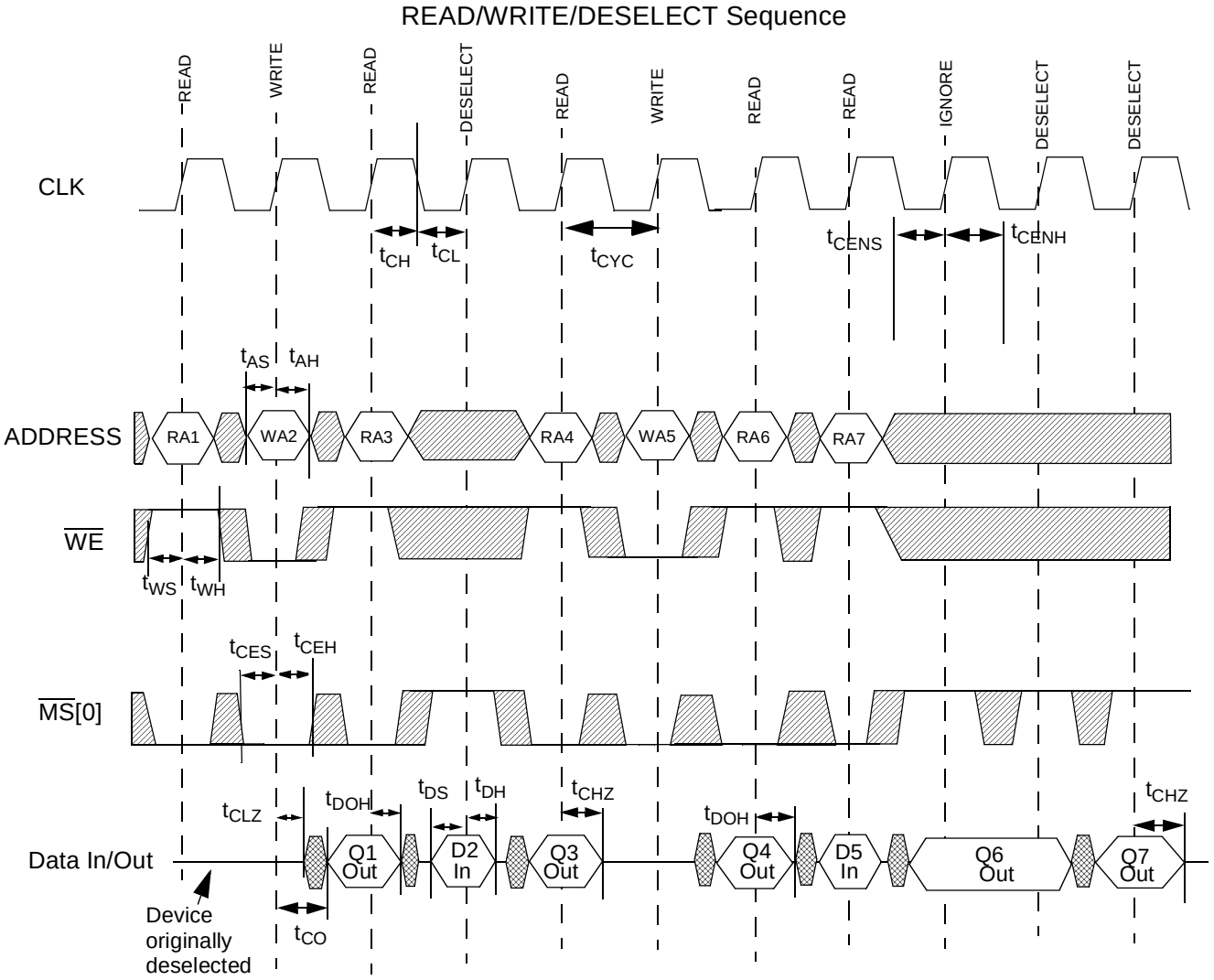
		133		117		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
Clock						
t_{CYC}	Clock Cycle Time	7.5		8.6		ns
F_{MAX}	Maximum Operating Frequency		133		117	MHz
t_{CH}	Clock HIGH	2.5		3		ns
t_{CL}	Clock LOW	2.5		3		ns
Output Times						
t_{CDV}	Data Output Valid After CLK Rise		4.4		4.8	ns
t_{EOV}	$\overline{OE}$ LOW to Output Valid[3, 5]		4.4		4.8	ns
t_{DOH}	Data Output Hold After CLK Rise	2.3		2.3		ns
t_{CHZ}	Clock to High-Z[3, 4, 5]		3. 8		3.8	ns
t_{CLZ}	Clock to Low-Z[3, 4, 5]	2.3		2.3		ns
t_{EOHZ}	$\overline{OE}$ HIGH to Output High-Z[3, 4, 5]		3.8		3.8	ns
t_{EOLZ}	$\overline{OE}$ LOW to Output Low-Z[3, 4, 5]	0		0		ns
Set-up Times						
t_{AS}	Address Set-Up Before CLK Rise	1.5		1.5		ns
t_{DS}	Data Input Set-Up Before CLK Rise	1.5		1.5		ns
t_{WES}	$\overline{WE}$ Set-Up Before CLK Rise	1.5		1.5		ns
t_{ALS}	ADV/$\overline{LD}$ Set-Up Before CLK Rise	1.5		1.5		ns
t_{CES}	Chip Selects Set-Up	1.5		1.5		ns
Hold Times						
t_{AH}	Address Hold After CLK Rise	0.5		0.5		ns
t_{DH}	Data Input Hold After CLK Rise	0.5		0.5		ns
t_{WEH}	$\overline{WE}$ Hold After CLK Rise	0.5		0.5		ns
t_{ALH}	ADV/$\overline{LD}$ Hold after CLK Rise	0.5		0.5		ns
t_{CEH}	Chip Selects Hold After CLK Rise	0.5		0.5		ns

Notes:

2. A/C test conditions assume signal transition time of 2 ns or less, timing reference levels, input pulse levels and output loading shown in AC Test Load for 2.5V devices.
3. t_{CHZ}, t_{CLZ}, t_{OEV}, t_{EOLZ}, and t_{EOHZ} are specified with AC test conditions shown in part (a) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
4. At any given voltage and temperature, t_{EOHZ} is less than t_{EOLZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High-Z prior to Low-Z under the same system conditions.
5. This parameter is sampled and not 100% tested.

Switching Waveforms

Read/Write/Deselect Timing

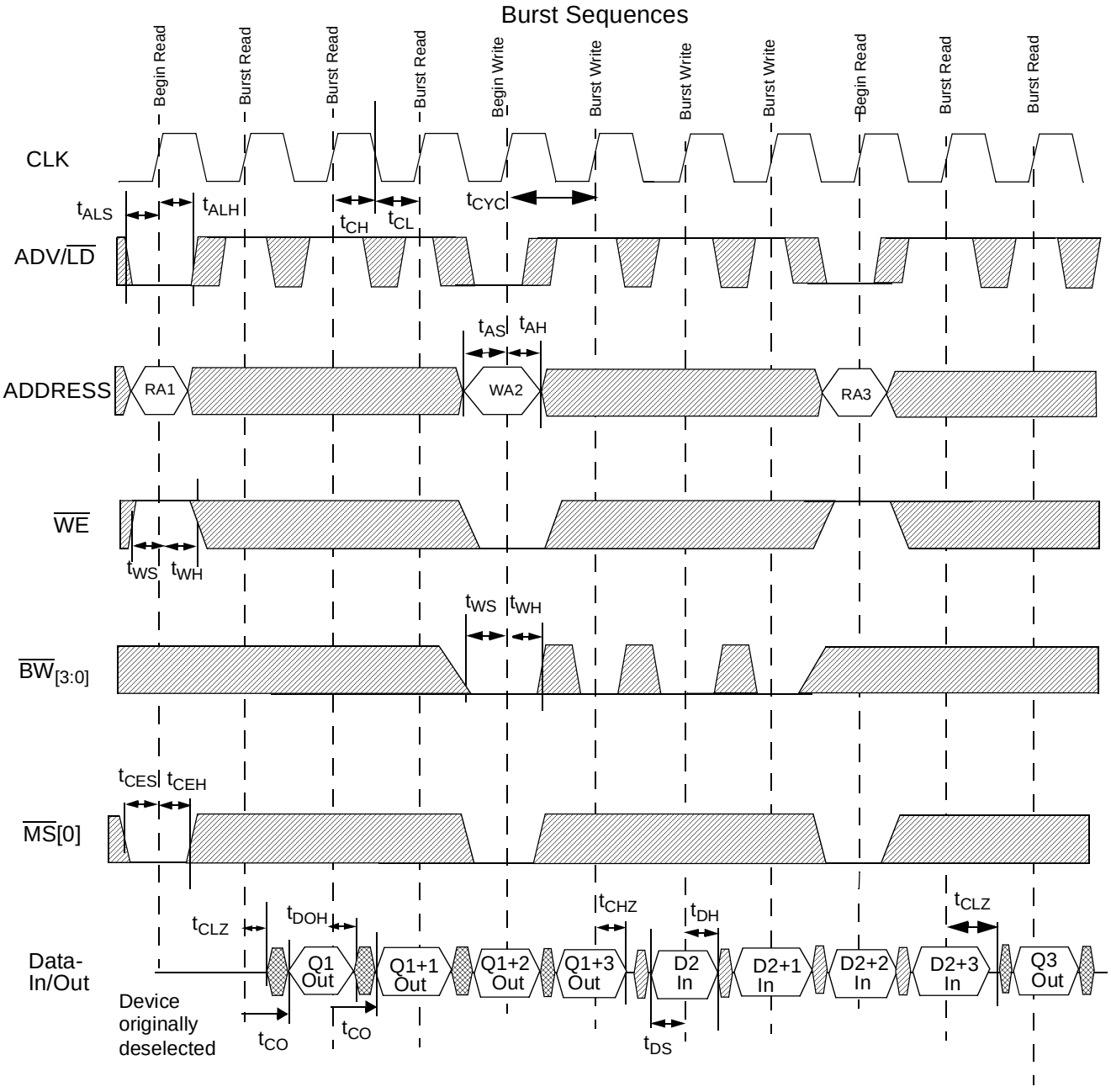


All chip enables need to be active in order to select the device. Any chip enable can deselect the device. RAx stands for Read Address X, WAx stands for Write Address X, Dx stands for Data-in for location X, Qx stands for Data-out for location X. ADV/$\overline{LD}$ held LOW. $\overline{OE}$ held LOW.

= DON'T CARE = UNDEFINED

Switching Waveforms (continued)

Burst Timing

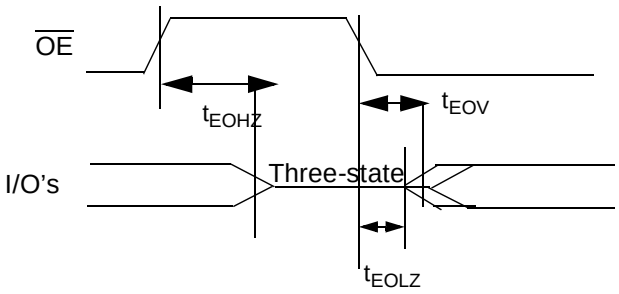


All chip enables need to be active in order to select the device. Any chip enable can deselect the device. RAx stands for Read Address X, WA stands for Write Address X, Dx stands for Data-in for location X, Qx stands for Data-out for location X. $\overline{CEN}$ held LOW. During burst writes, byte writes can be conducted by asserting the appropriate $\overline{BW}_{[3:0]}$ input signals. Burst order determined by the state of the Mode input. $\overline{OE}$ held LOW.

= DON'T CARE = UNDEFINED

Switching Waveforms (continued)

$\overline{OE}$ Timing



Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Description	Operating Range
133	CYM9291PZ-133C	PZxx	120-Pin ZIP	Pipelined NoBL 1M x 36	Commercial
117	CYM9291PZ-117C	PZxx	120-Pin ZIP	Pipelined NoBL 1M x 36	

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Package Diagrams

PZ13: 120 Pin Dual Sided ZIP Module