

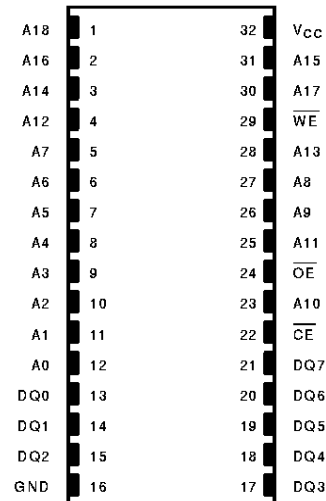
# DALLAS SEMICONDUCTOR

## DS1650Y/AB, DS1650YLPM/ABLPM Partitionable 4096K NV SRAM

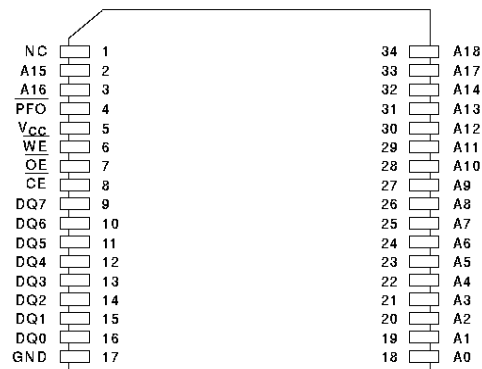
### FEATURES

- Data retention in the absence of  $V_{CC}$
- Data is automatically protected during power loss
- Directly replaces 512K x 8 volatile static RAM or EEPROM
- Write protects selected blocks of memory regardless of  $V_{CC}$  status when programmed
- Unlimited write cycles
- Low-power CMOS operation
- Over 10 years of data retention
- Standard 32-pin JEDEC pinout (DS1650Y/AB)
- Available in access times as fast as 70 ns
- Read cycle time equals write cycle time
- Full  $\pm 10\%$  operating range (DS1650Y and DS1650YLPM)
- Optional  $\pm 5\%$  operating range (DS1650AB and DS1650ABLPM)
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time.
- Optional industrial temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , designated IND
- Optional low profile module (LPM)
  - Fits into standard 68-pin PLCC surface mountable socket
  - 255 mils package height
  - Power fail output warns processor of impending power failure

### PIN ASSIGNMENT



32-PIN ENCAPSULATED PACKAGE  
(740 MIL EXTENDED)



34-PIN LOW PROFILE MODULE (LPM)

**PIN DESCRIPTION**

A0 - A18	-	Address Inputs
$\overline{CE}$	-	Chip Enable
GND	-	Ground
DQ0 - DQ7	-	Data In/Data Out
$V_{CC}$	-	Power (+5V)
$\overline{WE}$	-	Write Enable
$\overline{OE}$	-	Output Enable
NC	-	No Connect

**ORDERING INFORMATION**

DS1650YAB-XXX	32-pin thru-hole module
└─70	70 ns access
└─85	85 ns access
└─100	100 ns access
DS1650ABLPM-XXX	34-pin low profile module
└─70	70 ns access
└─100	100 ns access
DS1650Y-XXX	32-pin thru-hole module
└─70	70 ns access
└─85	85 ns access
└─100	100 ns access
DS1650YLPM-XXX	34-pin low profile module
└─70	70 ns access
└─100	100 ns access

**DESCRIPTION**

The DS1650Y/AB 4096K Nonvolatile SRAM is a 4,194,304 bit, fully static, nonvolatile SRAM organized as 524,288 words by 8 bits. The DS1650Y/AB has a self-contained lithium energy source and control circuitry which constantly monitors  $V_{CC}$  for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. In addition the device has the ability to unconditionally write protect blocks of memory so that inadvertent write cycles do not corrupt program and special data space. There is no limit on the number of write cycles which can be executed and no additional support circuitry is required for microprocessor interface. The nonvolatile static RAM can be used in place of existing 512K x 8 static RAM directly conforming to the popular byte-wide 32-pin DIP standard. The DS1650YLPM/ABLPM is a low profile module that fits into a standard 68-pin PLCC surface mountable socket and is functionally equivalent to the DS1650Y/AB. The DS1650YLPM/ABLPM also provides a power fail output that warns a processor of impending power failure.

**OPERATION - READ MODE**

The DS1650Y/AB executes a read cycle whenever  $\overline{WE}$  (Write Enable) is inactive (high) and  $\overline{CE}$  (Chip Enable) is active (low). The unique address specified by the 19 address inputs (A<sub>0</sub> - A<sub>18</sub>) defines which of the 524,288 bytes of data is accessed. Valid data will be available to the eight data output drivers within  $t_{ACC}$  (Access Time) after the last address input signal is stable, providing that  $\overline{CE}$  and  $\overline{OE}$  access times are also satisfied. If  $\overline{OE}$  and  $\overline{CE}$  access times are not satisfied, then data access must be measured from the later occurring signal ( $\overline{CE}$  or  $\overline{OE}$ ) and the limiting parameter is either  $t_{CO}$  for  $\overline{CE}$  or  $t_{OE}$  for  $\overline{OE}$  rather than address access.

**OPERATION - WRITE MODE**

The DS1650Y/AB is in the write mode whenever the  $\overline{WE}$  and  $\overline{CE}$  signals are in the active (low) state after address inputs are stable. The later occurring falling edge of  $\overline{CE}$  or  $\overline{WE}$  will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of  $\overline{CE}$  or  $\overline{WE}$ . All address inputs must be kept valid throughout the write cycle.  $\overline{WE}$  must return to the high state for a minimum recovery time ( $t_{WR}$ ) before another cycle can be initiated. The  $\overline{OE}$  control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ( $\overline{CE}$  and  $\overline{OE}$  active) then  $\overline{WE}$  will disable the outputs in  $t_{ODW}$  from its falling edge.

**DATA RETENTION MODE**

The DS1650Y provides full functional capability for  $V_{CC}$  greater than 4.5 volts and write protects by 4.37 volts nominal ( $V_{CC}$  greater than 4.75V and write protect at 4.62V nominal for DS1650AB). Data is maintained in the absence of  $V_{CC}$  without any additional support circuitry. The DS1650Y/AB constantly monitors  $V_{CC}$ . Should the supply voltage decay, the RAM will automatically write protect itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As  $V_{CC}$  falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when  $V_{CC}$  rises above approximately 3.0 volts, the power switching circuit connects external  $V_{CC}$  to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after  $V_{CC}$  exceeds 4.5 volts (4.75 volts for the DS1650AB).

### FRESHNESS SEAL AND SHIPPING

The N1LY/AB is shipped from Dallas Semiconductor with the lithium energy source disconnected, guaranteeing full energy capacity. When  $V_{CC}$  is applied at a level of greater than  $V_{TP}$ , the lithium energy source is enabled for battery backup operation.

### PARTITION PROGRAMMING MODE

The register controlling the partition switch is selected by recognition of a specific binary pattern which is sent on address lines A15 - A18. These address lines are the four upper order address lines being sent to RAM. The pattern is sent by 20 consecutive read cycles with the exact pattern as shown in Table 1. Pattern matching must be accomplished using read cycles; any write cycles will reset the pattern matching circuitry. If this pattern is matched perfectly, then the 21st through 24th

read cycle will load the partition switch. Since there are 16 possible write protected partitions the size of each partition is 512K/16 or 32K x 8. Each partition is represented by one of the 16 bits contained in the 21st through 24th read cycle as defined by A15 through A18 and shown in Table 2. A logical 1 in a bit location sets that partition to write protect. A logical 0 in a bit location disables write protection. For example, if during the pattern match sequence bit 22 on address pin A16 were a 1, this would cause the partition register location for partition 5 to be set to a 1. This in turn would cause the N1LY/AB to inhibit  $\overline{WE}$  internally when A18 A17 A16 A15=0101. Note that while setting the partition register, data which is being accessed from the RAM should be ignored as the purpose of the 24 read cycles is to set the partition switch and not for the purpose of accessing data from RAM.

**PATTERN MATCH TO WRITE PARTITION REGISTER** Table 1

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A15	1	0	1	1	1	1	0	0	1	1	1	0	0	0	0	0	1	1	0	1	X	X	X	X
A16	1	1	1	1	1	0	0	1	1	1	0	0	1	0	1	1	0	0	0	0	X	X	X	X
A17	1	1	1	1	0	0	1	1	1	0	0	1	0	1	0	1	0	0	0	1	X	X	X	X
A18	1	1	0	0	0	1	1	1	0	0	1	0	0	0	1	0	1	0	0	0	X	X	X	X

↙ FIRST BITS ENTERED

↘ LAST GROUP ENTERED

**PARTITION REGISTER MAPPING** Table 2

Address Pin	Bit number in pattern match sequence	Partition Number	Address State Affected (A <sub>18</sub> A <sub>17</sub> A <sub>16</sub> A <sub>15</sub> )
A15	BIT 21	PARTITION 0	0000
A16	BIT 21	PARTITION 1	0001
A17	BIT 21	PARTITION 2	0010
A18	BIT 21	PARTITION 3	0011
A15	BIT 22	PARTITION 4	0100
A16	BIT 22	PARTITION 5	0101
A17	BIT 22	PARTITION 6	0110
A18	BIT 22	PARTITION 7	0111
A15	BIT 23	PARTITION 8	1000
A16	BIT 23	PARTITION 9	1001
A17	BIT 23	PARTITION 10	1010
A18	BIT 23	PARTITION 11	1011
A15	BIT 24	PARTITION 12	1100
A16	BIT 24	PARTITION 13	1101
A17	BIT 24	PARTITION 14	1110
A18	BIT 24	PARTITION 15	1111

**ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature	0°C to 70°C, -40°C to +85°C for ind parts
Storage Temperature	-40°C to +70°C, -40°C to +85°C for ind parts
Soldering Temperature	260°C for 10 seconds

\* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS**

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1650Y Power Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V	
DS1650AB Power Supply Voltage	V <sub>CC</sub>	4.75	5.0	5.25	V	
Logic 1	V <sub>IH</sub>	2.2		V <sub>CC</sub>	V	
Logic 0	V <sub>IL</sub>	0.0		+0.8	V	

(0°C to 70°C; V<sub>CC</sub>=5V ± 5% for DS1650AB)(0°C to 70°C; V<sub>CC</sub>=5V ± 10% for DS1650Y)**DC ELECTRICAL CHARACTERISTICS**

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I <sub>IL</sub>	-1.0		+1.0	μA	
I/O Leakage Current CE ≥ V <sub>IH</sub> ≤ V <sub>CC</sub>	I <sub>IO</sub>	-1.0		+1.0	μA	
Output Current @ 2.4V	I <sub>OH</sub>	-1.0			mA	
Output Current @ 0.4V	I <sub>OL</sub>	2.0			mA	15
Standby Current CE = 2.2V	I <sub>CCS1</sub>		5.0	10.0	mA	
Standby Current CE = V <sub>CC</sub> - 0.5V	I <sub>CCS2</sub>		3.0	5.0	mA	
Operating Current	I <sub>CCO1</sub>			85	mA	
Write Protection Voltage (DS1650Y)	V <sub>TP</sub>	4.25	4.37	4.5	V	
Write Protection Voltage (DS1650AB)	V <sub>TP</sub>	4.50	4.62	4.75	V	

**CAPACITANCE**(t<sub>A</sub>=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>		5	10	pF	
Input/Output Capacitance	C <sub>I/O</sub>		5	10	pF	

(0°C to 70°C;  $V_{CC}=5V \pm 5\%$  for DS1650AB)(0°C to 70°C;  $V_{CC}=5V \pm 10\%$  for DS1650Y)**AC ELECTRICAL CHARACTERISTICS**

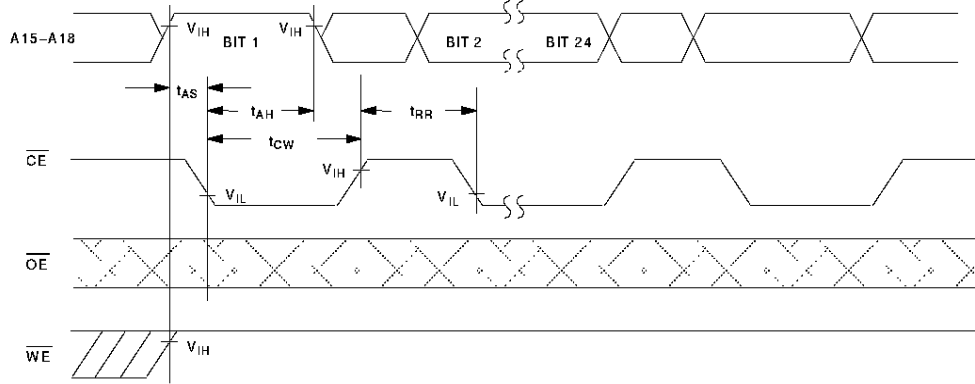
PARAMETER	SYM	DS1650Y/AB-70		DS1650Y/AB-85		DS1650Y/AB-100		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
Read Cycle Time	$t_{RC}$	70		85		100		ns	
Access Time	$t_{ACC}$		70		85		100	ns	
$\overline{OE}$ to Output Valid	$t_{OE}$		35		45		50	ns	
$\overline{CE}$ to Output Valid	$t_{CO}$		70		85		100	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Valid	$t_{COE}$	5		5		5		ns	5
Output High Z from Deselection	$t_{OD}$		25		30		35	ns	5
Output Hold from Address Change	$t_{OH}$	5		5		5		ns	
Write Cycle Time	$t_{WC}$	70		85		100		ns	
Write Pulse Width	$t_{WP}$	55		65		75		ns	3
Address Setup Time	$t_{AW}$	0		0		0		ns	
Write Recovery Time	$t_{WR1}$	10		10		10		ns	13
	$t_{WR2}$	10		10		10		ns	14
Output High Z from $\overline{WE}$	$t_{ODW}$		25		20		35	ns	5
Output Active from $\overline{WE}$	$t_{OEW}$	5		5		5		ns	5
Data Setup Time	$t_{DS}$	30		35		40		ns	4
Data Hold Time	$t_{DH1}$	5		5		5		ns	13
	$t_{DH2}$	5		5		5		ns	14

**AC ELECTRICAL CHARACTERISTICS**(0°C to 70°C;  $V_{CCI}=4.50V$  to  $5.50V$ )\*

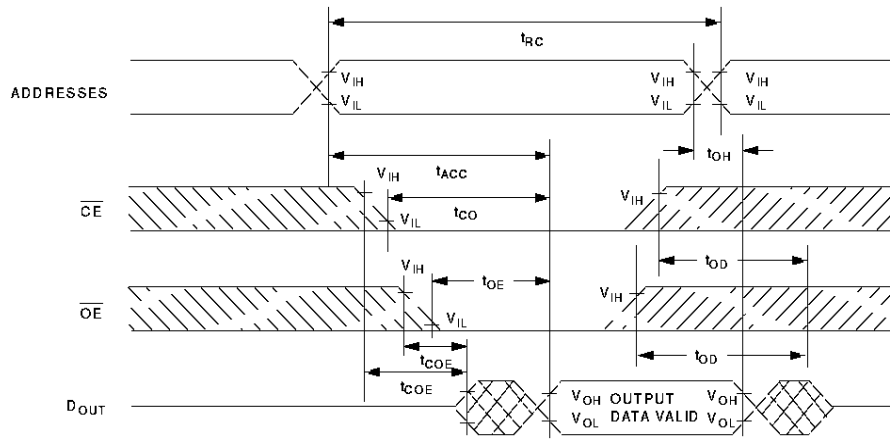
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	$t_{AS}$	0			ns	
Address Hold	$t_{AH}$	50			ns	
Read Recovery	$t_{RR}$	10			ns	
$\overline{CE}$ Pulse Width	$t_{CW}$	75			ns	

\*For loading partition register

**TIMING DIAGRAM: LOADING PARTITION REGISTER**

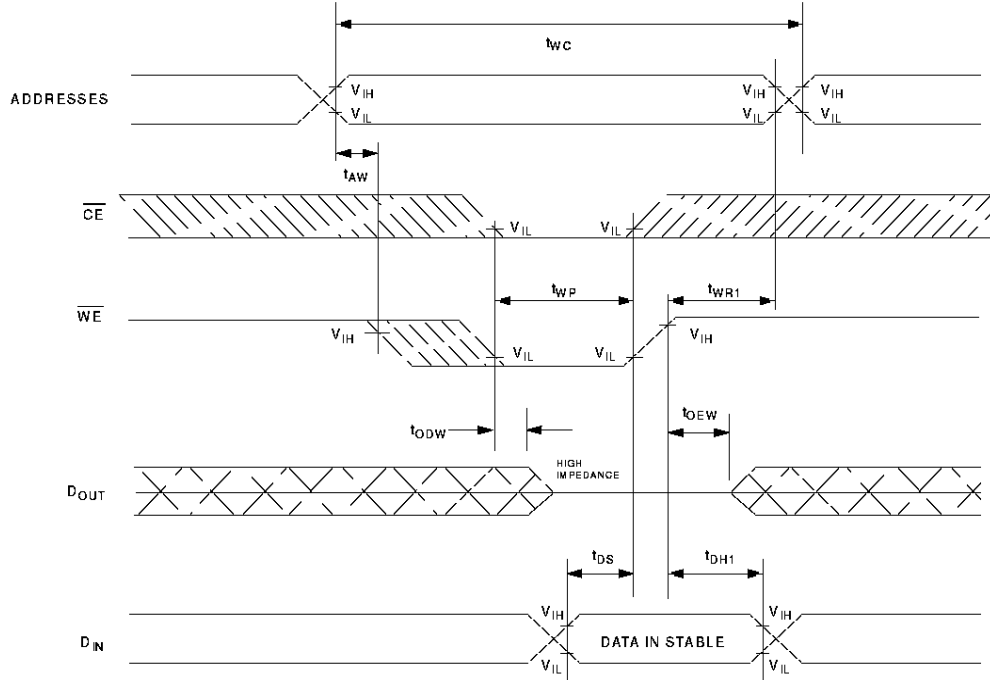


**READ CYCLE**



SEE NOTE 1

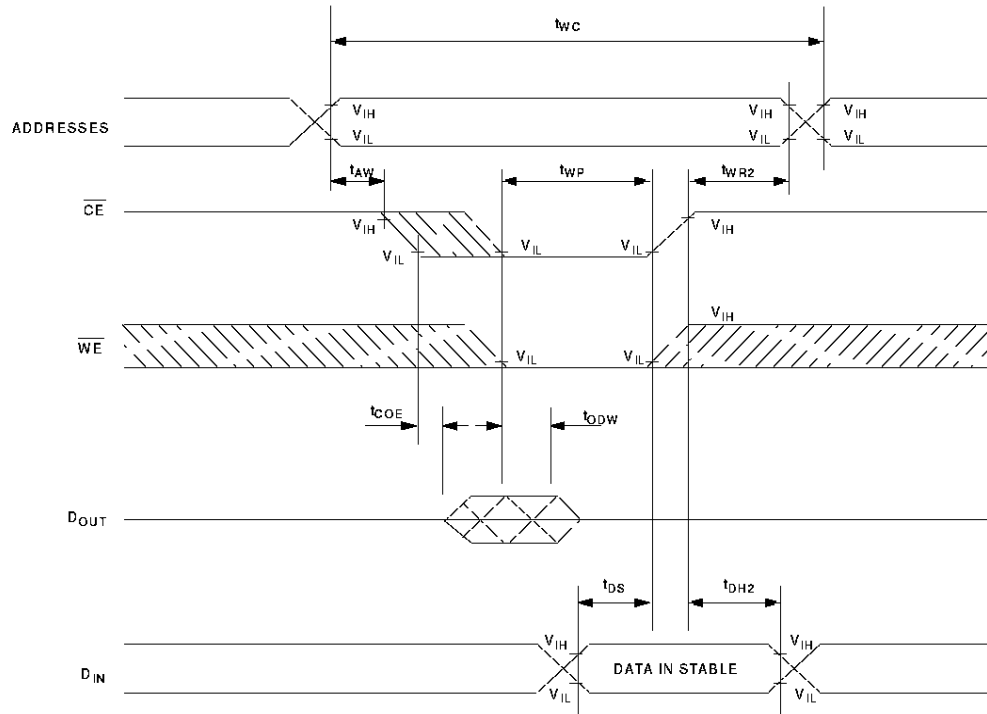
**WRITE CYCLE 1**



SEE NOTES 2, 6, AND 7

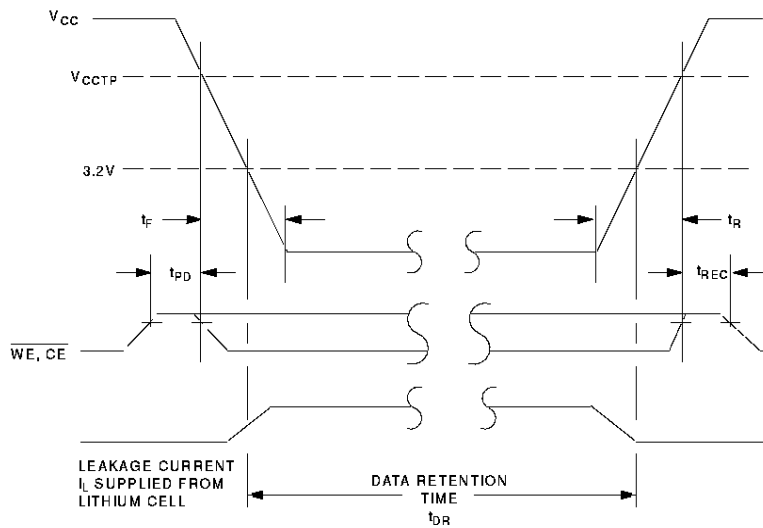


**WRITE CYCLE 2**



SEE NOTES 2 AND 8

**POWER-DOWN/POWER-UP CONDITION**



SEE NOTE 12

**POWER-DOWN/POWER-UP TIMING**

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
$t_{PD}$	$\overline{CE}$ , $\overline{WE}$ , at $V_{IH}$ before Power-Down	0			$\mu s$	12
$t_F$	$V_{CC}$ slew from 4.5V to 0V ( $\overline{CE}$ at $V_{IH}$ )	300			$\mu s$	
$t_R$	$V_{CC}$ slew from 0V to 4.5V ( $\overline{CE}$ at $V_{IH}$ )	0			$\mu s$	
$t_{REC}$	$\overline{CE}$ , $\overline{WE}$ at $V_{IH}$ after Power-Up	25		125	ms	

(t<sub>A</sub> = 25°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
$t_{DR}$	Expected Data Retention Time	10			years	9, 11

**WARNING:**

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

**NOTES:**

- $\overline{WE}$  is high for a read cycle.
- $\overline{OE} = V_{IH}$  or  $V_{IL}$ . If  $\overline{OE} = V_{IH}$  during write cycle, the output buffers remain in a high impedance state.
- $t_{WP}$  is specified as the logical AND of  $\overline{CE}$  and  $\overline{WE}$ .  $t_{WP}$  is measured from the latter of  $\overline{CE}$  or  $\overline{WE}$  going low to the earlier of  $\overline{CE}$  or  $\overline{WE}$  going high.
- $t_{DS}$  is measured from the earlier of  $\overline{CE}$  or  $\overline{WE}$  going high.
- These parameters are sampled with a 5 pF load and are not 100% tested.
- If the  $\overline{CE}$  low transition occurs simultaneously with or later than the  $\overline{WE}$  low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
- If the  $\overline{CE}$  high transition occurs prior to or simultaneously with the  $\overline{WE}$  high transition, the output buffers remain in a high impedance state during this period.
- If  $\overline{WE}$  is low or the  $\overline{WE}$  low transition occurs prior to or simultaneously with the  $\overline{CE}$  low transition, the output buffers remain in a high impedance state during this period.
- Each DS1650Y/AB has a built-in switch that disconnects the lithium source until  $V_{CC}$  is first applied by the user. The expected  $t_{DR}$  is defined as accumulative time in the absence of  $V_{CC}$  starting from the time power is first applied by the user.
- All DC operating conditions, DC electrical characteristics, and AC electrical characteristics apply to both standard parts and those designated IND. Parts with the IND designation meet specifications over a temperature range of -40°C to +85°C.
- The expected data retention time for parts designated IND meet or exceed the specified  $t_{DR}$  at 25°C. IND parts which are continuously exposed to 85°C will have a  $t_{DR}$  of 2 years. The amount of time that IND parts are exposed to temperatures of less than 85°C will significantly prolong data retention time. For example, parts exposed continuously to temperatures of 70°C will have a  $t_{DR}$  of 7 years.
- In a power down condition, the voltage on any pin may not exceed the voltage on  $V_{CC}$ .

- 13.  $t_{WR1}$ ,  $t_{DH1}$  are measured from  $\overline{WE}$  going high.
- 14.  $t_{WR2}$ ,  $t_{DH2}$  are measured from  $\overline{CE}$  going high.
- 15. The power fail output signal ( $\overline{PFO}$ ) is driven active ( $V_{OL}=0.4V$ ) when the  $V_{CC}$  trip point occurs. While active, the  $\overline{PFO}$  pin can sink 4 mA and will maintain a maximum output voltage of 0.4 volts. When inactive, the voltage output of  $\overline{PFO}$  is 2.4 volts minimum and will source a current of 1 mA. This signal is only present on the DS1650YLPM/ABLPM.

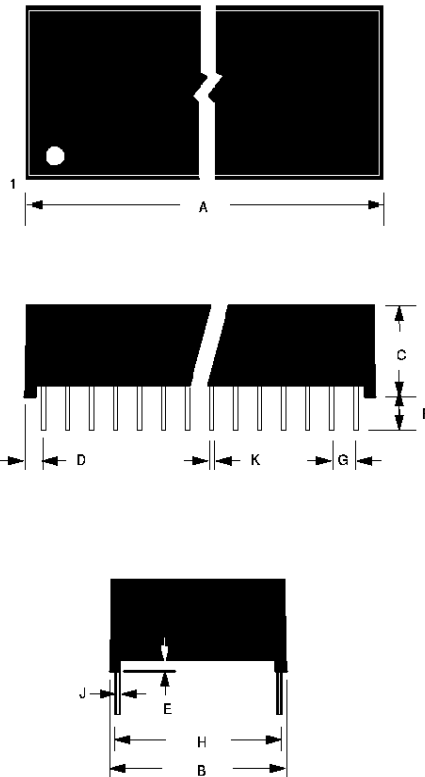
**DC TEST CONDITIONS**

Outputs Open  
 Cycle = 200 ns  
 All voltages are referenced to ground

**AC TEST CONDITIONS**

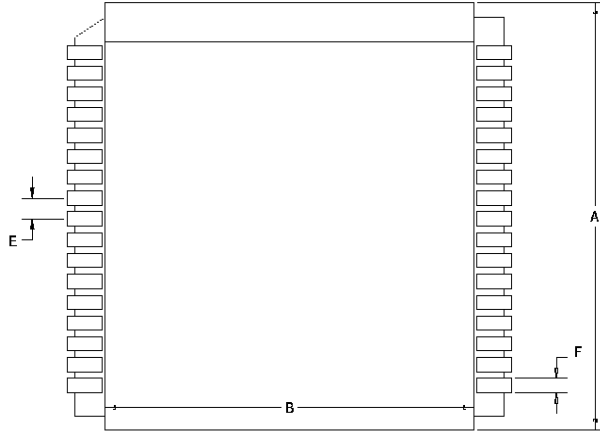
Output Load: 100 pF + 1TTL Gate  
 Input Pulse Levels: 0 - 3.0V  
 Timing Measurement Reference Levels  
 Input: 1.5V  
 Output: 1.5V  
 Input pulse Rise and Fall Times: 5 ns

**DS1650Y/AB NONVOLATILE SRAM 32 PIN 740 MIL MODULE**

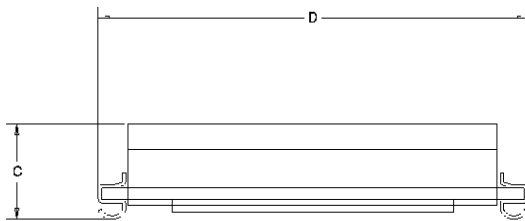


PKG	32-PIN	
	DIM	MIN
A IN.	1.680	1.700
MM	42.67	43.18
B IN.	0.720	0.740
MM	18.29	18.80
C IN.	0.355	0.375
MM	9.02	9.52
D IN.	0.080	0.110
MM	2.03	2.79
E IN.	0.015	0.025
MM	0.38	0.63
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

**DS1650YLPM/ABLPM 34-PIN LOW PROFILE MODULE (LPM)**



PKG	INCHES	
	DIM	MIN
A	0.955	0.970
B	0.840	0.855
C	0.230	0.250
D	0.975	0.995
E	0.050 BSC	
F	0.015	0.025



Suggested 68-pin PLCC surface mountable sockets with leads on two sides only are:

- McKenzie            34P-SMT-3
- Harwin             HIS-40001-04
- Dallas Semiconductor   DS34PIN-PLC

For recommended prototype/breadboard sockets, contact the Dallas Semiconductor factory.