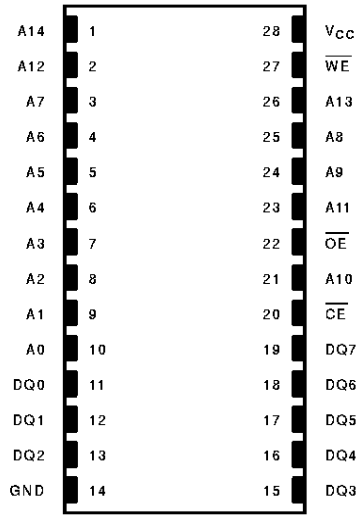
DALLAS SEMICONDUCTOR

DS1730Y/YLPM
3 Volt Partitionable 256K NV SRAM

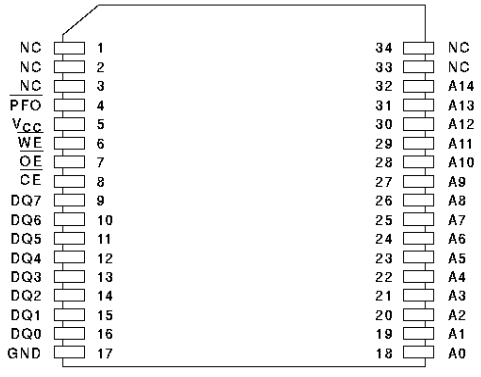
FEATURES

- Data retention in the absence of V_{CC}
- Data is automatically protected during power loss
- Directly replaces 32K x 8 volatile static RAMs or EEPROMs
- Write protects selected blocks of memory regardless of V_{CC} status when programmed
- Unlimited write cycles
- Low-power CMOS
- 2.7V to 3.6V operation
- Over 10 years of data retention
- Standard 28-pin JEDEC pinout (DS1730Y)
- Access times of 150 ns and 200 ns
- Read cycle time equals write cycle time
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Optional industrial temperature range of -40°C to +85°C, designated IND
- Optional low profile module (LPM)
  - Fits into standard 68–pin PLCC surface mountable socket
  - 255 mils package height
  - Power fail output warns processor of impending power failure

PIN ASSIGNMENT



28-PIN ENCAPSULATED PACKAGE
(740 MIL EXTENDED)



34–PIN LOW PROFILE MODULE (LPM)

PIN DESCRIPTION

A0 - A14	–	Address Inputs
$\overline{CE}$	–	Chip Enable
GND	–	Ground
DQ0 - DQ7	–	Data In/Data Out
V_{CC}	–	Power (2.7 to 3.6 volts)
$\overline{WE}$	–	Write Enable
$\overline{OE}$	–	Output Enable
$\overline{PFO}$	–	Power Fail Output (LPM only)
NC	–	No Connect

ORDERING INFORMATION

DS1730Y–XXX 28–pin thru–hole module
- –150 150 ns access
- –200 200 ns access

DS1730YLPM–XXX 34–pin low profile module
- –150 150 ns access
- –200 200 ns access

DESCRIPTION

The DS1730Y 256K Nonvolatile SRAM is a 262,144-bit, fully static SRAM organized as 32,768 words by 8 bits. The DS1730Y has a self-contained lithium energy source and control circuitry that constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. In addition, the device has the ability to unconditionally write protect blocks of memory so that inadvertent write cycles do not corrupt program and special data space. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interface. The nonvolatile SRAM can be used in place of existing 32K x 8 SRAMs directly conforming to the popular bytewide 28256 EEPROM, allowing direct substitution while enhancing performance. The DS1730YLPM is a low profile module that fits into a standard 68–pin PLCC surface mountable socket and is functionally equivalent to the DS1730Y. The DS1730YLPM also provides a power fail output that warns a processor of impending power failure.

READ MODE

The DS1730Y executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) is active (low). The unique address specified by the 15 address inputs (A_0 - A_{14}) defines which of the 32,768 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ (Output Enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

WRITE MODE

The DS1730Y is in the write mode whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1730Y device provides full functional capability for V_{CC} greater than 2.70 volts and write protects by 2.60 volts nominal. Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS1730Y constantly monitors V_{CC}. Should the supply voltage decay, the RAM will automatically write protect itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As V_{CC} falls below approximately 2.6 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 2.6 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} stabilizes above V_{TP}.

FRESHNESS SEAL AND SHIPPING

The DS1730Y is shipped from Dallas Semiconductor with the lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is applied and remains at a level of greater than V_{TP} for t_{REC}, the lithium energy source is enabled for battery backup operation.

PARTITION PROGRAMMING MODE

The register controlling the partition switch is selected by recognition of a specific binary pattern which is sent on address lines A11 - A14. These address lines are the four upper order address lines being sent to RAM. The pattern is sent by 20 consecutive read cycles with the exact pattern as shown in Table 1. Pattern matching must be accomplished using read cycles; any write cycles will reset the pattern matching circuitry. If this pattern is matched perfectly, then the 21st through 24th read cycle will load the partition switch. Since there are 16 possible write protected partitions the size of each partition is 32K/16 or 2K x 8. Each partition is represented by one of the 16 bits contained in the 21st through 24th read cycle as defined by A11 through A14 and shown in Table 2. A logical 1 in a bit location sets that partition to write protect. A logical 0 in a bit location disables write protection. For example, if during the pattern match sequence bit 22 on address pin A12 was a 1, this would cause the partition register location for partition 5 to be set to a 1. This in turn would cause the DS1730Y to inhibit $\overline{WE}$ internally when A14 A13 A12 A11=0101. Note that while setting the partition register, data which is being accessed from the RAM should be ignored as the purpose of the 24 read cycles is to set the partition switch and not for the purpose of accessing data from RAM.

PATTERN MATCH TO WRITE PARTITION REGISTER Table 1

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A11	1	0	1	1	1	1	0	0	1	1	1	0	0	0	0	0	1	1	0	1	X	X	X	X
A12	1	1	1	1	1	0	0	1	1	1	0	0	1	0	1	1	0	0	0	0	X	X	X	X
A13	1	1	1	1	0	0	1	1	1	0	0	1	0	1	0	1	0	0	0	1	X	X	X	X
A14	1	1	0	0	0	1	1	1	0	0	1	0	0	0	1	0	1	0	0	0	X	X	X	X

FIRST BITS ENTERED

LAST GROUP ENTERED

PARTITION REGISTER MAPPING Table 2

Address Pin	Bit number in pattern match sequence	Partition Number	Address State Affected (A_{14} A_{13} A_{12} A_{11})
A11	BIT 21	PARTITION 0	0000
A12	BIT 21	PARTITION 1	0001
A13	BIT 21	PARTITION 2	0010
A14	BIT 21	PARTITION 3	0011
A11	BIT 22	PARTITION 4	0100
A12	BIT 22	PARTITION 5	0101
A13	BIT 22	PARTITION 6	0110
A14	BIT 22	PARTITION 7	0111
A11	BIT 23	PARTITION 8	1000
A12	BIT 23	PARTITION 9	1001
A13	BIT 23	PARTITION 10	1010
A14	BIT 23	PARTITION 11	1011
A11	BIT 24	PARTITION 12	1100
A12	BIT 24	PARTITION 13	1101
A13	BIT 24	PARTITION 14	1110
A14	BIT 24	PARTITION 15	1111

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to +7.0V
Operating Temperature	0°C to 70°C, –40°C to +85°C for IND parts
Storage Temperature	–40°C to +70°C, –40°C to +85°C for IND parts
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1730Y Power Supply Voltage	V_{CC}	2.7		3.6	V	
Logic 1	V_{IH}	2.2		V_{CC}	V	
Logic 0	V_{IL}	0.0		+0.4	V	

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=2.7V to 3.6V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-1.0		+1.0	µA	
Output Current @ 2.2V	I_{OH}	-0.5			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	15
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		5.0	7.0	mA	
Standby Current $\overline{CE}$ = V_{CC} - 0.5V	I_{CCS2}		3.0	4.0	mA	
Operating Current	I_{CCO1}			40	mA	
Write Protection Voltage	V_{TP}	2.50	2.60	2.70	V	

AC ELECTRICAL CHARACTERISTICS

($0^{\circ}C$ to $70^{\circ}C$; V_{CC}=2.7V to 3.6V)

PARAMETER	SYMBOL	DS1730Y-150		DS1730Y-200		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	150		200		ns	
Access Time	t_{ACC}		150		200	ns	
$\overline{OE}$ to Output Valid	t_{OE}		70		100	ns	
$\overline{CE}$ to Output Valid	t_{CO}		150		200	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Valid	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		50		50	ns	5
Output Hold from Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	150		200		ns	
Write Pulse Width	t_{WP}	120		150		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR1} t_{WR2}	10 10		10 10		ns ns	13 14
Output High Z from $\overline{WE}$	t_{ODW}		50		50	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		ns	5
Data Setup Time	t_{DS}	60		80		ns	4
Data Hold Time	t_{DH1} t_{DH2}	10 10		10 10		ns ns	13 14

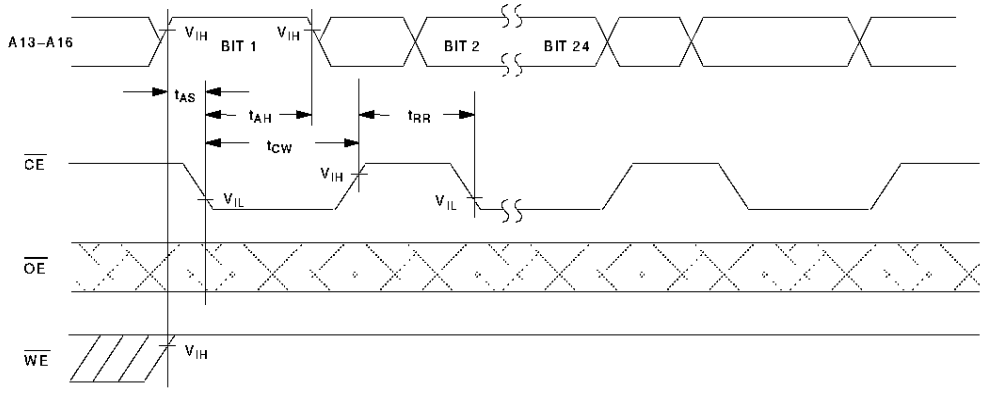
AC ELECTRICAL CHARACTERISTICS

($0^{\circ}C$ to $70^{\circ}C$; V_{CC}=2.7V to 3.6V)*

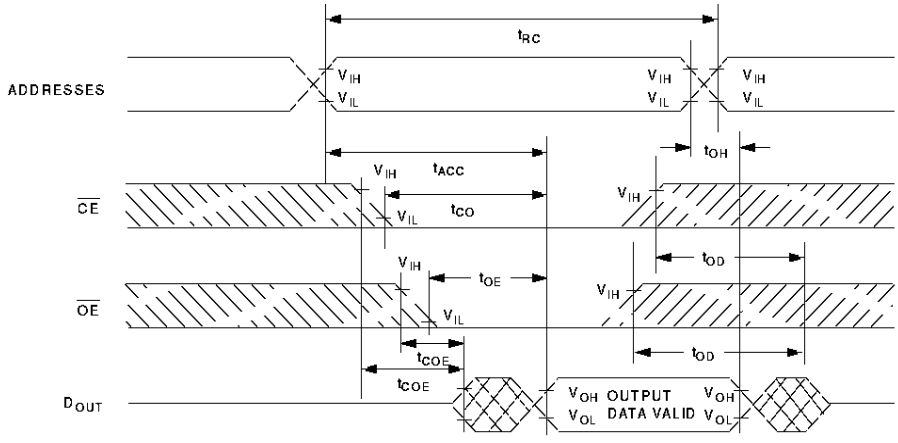
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	t_{AS}	0			ns	
Address Hold	t_{AH}	50			ns	
Read Recovery	t_{RR}	20			ns	
$\overline{CE}$ Pulse Width	t_{CW}	75			ns	

*For loading partition register

TIMING DIAGRAM: LOADING PARTITION REGISTER

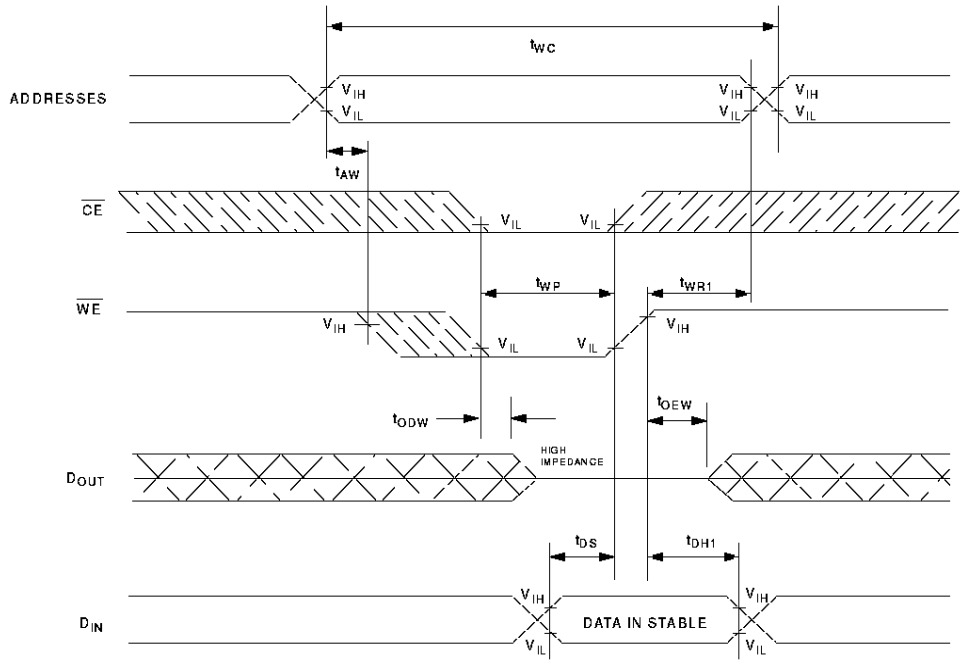


READ CYCLE



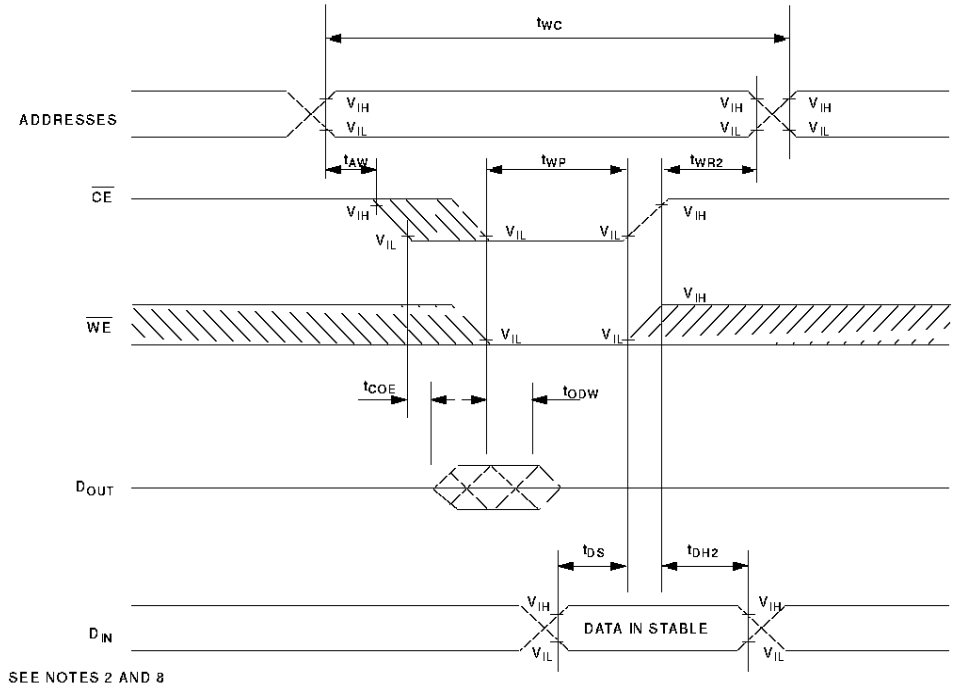
SEE NOTE 1

WRITE CYCLE 1



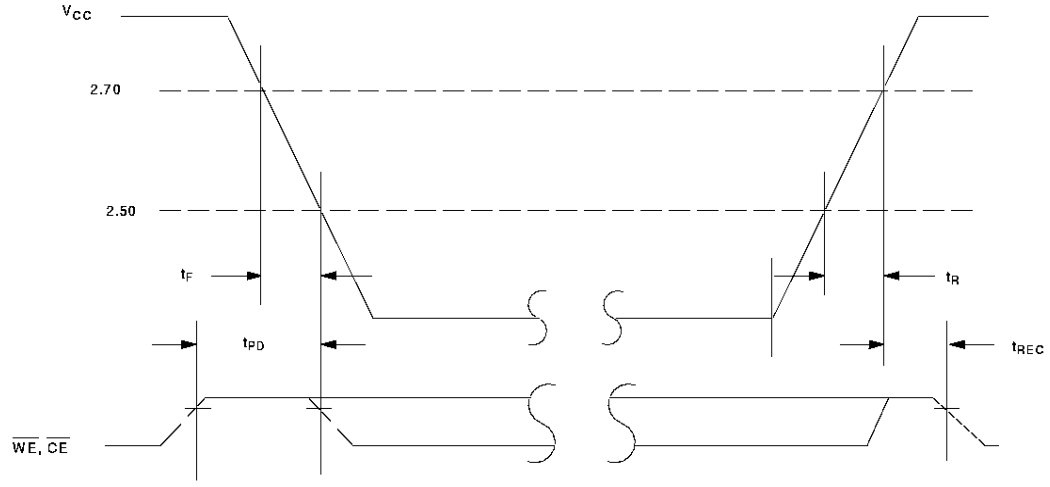
SEE NOTES 2, 6, AND 7

WRITE CYCLE 2



SEE NOTES 2 AND 8

POWER-DOWN/POWER-UP CONDITION



SEE NOTE 12

POWER-DOWN/POWER-UP TIMING

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$, $\overline{WE}$ at V_{IH} before Power-Down	t_{PD}	0			µs	12
Power–Down Slew	t_F	300			µs	
Power–Up Slew	t_R	0			µs	
$\overline{CE}$, $\overline{WE}$ at V_{IH} after Power-Up	t_{REC}	100		200	ms	

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	10			years	9, 11

WARNING:

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DS} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1730Y or DS1730YLPM has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.
10. All DC operating conditions, DC electrical characteristics, and AC electrical characteristics apply to both standard parts and those designated IND. Parts with the IND designation meet specifications over a temperature range of -40°C to +85°C.
11. The expected data retention time for parts designated IND meet or exceed the specified t_{DR} at 25°C. IND parts which are continuously exposed to 85°C will have a t_{DR} of 2 years. The amount of time that IND parts are exposed to temperatures of less than 85°C will significantly prolong data retention time. For example, parts exposed continuously to temperatures of 70°C will have a t_{DR} of 7 years.
12. In a power down condition the voltage on any pin may not exceed the voltage on V_{CC}.
13. t_{WR1}, t_{DH1} are measured from $\overline{WE}$ going high.
14. t_{WR2}, t_{DH2} are measured from $\overline{CE}$ going high.
15. The power fail output signal ($\overline{PFO}$) is driven active (V_{OL}=0.4V) when the V_{CC} trip point occurs. While active, the $\overline{PFO}$ pin can sink 4 mA and will maintain a maximum output voltage of 0.4 volts. When inactive, the voltage output of $\overline{PFO}$ is 2.4 volts minimum and will source a current of 1 mA. This signal is only present on the DS1730YLPM.

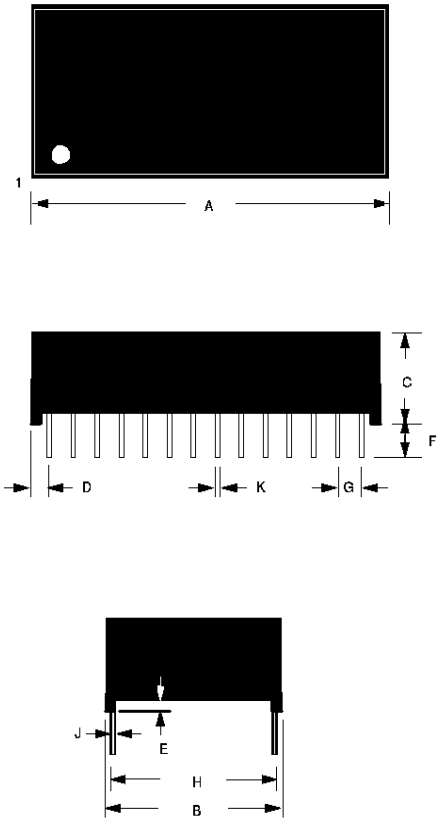
DC TEST CONDITIONS

Outputs Open
Cycle = 200 ns
All voltages are referenced to ground

AC TEST CONDITIONS

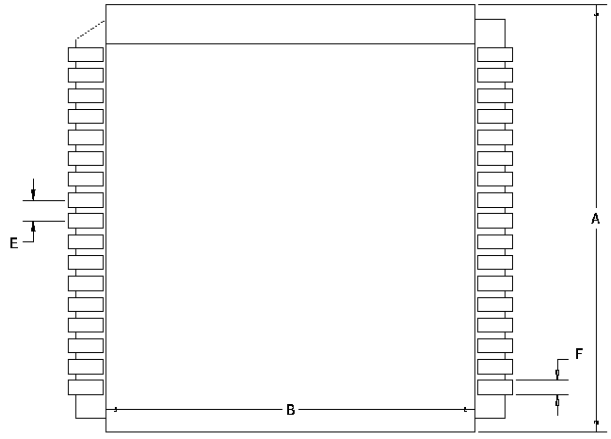
Output Load: 100 pF + 1TTL Gate
Input Pulse Levels:
  0.0 to 2.7 volts
Timing Measurement Reference Levels
  Input: 1.5V
  Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns

DS1730Y NONVOLATILE SRAM 28–PIN 740 MIL MODULE

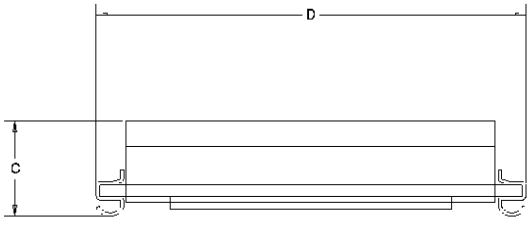


PKG	28-PIN	
DIM	MIN	MAX
A IN.	1.480	1.500
MM	37.60	38.10
B IN.	0.720	0.740
MM	18.29	18.80
C IN.	0.355	0.375
MM	9.02	9.52
D IN.	0.080	0.110
MM	2.03	2.79
E IN.	0.015	0.025
MM	0.38	0.63
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

DS1730YLPM 34–PIN LOW PROFILE MODULE (LPM)



PKG	INCHES	
DIM	MIN	MAX
A	0.955	0.970
B	0.840	0.855
C	0.230	0.250
D	0.975	0.995
E	0.050 BSC	
F	0.015	0.025



Suggested 68–pin PLCC surface mountable sockets with leads on two sides only are:

McKenzie	PLCC34P–SMT–3
Harwin	HIS–40001–04
Dallas Semiconductor	DS34PIN–PLC

For recommended prototype/breadboard sockets, contact the Dallas Semiconductor factory.