128-MBit Synchronous Low-Power DRAM in Chipsize Packages

Preliminary Datasheet (Rev. 04/01)

High Performance:

	-7.5	-8	Units
$f_{CK,MAX}$	133	125	MHz
$t_{CK3,MIN}$	7.5	8	ns
$t_{AC3,MAX}$	5.4	6	ns
$t_{CK2,MIN}$	10	10	ns
$t_{AC2,MAX}$	6	6	ns

- 8Mbit x 16 & 16Mbit x8 organisation
- VDD = 2.5V / VDDQ = 1.8V (2.5V tolerant)
- Fully Synchronous to Positive Clock Edge
- Four Banks controlled by BA0 & BA1
- Programmable $\overline{CAS}$ Latency: 2, 3
- Programmable Wrap Sequence: Sequential or Interleave
- Deep Power Down Mode
- Automatic and Controlled Precharge Command
- Programmable Burst Length: 1, 2, 4, 8 and full page
- Programmable Power Reduction Feature by partial array activation during Self-Refresh
- Data Mask for byte control
- Auto Refresh (CBR)
- Self Refresh with programmble refresh period
- Power Down and Clock Suspend Mode
- Random Column Address every CLK (1-N Rule)
- 54-FBGA , with 9 x 6 ball array with 3 depopulated rows, 9 x 8 mm
- Operating Temperature Range
  Commerical (0^0 to 70^0C)
  Extended (-25°C to +85°C)

The HYB/E 25L128800/160AC Mobile RAMs are new generation of low power, four bank Synchronous DRAM's organized as 4 banks × 2Mbit x16 and 4 banks x 4Mbit x 8 with additional features for mobile applications. These synchronous Mobile RAMs achieve high speed data transfer rates by employing a chip architecture that prefetches multiple bits and then synchronizes the output data to a system clock. The chip is fabricated using the Infineon advanced process technology.

The device adds new features to the industry standards set for synchronous DRAM products.
Only partials of the memory array can be selected for Self-Refresh and the refresh period during Self-Refresh is programmable in 4 steps which drastically reduces the self refresh current, depending on the case temperature of the components in the system application. In addition a "Deep Power Down Mode" is available. Operating the four memory banks in an interleave fashion allows random access operation to occur at higher rate. A sequential and gapless data rate is possible depending on burst length, $\overline{CAS}$ latency and speed grade of the device. The device operates from a 2.5V power supply for the core and 1.8V for the bus interface. The Mobile RAM is housed in a FBGA "chip-size" package. The Mobile RAM is available in the commercial (0^0 to 70^0C) and Extended (-25°C to +85°C) temperature range

Ordering Information

Type	Function Code	Package	Description
Commercial temperature range:			
HYB 25L128800AC-7.5	PC133-333-522	BGA-BOC	133 MHz 4B × 4M x 8 LP-SDRAM
HYB 25L128800AC-8	PC100-222-620	BGA-BOC	100 MHz 4B × 4M x 8 LP-SDRAM
HYB 25L128160AC-7.5	PC133-333-522	BGA-BOC	133 MHz 4B × 2M x16 LP-SDRAM
HYB 25L128160AC-8	PC100-222-620	BGA-BOC	100 MHz 4B × 2M x16 LP-SDRAM
Extended temperature range:			
HYE 25L128800AC-7.5	PC133-333-522	BGA-BOC	133 MHz 4B × 4M x 8 LP-SDRAM
HYE 25L128800AC-8	PC100-222-620	BGA-BOC	100 MHz 4B × 4M x 8 LP-SDRAM
HYE 25L128160AC-7.5	PC133-333-522	BGA-BOC	133 MHz 4B × 2M x16 LP-SDRAM
HYE 25L128160AC-8	PC100-222-620	BGA-BOC	100 MHz 4B × 2M x16 LP-SDRAM

Pin Definitions and Functions

CLK	Clock Input	DQ	Data Input/Output
CKE	Clock Enable	LDQM, UDQM	Data Mask for x16
$\overline{CS}$	Chip Select	V_{DD}	Power (+ 2.5V)
$\overline{RAS}$	Row Address Strobe	V_{SS}	Ground
$\overline{CAS}$	Column Address Strobe	V_{DDQ}	Power for DQ's (+1.8 V)
$\overline{WE}$	Write Enable	V_{SSQ}	Ground for DQ's
A0 - A11, A0 - A8, A10	Row Addresses Column Addresses	N.C.	Not connected
BA0, BA1	Bank Select		

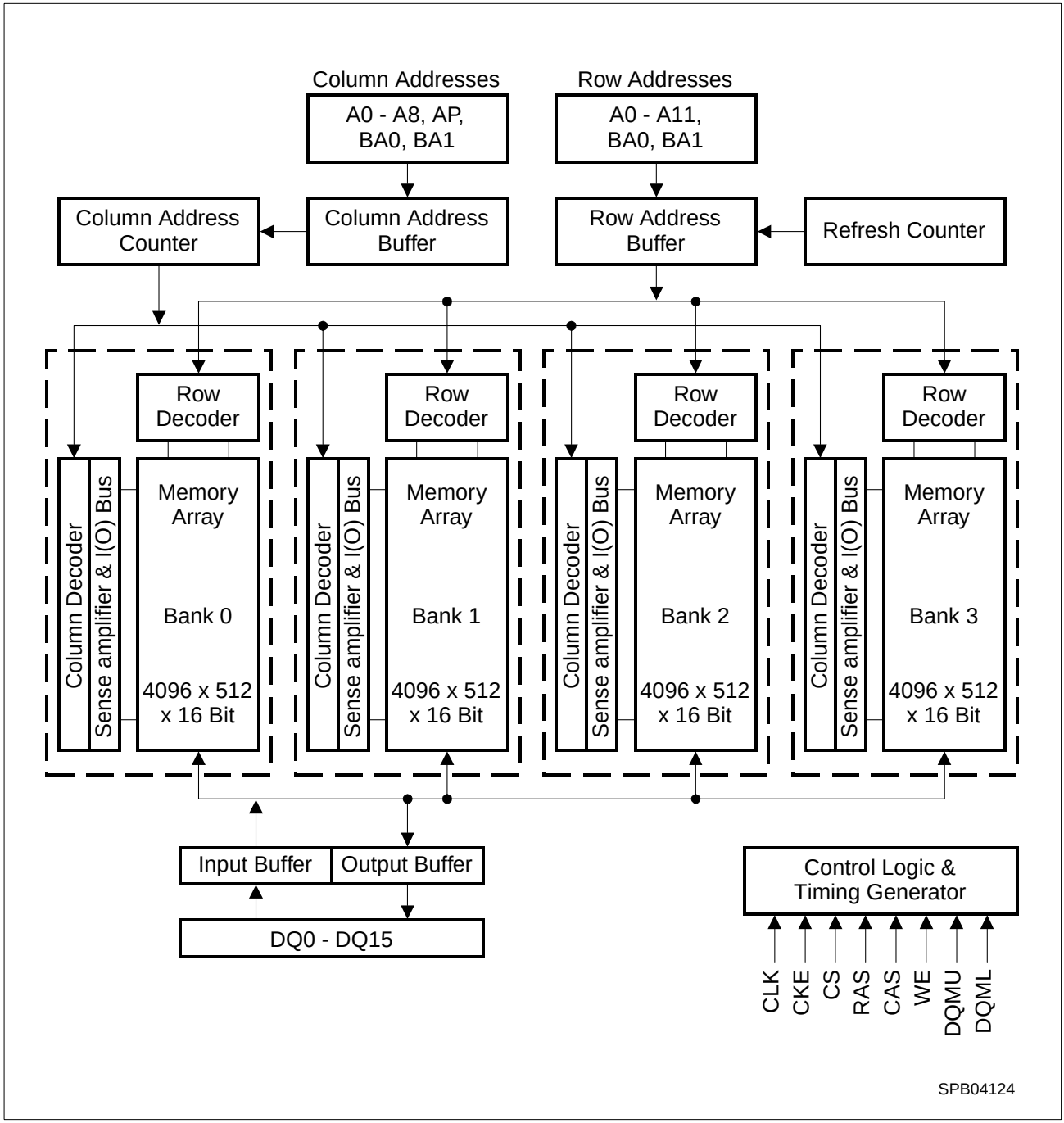
Pin Configuration for x16 devices:

1	2	3		7	8	9
VSS	DQ15	VSSQ	A	VDDQ	DQ0	VDD
DQ14	DQ13	VDDQ	B	VSSQ	DQ2	DQ1
DQ12	DQ11	VSSQ	C	VDDQ	DQ4	DQ3
DQ10	DQ9	VDDQ	D	VSSQ	DQ6	DQ5
DQ8	NC	VSS	E	VDD	LDQM	DQ7
UDQM	CLK	CKE	F	$\overline{CAS}$	$\overline{RAS}$	$\overline{WE}$
NC	A11	A9	G	BA0	BA1	$\overline{CS}$
A8	A7	A6	H	A0	A1	A10
VSS	A5	A4	J	A3	A2	VDD

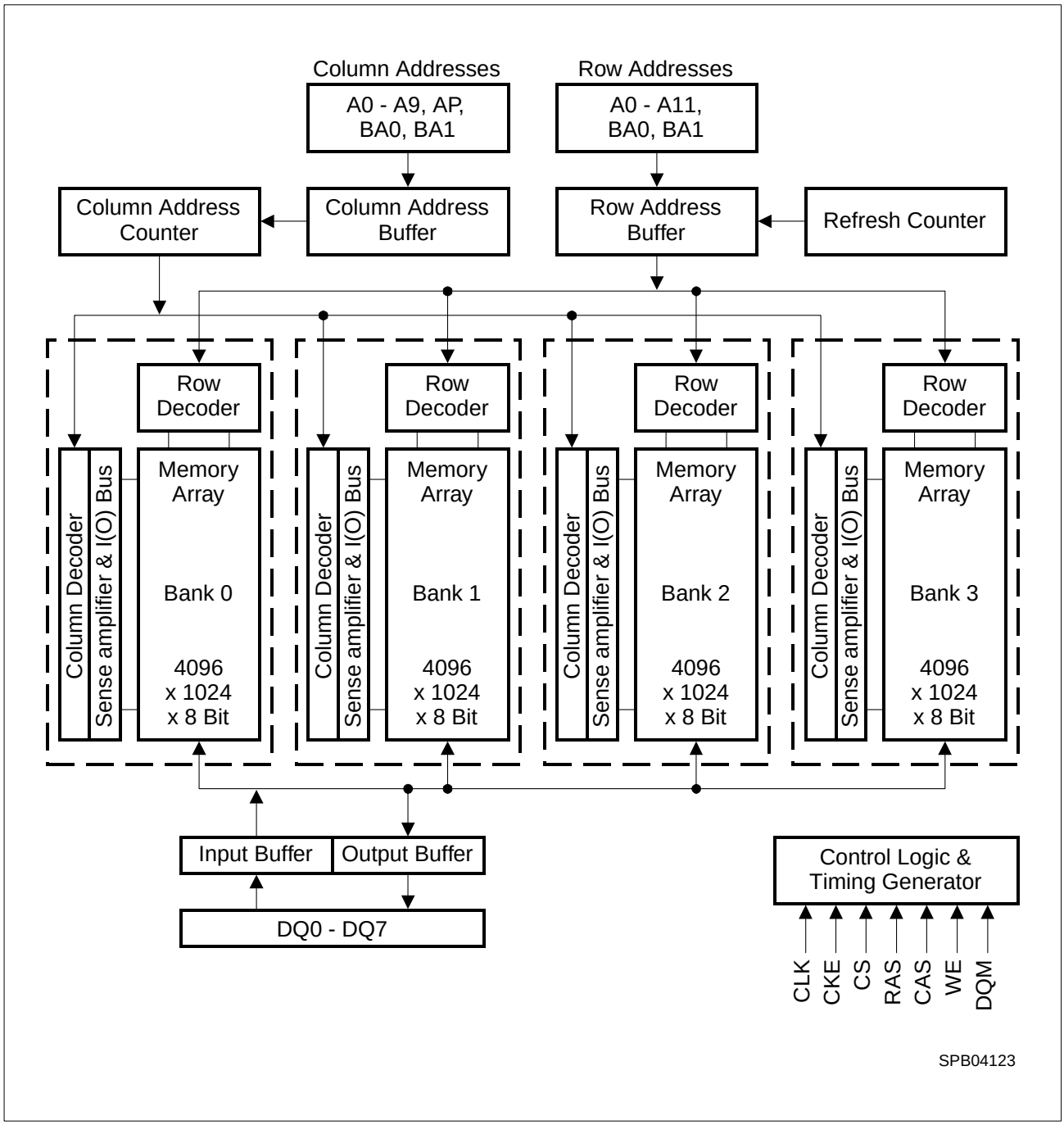
Pin Configuration for x8 devices: (t.b.d.)

1	2	3		7	8	9
VSS	DQ7	VSSQ	A	VDDQ	DQ0	VDD
NC	DQ6	VDDQ	B	VSSQ	DQ1	NC
NC	DQ5	VSSQ	C	VDDQ	DQ2	NC
NC	DQ4	VDDQ	D	VSSQ	DQ3	NC
NC	NC	VSS	E	VDD	NC	NC
DQM	CLK	CKE	F	$\overline{CAS}$	$\overline{RAS}$	$\overline{WE}$
NC	A11	A9	G	BA0	BA1	$\overline{CS}$
A8	A7	A6	H	A0	A1	A10
VSS	A5	A4	J	A3	A2	VDD

Functional Block Diagrams



Block Diagram: 8Mb x16 SDRAM (12 / 9 / 2 addressing)



Block Diagram: 16M x8 SDRAM (12 / 10 / 2 addressing)

Signal Pin Description

Pin	Type	Signal	Polarity	Function
CLK	Input	Pulse	Positive Edge	The system clock input. All of the SDRAM inputs are sampled on the rising edge of the clock.
CKE	Input	Level	Active High	Activates the CLK signal when high and deactivates the CLK signal when low, thereby initiates either the Power Down mode, Suspend mode, or the Self Refresh mode.
$\overline{CS}$	Input	Pulse	Active Low	$\overline{CS}$ enables the command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$ $\overline{CAS}$ $\overline{WE}$	Input	Pulse	Active Low	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the command to be executed by the SDRAM.
A0 - A11	Input	Level	–	During a Bank Activate command cycle, A0 - A11 define the row address (RA0 - RA11) when sampled at the rising clock edge. During a Read or Write command cycle, A0-An define the column address (CA0 - CAn) when sampled at the rising clock edge.CAn depends from the SDRAM organization: 16M x8 SDRAM CA0 - CA9 (Page Length = 1024 bits) 8M x16 SDRAM CA0 - CA8 (Page Length = 512 bits) In addition to the column address, A10(= AP) is used to invoke autoprecharge operation at the end of the burst read or write cycle. If A10 is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If A10 is low, autoprecharge is disabled. During a Precharge command cycle, A10 (= AP) is used in conjunction with BA0 and BA1 to control which bank(s) to precharge. If A10 is high, all four banks will be precharged regardless of the state of BA0 and BA1. If A10 is low, then BA0 and BA1 are used to define which bank to precharge.
BA0, BA1	Input	Level	–	Bank Select Inputs. Selects which bank is to be active.
DQx	Input Output	Level	–	Data Input/Output pins operate in the same manner as on conventional DRAMs.

Pin	Type	Signal	Polarity	Function
LDQM UDQM,	Input	Pulse	Active High	The Data Input/Output mask places the DQ buffers in a high impedance state when sampled high. In Read mode, DQM has a latency of two clock cycles and controls the output buffers like an output enable. In Write mode, DQMx has a latency of zero and operates as a word mask by allowing input data to be written if it is low but blocks the write operation if DQM is high. LDQM and UDQM controls the lower and upper bytes in x16 SDRAM.
V_{DD} V_{SS}	Supply	–	–	Power and ground for the input buffers and the core logic.
V_{DDQ} V_{SSQ}	Supply	–	–	Isolated power supply and ground for the output buffers to provide improved noise immunity.

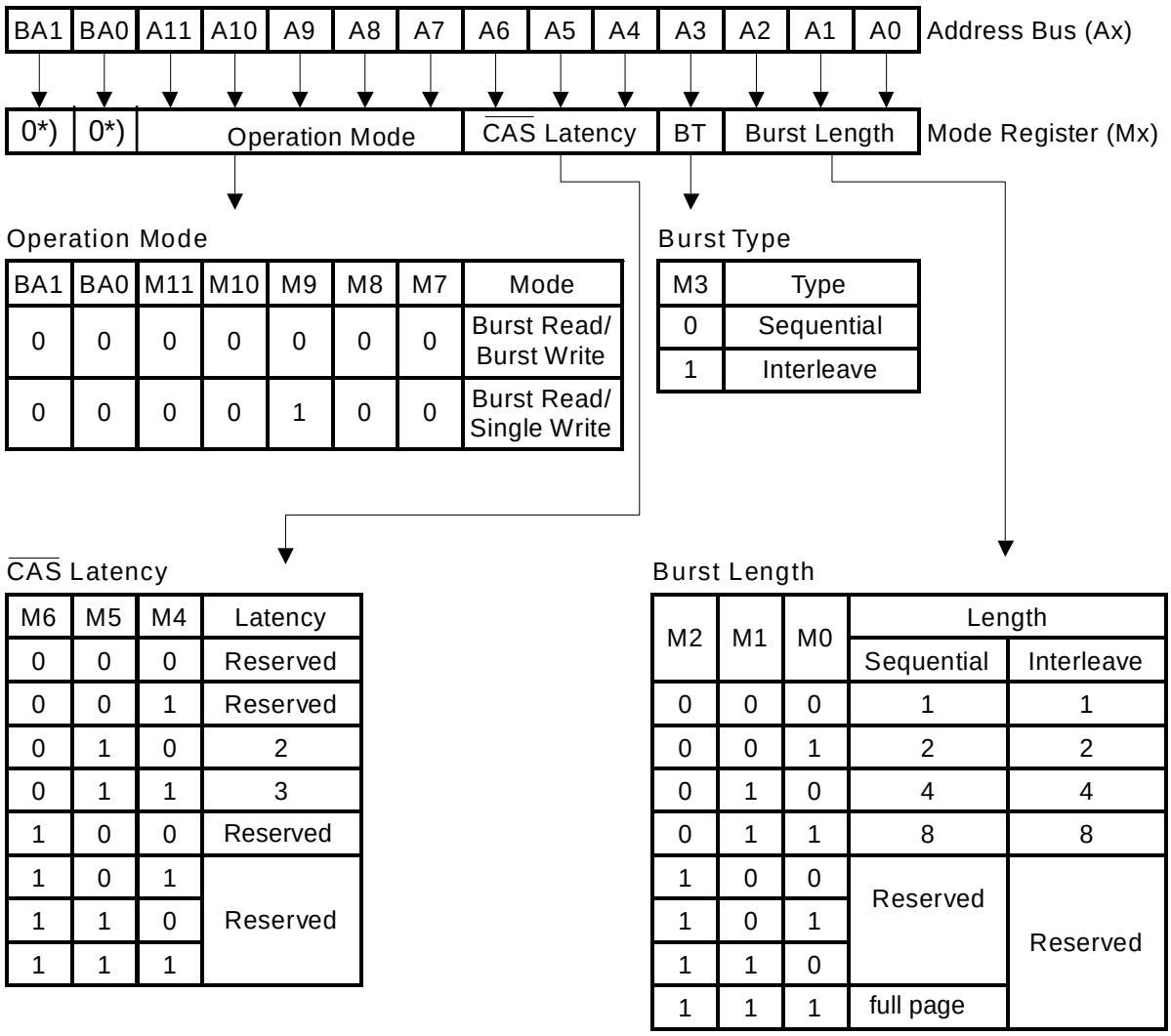
Operation Definition

All of SDRAM operations are defined by states of control signals $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, and DQMx at the positive edge of the clock. The following list shows the truth table for the operation commands.

Operation	Device State	CKE n-1	CKE n	DQM	BA0 BA1	AP= A10	Addr	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$
Bank Active	Idle[3]	H	X	X	V	V	V	L	L	H	H
Bank Precharge	Any	H	X	X	V	L	X	L	L	H	L
Precharge All	Any	H	X	X	X	H	X	L	L	H	L
Write	Active[3]	H	X	X	V	L	V	L	H	L	L
Write with Autoprecharge	Active[3]	H	X	X	V	H	V	L	H	L	L
Read	Active[3]	H	X	X	V	L	V	L	H	L	H
Read with Autoprecharge	Active[3]	H	X	X	V	H	V	L	H	L	H
Mode Register Set	Idle	H	X	X	V	V	V	L	L	L	L
No Operation	Any	H	X	X	X	X	X	L	H	H	H
Burst Stop	Active	H	X	X	X	X	X	L	H	H	L
Device Deselect	Any	H	X	X	X	X	X	H	X	X	X
Auto Refresh	Idle	H	H	X	X	X	X	L	L	L	H
Self Refresh Entry	Idle	H	L	X	X	X	X	L	L	L	H
Self Refresh Exit	Idle (Self Refr.)	L	H	X	X	X	X	H	X	X	X
								L	H	H	X
Power Down Entry (Precharge or active standby)	Idle	H	L	X	X	X	X	H	X	X	X
	Active[4]							L	H	H	H
Power Down Exit	Any (Power Down)	L	H	X	X	X	X	H	X	X	X
								L	H	H	L
Data Write/Output Enable	Active	H	X	L	X	X	X	X	X	X	X
Data Write/Output Disable	Active	H	X	H	X	X	X	X	X	X	X
Deep Power Down Entry	Idle	H	L	X	X	X	X	L	H	H	L
Deep Power Down Exit	Deep[5] Power Down	L	H	X	X	X	X	X	X	X	X

Notes:

1. V = Valid, x = Don't Care, L = Low Level, H = High Level.
2. CKEn signal is input level when commands are provided, CKEn-1 signal is input level one clock before the commands are provided.
3. This is the state of the banks designated by BA0, BA1 signals.
4. Power Down Mode can not entry in the burst cycle. Address Input for Mode Set (Mode Register Operation)
5. After Deep Power Down mode exit a full new initialisation of the memory device is mandatory.



Operation Mode

BA1	BA0	M11	M10	M9	M8	M7	Mode
0	0	0	0	0	0	0	Burst Read/ Burst Write
0	0	0	0	1	0	0	Burst Read/ Single Write

Burst Type

M3	Type
0	Sequential
1	Interleave

$\overline{CAS}$ Latency

M6	M5	M4	Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	
1	1	1	

Burst Length

M2	M1	M0	Length	
			Sequential	Interleave
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1		
1	1	0		
1	1	1	full page	

*) BA0 and BA1 must be 0, 0 to select the Mode Register (Vs. the Extended Mode Register)

Mode Register Table

Power On and Initialization

The default power on state of the mode register is supplier specific and may be undefined. The following power on and initialization sequence guarantees the device is preconditioned to each users specific needs. Like a conventional DRAM, the Synchronous DRAM must be powered up and initialized in a predefined manner.During power on, all V_{DD} and V_{DDQ} pins must be built up simultaneously to the specified voltage when the input signals are held in the “NOP” or “DESELECT” state. The power on voltage must not exceed V_{DD} + 0.3 V on any of the input pins or VDD supplies. The CLK signal must be started at the same time. After power on, an initial pause of 200 µs is required followed by a precharge of all banks using the precharge command. To prevent data contention on the DQ bus during power on, it is required that the DQM and CKE pins be held high during the initial pause period. Once all banks have been precharged, the Mode Register Set Command must be issued to initialize the Mode Register. A minimum of eight Auto Refresh cycles (CBR) are also required.These may be done before or after programming the Mode Register. Failure to follow these steps may lead to unpredictable start-up modes.

Programming the Mode Register

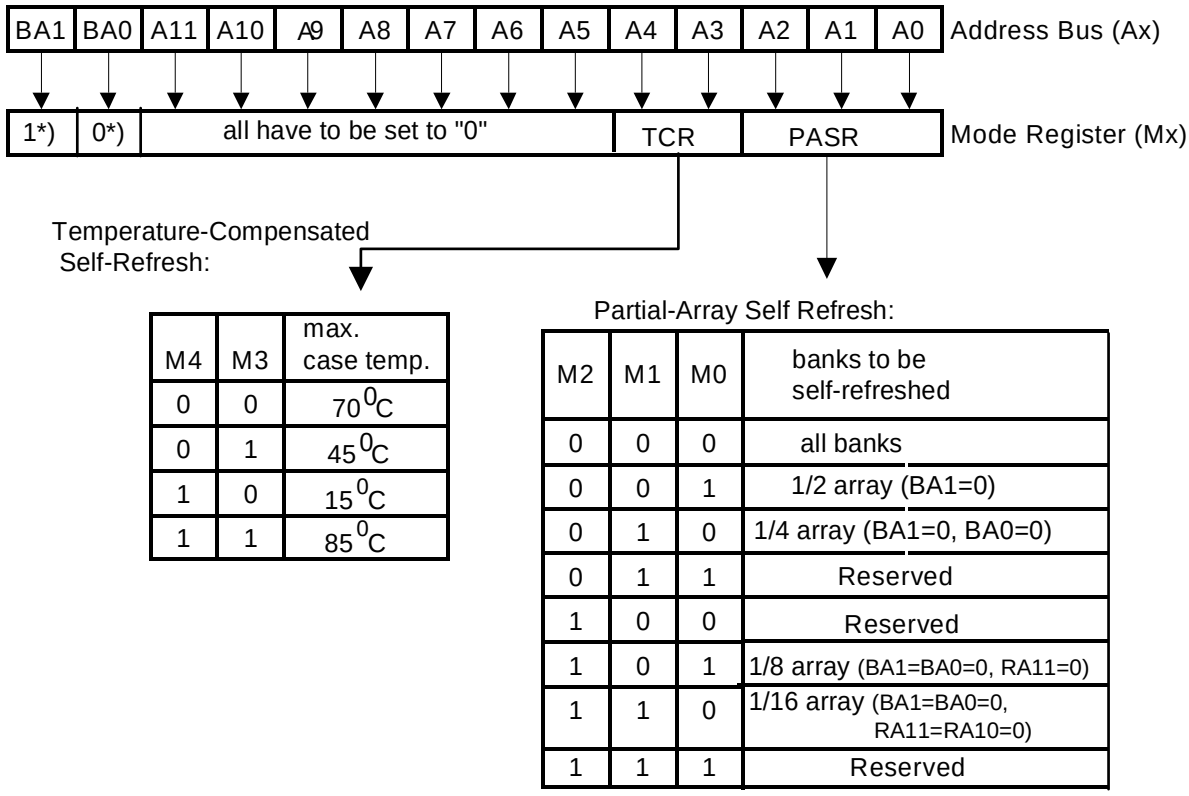
The Mode Register designates the operation mode at the read or write cycle. This register is divided into 4fields. A Burst Length Field to set the length of the burst, an Addressing Selection bit to program the column access sequence in a burst cycle (interleaved or sequential), and a $\overline{\text{CAS}}$ Latency Field to set the access time at clock cycle, an The mode set operation must be done before any activate command after the initial power up. Any content of the mode register can be altered by re-executing the mode set command. All banks must be in precharged state and CKE must be high at least one clock before the mode set operation. After the mode register is set, a Standby or NOP command is required. Low signals of $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\overline{\text{WE}}$ at the positive edge of the clock activate the mode set operation. Address input data at this timing defines parameters to be set as shown in the previous table. BA0 and BA1 have to be set to “0” to enter the Mode Register.

Extended Mode Register

The Extended Mode Register controls functions beyond those controlled by the Mode Register. These additional functions are unique to Mobile RAMs and includes a Refresh Period field (TCR) for temperature compensated self-refresh and a Partial-Array Self Refresh field (PASR). The PASR field is used to specify whether only one quarter (bank0), one half (banks 0 + 1) or all banks of the SDRAM array are enabled. Disabled banks will not be refreshed in Self-Refresh mode and written data will get lost. When only bank 0 is selected, it is possible to partial select only half or one quarter of bank 0. The TCR field has four entries to set Refresh Period during self-refresh depending on the case temperature of the Mobile RAM devices.

The Extended Mode Register is programmed via the Mode Register Set command (with BA0 = 0 and BA1 = 1) and retains the stored information until it is programmed again or the device loses power. The Extended mode Register must be loaded when all banks are idle, and the controller must wait the specified time before initiating any subsequent operation. Violating either these requirements result in unspecified operation. Unused bit A5 to A11 have to be programmed to “0”.

Extended Mode Register Table



M4	M3	max. case temp.
0	0	70^0C
0	1	45^0C
1	0	15^0C
1	1	85^0C

M2	M1	M0	banks to be self-refreshed
0	0	0	all banks
0	0	1	1/2 array (BA1=0)
0	1	0	1/4 array (BA1=0, BA0=0)
0	1	1	Reserved
1	0	0	Reserved
1	0	1	1/8 array (BA1=BA0=0, RA11=0)
1	1	0	1/16 array (BA1=BA0=0, RA11=RA10=0)
1	1	1	Reserved

*)BA1 and BA0 must be 1, 0 to select the Extended Mode Register (Vs. the Mode Register)

Read and Write Operation

When $\overline{RAS}$ is low and both $\overline{CAS}$ and $\overline{WE}$ are high at the positive edge of the clock, a $\overline{RAS}$ cycle starts. According to address data, a word line of the selected bank is activated and all of sense amplifiers associated to the wordline are set. A $\overline{CAS}$ cycle is triggered by setting $\overline{RAS}$ high and $\overline{CAS}$ low at a clock timing after a necessary delay, t_{RCD}, from the $\overline{RAS}$ timing. $\overline{WE}$ is used to define either a read ($\overline{WE}$ = H) or a write ($\overline{WE}$ = L) at this stage.

SDRAM provides a wide variety of fast access modes. In a single $\overline{CAS}$ cycle, serial data read or write operations are allowed at up to a 133 MHz data rate. The numbers of serial data bits are the burst length programmed at the mode set operation, i.e., one of 1, 2, 4, 8 and full page. Column addresses are segmented by the burst length and serial data accesses are done within this boundary. The first column address to be accessed is supplied at the $\overline{CAS}$ timing and the subsequent addresses are generated automatically by the programmed burst length and its sequence. For example, in a burst length of 8 with interleave sequence, if the first address is ‘2’, then the rest of the burst sequence is 3, 0, 1, 6, 7, 4, and 5.

Full page burst operation is only possible using the sequential burst type and page length is a function of the I/O organisation and column addressing. Full page burst operation do not self terminate once the burst length has been reached. In other words, unlike burst length of 2, 4 and 8, full page burst continues until it is terminated using another command.

Similar to the page mode of conventional DRAM's, burst read or write accesses on any column address are possible once the $\overline{RAS}$ cycle latches the sense amplifiers. The maximum t_{RAS} or the refresh interval time limits the number of random column accesses. A new burst access can be done even before the previous burst ends. The interrupt operation at every clock cycle is supported. When the previous burst is interrupted, the remaining addresses are overridden by the new address with the full burst length. An interrupt which accompanies an operation change from a read to a write is possible by exploiting DQM to avoid bus contention.

When two or more banks are activated sequentially, interleaved bank read or write operations are possible. With the programmed burst length, alternate access and precharge operations on two or more banks can realize fast serial data access modes among many different pages. Once two or more banks are activated, column to column interleave operation can be performed between different pages. When the partial array activation is set, data will get lost when self-refresh is used in all non activated banks.

Burst Length and Sequence

Burst Length	Starting Address (A2 A1 A0)	Sequential Burst Addressing (decimal)	Interleave Burst Addressing (decimal)
2	xx0	0, 1	0, 1
	xx1	1, 0	1, 0
4	x00	0, 1, 2, 3	0, 1, 2, 3
	x01	1, 2, 3, 0	1, 0, 3, 2
	x10	2, 3, 0, 1	2, 3, 0, 1
	x11	3, 0, 1, 2	3, 2, 1, 0
8	000	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7
	001	1 2 3 4 5 6 7 0	1 0 3 2 5 4 7 6
	010	2 3 4 5 6 7 0 1	2 3 0 1 6 7 4 5
	011	3 4 5 6 7 0 1 2	3 2 1 0 7 6 5 4
	100	4 5 6 7 0 1 2 3	4 5 6 7 0 1 2 3
	101	5 6 7 0 1 2 3 4	5 4 7 6 1 0 3 2
	110	6 7 0 1 2 3 4 5	6 7 4 5 2 3 0 1
	111	7 0 1 2 3 4 5 6	7 6 5 4 3 2 1 0
Full Page	nnn	Cn, Cn+1, Cn+2	not supported

Refresh Mode

SDRAM has two refresh modes, Auto Refresh and Self Refresh.

Auto-Refresh

Auto Refresh is similar to the $\overline{CAS}$ -before-$\overline{RAS}$ refresh of conventional DRAMs. All of banks must be precharged before applying any refresh mode. An on-chip address counter increments the word and the bank addresses and no bank information is required for both refresh modes.

The chip enters the Auto Refresh mode, when $\overline{RAS}$ and $\overline{CAS}$ are held low and CKE and $\overline{WE}$ are held high at a clock timing. The mode restores word line after the refresh and no external precharge command is necessary. A minimum t_{RC} time is required between two automatic refreshes in a burst refresh mode. The same rule applies to any access command after the automatic refresh operation.

In Auto-Refresh mode all banks are refreshed, independed if the partial activation has been set.

Self-Refresh:

The chip has an on-chip timer and the Self Refresh mode is available. It enters the mode when $\overline{RAS}$, $\overline{CAS}$, and CKE are low and $\overline{WE}$ is high at a clock timing. All of external control signals including the clock are disabled. Returning CKE to high enables the clock and initiates the refresh exit operation. After the exit command, at least one t_{RC} delay is required prior to any access command. Low Power SDRAMs have the possibility to program the refresh period of the on-chip time with the use of an appropriate MRS command in three steps, depending on the maximum operation case temperature in the application. In partial activation mode only the selected banks will be refreshed. Data written to the non activated banks will get lost after a period defined by tref.

DQM Function

DQMx has two functions for data I/O read and write operations. During reads, when it turns to “high” at a clock timing, data outputs are disabled and become high impedance after two clock delay (DQM Data Disable Latency t_{DQZ}). It also provides a data mask function for writes. When DQM is activated, the write operation at the next clock is prohibited (DQM Write Mask Latency t_{DQW} = zero clocks).

Suspend Mode

During normal access mode, CKE is held high enabling the clock. When CKE is low, it freezes the internal clock and extends data read and write operations. One clock delay is required for mode entry and exit (Clock Suspend Latency t_{CSL}).

Power Down

In order to reduce standby power consumption, a power down mode is available. All banks must be precharged and the necessary Precharge delay (t_{RP}) must occur before the SDRAM can enter the Power Down mode. Once the Power Down mode is initiated by holding CKE low, all of the receiver circuits except CLK and CKE are gated off. The Power Down mode does not perform any refresh operations, therefore the device can’t remain in Power Down mode longer than the Refresh period (t_{REF}) of the device. Exit from this mode is performed by taking CKE “high”. One clock delay is required for power down mode entry and exit.

Deep Power Down Mode

The Deep Power Down Mode is an unique function on Mobile RAMs with very low standby currents. All internal voltage generators inside the Mobile RAMs are stopped and all memory data will be lost in this mode. To enter the Deep Power Down mode all banks must be precharged and the necessary Precharge delay (t_{RP}) must occur.

Auto Precharge

Two methods are available to precharge SDRAMs. In an automatic precharge mode, the $\overline{CAS}$ timing accepts one extra address, CA10, to determine whether the chip restores or not after the operation. If CA10 is high when a Read Command is issued, the Read with Auto-Precharge function is initiated. If CA10 is high when a Write Command is issued, the Write with Auto-Precharge function is initiated. The SDRAM automatically enters the precharge operation a time delay equal to t_{WR} (Write recovery time) after the last data in.

Precharge Command

There is also a separate precharge command available. When $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at a clock timing, it triggers the precharge operation. Three address bits, BA0, BA1 and A10 are used to define banks as shown in the following list. The precharge command can be imposed one clock before the last data out for $\overline{CAS}$ latency = 2 and two clocks before the last data out for $\overline{CAS}$ latency = 3. Writes require a time delay t_{WR} from the last data out to apply the precharge command.

Bank Selection by Address Bits:

A10	BA0	BA1	
0	0	0	Bank 0
0	0	1	Bank 1
0	1	0	Bank 2
0	1	1	Bank 3
1	x	x	all Banks

Burst Termination

Once a burst read or write operation has been initiated, there are several methods in which to terminate the burst operation prematurely. These methods include using another Read or Write Command to interrupt an existing burst operation, use a Precharge Command to interrupt a burst cycle and close the active bank, or using the Burst Stop Command to terminate the existing burst operation but leave the bank open for future Read or Write Commands to the same page of the active bank. When interrupting a burst with another Read or Write Command care must be taken to avoid DQ contention. The Burst Stop Command, however, has the fewest restrictions making it the easiest method to use when terminating a burst operation before it has been completed. If a Burst Stop command is issued during a burst write operation, then any residual data from the burst write cycle will be ignored. Data that is presented on the DQ pins before the Burst Stop Command is registered will be written to the memory.

Electrical Characteristics

Absolute Maximum Ratings

Operating Case Temperature Range (commercial) ..... 0 to + 70 C
Operating Case Temperature Range (extended) ..... -25 to + 85 C
Storage Temperature Range ..... – 55 to + 150 C
Input/Output Voltage ..... – 0.3 to V_{DD} + 0.3 V
Power Supply Voltage V_{DD} ..... – 0.3 to + 3.6 V
Power Dissipation ..... 0.7 W
Data out Current (short circuit) ..... 50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operation and DC Characteristics

T_{CASE} = 0 to 70 °C (commercial) / -25 to 85°C (Extended);
V_{SS} = 0 V; V_{DD}= 2.5V ± 0.2 V, V_{DDQ} = 1.8V ± 0.15 V

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
DRAM Core Supply Voltage	V_{DD}	2.3	2.7	V	
I/O Supply Voltage	V_{DDQ}	1.65	1.95	V	3
Input High Voltage (CMD, Addr.)	V_{IH}	0.8 x V_{DDQ}	V_{DDQ} + 0.3	V	1, 2
Input Low Voltage (CMD, Addr.)	V_{IL}	– 0.3	+ 0.3	V	1, 2
Data Input High (Logic 1) Voltage	V_{IH}	0.8 x V_{DDQ}	V_{DDQ} + 0.3	V	
Data Input Low (Logic 0) Voltage	V_{IL}	– 0.3	+ 0.3	V	
Data Output High (Logic 1) Voltage (I_{OH}=-0.1mA)	V_{OH}	V_{DDQ} - 0.2	–	V	–
Date Output Low (Logic 0) Voltage (I_{OL}=+0.1mA)	V_{OL}	–	0.2	V	4
Input Leakage Current, any input (0 V < V_{IN} < V_{DDQ}, all other inputs = 0 V)	$I_{I(L)}$	– 5	5	µA	4
Output Leakage Current (DQ is disabled, 0 V < V_{OUT} < V_{DD})	$I_{O(L)}$	– 5	5	µA	–

Notes

1. All voltages are referenced to V_{SS}.
2. V_{IH} may overshoot to V_{DD} + 0.8V for pulse width of < 4 ns with 2.5V. V_{IL} may undershoot to – 0.8 V for pulse width < 4.0 ns with 2.5V. Pulse width measured at 50% points with amplitude measured peak to DC reference.
3. I/O supply voltage is V_{DD} + 0.2 V tolerant
4. I/O driver characteristics will be defined in a later version of this document. An IBIS model will be available.

Capacitance :

T_{CASE} = 0 to 70 °C (commercial) / -25 to 85°C (Extended);
V_{DD} = 2.5V ± 0.2 V,V_{DDQ} = 1.8V ± 0.15 V, f = 1 MHz

Parameter	Symbol	Values		Unit
		min.	max.	
Input Capacitance (CLK)	C_{I1}	-	3.5	pF
Input Capacitance (A0 - A11, BA0, BA1, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, DQM)	C_{I2}	-	3.8	pF
Input/Output Capacitance (DQ)	C_{IO}	-	6.0	pF

Operating Currents

T_{CASE} = 0 to 70 °C (commercial) / -25 to 85°C (Extended);
V_{DD} = V_{DDQ}=2.5 V ± 0.2 V, V_{DDQ} = 1.8V ± 0.15 V
(Recommended Operating Conditions unless otherwise noted)

Parameter & Test Condition		Symb.	-7.5	-8	Unit	Note
Operating current t_{CK} = $t_{CK(MIN.)}$ All banks operated in random access, all banks operated in ping-pong manner	–	I_{CC1}	160	150	mA	3,4
Precharge standby current in Power Down Mode $\overline{CS}$ = $V_{IH\ (MIN.)}$, CKE ≤ $V_{IL(MAX.)}$	t_{CK} = min	I_{CC2P}		t.b.d.	mA	
Precharge standby current in Non Power Down Mode $\overline{CS}$ = $V_{IH\ (MIN.)}$, CKE ≥ $V_{IH(MIN.)}$	t_{CK} = min	I_{CC2N}	40	35	mA	
No operating current t_{CK} = min., $\overline{CS}$ = $V_{IH\ (MIN.)}$, active state (max. 4 banks)	CKE ≥ $V_{IH(MIN.)}$	I_{CC3N}	50	45	mA	
	CKE ≤ $V_{IL(MAX.)}$	I_{CC3P}			mA	
Burst Operating Current t_{CK} = min Read command cycling	–	I_{CC4}	100	90	mA	3, 4
Auto Refresh Current t_{CK} = min, trc = trcmin. Auto Refresh command cycling	–	I_{CC5}	230	210	mA	3
Deep Power Down Mode Current		I_{CC7}	10		µA	

Programmable Self-Refresh Currents:

Parameter & Test Condition	Extended Mode Register M[4:3] Tcase [°C]	Symb.	max.	Unit	Note
Self Refresh Current Self Refresh Mode CKE = 0.2 V, tck=infinity, full array activations, all banks	85°C max.	I_{CC6}	800	µA	7)
	70°C max.		400	µA	7)
	45°C max.		200	µA	7)
	15°C max.		t.b.d	µA	7)
Self Refresh Current Self Refresh Mode CKE = 0.2 V, tck=infinity, half array activations, Bank 0 +1	85°C max.	I_{CC6}	450	µA	7)
	70°C max.		225	µA	7)
	45°C max.		150	µA	7)
	15°C max.		t.b.d	µA	7)
Self Refresh Current Self Refresh Mode CKE = 0.2 V, tck=infinity, quarter array activation, Bank 0	85°C max.	I_{CC6}	225	µA	7)
	70°C max.		125	µA	7)
	45°C max.		75	µA	7)
	15°C max.		t.b.d	µA	7)

Notes:

5. These parameters depend on the cycle rate. These values are measured at 133 MHz for -7 & -7.5 and at 100 MHz for -8 parts. Input signals are changed once during t_{CK}. If the devices are operating at a frequency less than the maximum operation frequency, these current values are reduced by 1/ freq, meaning operation at half the maximum frequency reduces these current value by a factor of 2.
6. These parameters are measured with continuous data stream during read access and all DQ toggling. CL = 3 and BL = 4 is assumed and the V_{DDQ} current is excluded.
7. Target values to be verified on final product and may change.

AC Characteristics [1, 2]

T_{CASE} = 0 to 70 °C (commercial) / -25 to 85°C (Extended);
V_{SS} = 0 V; V_{DD} = V_{DDQ} = 2.5V ± 0.2 V, V_{DDQ} = 1.8V ± 0.15 V, t_T = 1 ns

Parameter	Symb.	-7.5		-8		Unit	Note
		min.	max.	min.	max.		
Clock and Clock Enable							
Clock Cycle Time							–
$\overline{CAS}$ Latency = 3	t_{CK}	7.5	–	8	–	ns	
$\overline{CAS}$ Latency = 2		10	–	10	–	ns	
Clock frequency							–
$\overline{CAS}$ Latency = 3	t_{CK}	–	133	–	125	MHz	
$\overline{CAS}$ Latency = 2		–	100	–	100	MHz	
Access Time from Clock							2, 3, 6
$\overline{CAS}$ Latency = 3	t_{AC}	–	5.4	–	6	ns	
$\overline{CAS}$ Latency = 2		–	6	–	6	ns	
Clock High Pulse Width	t_{CH}	2.5	–	3	–	ns	–
Clock Low Pulse Width	t_{CL}	2.5	–	3	–	ns	–
Transition Time	t_T	0.3	1.2	0.5	1.5	ns	–
Setup and Hold Times							
Input Setup Time	t_{IS}	1.5	–	2	–	ns	4
Input Hold Time	t_{IH}	0.8	–	1	–	ns	4
CKE Setup Time	t_{CKS}	1.5	–	2	–	ns	4
CKE Hold Time	t_{CKH}	0.8	–	1	–	ns	4
Mode Register Set-up Time	t_{RSC}	2	–	2	–	CLK	–
Power Down Mode Entry Time	t_{SB}	0	7.5	0	8	ns	–
Common Parameters							
Row to Column Delay Time	t_{RCD}	20	–	20	–	ns	5
Row Precharge Time	t_{RP}	20	–	20	–	ns	5
Row Active Time	t_{RAS}	45	100k	48	100k	ns	5
Row Cycle Time	t_{RC}	67	–	70	–	ns	5
Activate(a) to Activate(b) Command Period	t_{RRD}	15	–	16	–	ns	5

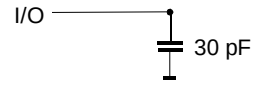
AC Characteristics (cont'd)[1, 2]

T_{CASE} = 0 to 70 °C (commercial) / -25 to 85°C (Extended);
V_{SS} = 0 V; V_{DD} = V_{DDQ} = 2.5V ± 0.2 V, V_{DDQ} = 1.8V ± 0.15 V, t_T = 1 ns

Parameter	Symb.	-7.5		-8		Unit	Note
		min.	max.	min.	max.		
$\overline{CAS}$(a) to $\overline{CAS}$(b) Command Period	t_{CCD}	1	–	1	–	CLK	–
Refresh Cycle							
Refresh Period	t_{REF}	–	64	–	64	ms	–
Self Refresh Exit Time	t_{SREX}	1	–	1	–	CLK	
Read Cycle							
Data Out Hold Time	t_{OH}	3	–	3	–	ns	2, 5, 6
Data Out to Low Impedance Time	t_{LZ}	1	–	0	–	ns	–
Data Out to High Impedance Time	t_{HZ}	3	7	3	8	ns	–
DQM Data Out Disable Latency	t_{DQZ}	–	2	–	2	CLK	–
Write Cycle							
Write Recovery Time	t_{WR}	14	–	14	–	ns	7
DQM Write Mask Latency	t_{DQW}	0	–	0	–	CLK	–

Notes

1. For proper power-up see the operation section of this data sheet.
2. AC timing tests are referenced to the 0.9 V crossover point for VDDQ = 1.8 V components. The transition time is measured between V_{IH} and V_{IL}. All AC measurements assume t_T = 1 ns with the AC output load circuit (details will be defined later). Specified t_{AC} and t_{OH} parameters are measured with a 30 pF only, without any resistive termination and with a input signal of 1V / ns edge rate.

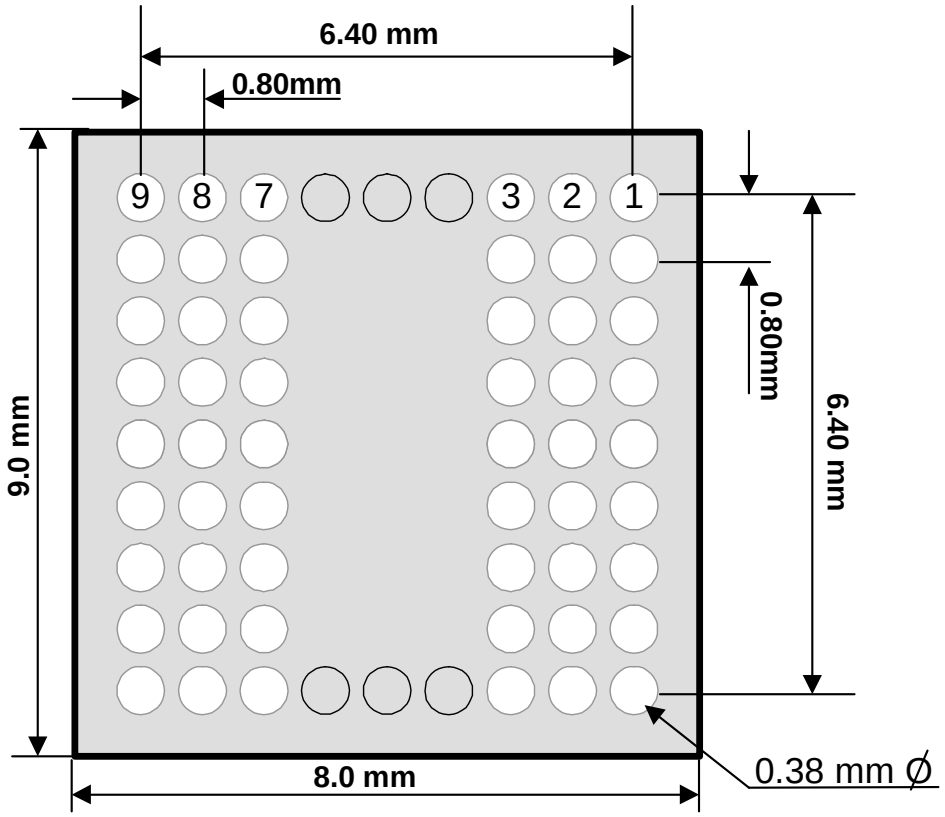


Measurement conditions for
t_{AC} and t_{OH}

3. If clock rising time is longer than 1 ns, a time (t_T/2 - 0.5) ns has to be added to this parameter.
4. If t_T is longer than 1 ns, a time (t_T - 1) ns has to be added to this parameter.
5. These parameter account for the number of clock cycle and depend on the operating frequency of the clock, as follows:
   the number of clock cycle = specified value of timing period (counted in fractions as a whole number)
6. Access time from clock tac is 4.6 ns for PC133 components with no termination and 0 pF load, Data out hold time toh is 1.8 ns for PC133 components with no termination and 0 pF load.
7. The write recovery time of twr = 14 ns cycles allows the use of one clock cycle for the write recovery time when the memory operation frequency is equal or less than 72MHz. For all memory operation frequencies higher than 72MHz two clock cycles for twr are mandatory. INFINEON recommends to use two clock cylces for the write recovery time in all applications.

Package Outlines

FBGA-BOC package
54 BGA package with 3 depop. rows

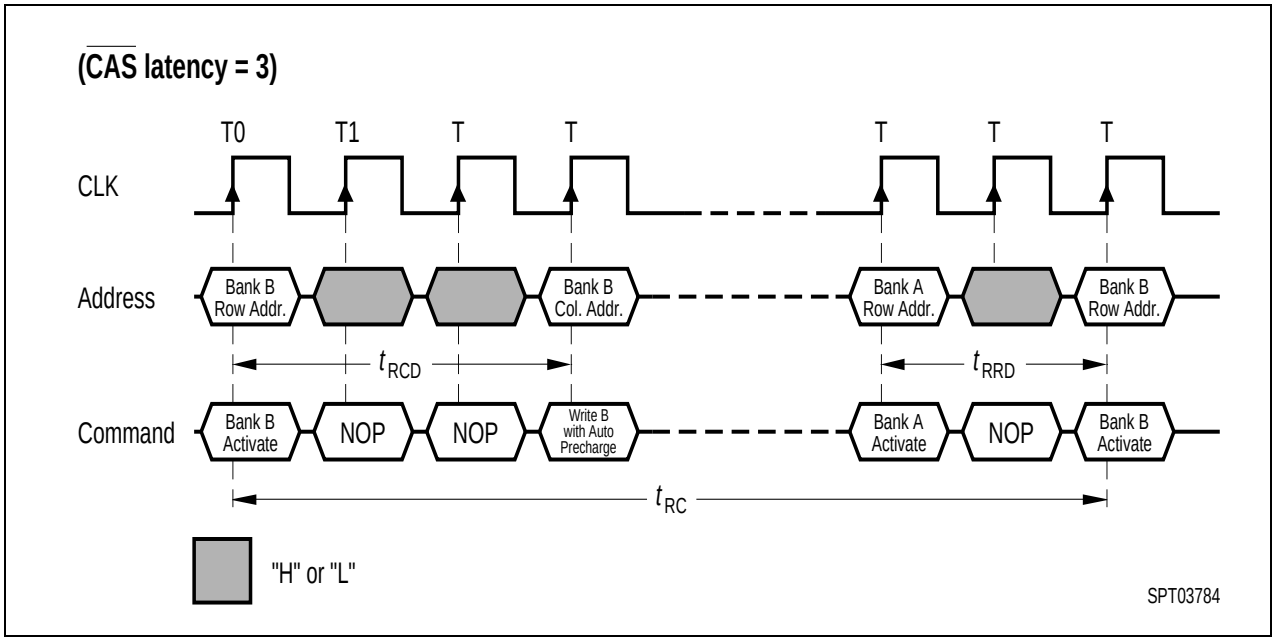


(Bottom View)

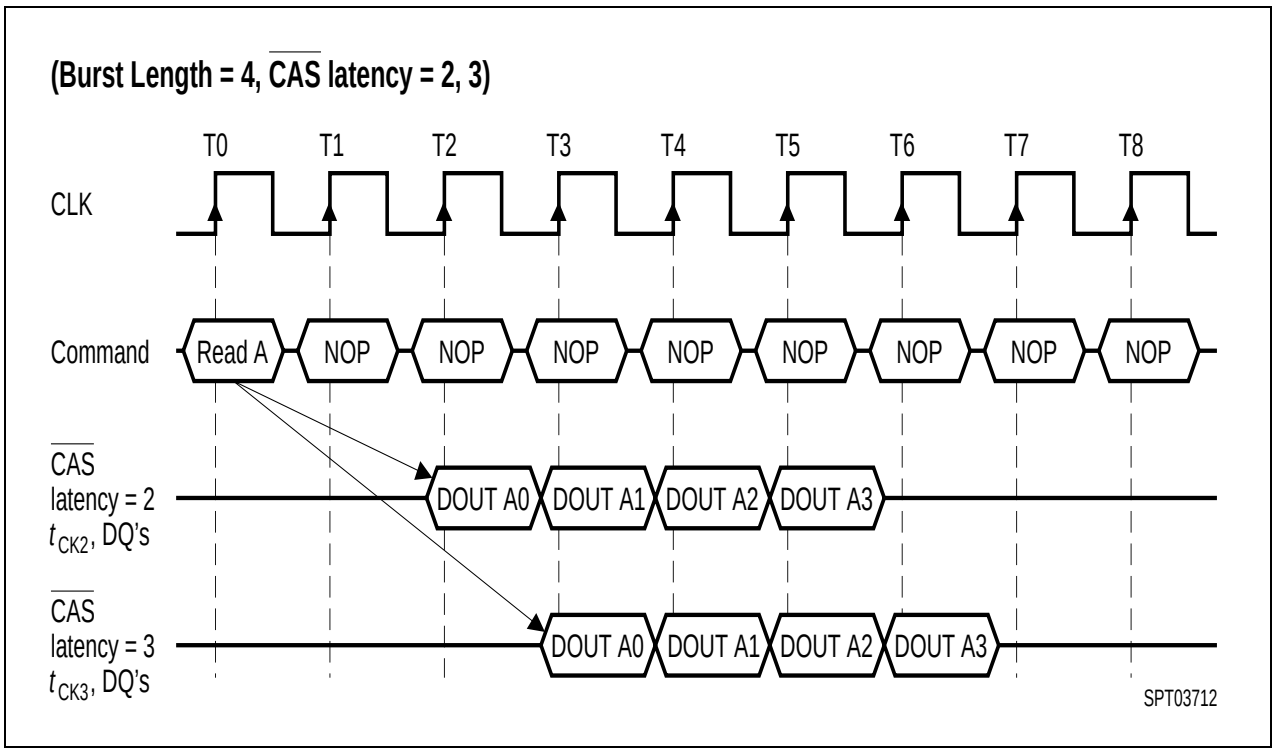
Marking Examples of BGA Packages:

Timing Diagrams

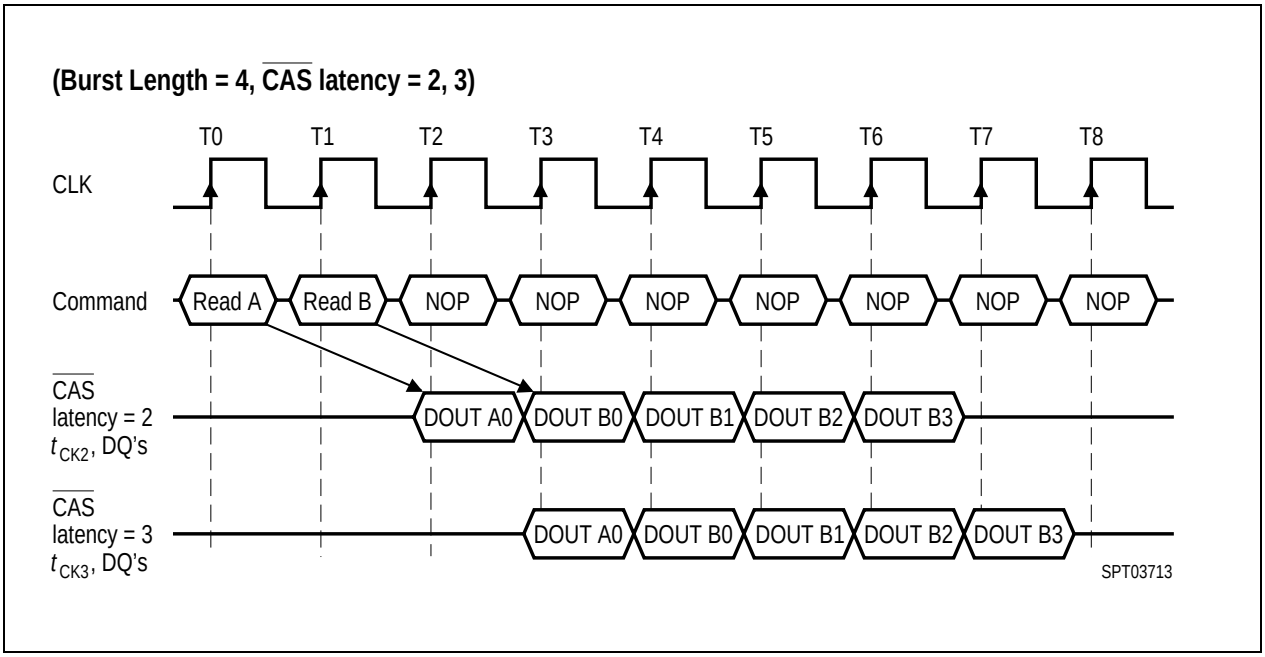
1. Bank Activate Command Cycle



2. Burst Read Operation

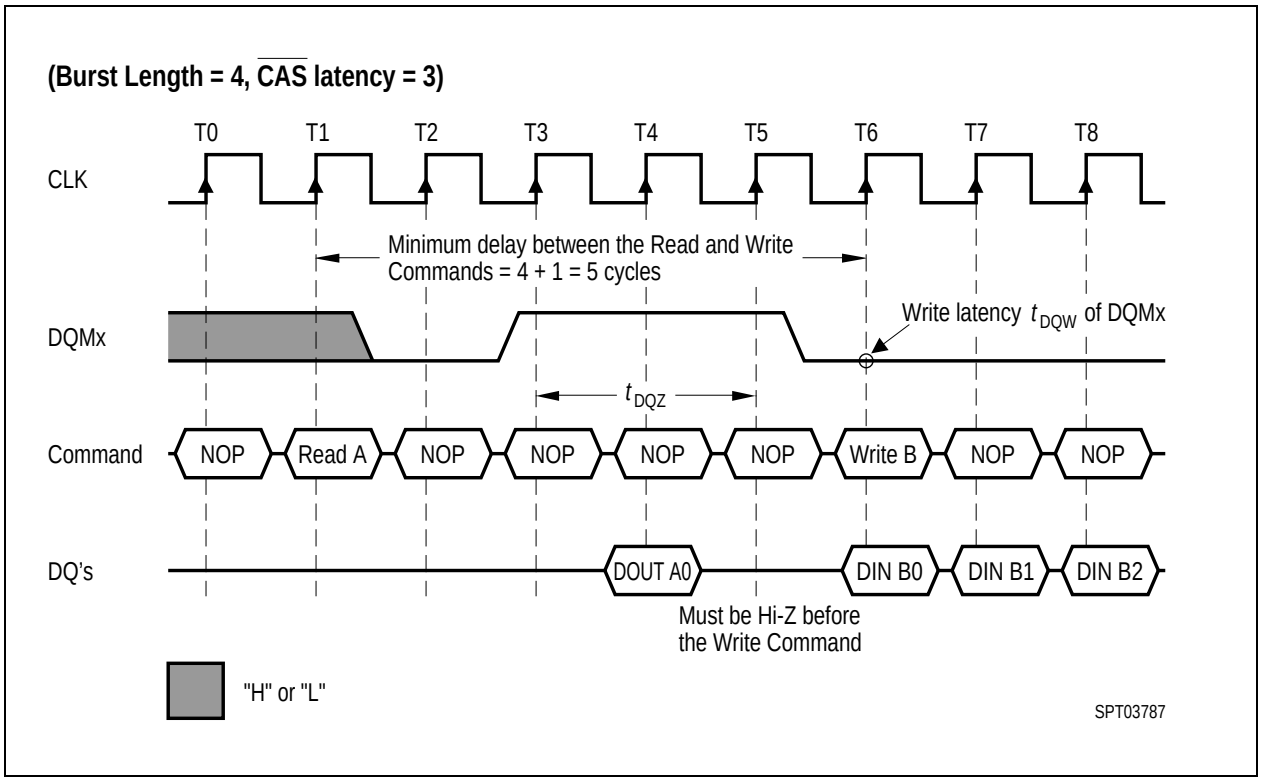


3. Read Interrupted by a Read

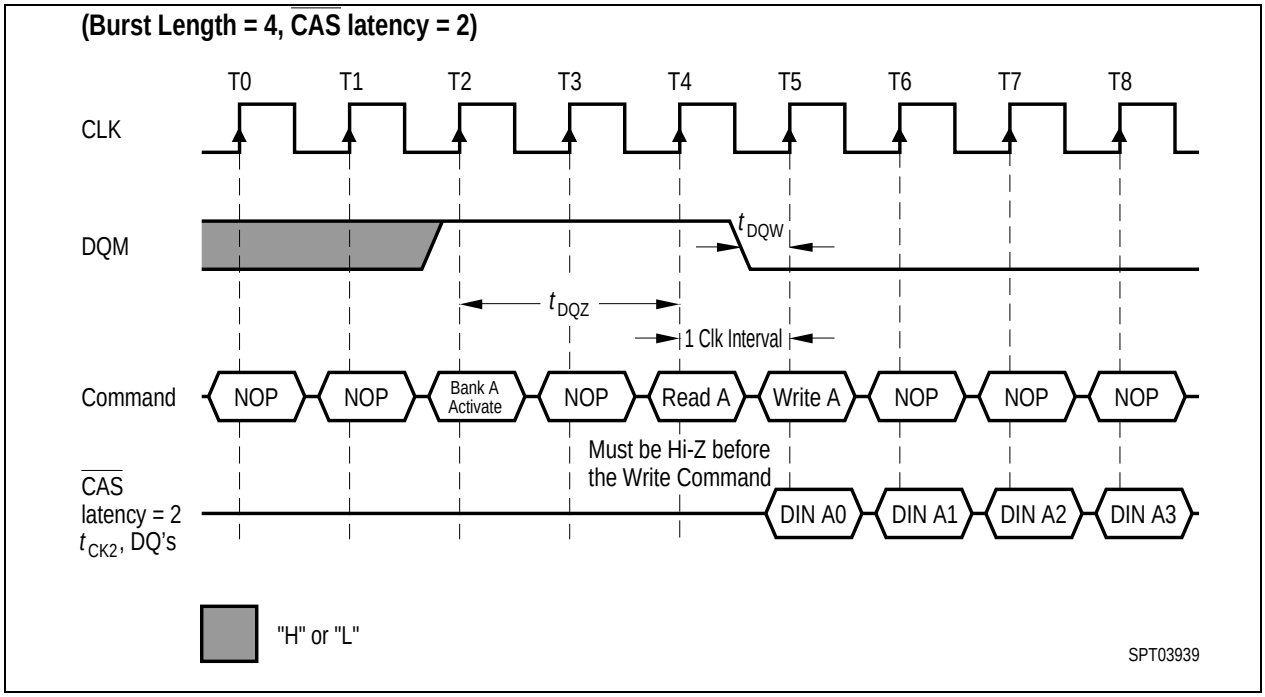


4. Read to Write Intrerval

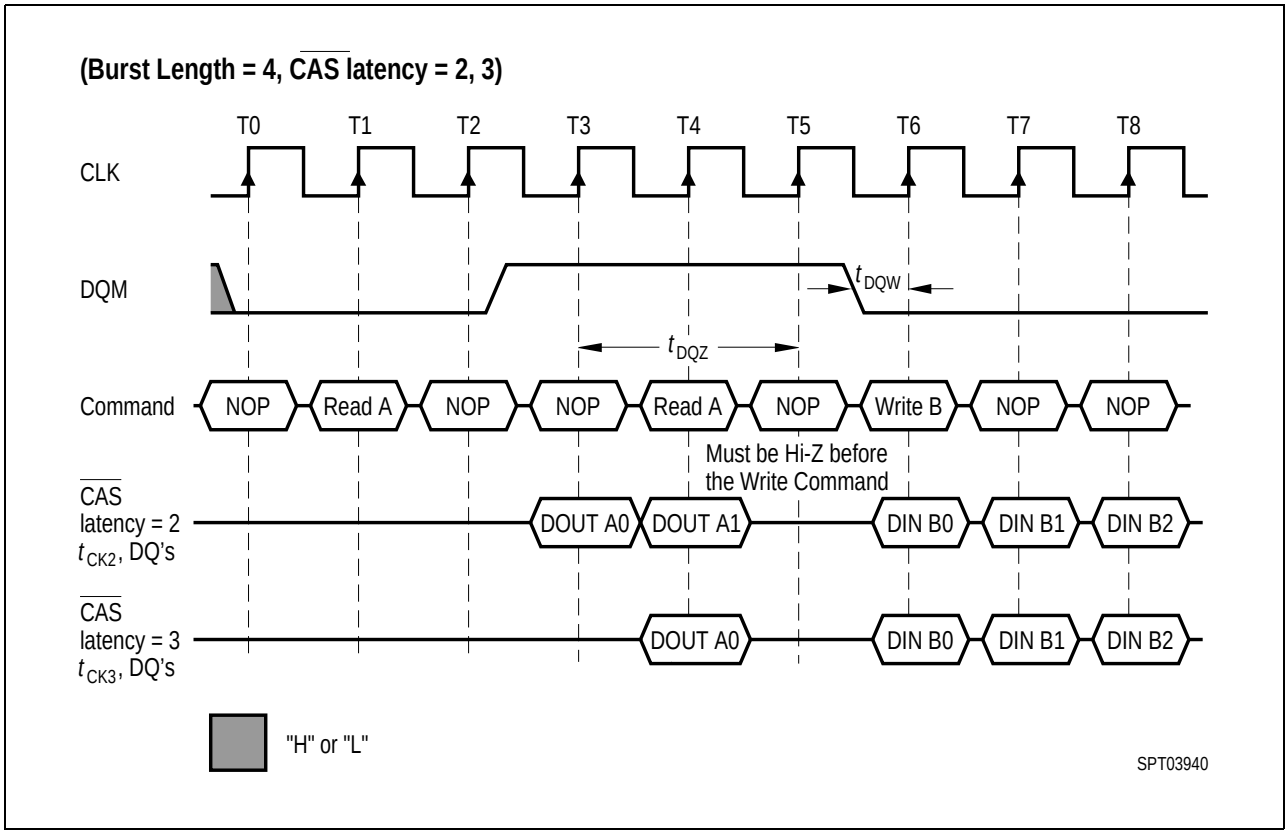
4.1 Read to Write Interval



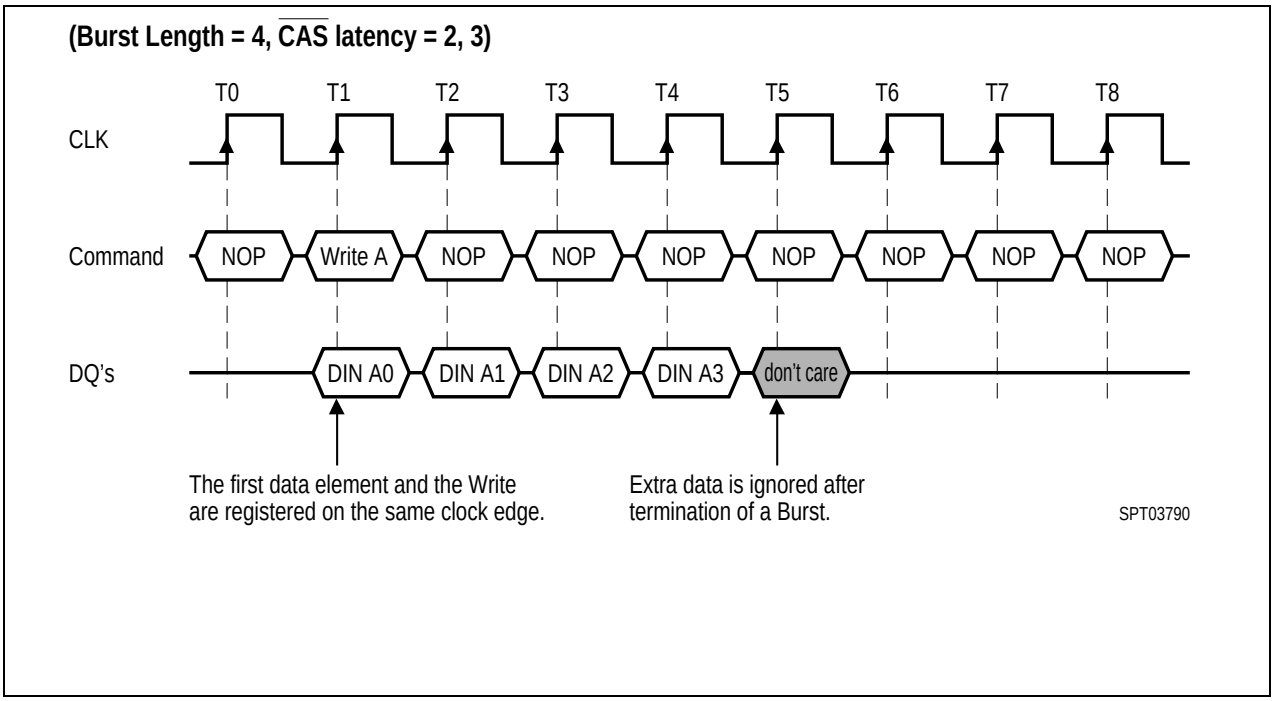
4 2. Minimum Read to Write Interval



4. 3. Non-Minimum Read to Write Interval

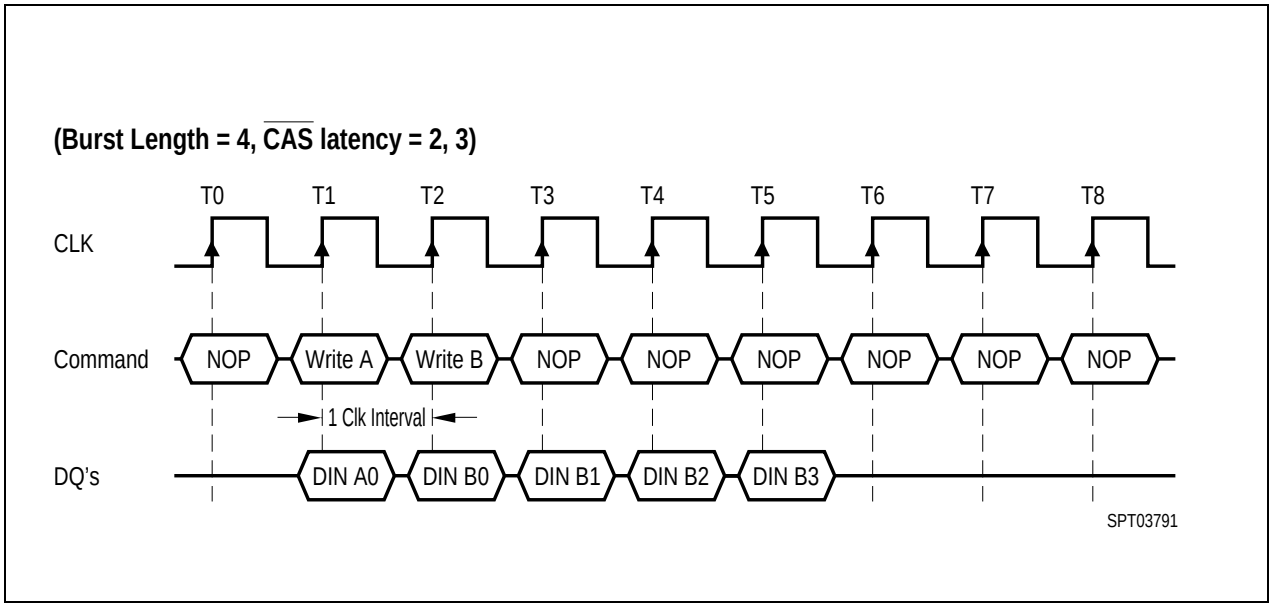


5. Burst Write Operation

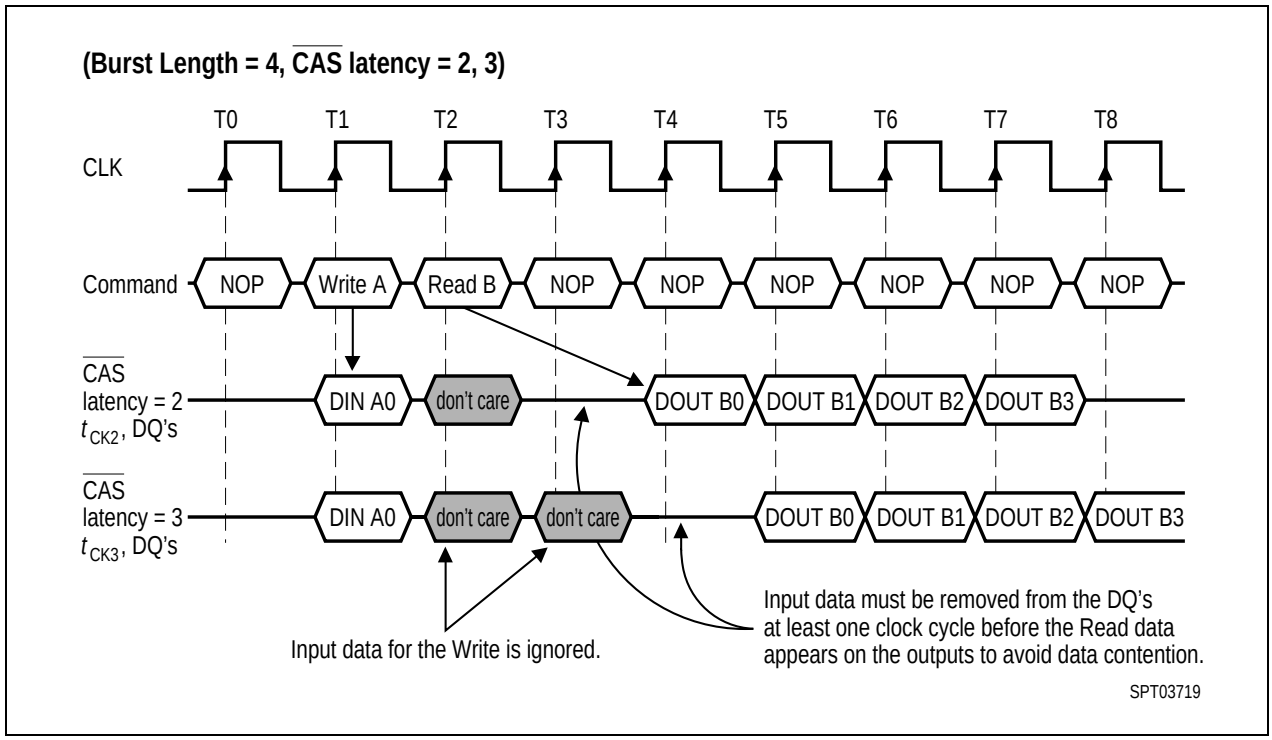


6. Write and Read Interrupt

6.1 Write Interrupted by a Write

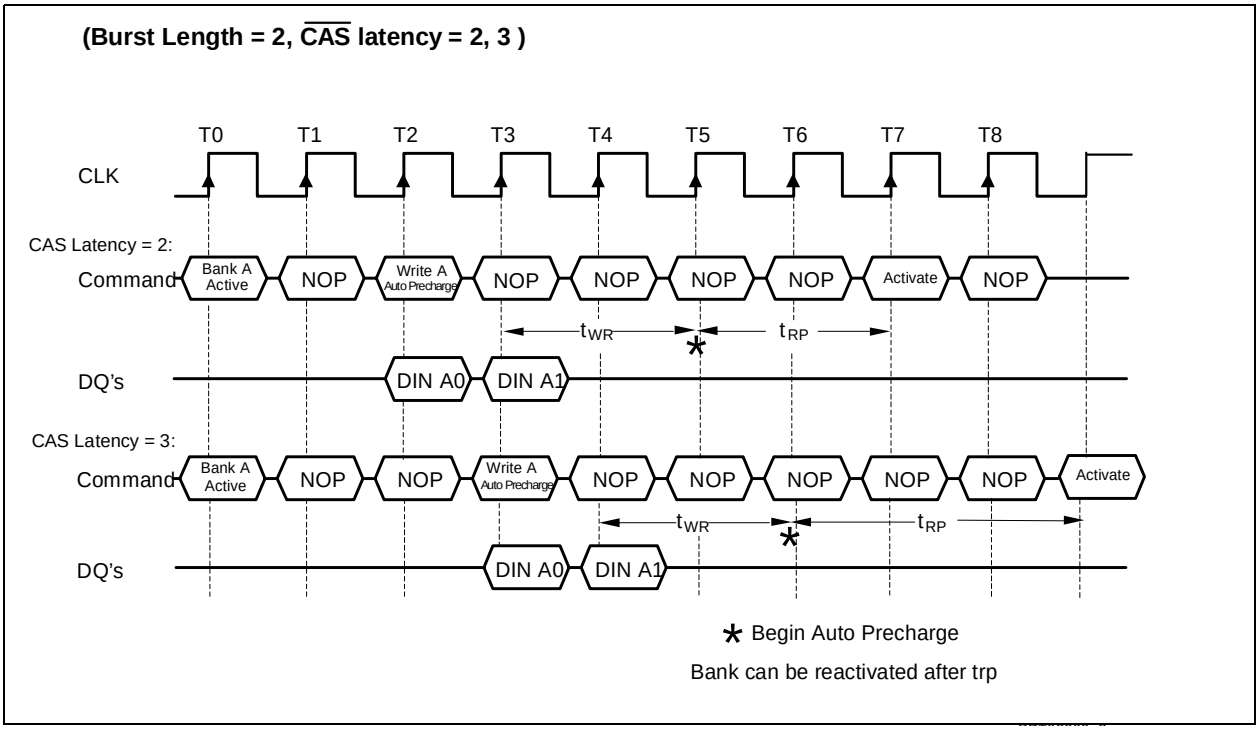


6.2 Write Interrupted by a Read

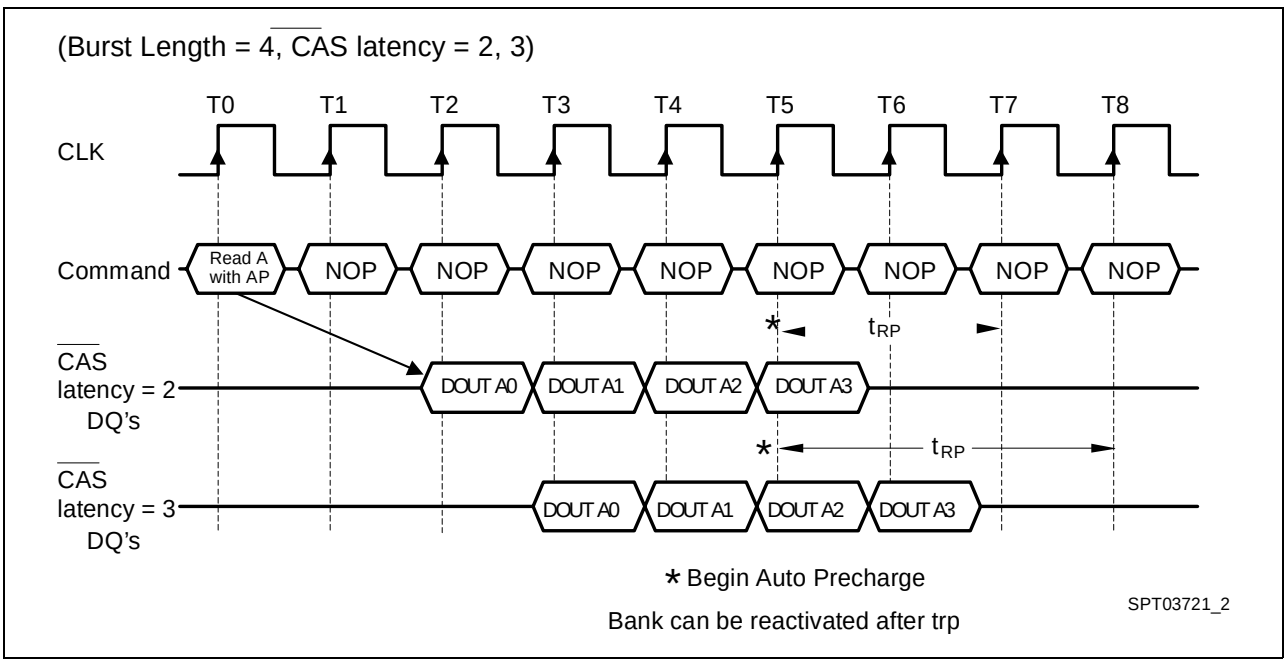


7. Burst Write and Read with Auto Precharge

7.1 Burst Write with Auto-Precharge

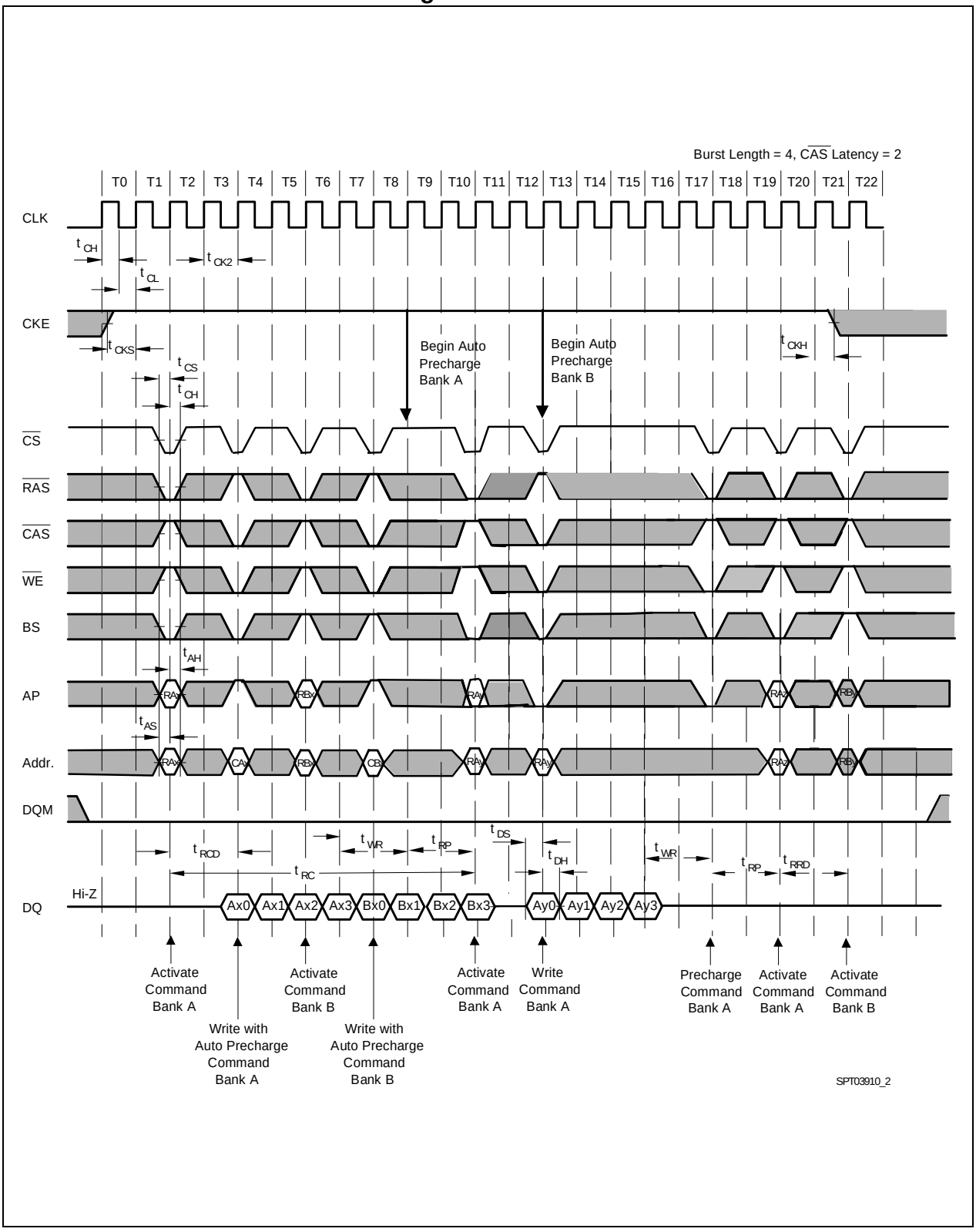


7.2 Burst Read with Auto-Precharge

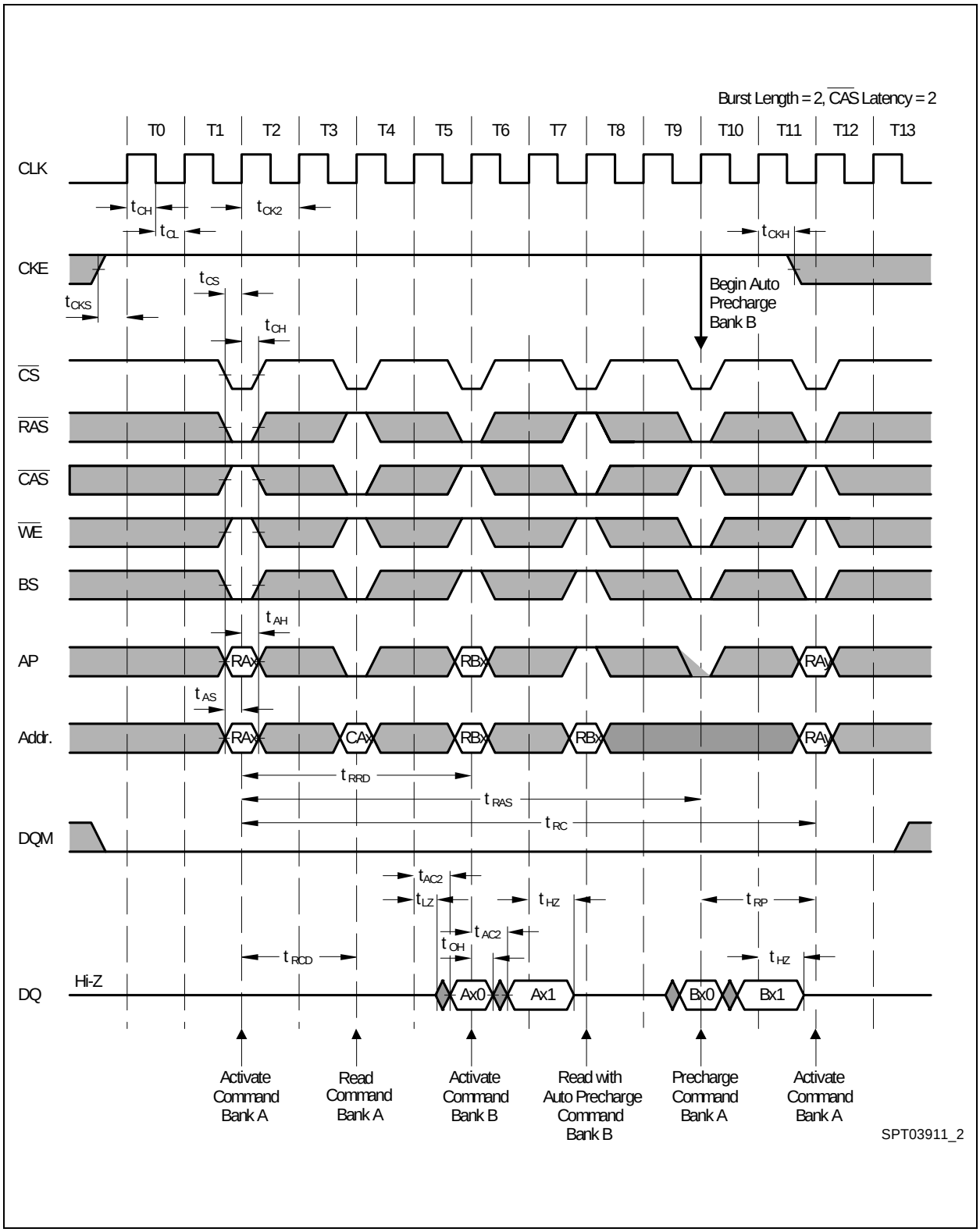


8. AC Parameters

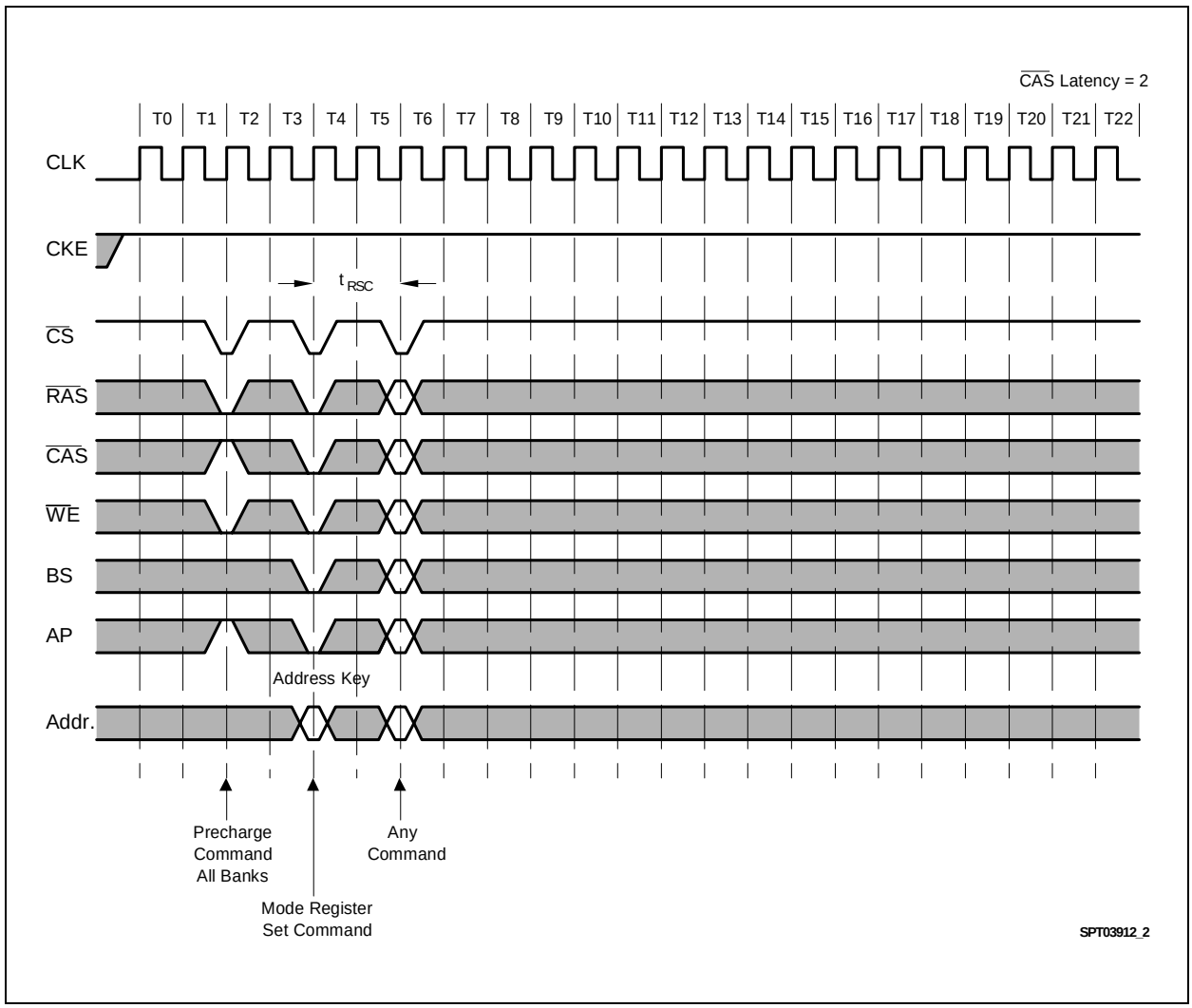
8.1 AC Parameters for a Write Timing



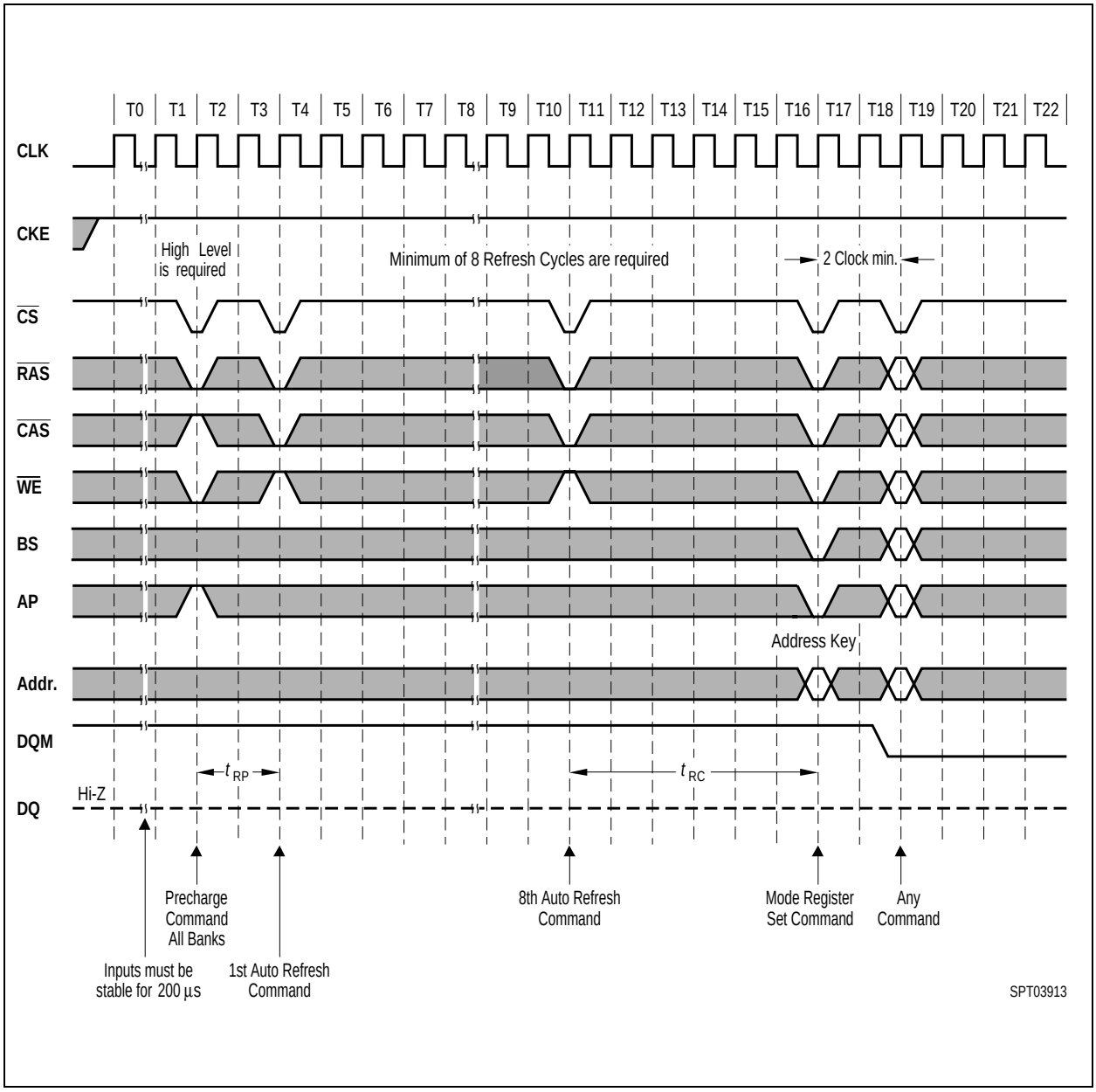
8.2 AC Parameters for a Read Timing



9. Mode Register Set

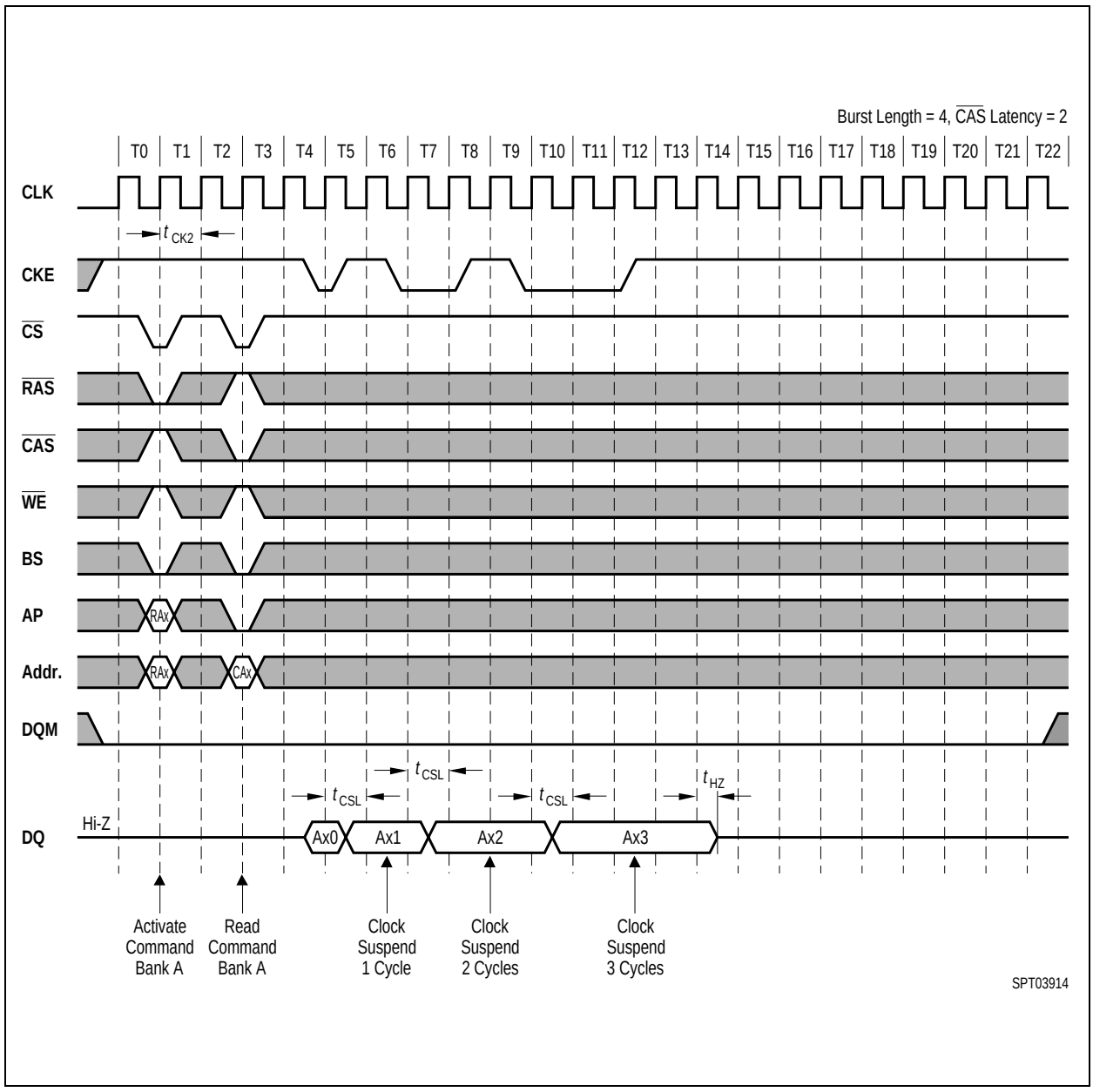


10. Power on Sequence and Auto Refresh (CBR)

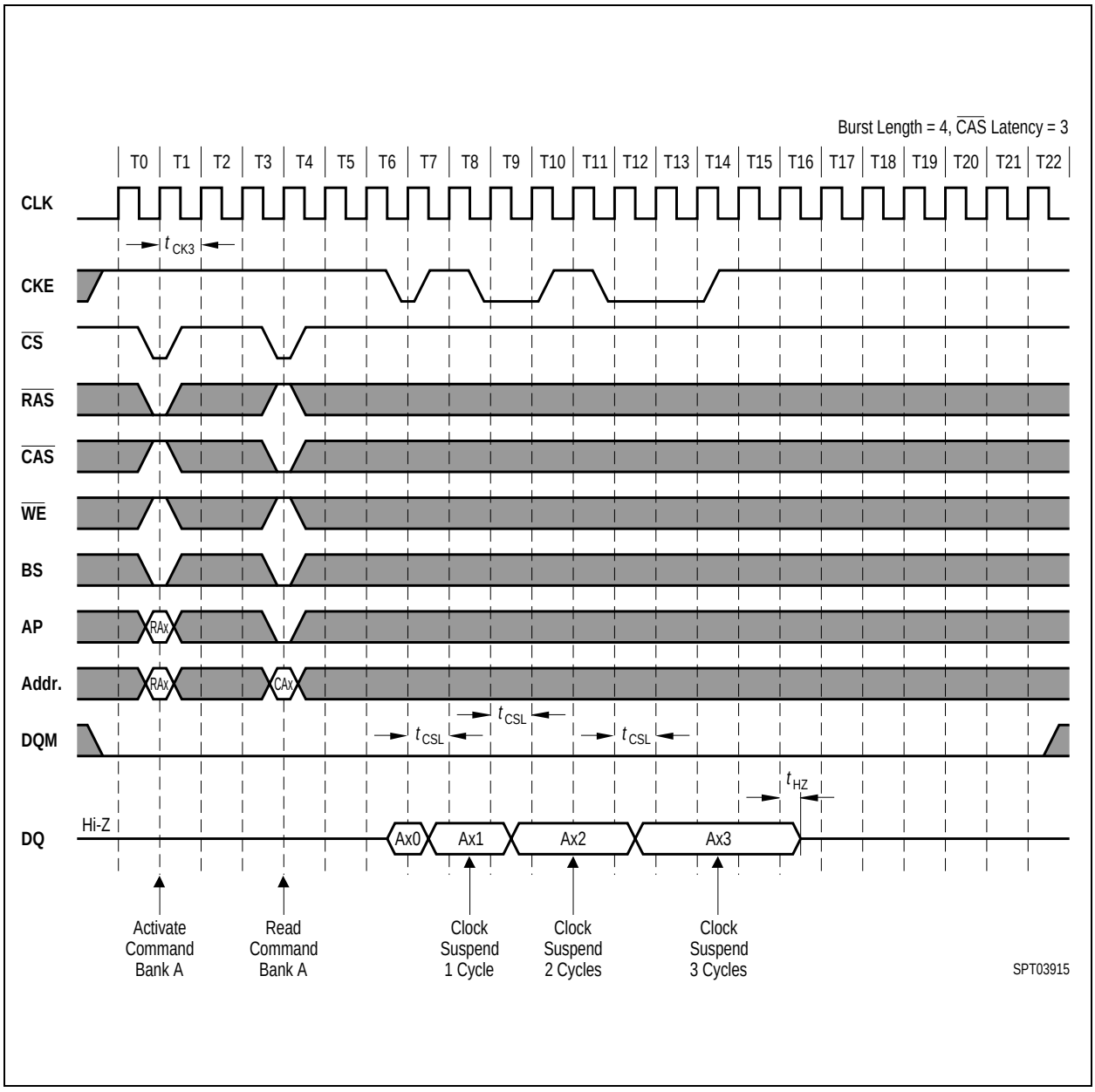


11. Clock Suspension (Using CKE)

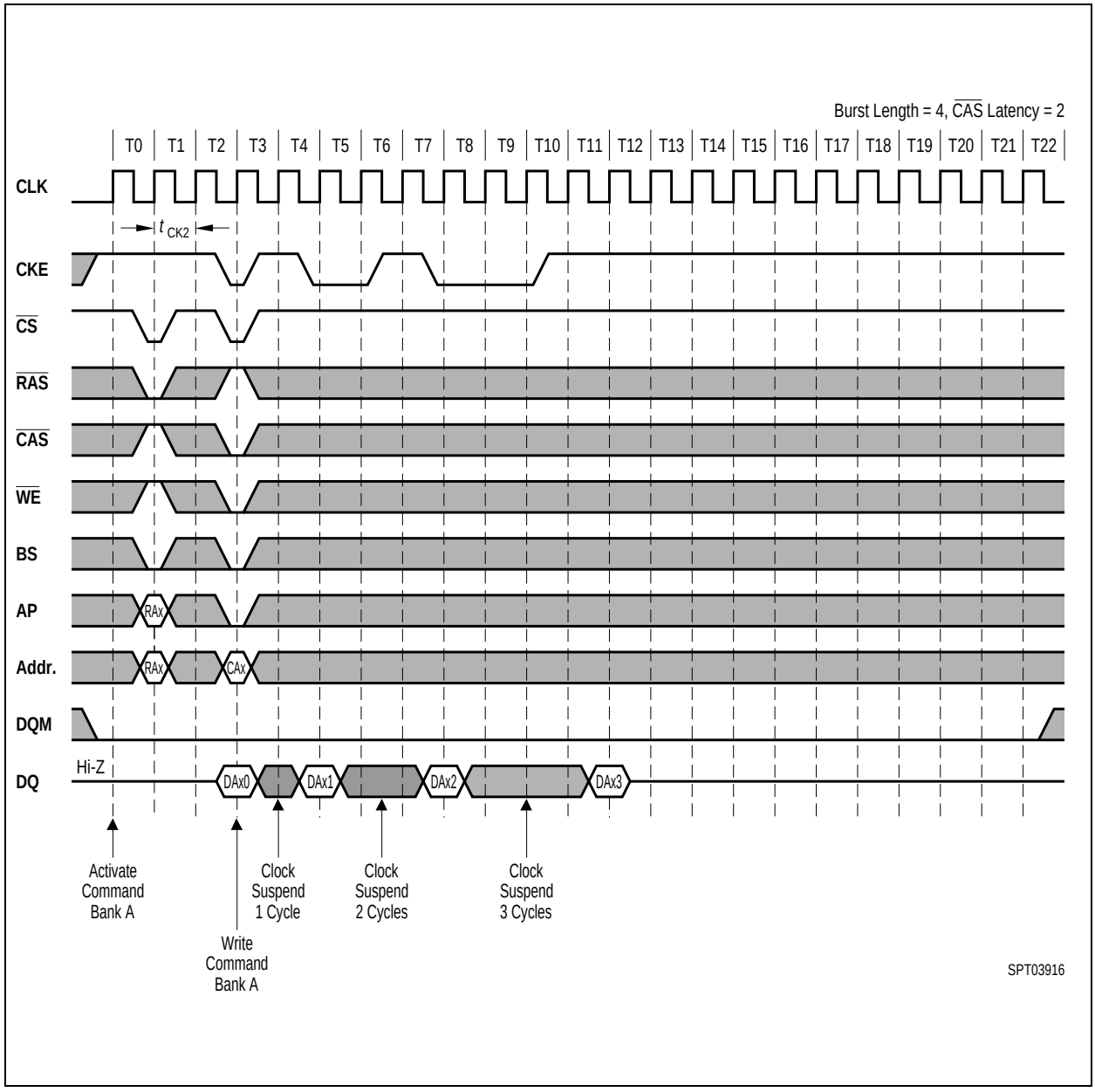
11.1 Clock Suspension During Burst Read $\overline{\text{CAS}}$ Latency = 2



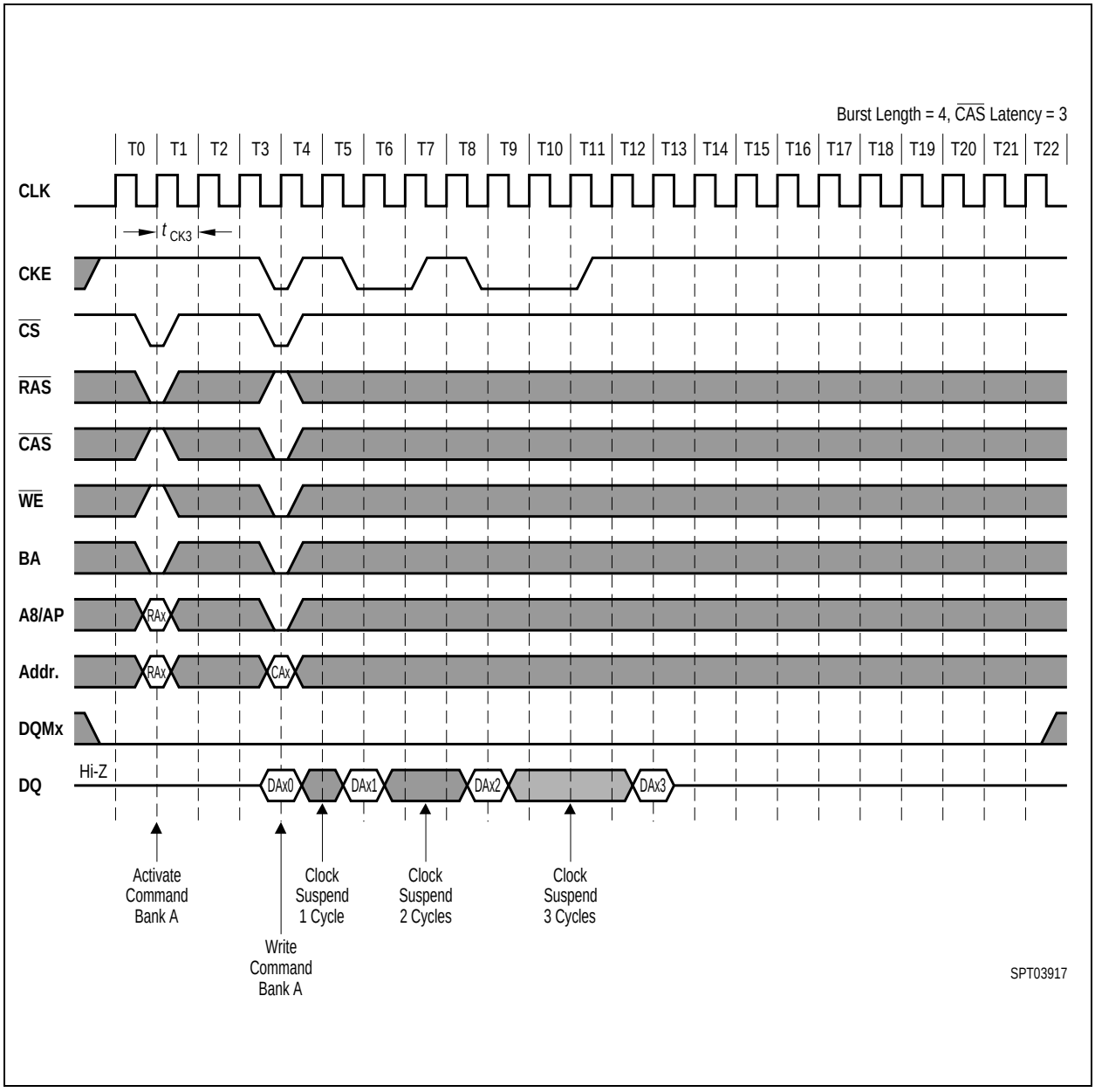
11.2 Clock Suspension During Burst Read $\overline{\text{CAS}}$ Latency = 3



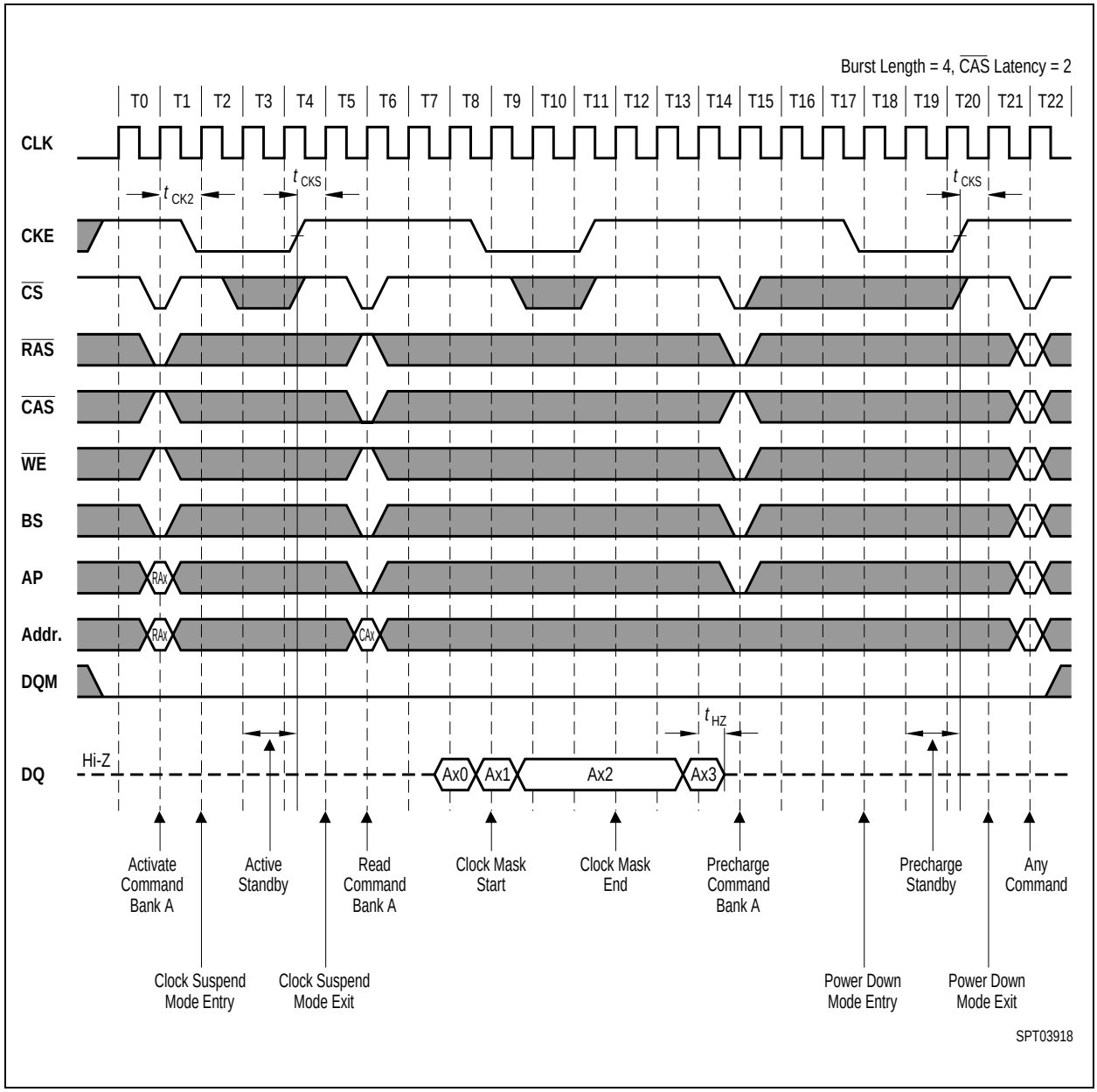
11.3 Clock Suspension During Burst Write $\overline{\text{CAS}}$ Latency = 2



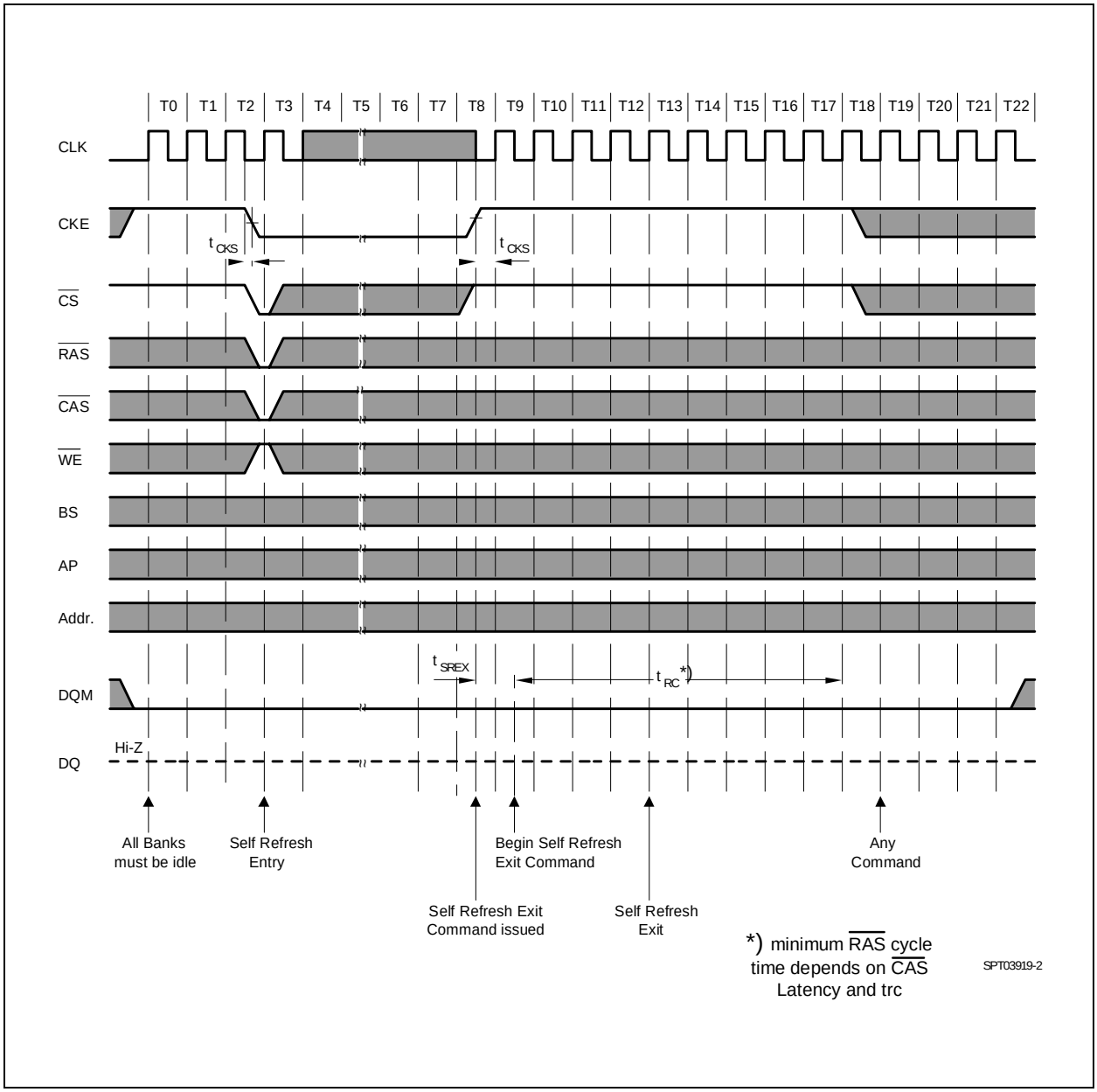
11.4 Clock Suspension During Burst Write $\overline{\text{CAS}}$ Latency = 3



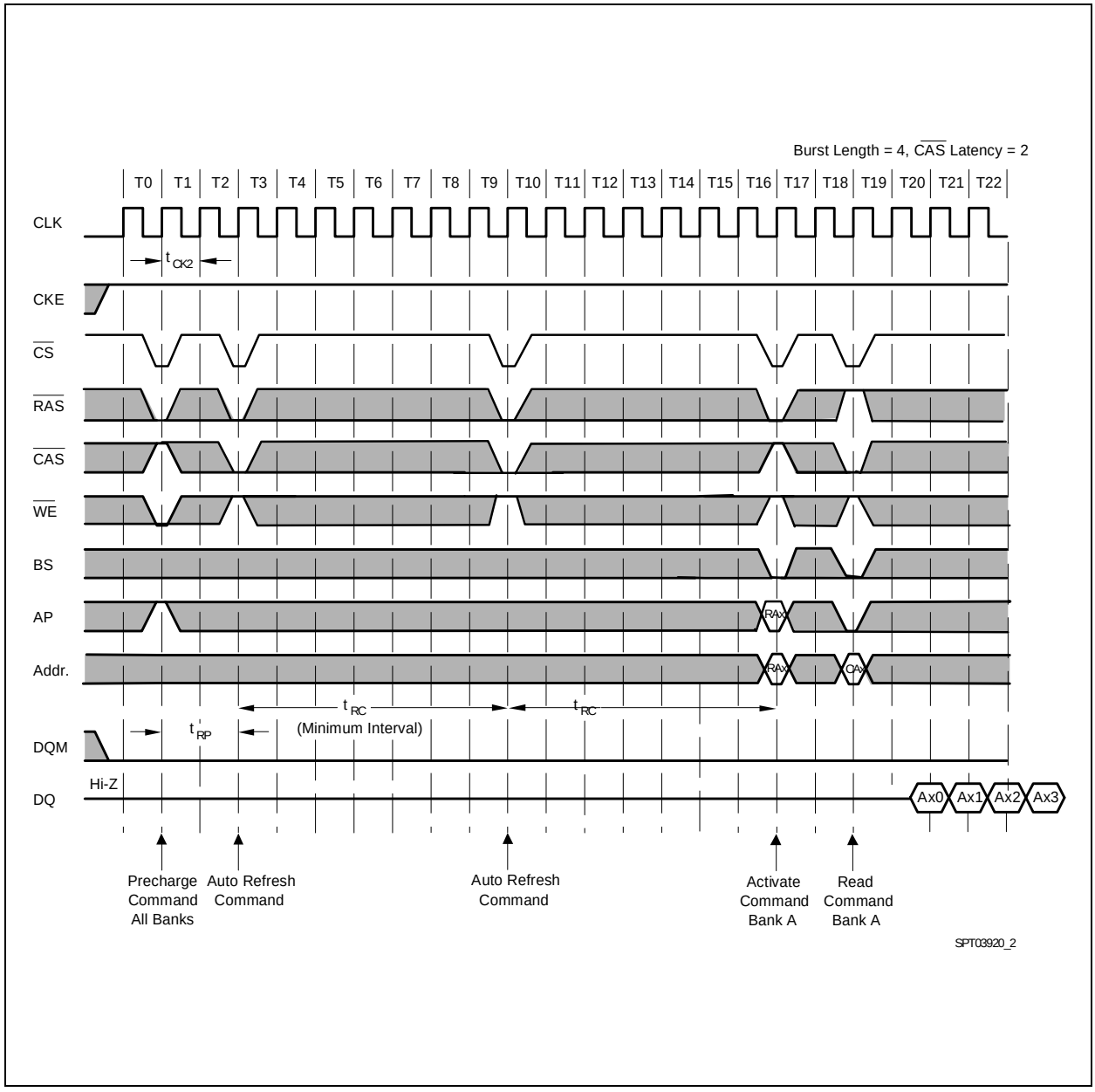
12. Power Down Mode and Clock Suspend



13. Self Refresh (Entry and Exit)

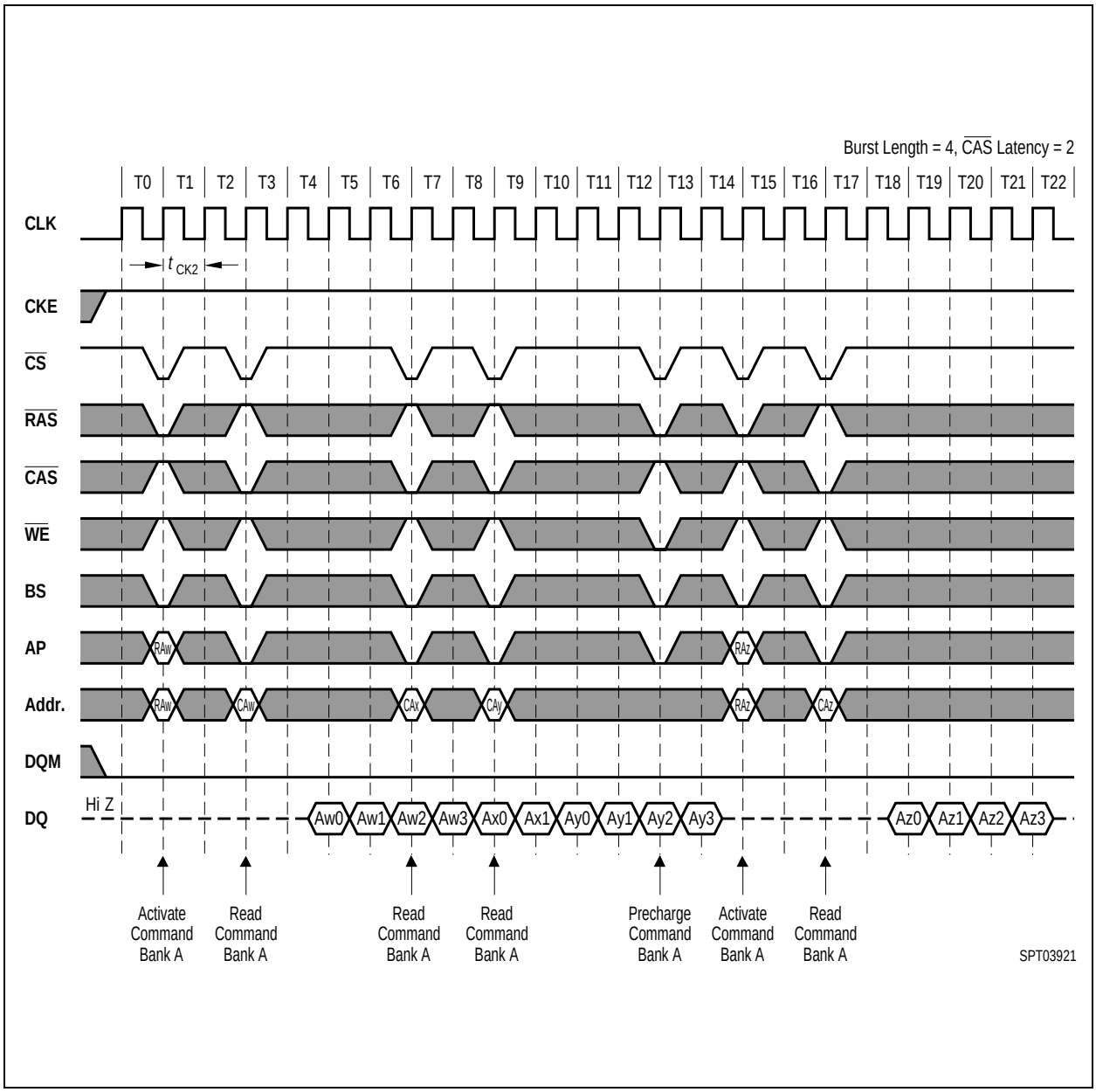


14. Auto Refresh (CBR)

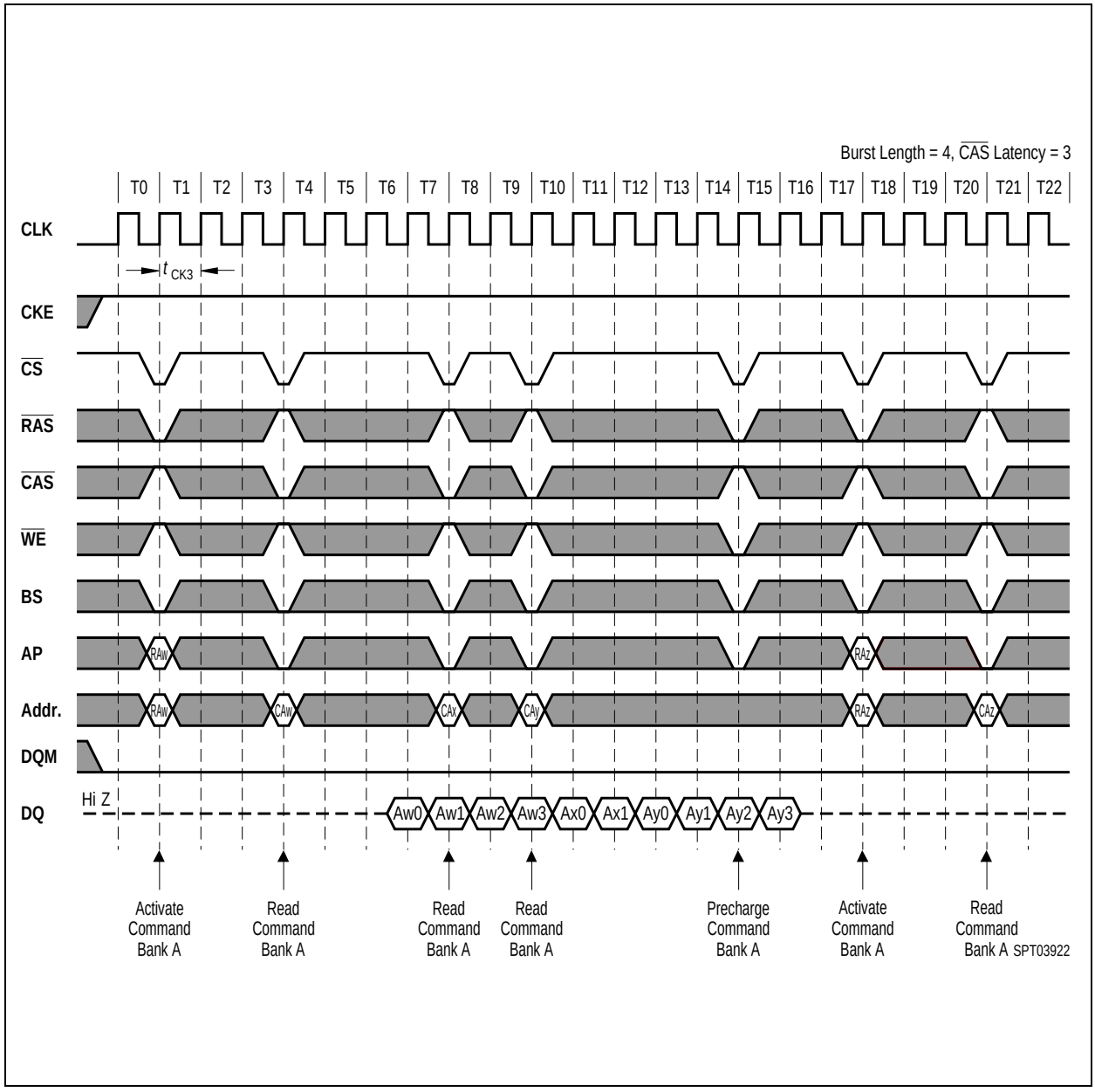


15. Random Column Read (Page within same Bank)

15.1 $\overline{\text{CAS}}$ Latency = 2

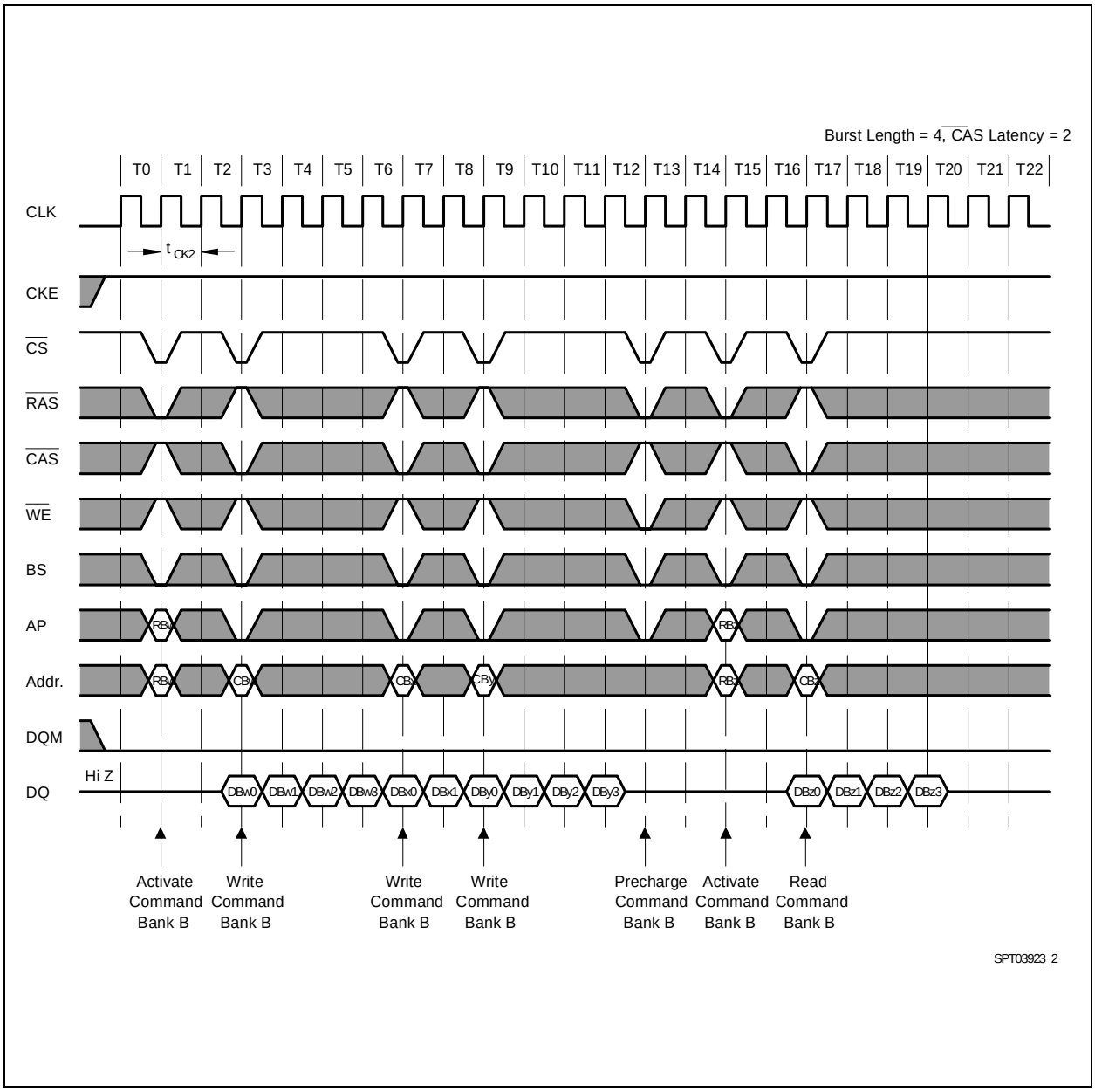


15.2 $\overline{\text{CAS}}$ Latency = 3

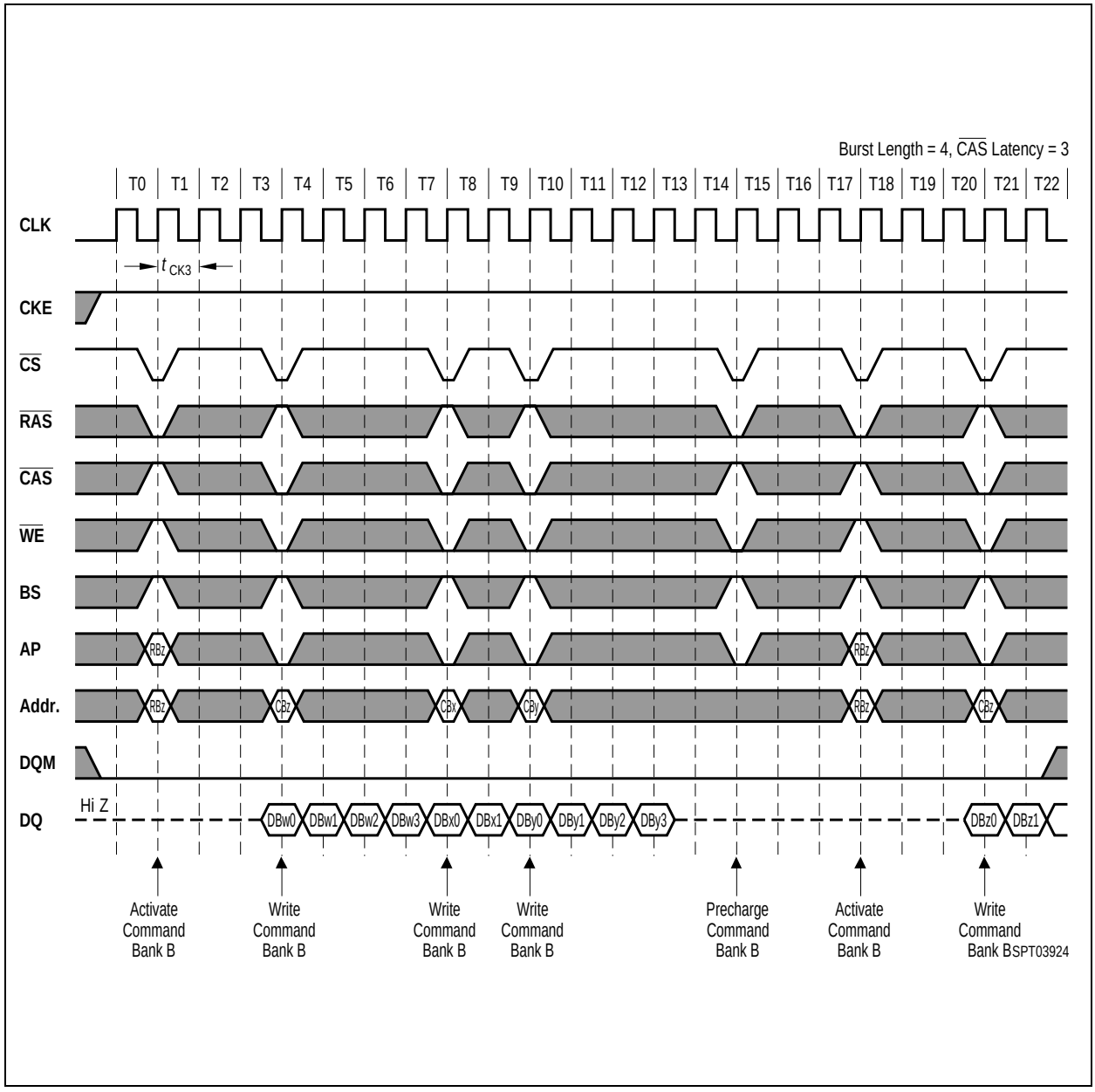


16. Random Column write (Page within same Bank)

16.1 $\overline{\text{CAS}}$ Latency = 2

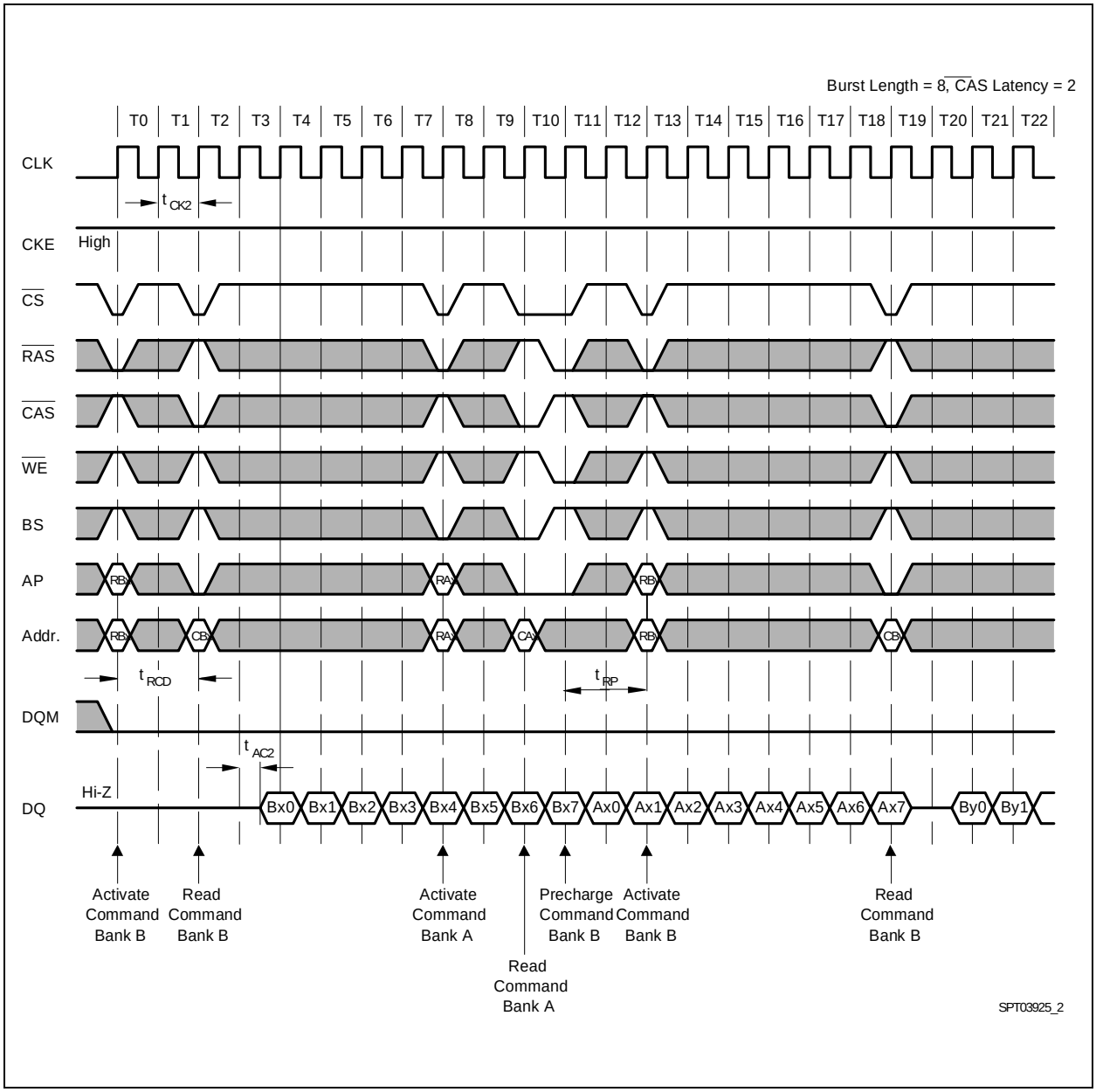


16.2. $\overline{\text{CAS}}$ Latency = 3

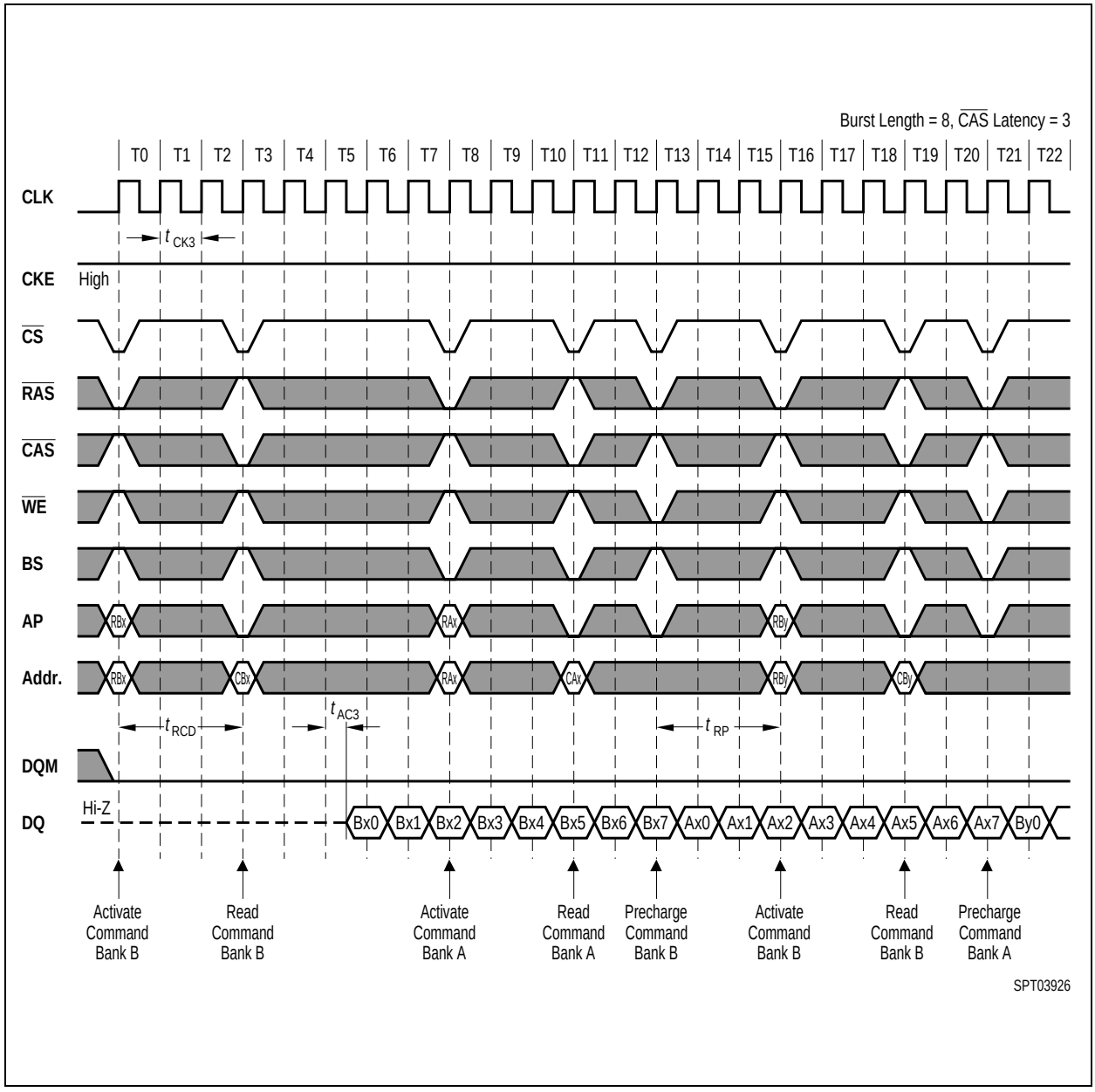


17. Random Row Read (Interleaving Banks) with Precharge

17.1 $\overline{\text{CAS}}$ Latency = 2

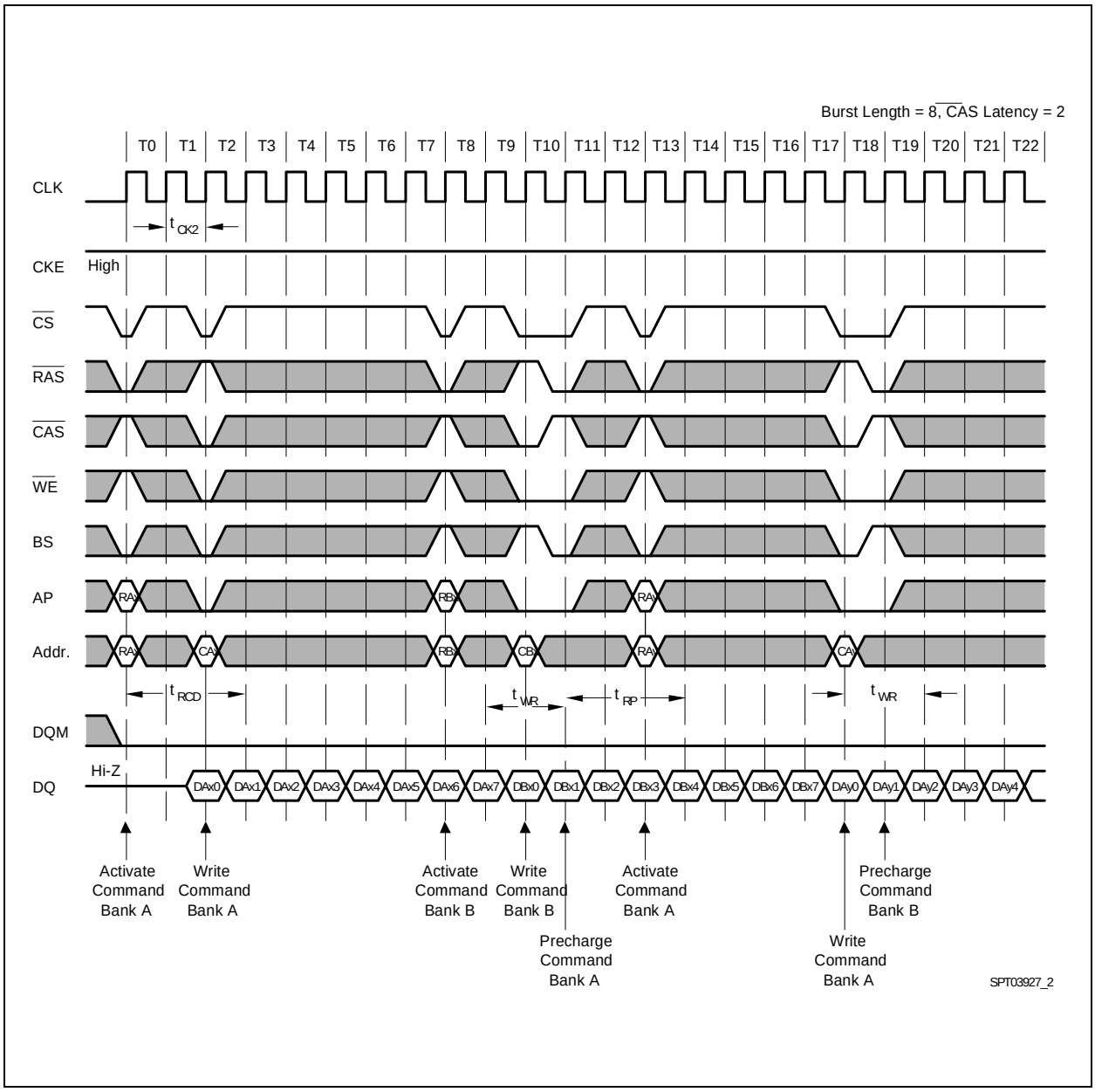


17.2 $\overline{\text{CAS}}$ Latency = 3

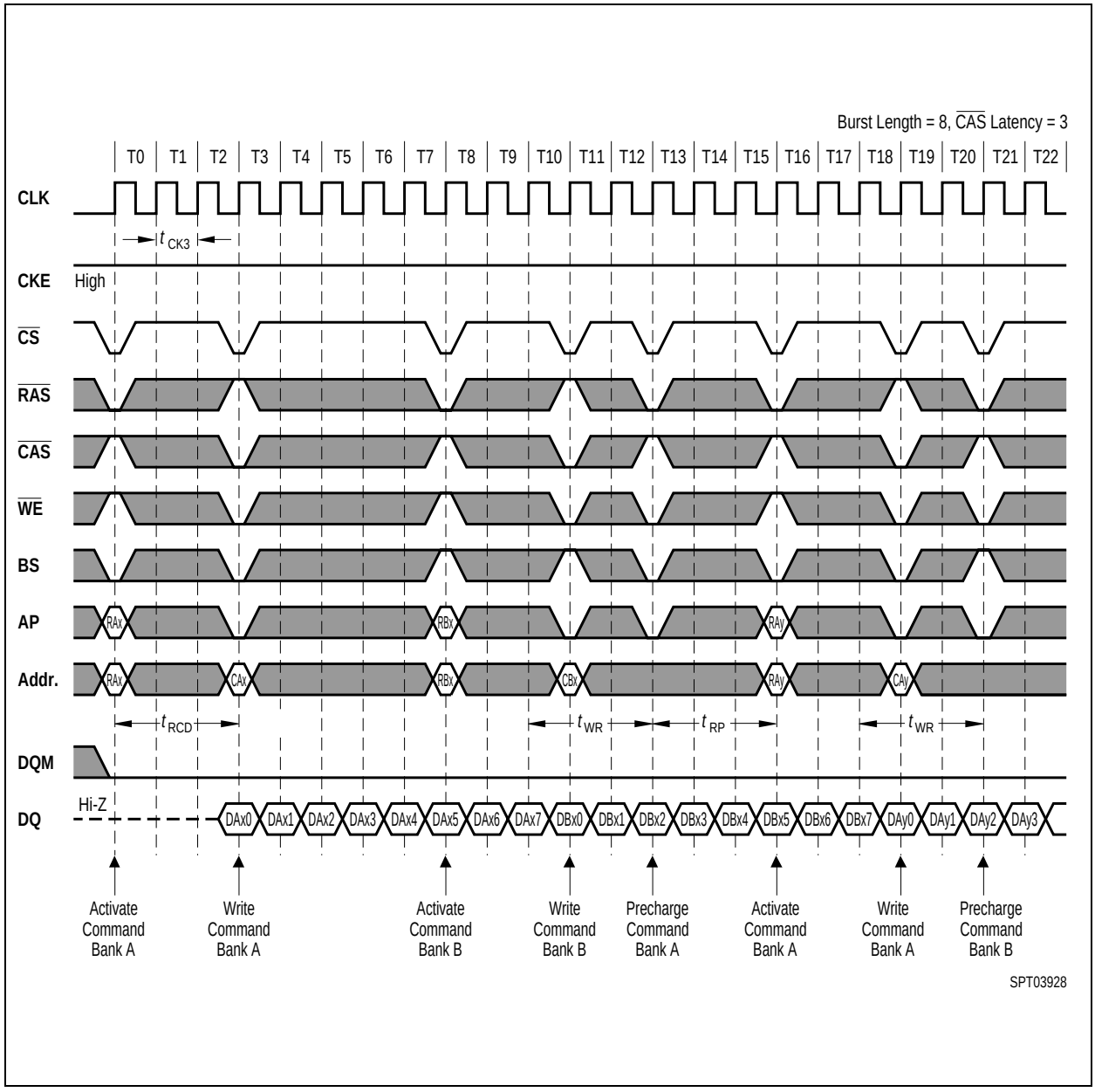


18. Random Row Write (Interleaving Banks) with Precharge

18.1 $\overline{\text{CAS}}$ Latency = 2

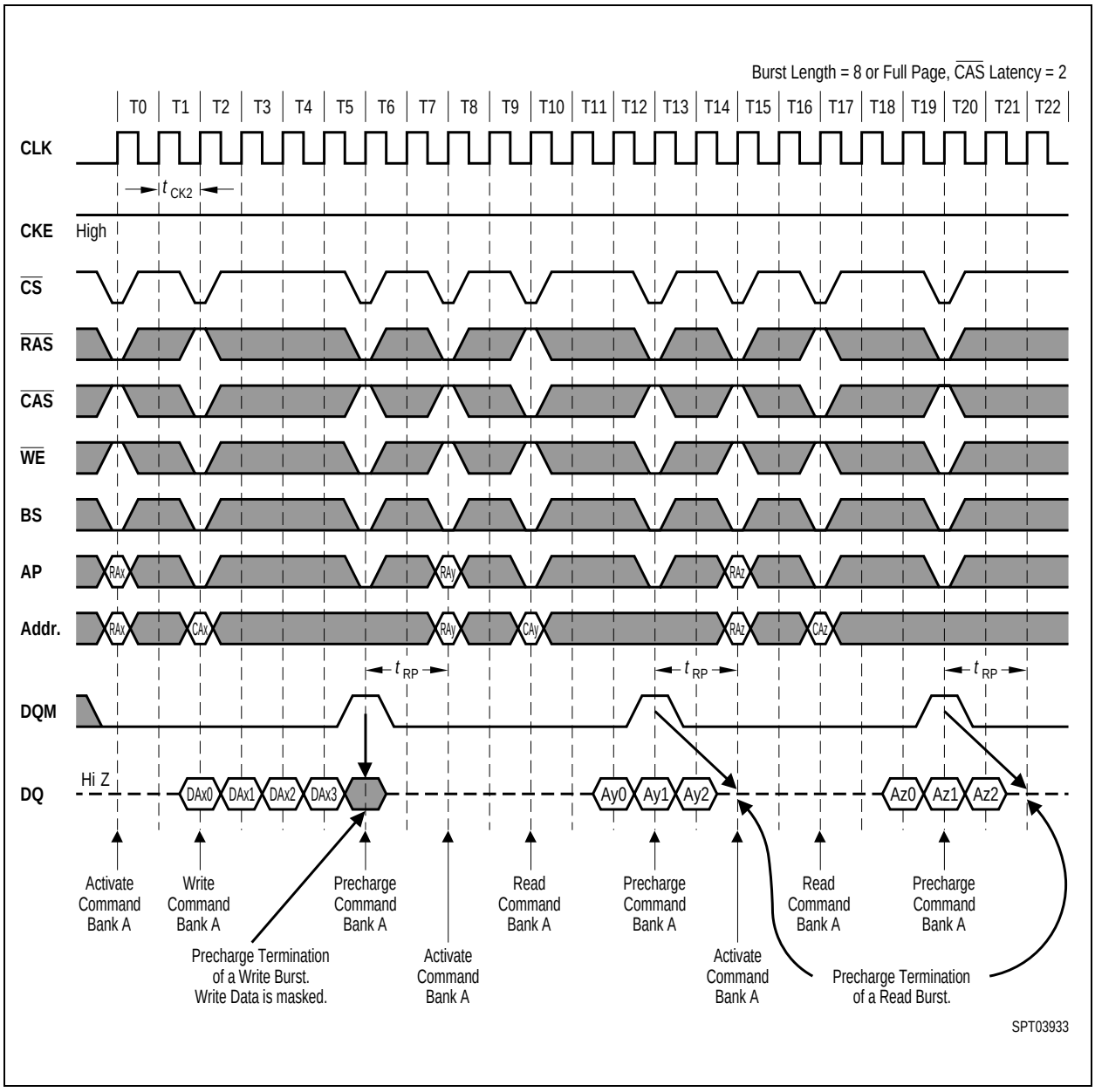


18.2 $\overline{\text{CAS}}$ Latency = 3



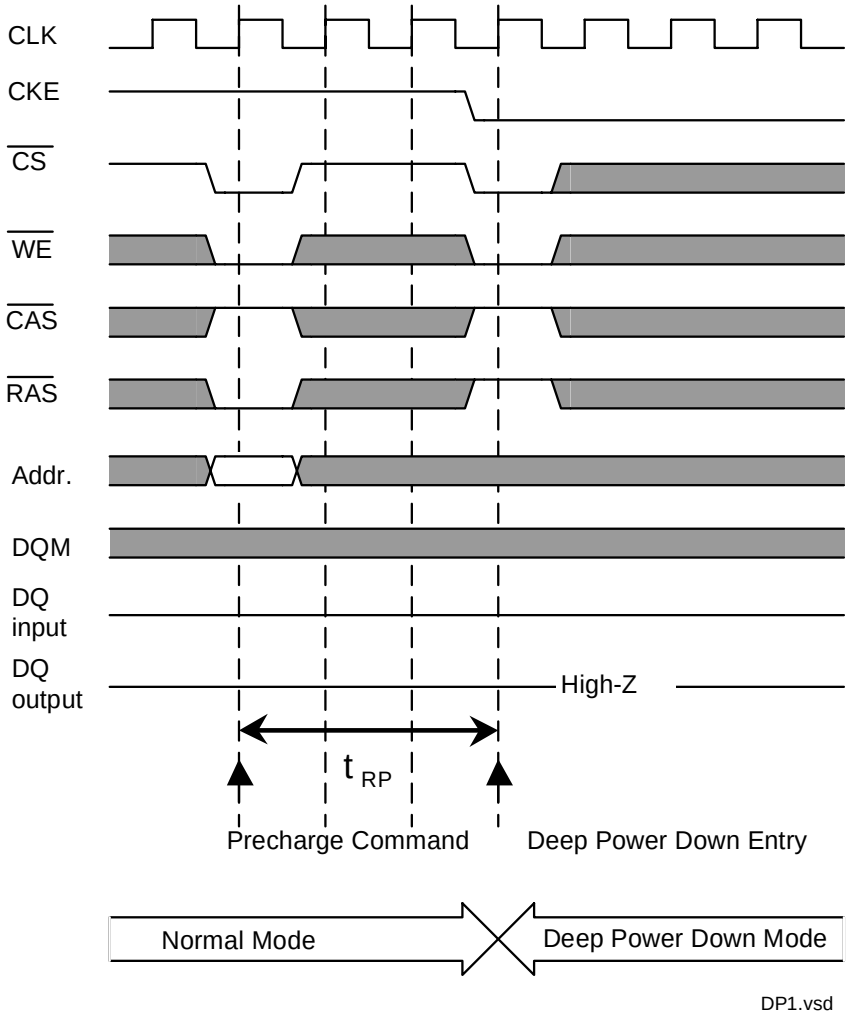
19. Precharge termination of a Burst

19.1 $\overline{\text{CAS}}$ Latency = 2



20. Deep Power Down Mode

20.1 Deep Power Down Mode Entry



20. Deep Power Down Mode

20.2 Deep Power Down Exit

The deep power down mode is exited by asserting CKE high. After the exit, the following sequence is needed to enter a new command:

1. Maintain NOP input conditions for a minimum of 200 µs
2. Issue precharge commands for all banks of the device
3. Issue eight or more autorefresh commands
4. Issue a mode register set command to initialize the mode register
5. Issue an extended mode register set command to initialize the extende mode register