DESCRIPTION

The Hynix HYM4V33100DTYG Series are 1Mx16bits Synchronous DRAM Modules. The modules are composed of two 1Mx16bits CMOS Synchronous DRAMs in 400mil 50pin TSOP-II package, on a 132pin glass-epoxy printed circuit board. Two 0.22uF and one 0.1uF decoupling capacitors per each SDRAM are mounted on the PCB.

The Hyundai HYM4V33100DTYG Series are AGP In-line Memory Modules suitable for easy interchange and addition of 4Mbytes memory. The Hyundai HYM4V33100DTYG Series are fully synchronous operation referenced to the positive edge of the clock . All inputs and outputs are synchronized with the rising edge of the clock input. The data paths are internally pipelined to achieve very high bandwidth.

FEATURES

- PC133/PC100MHz support
- 132pin SDRAM AIMM
- 1.4" (35.56mm) Height PCB with double sided components
- Single 3.3±0.3V power supply
- All device pins are compatible with LVTTL interface
- Data mask function by DQM
- SDRAM internal banks : two banks
- Module bank : one physical bank
- Auto refresh and self refresh
- 4096 refresh cycles / 64ms
- Programmable Burst Length and Burst Type
  - 1, 2, 4 or 8 or Full page for Sequential Burst
  - 1, 2, 4 or 8 for Interleave Burst
- Programmable $\overline{CAS}$ Latency ; 2, 3 Clocks

ORDERING INFORMATION

Part No.	Clock Frequency	Internal Bank	Ref.	Power	SDRAM Package	Plating
HYM4V33100DTYG-75	133MHz	4 Banks	4K	Normal	TSOP-II	Gold

PIN DESCRIPTION

PIN	PIN NAME	DESCRIPTION
CK0, CK1	Clock Inputs	The system clock input. All other inputs are registered to the SDRAM on the rising edge of CLK
CKE	Clock Enable	Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh
/CS	Chip Select	Enables or disables all inputs except CK, CKE and DQM
BA	SDRAM Bank Address	Selects bank to be activated during /RAS activity Selects bank to be read/written during /CAS activity
A0 ~ A10	Address	Row Address : RA0 ~ RA10, Column Address : CA0 ~ CA7 Auto-precharge flag : A10
/RAS, /CAS, /WE	Row Address Strobe, Column Address Strobe, Write Enable	/RAS, /CAS and /WE define the operation Refer function truth table for details
DQM0~DQM3	Data Input/Output Mask	Controls output buffers in read mode and masks input data in write mode
DQ0 ~ DQ31	Data Input/Output	Multiplexed data input / output pin
VCC	Power Supply (3.3V)	Power supply for internal circuits and input buffers
VSS	Ground	Ground
NC	No Connection	No connection

PIN ASSIGNMENTS

FRONT SIDE		BACK SIDE		FRONT SIDE		BACK SIDE	
PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME
1	NC	2	TYPEDET	67	NC	68	NC
3	NC	4	NC	69	NC	70	NC
5	GND	6	NC	71	GND	72	NC
7	NC	8	NC	73	NC	74	DQ27
9	VCC	10	DQM3	75	VCC	76	DQ28
11	NC	12	DQ24	77	DQ29	78	DQ30
13	GND	14	NC	79	GND	80	NC
15	DQ25	16	VCC	81	DQ31	82	VCC
17	DQ26	18	NC	83	DQM2	84	NC
19	GND	20	WE	85	GND	86	DQ23
21	FSEL	22	KEYWAY	87	DQ22	88	KEYWAY
23	KEYWAY	24	KEYWAY	89	KEYWAY	90	KEYWAY
25	KEYWAY	26	TCLK0	91	KEYWAY	92	DQ21
27	TCLK1	28	VCC	93	DQ20	94	VCC
29	CAS	30	NC	95	DQ19	96	DQ18
31	GND	32	NC	97	GND	98	NC
33	RAS	34	VDDQ	99	DQ17	100	VDDQ
35	A0	36	A9	101	DQ16	102	DQ15
37	GND	38	A11	103	GND	104	DQ14
39	A8	40	VDDQ	105	DQ13	106	VDDQ
41	A10	42	NC	107	DQ12	108	NC
43	GND	44	NC	109	GND	110	NC
45	VCC	46	A7	111	VCC	112	DQ11
47	CS	48	NC	113	VDDQ	114	NC
49	GND	50	A6	115	GND	116	NC
51	A1	52	VDDQ	117	DQ10	118	VDDQ
53	A5	54	A2	119	DQ9	120	DQ8
55	GND	56	A4	121	GND	122	DQM1
57	A3	58	VDDQ	123	DQ0	124	VDDQ
59	NC	60	DQ5	125	NC	126	DQ1
61	GND	62	DQ6	127	GND	128	DQ2
63	DQ7	64	VDDQ	129	DQ3	130	VDDQ
65	DQM0	66	NC	131	DQ4	132	NC

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Ambient Temperature	TA	0 ~ 70	°C
Storage Temperature	TSTG	-55 ~ 125	°C
Voltage on Any Pin relative to VSS	VIN, VOUT	-1.0 ~ 4.6	V
Voltage on VDD relative to VSS	VDD, VDDQ	-1.0 ~ 4.6	V
Short Circuit Output Current	IOS	50	mA
Power Dissipation	PD	1	W
Soldering Temperature · Time	TSOLDER	260 · 10	°C · Sec

Note : Operation at above absolute maximum rating can adversely affect device reliability.

DC OPERATING CONDITION (TA=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	VDD, VDDQ	3.0	3.3	3.6	V	1
Input High voltage	VIH	2.0	3.0	VDDQ + 0.3	V	1,2
Input Low voltage	VIL	-0.3	0	0.8	V	1,3

Note :
1.All voltages are referenced to VSS = 0V
2.VIH(max) is acceptable 5.6V AC pulse width with <=3ns of duration.
3.VIL(min) is acceptable -2.0V AC pulse width with <=3ns of duration.

AC OPERATING TEST CONDITION (TA=0 to 70°C, VDD=3.3±0.3V, VSS=0V)

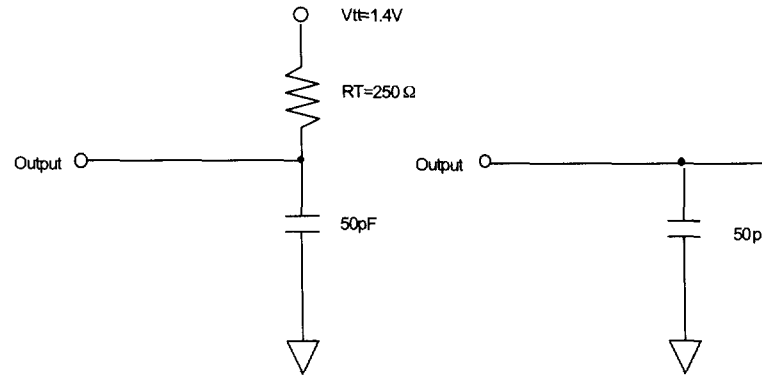
Parameter	Symbol	Value	Unit	Note
AC Input High / Low Level Voltage	VIH / VIL	2.4/0.4	V	
Input Timing Measurement Reference Level Voltage	Vtrip	1.4	V	
Input Rise / Fall Time	tR / tF	1	ns	
Output Timing Measurement Reference Level Voltage	Voutref	1.4	V	
Output Load Capacitance for Access Time Measurement	CL	50	pF	1

Note :
1.Output load to measure access times is equivalent to two TTL gates and one capacitor (50pF). For details, refer to AC/DC output load circuit

CAPACITANCE (TA=25°C, f=1MHz)

Parameter	Pin	Symbol	-75		Unit
			Min	Max	
Input Capacitance	CK0, CK1	CI1	5	10	pF
	CKE0, CKE1	CI2	5	10	pF
	/S0, /S1	CI3	10	15	pF
	A0~10, BA0	CI4	10	20	pF
	/RAS, /CAS, /WE	CI5	10	20	pF
	DQM0~DQM3	CI6	5	10	pF
Data Input / Output Capacitance	DQ0 ~ DQ31	CI/O	5	15	pF

OUTPUT LOAD CIRCUIT



DC Output Load Circuit

AC Output Load Circuit

DC CHARACTERISTICS I (TA=0 to 70°C, VDD=3.3±0.3V)

Parameter	Symbol	Min.	Max	Unit	Note
Input Leakage Current	ILI	-8	8	uA	1
Output Leakage Current	ILO	-1	1	uA	2
Output High Voltage	VOH	2.4	-	V	IOH = -4mA
Output Low Voltage	VOL	-	0.4	V	IOL = +4mA

Note :
1.VIN = 0 to 3.6V, All other pins are not tested under V IN =0V
2.DOUT is disabled, VOUT=0 to 3.6

DC CHARACTERISTICS II

Parameter	Symbol	Test Condition		Speed -75	Unit	Note
Operating Current	IDD1	Burst length=1, One bank active tRC ≥ tRC(min), IOL=0mA		220	mA	1
Precharge Standby Current in Power Down Mode	IDD2P	CKE ≤ VIL(max), tCK = min		2	mA	
	IDD2PS	CKE ≤ VIL(max), tCK = ∞		2		
Precharge Standby Current in Non Power Down Mode	IDD2N	CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tCK = min Input signals are changed one time during 2clks. All other pins ≥ VDD-0.2V or ≤ 0.2V		40	mA	
	IDD2NS	CKE ≥ VIH(min), tCK = ∞ Input signals are stable.		30		
Active Standby Current in Power Down Mode	IDD3P	CKE ≤ VIL(max), tCK = min		60	mA	
	IDD3PS	CKE ≤ VIL(max), tCK = ∞		60		
Active Standby Current in Non Power Down Mode	IDD3N	CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tCK = min Input signals are changed one time during 2clks. All other pins ≥ VDD-0.2V or ≤ 0.2V		100	mA	
	IDD3NS	CKE ≥ VIH(min), tCK = ∞ Input signals are stable.		60		
Burst Mode Operating Current	IDD4	tCK ≥ tCK(min), IOL=0mA All banks active	CL=3	220	mA	1
Auto Refresh Current	IDD5	tRRC ≥ tRRC(min), All banks active		220	mA	2
Self Refresh Current	IDD6	CKE ≤ 0.2V		4	mA	3

Note :
1. IDD1 and IDD4 depend on output loading and cycle rates. Specified values are measured with the output open
2. Min. of tRRC (Refresh RAS cycle time) is shown at AC CHARACTERISTICS II
3.HYM4v33100DTYG-75

AC CHARACTERISTICS I (AC operating conditions unless otherwise noted)

Parameter		Symbol	-75		Unit	Note
			Min	Max		
System Clock Cycle Time	$\overline{CAS}$ Latency = 3	tCK3	7.5	1000	ns	
	$\overline{CAS}$ Latency = 2	tCK2	10		ns	
Clock High Pulse Width		tCHW	2.5	-	ns	1
Clock Low Pulse Width		tCLW	2.5	-	ns	1
Access Time From Clock	$\overline{CAS}$ Latency = 3	tAC3	-	5.4	ns	2
	$\overline{CAS}$ Latency = 2	tAC2	-	6	ns	
Data-Out Hold Time		tOH	2.7	-	ns	
Data-Input Setup Time		tDS	1.5	-	ns	1
Data-Input Hold Time		tDH	0.8	-	ns	1
Address Setup Time		tAS	1.5	-	ns	1
Address Hold Time		tAH	0.8	-	ns	1
CKE Setup Time		tCKS	1.5	-	ns	1
CKE Hold Time		tCKH	0.8	-	ns	1
Command Setup Time		tCS	1.5	-	ns	1
Command Hold Time		tCH	0.8	-	ns	1
CLK to Data Output in Low-Z Time		tOLZ	1	-	ns	
CLK to Data Output in High-Z Time	$\overline{CAS}$ Latency = 3	tOHZ3	2.7	5.4	ns	
	$\overline{CAS}$ Latency = 2	tOHZ2	3	6	ns	

Note :

1.Assume tR / tF (input rise and fall time) is 1ns
If tR & tF > 1ns, then [(tR+tF)/2-1]ns should be added to the parameter

2.Access times to be measured with input signals of 1v/ns edge rate, from 0.8v to 2.0v
If tR > 1ns, then (tR/2-0.5)ns should be added to the parameter

AC CHARACTERISTICS II

Parameter		Symbol	-75		Unit	Note
			Min	Max		
$\overline{RAS}$ Cycle Time	Operation	tRC	65	-	ns	
	Auto Refresh	tRRC	65	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay		tRCD	20	-	ns	
$\overline{RAS}$ Active Time		tRAS	45	100K	ns	
$\overline{RAS}$ Precharge Time		tRP	20	-	ns	
$\overline{RAS}$ to $\overline{RAS}$ Bank Active Delay		tRRD	15	-	ns	
$\overline{CAS}$ to $\overline{CAS}$ Delay		tCCD	1	-	CLK	
Write Command to Data-In Delay		tWTL	0	-	CLK	
Data-In to Precharge Command		tDPL	2	-	CLK	
Data-In to Active Command		tDAL	5	-	CLK	
DQM to Data-Out Hi-Z		tDQZ	2	-	CLK	
DQM to Data-In Mask		tDQM	0	-	CLK	
MRS to New Command		tMRD	2	-	CLK	
Precharge to Data Output Hi-Z	$\overline{CAS}$ Latency = 3	tPROZ3	3	-	CLK	
	$\overline{CAS}$ Latency = 2	tPROZ2	2	-	CLK	
Power Down Exit Time		tPDE	1	-	CLK	
Self Refresh Exit Time		tSRE	1	-	CLK	1
Refresh Time		tREF	-	64	ms	

Note :

1. A new command can be given tRRC after self refresh exit

DEVICE OPERATING OPTION TABLE

HYM4V33100DTYG-75

	$\overline{CAS}$ Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
133MHz(7.5ns)	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	5.4ns	2.7ns

COMMAND TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	ADDR	A10/ AP	BA	Note
Mode Register Set		H	X	L	L	L	L	X	OP code			
No Operation		H	X	H	X	X	X	X	X			
				L	H	H	H					
Bank Active		H	X	L	L	H	H	X	RA		V	
Read		H	X	L	H	L	H	X	CA	L	V	
Read with Autoprecharge										H		
Write		H	X	L	H	L	L	X	CA	L	V	
Write with Autoprecharge										H		
Precharge All Banks		H	X	L	L	H	L	X	X	H	X	
Precharge selected Bank										L	V	
Burst Stop		H	X	L	H	H	L	X	X			
DQM		H	X					V	X			
Auto Refresh		H	H	L	L	L	H	X	X			
Self Refresh[1]	Entry	H	L	L	L	L	H	X	X			
	Exit	L	H	H	X	X	X	X				
				L	H	H	H					
Precharge power down	Entry	H	L	H	X	X	X	X	X			
				L	H	H	H					
	Exit	L	H	H	X	X	X	X				
				L	H	H	H					
Clock Suspend	Entry	H	L	H	X	X	X	X	X			
				L	V	V	V					
	Exit	L	H	X				X				

Note :

1. Exiting Self Refresh occurs by asynchronously bringing CKE from low to high
2. X = Don't care, H = Logic High, L = Logic Low. BA =Bank Address, RA = Row Address, CA = Column Address, Opcode = Operand Code, NOP = No Operation

PACKAGE DEMENSION