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128K x 32 SRAM MODULE

SYS32128ZK/LK - 010/012/015/017

Issue 1.3 : January 1999

Description

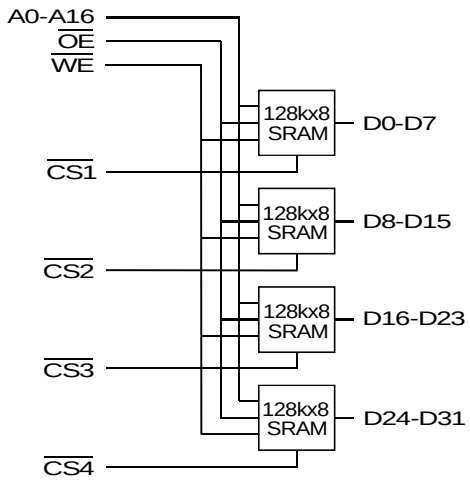
The SYS32128ZK/LK is a plastic 4Mbit Static RAM Module offered in 64 pin ZIP and 64 lead SIMM packages, organised as 128K x 32. The module utilises four fast 128kx8 SRAMs housed in SOJ packages, surface mounted onto an FR4 epoxy PCB.

Four chip selects are used to independently enable the four bytes. Reading or Writing is executed on individual or any combination of multiple bytes. Two pins PD0 & PD1 are used to identify module memory density where alternative versions of the JEDEC standard modules can be interchanged.

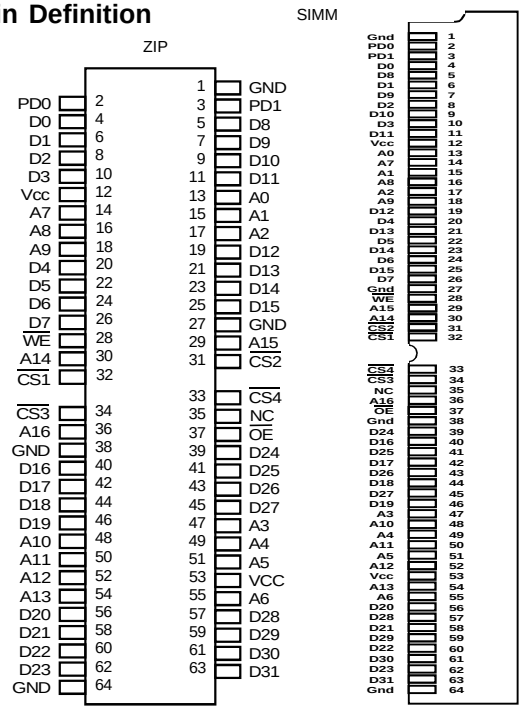
Features

- Access Times of 10/12/15/17 ns.
- 64 Pin ZIP & SIMM standard pinouts.
- 5 Volt Supply ± 10%.
- Power Dissipation :
  Operating (10ns) 5.5 W (maximum).
  Standby (CMOS) -L 44mW (maximum).
- Completely Static Operation.
- Equal Access and Cycle Times.
- On-board Supply Decoupling Capacitors.
- Data Retention capability. (-L version only).

Block Diagram



Pin Definition



Pin Functions

Address Inputs	**A0 - A16**
Data Input/Output	**D0 - D31**
Chip Selects	**$\overline{CS1}$~$\overline{4}$**
Write Enable	**$\overline{WE}$**
Output Enable	**$\overline{OE}$**
No Connect	**NC**
Presence Detect	**PD0~1**
Power (+5V)	**V_{cc}**
Ground	**GND**

Package Details

Plastic 64 Pin JEDEC ZIP

Plastic 64 Pin JEDEC SIMM

DC OPERATING CONDITIONS

Absolute Maximum Ratings (1)

Parameter	*Symbol*	*min*	*typ*	*max*	*unit*
Voltage on any pin relative to V_{SS}	V_T	-0.5	-	+7.0	V
Power Dissipation	P_T	-	-	4.0	W
Storage Temperature	T_{STG}	-55	-	+125	°C

Notes :

(1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	*Symbol*	*min*	*typ*	*max*	*unit*
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	-	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	-0.5(2)	-	0.8	V
Operating Temperature	T_A	0	-	70	°C
	T_{AI}	-40	-	85	°C (I)

(2) V_T can be -1.5 V pulse of less than 10 ns.

DC Electrical Characteristics (V_{CC}=5V±10%) T_A 0 to 70°C

Parameter	*Symbol*	*Test Condition*		*min*	*typ*	*max*	*Unit*
I/P Leakage Current	I_{LI}	V_{IN} = GND to V_{CC}		-20	-	20	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = GND to V_{CC}		-20	-	20	µA
Operating Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, min cycle,	10ns	-	-	1000	mA
			12ns	-	-	920	mA
		100% duty, $I_{I/O}$=0mA ,	15ns	-	-	780	mA
			17ns	-	-	720	mA
Standby Supply Current TTL levels	I_{SB1}	$\overline{CS}$ = V_{IH}		-	-	280	mA
-L (CMOS levels)	I_{SB}	$\overline{CS}$ = V_{CC}-0.2V, 0.2 > V_{IN} > V_{CC}-0.2V		-	-	80	mA
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA	-	-	0.4	V	
Output High Voltage	V_{OH}	I_{OH} = -4.0mA	2.4	-	-	V	

Typical values are at V_{CC}=5.0V,T_A=25°C and specified loading. All values specified for 32 bit operation.
$\overline{CS}$ above refers to $\overline{CS1~4}$ on the module.

Capacitance (V_{CC}=5V±10%,T_A=25°C) Note: Capacitance calculated, not measured.

Parameter	*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance ($\overline{CS1~4}$)	C_{IN1}	V_{IN} = 0V	-	8	pF
Input Capacitance (other)	C_{IN2}	V_{IN} = 0V	-	32	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	-	8	pF

Operation Truth Table

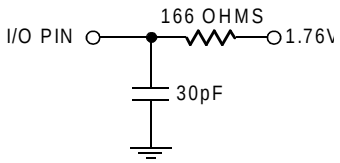
$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	DATA PINS	SUPPLY CURRENT	MODE
H	X	X	High Impedance	I_{SB1} , I_{SB2}	Standby
L	L	H	Data Out	I_{CC}	Read
L	X	L	Data In	I_{CC}	Write
L	H	H	High Impedance	I_{CC}	Output Disabled

Notes : H = V_{IH} : L =V_{IL} : X = V_{IH} or V_{IL}

AC Test Conditions

* Input pulse levels: 0 V to 3.0V
* Input rise and fall times: 5ns
* Input and Output timing reference levels: 1.5V
* Output load: see diagram
* V_{CC} = 5V± 10%

Output Load



Low V_{CC} Data Retention Characteristics - L Version Only

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}$-0.2V	2.0	-	-	V
Data Retention Current	I_{CCDR1}	V_{CC}=2.0V,$\overline{CS} \geq$1.8V,$T_{OP}=T_A$	-	-	3	mA
	I_{CCDR2}	V_{CC}=3.0V,$\overline{CS} \geq$2.8V,$T_{OP}=T_{AI}$	-	-	3.5	mA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	t_{RC} (1)	-	-	ns

Notes: (1) t_{RC}=Read Cycle Time

AC OPERATING CONDITIONS

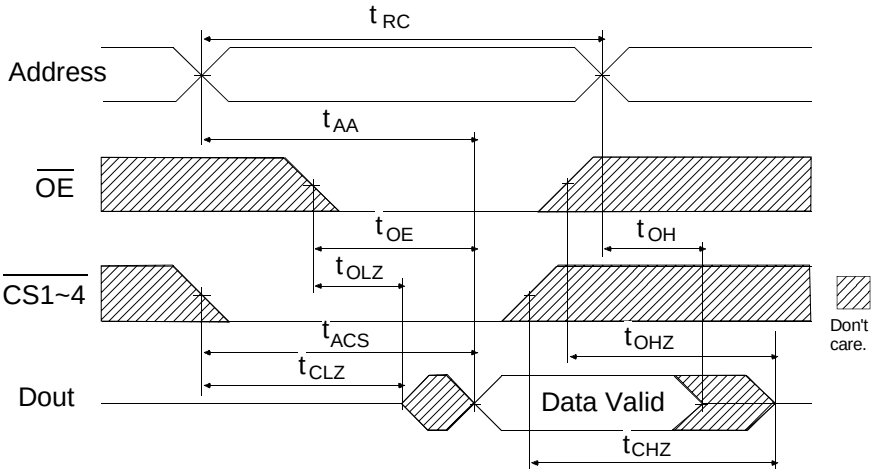
Read Cycle (1)

		-010		-012		-015		-017		
Parameter	Symbol	min	max	min	max	min	max	min	max	Unit
Read Cycle Time	t_{RC}	10	-	12	-	15	-	17	-	ns
Address Access Time	t_{AA}	-	10	-	12	-	15	-	17	ns
Chip Select Access Time	t_{ACS}	-	10	-	12	-	15	-	17	ns
Output Enable to Output Valid	t_{OE}	-	6	-	6	-	8	-	9	ns
Output Hold from Address Change	t_{OH}	2	-	3	-	3	-	3	-	ns
Chip Selection to Output in Low Z	t_{CLZ}	0	-	0	-	0	-	0	-	ns
Output Enable to Output in Low Z	t_{OLZ}	0	-	0	-	0	-	0	-	ns
Chip Deselection to O/P in High Z (2)	t_{CHZ}	0	6	0	6	0	7	0	8	ns
Output Disable to Output in High Z (2)	t_{OHZ}	0	6	0	6	0	6	0	7	ns

Write Cycle

		-010		*-12*		*-15*		*-17*		
Parameter	Symbol	min	max	min	max	min	max	min	max	Unit
Write Cycle Time	t_{WC}	10	-	12	-	15	-	17	-	ns
Chip Selection to End of Write	t_{CW}	9	-	10	-	12	-	13	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	0	-	ns
Address Valid to End of Write	t_{AW}	9	-	10	-	12	-	13	-	ns
Write Pulse Width	t_{WP}	7	-	9	-	12	-	13	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	0	-	ns
Write to Output in High Z (3)	t_{WHZ}	0	6	0	7	0	8	0	9	ns
Data to Write Time Overlap	t_{DW}	6	-	7	-	8	-	9	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	0	-	ns
Output active from end of write	t_{OW}	0	-	0	-	0	-	0	-	ns

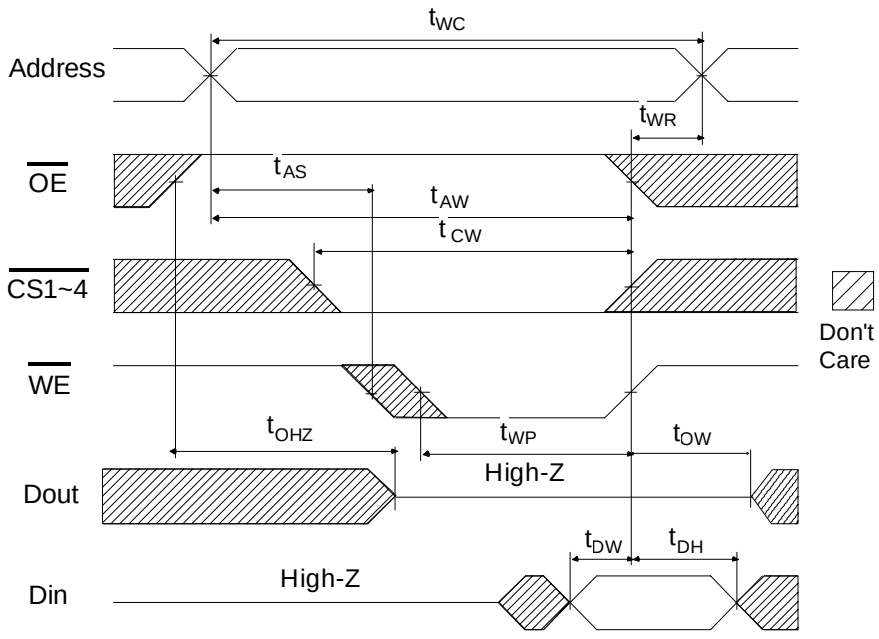
Read Cycle Timing Waveform (1,2)



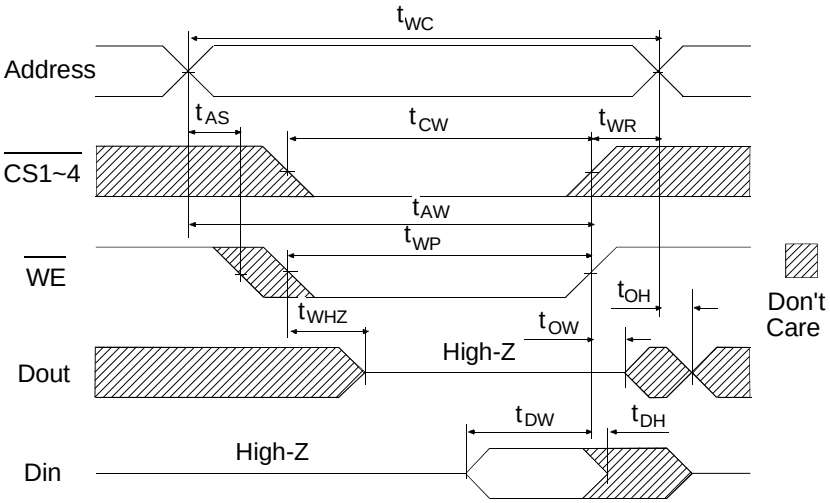
(1) $\overline{WE}$ is High for Read Cycle.

(2) t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.

Write Cycle No.1 Timing Waveform (1-10)



Write Cycle No.2 Timing Waveform (1-10)



AC Characteristics Notes

(1) A write occurs during the overlap (t_{WP}) of a low $\overline{CS1\sim4}$ and a low $\overline{WE}$.

(2) All write cycle timing is referenced from the last valid address to the first transition address.

(3) Defined as the time at which the outputs achieve open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.

(4) At any given temperature and voltage condition, t_{WHZ} (max) is less than t_{OW} (min) both for a given module and from module to module.

(5) Module is continuously selected with $\overline{CS1\sim4}$ = V_{IL}.

(6) $\overline{CS1\sim4}$ or $\overline{WE}$ must be high during address transition.

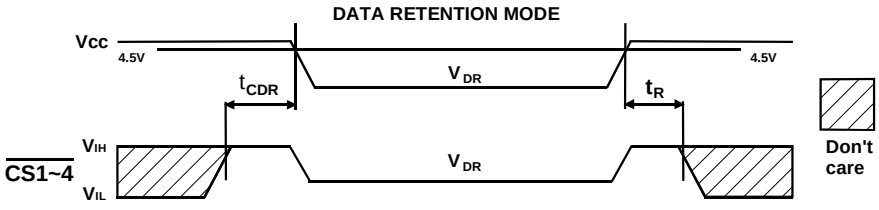
(7) $\overline{WE}$ is High for Read Cycle.

(8) All read cycle timing is referenced from the last valid address to the first transition address.

(9) At any given temperature and voltage condition, t_{CHZ} (max) is less than t_{CLZ} (min) both for a given module
and from module to module.

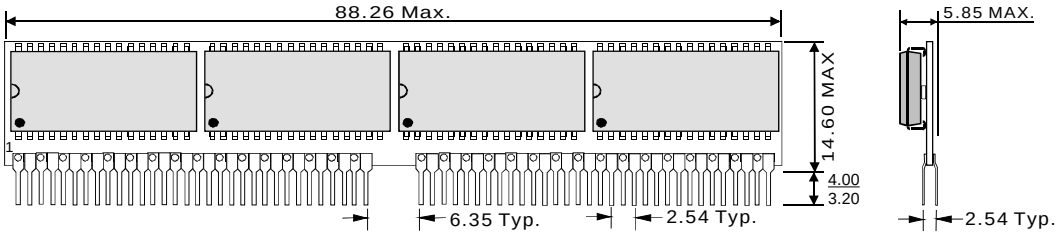
(10) Address is valid prior to or coincident with $\overline{CS1\sim4}$ transition low.

Data Retention Waveform

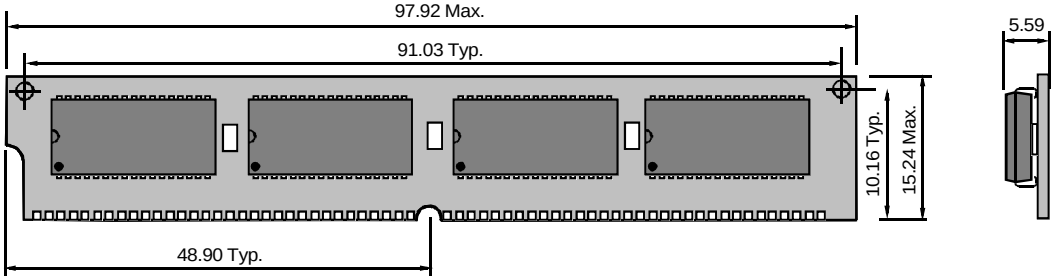


Package Information Dimensions in mm

Plastic 64 Pin Zig-Zag-In-line Package (ZIP)



Plastic 64 Pin Single In-line Memory Module (SIMM)



Ordering Information

SYS32128 ZK/LK LI-010

Speed	010	= 10ns
	012	= 12 ns
	015	= 15 ns
	017	= 17 ns
Temperature range	Blank	= Commercial Temp.
	I	= Industrial Temp.
Power Consumption	Blank	= Standard Part
	L	= Low Power Part
Package	ZK	= Plastic 64 Pin ZIP
	LK	= Plastic 64 Pin SIMM
Organisation	32128	= 128K X 32
Memory Type	SYS	= Static RAM

Note :

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Our products are subject to a constant process of development. Data may be changed at any time without notice.

Products are not authorised for use as critical components in life support devices without the express written approval of a company director.