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256K x 32 SRAM MODULE

SYS32256ZK/LK - 020/25/30/35

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Description

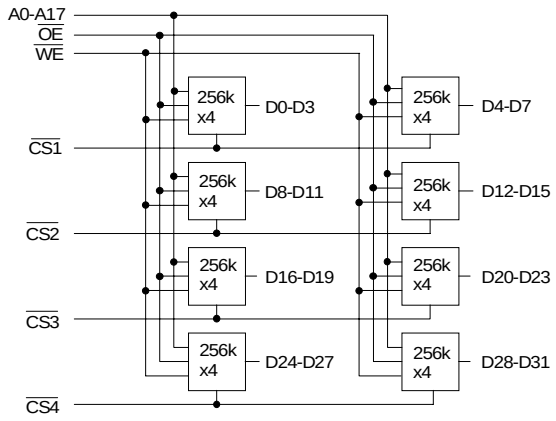
The SYS32256 is a plastic 8M Static RAM Module offered in 64 pin ZIP and 64 lead SIMM package, organised as 256K x 32. The module utilises eight very fast SRAMs housed in SOJ packages, and uses double sided surface mount techniques, to achieve a very high density module.

Four chip selects are used to independently enable the four bytes. Reading or Writing is executed on individual or any combination of multiple bytes. Two pins PD0 & PD1 are used to identify module memory density where alternative versions of the JEDEC standard modules can be interchanged.

Features

- Access Times of 020/25/30/35 ns.
- 64 Pin ZIP & SIMM JEDEC standard pinouts.
- 5 Volt Supply ± 10%.
- Power Dissipation 35ns:
  Operating (32bit mode) 6.60 W (maximum).
  Standby (CMOS) -L 4.40 mW (maximum).
- Completely Static Operation.
- Equal Access and Cycle Times.
- All Inputs and Outputs Directly TTL Compatible.
- On-board Supply Decoupling Capacitors.

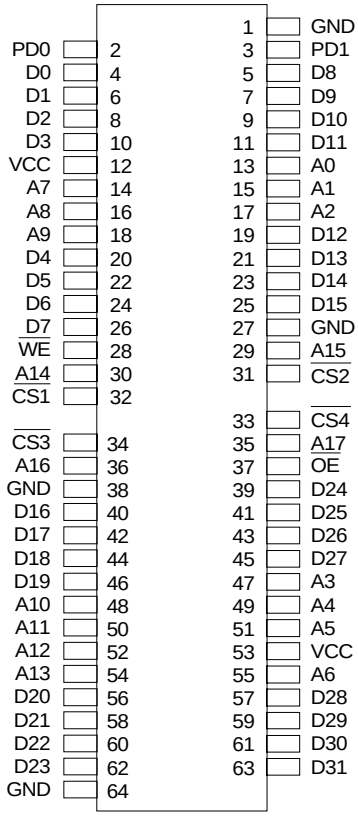
Block Diagram



Pin Functions

Address Inputs	**A0 - A17**
Data Input/Output	**D0 - D31**
Chip Select Input	**$\overline{CS1}$- $\overline{CS4}$**
Read/Write Input	**$\overline{WE}$**
Output Enable Input	**$\overline{OE}$**
Power (+5V)	**V_{cc}**
Ground	**GND**

Pin Definition



DC OPERATING CONDITIONS

Absolute Maximum Ratings (1)

Parameter	*Symbol*	*min*	*typ*	*max*	*unit*
Voltage on any pin relative to V_{SS}	V_T	-0.5V	-	+7.0	V
Power Dissipation	P_T	-	4.0	-	mW
Storage Temperature	T_{STG}	-55	-	+125	°C

Notes :

(1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	*Symbol*	*min*	*typ*	*max*	*unit*	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input High Voltage	V_{IH}	2.2	-	6.0	V	
Input Low Voltage	V_{IL}	-0.3	-	0.8	V	
Operating Temperature	T_A	0	-	70	°C	
	T_{AI}	-40	-	85	°C	(I)

DC Electrical Characteristics (V_{CC}=5V±10%) T_A 0 to 70°C

Parameter	Symbol	Test Condition	min	typ	max	Unit
I/P Leakage Current	I_{LI}	V_{IN} = GND to V_{CC}, V_{cc}=max.	-	-	±16	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = GND to V_{CC}	-	-	±16	µA
Average Supply Current (20/25/30)	I_{CC1}	t_{CYC} = 20ns, $\overline{CS}$ = V_{IL}, V_{IN} = V_{IL}/V_{CC}-2.1V	-	-	1440	mA
Average Supply Current (35/45/55)	I_{CC2}	t_{CYC} = 35ns, $\overline{CS}$= V_{IL}, V_{IN} =V_{IL}/V_{CC}-2.1V	-	-	1200	mA
Standby Supply Current TTL levels	I_{SB1}	$\overline{CS}$ = V_{CC}-2.1V, V_{IL} > V_{IN} > V_{CC}-2.1V	-	-	320	mA
CMOS levels	I_{SB2}	$\overline{CS}$ = V_{CC}-0.2V, 0.2 > V_{IN} > V_{CC}-0.2V	-	3.20	16	mA
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA	-	-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA	2.4	-	-	V

Typical values are at V_{CC}=5.0V,T_A=25°C and specified loading.

All values specified for 32 bit operation. I_{SB2} = 0.8mA max. for low power option.

Capacitance (V_{CC}=5V±10%,T_A=25°C) Note: Capacitance calculated, not measured.

Parameter	*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance ($\overline{CS}$)	C_{IN1}	V_{IN} = 0V	-	12	pF
Input Capacitance (other)	C_{IN2}	V_{IN} = 0V	-	48	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	-	8	pF

Operation Truth Table

$\overline{CS}$n	***$\overline{OE}$***	***$\overline{WE}$***	***DATA PINS***	***SUPPLY CURRENT***	***MODE***
H	X	X	High Impedance	I_{SB1} , I_{SB2}	Standby
L	L	H	Data Out	I_{CC1} , I_{CC2}	Read
L	X	L	Data In	I_{CC1} , I_{CC2}	Write (1)
L	L	L	Data In	I_{CC1} , I_{CC2}	Write (2)

Notes : H = V_{IH} : L =V_{IL} : X = V_{IH} or V_{IL}

Low V_{cc} Data Retention Characteristics - L Version Only (T_{OP} = 0°C to 70°C)

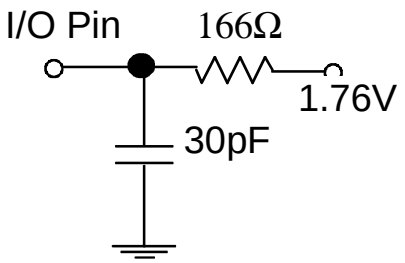
Parameter	*Symbol*	*Test Condition*	*min*	*-L Part typ(1)*	*max*	*Unit*
V_{CC} for Data Retention	V_{DR}	$\overline{CS}$ - V_{CC}-0.2V 0.2V ≥ V_{in} ≥ V_{cc}-0.2	2.0	-	-	V
Data Retention Current	I_{CCDR}	V_{CC} = 3.0V, $\overline{CS}$ = V_{CC}-0.2V 0.2V ≥ V_{in} ≥ V_{cc}-0.2	-	16	400	µA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	5	-	-	ms

Notes (1) Typical figures are measured at 25°C.

AC Test Conditions

* Input pulse levels: Vss to 3.0V
* Input rise and fall times: 5ns
* Input and Output timing reference levels: 1.5V
* Output load: see diagram
* V_{CC} = 5V± 10%

Output Load



AC OPERATING CONDITIONS

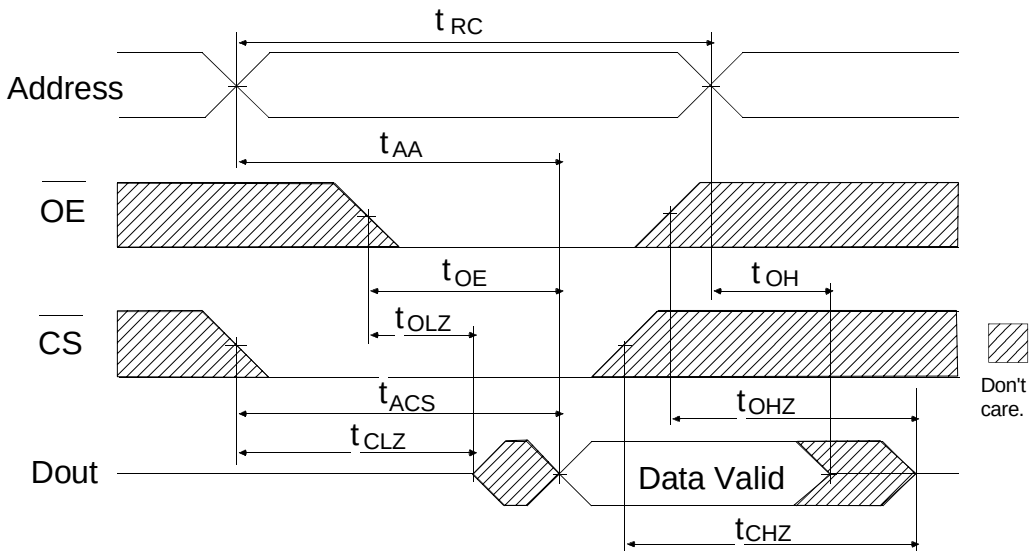
Read Cycle [1,2]

		-020		-25		-30		-35		
Parameter	Symbol	min	max	min	max	min	max	min	max	Unit
Read Cycle Time	t_{RC}	20	-	25	-	30	-	35	-	ns
Address Access Time	t_{AA}	-	20	-	25	-	30	-	35	ns
Chip Select Access Time	t_{ACS}	-	20	-	25	-	30	-	35	ns
Output Enable to Output Valid	t_{OE}	-	10	-	13	-	15	-	20	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	3	-	ns
Chip Selection to Output in Low Z	t_{CLZ}	3	-	3	-	3	-	3	-	ns
Output Enable to Output in Low Z	t_{OLZ}	0	-	0	-	0	-	0	-	ns
Chip Deselection to O/P in High Z	t_{CHZ}	0	12	0	15	0	15	0	20	ns
Output Disable to Output in High Z	t_{OHZ}	0	10	0	10	0	12	0	20	ns

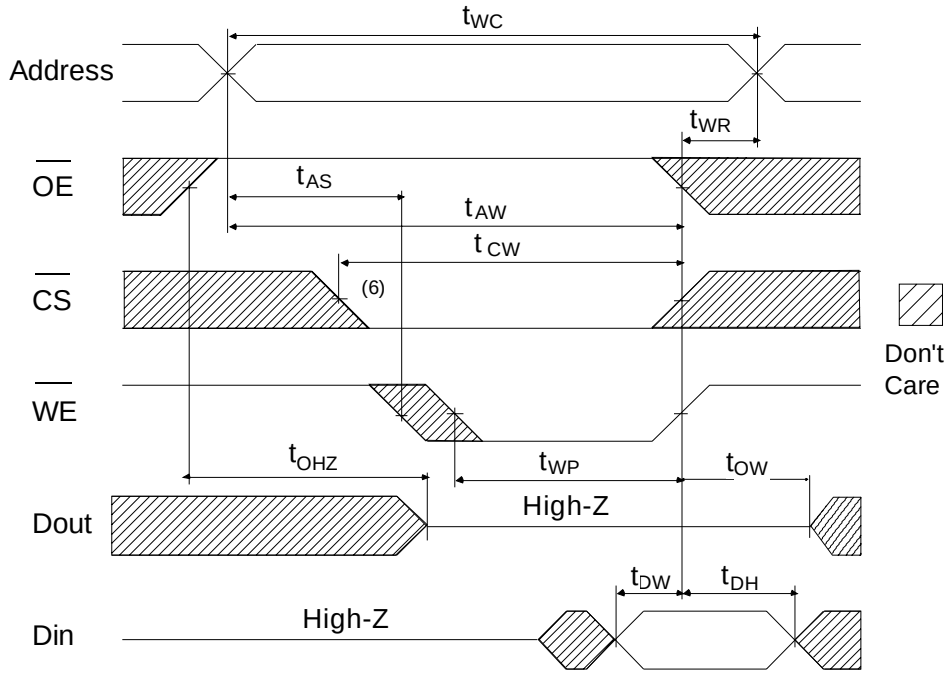
Write Cycle

		-020		-25		-30		-35		
Parameter	Symbol	min	max	min	max	min	max	min	max	Unit
Write Cycle Time	t_{WC}	20	-	25	-	30	-	35	-	ns
Chip Selection to End of Write	t_{CW}	17	-	20	-	25	-	30	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	0	-	ns
Address Valid to End of Write	t_{AW}	15	-	20	-	25	-	30	-	ns
Write Pulse Width	t_{WP}	15	-	20	-	22	-	25	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	0	-	ns
Write to Output in High Z [3]	t_{WHZ}	0	8	0	10	0	12	0	15	ns
Data to Write Time Overlap	t_{DW}	12	-	15	-	18	-	20	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	0	-	ns
Output active from end of write	t_{OW}	0	-	0	-	0	-	0	-	ns

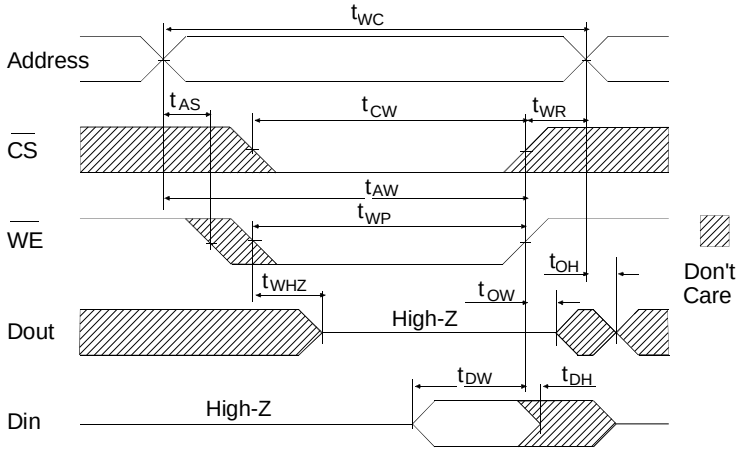
Read Cycle Timing Waveform (1,2)



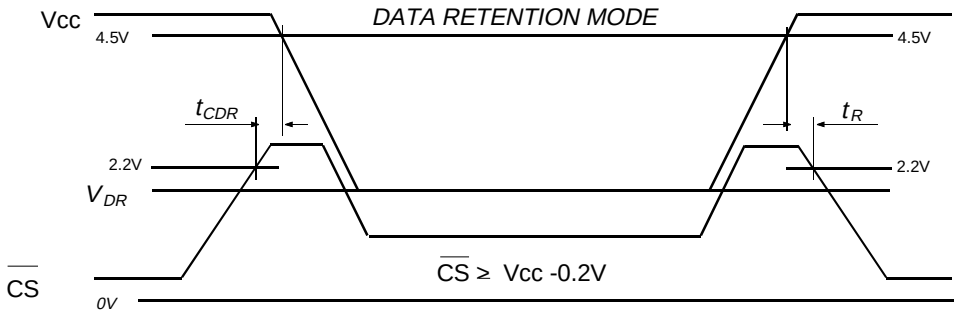
Write Cycle No.1 Timing Waveform



Write Cycle No.2 Timing Waveform



Data Retention Waveform

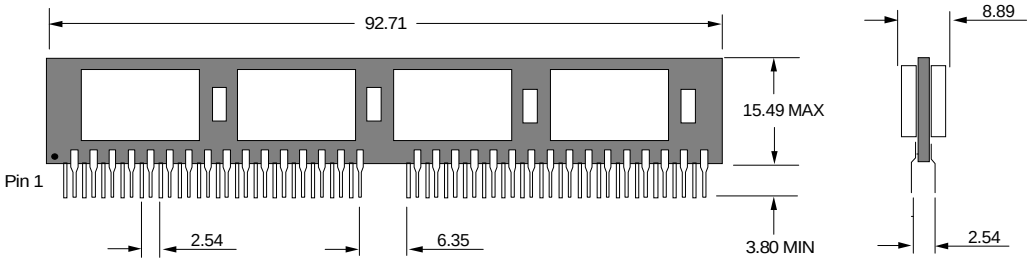


AC Characteristics Notes

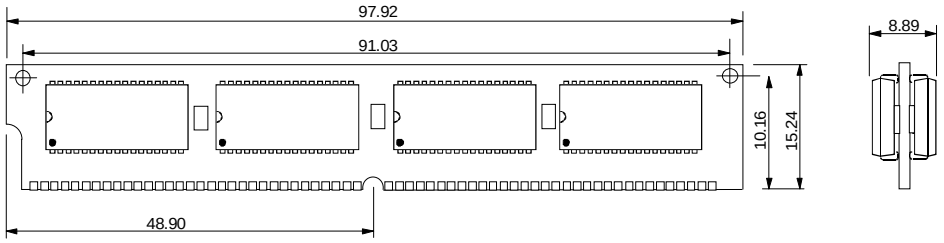
(1) $\overline{WE}$ is High for Read Cycle.
(2) All read cycle timing is referenced from the last valid address to the first transition address.
(3) At any given temperature and voltage condition, t_{CHZ} (max) is less than t_{CLZ} (min) both for a given module and from module to module.
(4) Module is continuously selected with $\overline{CS}$ = V_{IL}.
(5) Address is valid prior to or coincident with $\overline{CS}$ transition low.
(6) A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
(7) All write cycle timing is referenced from the last valid address to the first transition address.
(8) Defined as the time at which the outputs achieve open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.
(9) At any given temperature and voltage condition, t_{WHZ} (max) is less than t_{OW} (min) both for a given module and from module to module.
(10) $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

Package Information

64 PIN ZIP



64 LEAD SIMM



Dimensions in mm.

Ordering Information

SYS32256ZKLI - 30

Speed	020	=	20 ns
	25	=	25 ns
	30	=	30 ns
	35	=	35 ns
Temperature Range	Blank	=	Commercial Temperature
	I	=	Industrial Temperature
Power Rating	Blank	=	Standard
	L	=	Low Power
Package	ZK	=	Plastic 64 pin JEDEC ZIP
	LK	=	Plastic 64 pin JEDEC SIMM
Organization	32256	=	256k x 32
Memory Type	SYS	=	Static RAM

Note:
Although this data is believed to be accurate the information contained herein is not intended to and does not create any warranty of merchantibility or fitness for a particular purpose.
Our products are subject to a constant process of development. Data may be changed at any time without notice.
Products are not authorised for use as critical components in life support devices without the express written approval of a company director.