

Parallel FRAM® Memories

Product Family Summary - Complete datasheets available at www.ramton.com

Features

■ Nonvolatile ■ 10¹⁰ Endurance ■ No Write delay

■ Low Power ■ Industrial Temp Range

Description

Ramtron's parallel ferroelectric random access memories, or FRAM® memories, integrate the flexibility of a low power SRAM with the nonvolatile data integrity of an EEPROM. They are useful in a wide variety of applications for the storage of calibration data, configuration information, user programmable data/features, and state upon power loss.

With Ramtron's ferroelectric technology, all writes are nonvolatile, eliminating long delays, extra control sequencing, or high voltage pins. The technology is designed for highly reliable operation, offering very high endurance and 10 year data retention over commercial and industrial temperature ranges.

The parts synchronously latch the address on the falling edge of $\overline{\text{CE}}$, eliminating the need for an external address latch in systems with multiplexed bus structures.

The FRAM family uses the JEDEC approved pinout for SRAM and EEPROM devices and is plug compatible with both in many applications. Parallel FRAM memories are available in a 600 mil DIP and 300 mil SOP.

Product	Density/Org.	Active Current	Standby Current	Access Time	Voltage	Packaging
FM1608S	64K (8192 x 8)	25mA	50μA	200ns	4.5V to 5.5V	28-pin DIP/SOP

Packaging and Pin Names

Pin Names	Function	Pin Names	Function
A _x	Address Inputs	ŌĒ	Output Enable Input
1/0 ₀ -1/0 ₇	Data Input/Output	V _{CC}	Supply
CE	Chip Enable Input	GND	Ground
WE	Write Enable Input	NC	No Connect

FM1608



FRAM Technology

Ramtron is the first semiconductor company to make the necessary breakthroughs in materials, processing, and design to manufacture solid state ferroelectric memories. The result of these achievements is a process which merges ferroelectrics with silicon to create FRAM memories with significant benefits compared to existing products.

The ferroelectric effect is the ability of a material to retain an electric polarization without an applied electric field. This stable polarization results from the alignment of internal dipoles within the Perovskite crystal units in the ferroelectric material. Application of an electric field that exceeds the coercive field of the material will cause this alignment, while reversal of the field reverses the alignment of these internal dipoles.

The name *ferroelectric* derives from the similarity to a ferromagnetic material's ability to exhibit a magnetic polarization without an applied magnetic field. Ferroelectric materials are insensitive to magnetic fields. The construction of the FRAM products also makes them insensitive to practical external electric fields.

A simplified model of a unit ferroelectric crystal is shown. An externally applied electric field will move the center atom into one of the two stable positions based upon the direction of the field. Once the external field is removed, the atom remains in a stable position. Since no external electric field or current is required for the ferroelectric material to remain polar-

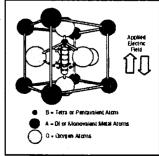
ized in either state, a memory device can be built for storing digital (binary) data that will not require power to retain information stored within it.

Ramtron has developed a complex proprietary thin-film ferroelectric material which is compatible with standard semiconductor fabrication techniques. The nonvolatile storage element in FRAM memories is a capacitor constructed from two metal electrodes and a ferroelectric thin film inserted between the transistor and metallization layers of a CMOS process.

Data stored in a ferroelectric memory cell can be read by applying an electric field to the capacitor. If the applied field is in the direction to switch the internal dipoles, more charge will be moved than if the dipoles are not reversed. Sense amplifiers built into the chips measure this charge and produce either

a zero or one on the output pins. After the read takes place, the chip automatically restores the correct data to the cell.

As development efforts of the FRAM memory continues, the capabilities will continue to increase and the cost will decrease. Using advanced ferroelectric technology, Ramtron will be able to reach the density and manufacturing economics of DRAM memory, providing the ideal memory solution.





Serial FRAM® Memories

Product Family Summary - Complete datasheets available at www.ramtron.com

Features

■ Nonvolatile

■ 10¹⁰ Endurance

■ No Write delay

■ Low Power

■ True 5V Operation

Description

Ramtron's serial ferroelectric random access memory, or serial FRAM® memory, provides nonvolatile data integrity in a compact package. The I²C and SPI serial interfaces provide access to any byte within the memory while reducing the cost of the processor interface (as compared to parallel access memories). The serial family of FRAM products is useful in a wide variety of applications for the storage of configuration information, user programmable data/features, and calibration data.

With Ramtron's ferroelectric technology, all writes are nonvolatile, eliminating long delays, extra page mode control, or high voltage pins. The technology is designed for highly reliable operation, offering extended endurance and 10 year data retention.

Ramtron's serial FRAM products use industry standard protocols for serial chip communication (I²C and SPI). All versions are available in 300 mil DIP and 150 mil SOP packages.

Product	Density/ Organization	Active Current	Standby Current	Bus	Max. Frequency	Read/Write Endurance	Operating Temperature	Packaging
FM24C04	4K (512 x 8)	100µA	60µА	I ² C	400KHz	10 ¹⁰	-40° to +85°C	8-pin DIP/SOIC
FM24C16	16K (2048 x 8)	300μΑ	60µА	I ² C	400KHz	1010	-40° to +85°C	8-pin DIP/SOIC
FM25040	4K (512 x 8)	1.5mA	60µA	SPI	2.1MHz	1010	-40° to +85°C	8-pin DIP/SOIC
FM25160	16K (2048 x 8)	1.5mA	60µA	SPI	2.1MHz	10 ¹⁰	-40° to +85°C	8-pin DIP/SOIC

Packaging and Pin Names

24C04

Pin Hamos	Function	off .
A ₁ · A ₂	Device Address	
SDA	Serial Data/Address	NC (1 8 D Vcc
SCL	Serial Clock	A 1 (2 7) WP
WP	Write Protect	7 A2 93 6 P SCL
Vss	Ground	Vss [4 5] SDA
Vcc	+5 Volts	ॏ———

24C16

Pin Harnes	Func		
SDA	Serial Data/Address		
SCL	Serial Clock	NC [T	∞ە 18 ك
WP	Write Protect	NC C 2	7 J WP
∨ _{ss}	Ground	NC [3	6 D SCL
Vœ	+5 Volts	Vss [4	5 D SDA

25040

Pin Hames	Fun]	
ČŠ.	Chip Select		1
SO .	Serial Data Out	cs d T C	8) V _{CC}
WP	Write Protect		7 D HOLD
Vss	Ground	SO 0 2 3	6 D SCK
SI	Serial Data in	V _{SS} (14	5 D SI
SCK	Seriai Clock		
HOLD	Hold Input		
V _{CC}	+5 Volts		

25160

Pin Names	F		
ই	Chip Select		<u> </u>
20	Serial Data Out		8) Vcc
WP.	Write Protect	So t 2	7 HOLD
V _{SS}	Ground	WP tl3	6 D SCK
Si	Serial Data In	√ss [[4	5 D SI
SCK	Serial Clock	7	_
HOLD	Hold input		7
V _{OC}	+5 Volts	-	