DATA SHEET

RDA5888E

Fully Integrated, Low Power Analog TV On a Chip

Update History

Rev	Date	Author	History Description
1.0	2010-083-11	Hanlingcai	The primary datasheet

Features

- Single-chip Tuner with NTSC/PAL/SECAM decoder
- Worldwide FM radio reception
- 100mA power consumption with digital output buffer
- Minimal external passive components
- Simple LNA matching components
- 50M- 870 MHz RF reception
- 100dB dynamic range
- <6 dB noise figure
- Fully integrated digital AGC loop
- Fully integrated channel selectivity
- Fully integrated PLL (including loop filter)
- > 35 dBc first-adjacent rejection
- Internal blank-level clamping
- Dynamic ghosting/fading compensation
- Support 26/27 MHz crystal
- All-digital video timing generation
- ITU-601 compliant
- Analog and I2S digital audio output
- I2C control port
- On chip regulator voltage input 3V to 4.5V.
- 40-pin 6x6 QFN package

Applications

- Portable applications such as laptops, portable DVD players
- Handheld applications such as cellular phones and PDAs

General Description

The RDA5888E is a fully integrated direct conversion SOC for NTSC/PAL/SECAM analog TV standards. The receiving frequency range is from 50MHz to 870MHz.The RDA5888E is a true single-chip design, requiring no external SAW or ceramic filters, even high Q off-chip inductors to achieve full channel selectivity with an average current consumption of 100mA.

The RDA5888E utilizes a direct-conversion, zero-IF architecture that allows for extremely good image and adjacent channel signal rejection. The RDA5888E consists of a variable gain LNA, quadrature downconverter, variable low-pass filters, reference oscillator, VCOs, synthesizer, high performance ADC, DSP for decoder. The DSP provides final adjacent-channel rejection and audio/video carrier demodulation. The audio stream is FM-demodulated and passed to the audio output port, whereas the CVBS video stream is separated into component dideo and output onto the video data bus.

Based on RDA's some innovative technique, the RDA5888E offers excellent phase noise and very low implementation loss, required for NTSC/PAL/SECAM decoder. This tuner RF IC does not require a balun and its fully integrated design saves valuable board space and simplifies RF layout.

Block Diagram

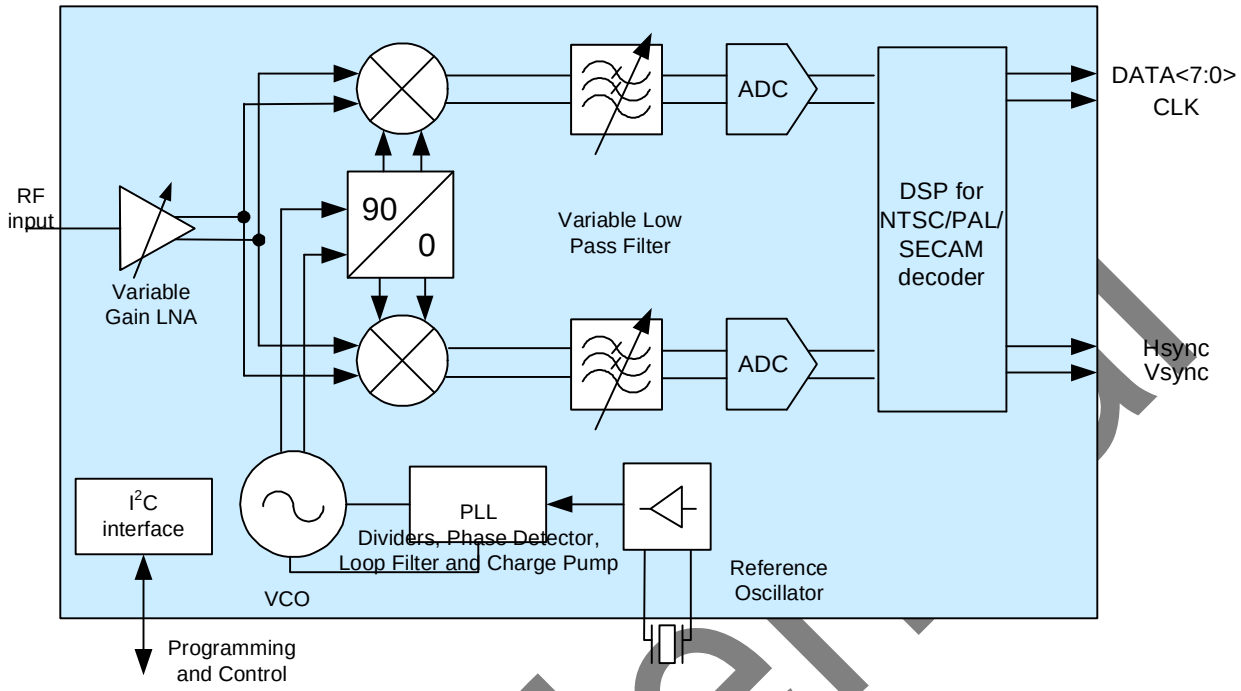


Figure 1. RDA5888E Block Diagram

DSP Functional Description

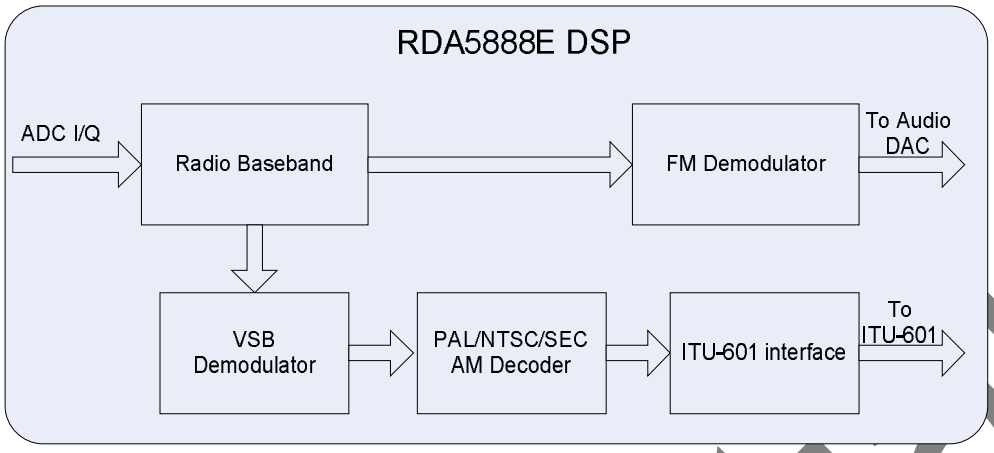


Figure 2. RDA5888E DSP Block Diagram

Radio Baseband

The radio basebasnd receive I/Q signal from ADC,it includes sinc downsample,AGC(auto RF gain and digital gain control) ,RSSI(receive signal strength indicator) and channel filtering.

FM Demodulator

The FM demodulator includes channel selection, FM demodulation,adaptive noise cancellation, programmable de-emphasis(50/75 μs),bass boost, volume control. Digital audio stream is converted into analog througn DAC.

VSB Demodulator

The VSB demodulator is an AM Vestigial Sideband demodulator for CVBS signal recovery.

PAL/NTSC/SECAM Decoder

The PAL/NTSC/SECAM decoder can handle NTSC,PAL,SECAM, M,D,B,I,G,H,L,K in CVBS format according to register-selected. It can be divided into a luminance path and a chrominance path. The luminance path first clamp the video signal, then calibration to target level and through a luma filter. The chrominance path has a color subcarrier recovery unit to regenerate the color subcarrier for any modulated chroma scheme and then performs an AM demodulation for PAL and NTSC and an FM demodulation for SECAM according to register-selected. YcbCr to ITU-601 interface is converted from YUV/YIQ/YRB . .

I2S interface

RDA5888E support standard I2S interface to output stereo audio signal.

ITU-601 Interface

The ITU-601 Interface is an ITU-601 compliant 8bit 4:2:2(YcbCr) parallel interface which include dclk,hsync,vsync,data[7:0].dclk,hsync,vsync all have polarity option. Below is the timing for the bus:

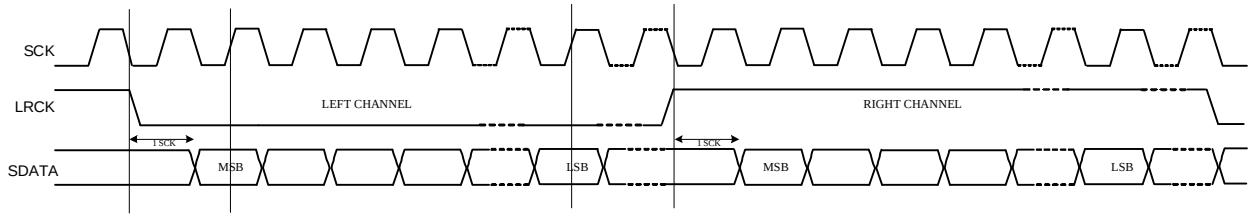


Figure 3 I2S Digital Audio Format

525 Timing

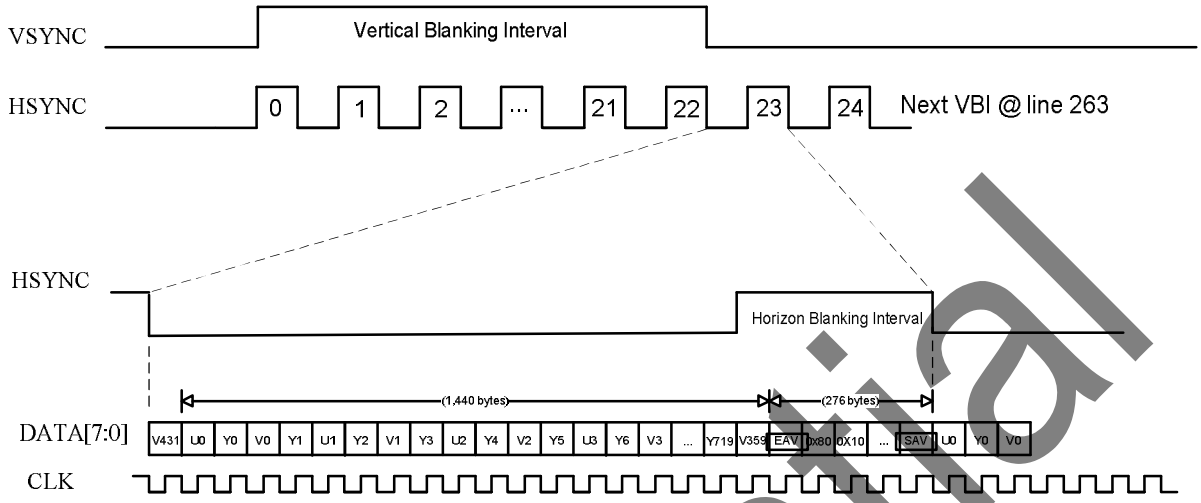


Figure 4. 525 Line ITU-601 Timing Diagram

625 Timing

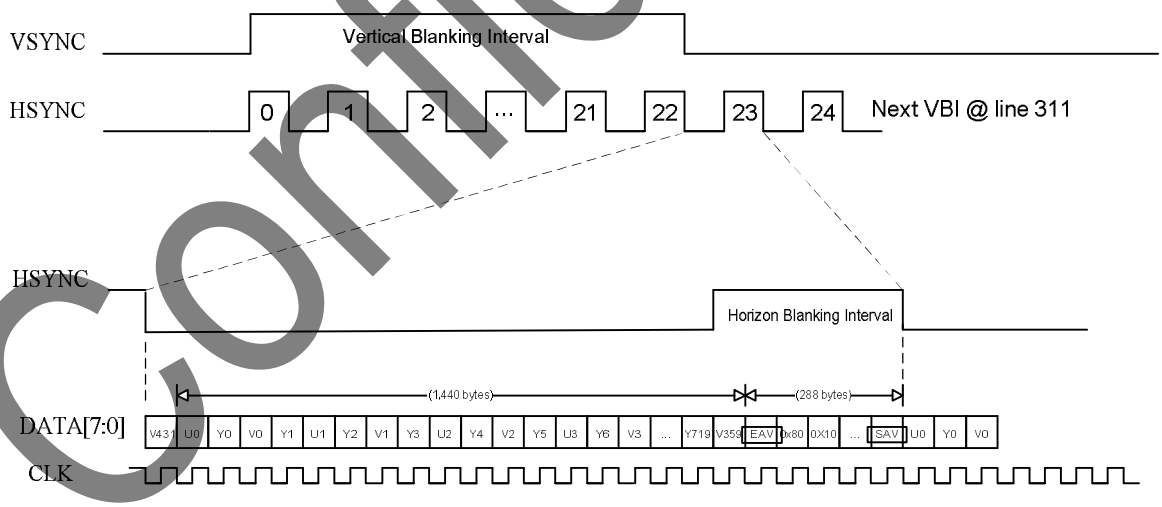


Figure 5. 625 Line ITU-601 Timing Diagram

Electrical Specifications

Table 1 Recommended Operating Conditions

Parameter	Symbol	MIN	TYP	MAX	UNIT
Analog Supply Voltage	VBAT	3	3.3	+4.5	V
Ambient Temperature	T_A	-25	27	+85	°C

Table 2 DC Electrical Specification

Parameter	Symbol	MIN	TYP	MAX	UNIT
CMOS Low Level Input Voltage	V_{IL}	0		0.3*VDD	V
CMOS High Level Input Voltage	V_{IH}	0.7*VDD		VDD	V
CMOS Threshold Voltage	V_{TH}		0.5*VDD		V

Table 3 Power consumption specification

(Vbat = 3 to 4.5 V, T_A = -25 to 85 °C, unless otherwise specified)

Symbol	Description	Condition	TYP	UNIT
ICC	Receiver on		100	mA
ICC(sleep)	Sleep mode (PDN = 0)		40	μA

Table 4 System Characteristics

(Vbat = 3 to 4.5 V, T_A = -25 to 85 °C, unless otherwise specified)

Parameter	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
RF input frequency	f_{IN}		50		870	MHz
Maximum RF input	RFIH			-10		dBm
Noise Figure	NF	Max Gain		5	8	dB
Input refered third-order intercept	IIP3	Max Gain	-14	-12		dBm
Input refered econd-order intercept	IIP2	Max Gain		35		dBm
IQ amplitude balance	IQAB				0.1	dB
IQ phase balance	IQPB				0.2	Deg
Matched input resistance	R_{IN}			50		Ω
Power up setting time	PUST			200		ms

Table 5 Frequency Synthesizer Characteristics

(Vbat = 3 to 4.5 V, T_A = -25 to 85 °C, unless otherwise specified)

SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
t_{SW}	RX Switch on time			200		us
f_{RFLO}	synthesizer frequency		50		870	MHz
PN1	Phase noise	Δf=1kHz	-120	-100	-85	dBc/Hz
PN2		Δf=10kHz	-125	-105	-95	dBc/Hz
PN3		Δf=100kHz	-130	-110	-100	dBc/Hz
PN4		Δf=1MHz	-150	-130	-120	dBc/Hz

Control Interface

RDA5888E enable software programming through I2C interface. Software controls chip working states, and allows user read status registers to get operation result through I2C interface.

The I2C interface of RDA5888E is compliant to I2C-Bus Specification 2.1(Fast-mode, bit rate up to 400Kbit/s). It includes two pins: SCLK and SDA. SCLK is an input pin; SDA is a bi-direction pin.

The I2C interface transfer begins with START condition, a command byte and data bytes, each byte has a followed ACK (or NACK) bit, and ends with STOP condition. The command byte includes a 7-bit device address {chip_id[6:0](default is 7'b1100_010)} and a r/w bit. The ACK (or NACK) is always sent out by the receiver. When in write transfer process, data bytes are written out from MCU, and when in read transfer process, data bytes are read out from RDA5888E. The RDA5888E contains status/control registers. These read/write registers are addressed as sub-address on the I2C bus. RDA5888E I2C interface supports both single and sequential register access. Software could follow the following ways to perform register read/write access:

Random access single write

Start	Device address	W	A	Register address	A	Register data[15:8]	A	Register data[7:0]	A	Stop

Random access single read

Start	Device address	W	A	Register address	A	start	Device address	R	A	
Registe Data[15:8]	A	Registe Data[7:0]	N	stop						

W: Write Bit (0: write; 1: read)
A: Acknowledge Bit (ACK)
N: Not Acknowledge Bit (NO ACK)

For random access single write transfer, MCU sends out the START signal, RDA5880's device address and 1 bit write signal in sequence to the I2C bus. After receiving RDA5888E' s ACK signal, MCU sends out the target register's address (8 bits) to RDA5888E and then programs this register with proper data (8 bits). A STOP signal is sent out by MCU to end this transfer when programming is finished.

For random access single read transfer, MCU first sends out the START signal, the RDA5888E's device address and 1 bit write signal to the I2C bus. After receiving RDA5888E's ACK signal, MCU sends the target register's address to the interface. Then MCU should send another command byte, including a RESTART signal, the RDA5888E's device address and 1 bit read signal. RDA5888E will send the register's data to MCU through I2C bus. After the byte has been received, MCU should send a NO ACK response signal and a STOP signal to finish this read transfer.

Table 6 I^2C bus characteristics

(VDD = 2.7 to 3.6 V, T_A = -25 to 85 °C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
SCLK Frequency	f_{scl}		0	-	200	KHz
SCLK High Time	t_{high}		0.6	-	-	µs
SCLK Low Time	t_{low}		1.3	-	-	µs
Setup Time for START Condition	$t_{su:sta}$		0.6	-	-	µs
Hold Time for START Condition	$t_{hd:sta}$		0.6	-	-	µs
Setup Time for STOP Condition	$t_{su:sto}$		0.6	-	-	µs
SDIO Input to SCLK↑ Setup	$t_{su:dat}$		100	-	-	ns
SDIO Input to SCLK↓ Hold	$t_{hd:dat}$		0	-	900	ns
STOP to START Time	t_{buf}		1.3	-	-	µs
SDIO Output Fall Time	$t_{f:out}$		$20+0.1C_b$	-	250	ns
SDIO Input, SCLK Rise/Fall Time	$t_{r:in}$ / $t_{f:in}$		$20+0.1C_b$	-	300	ns
Input Spike Suppression	t_{sp}		-	-	50	ns
SCLK, SDIO Capacitive Loading	C_b		-	-	50	pF
Digital Input Pin Capacitance					5	pF

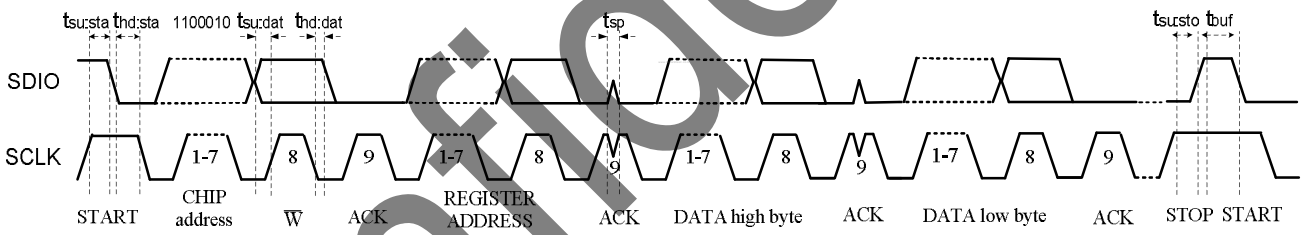


Figure 6. I^2C Interface Write Timing Diagram

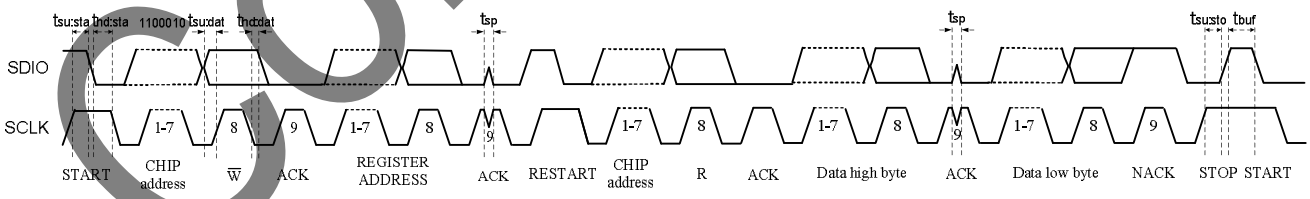
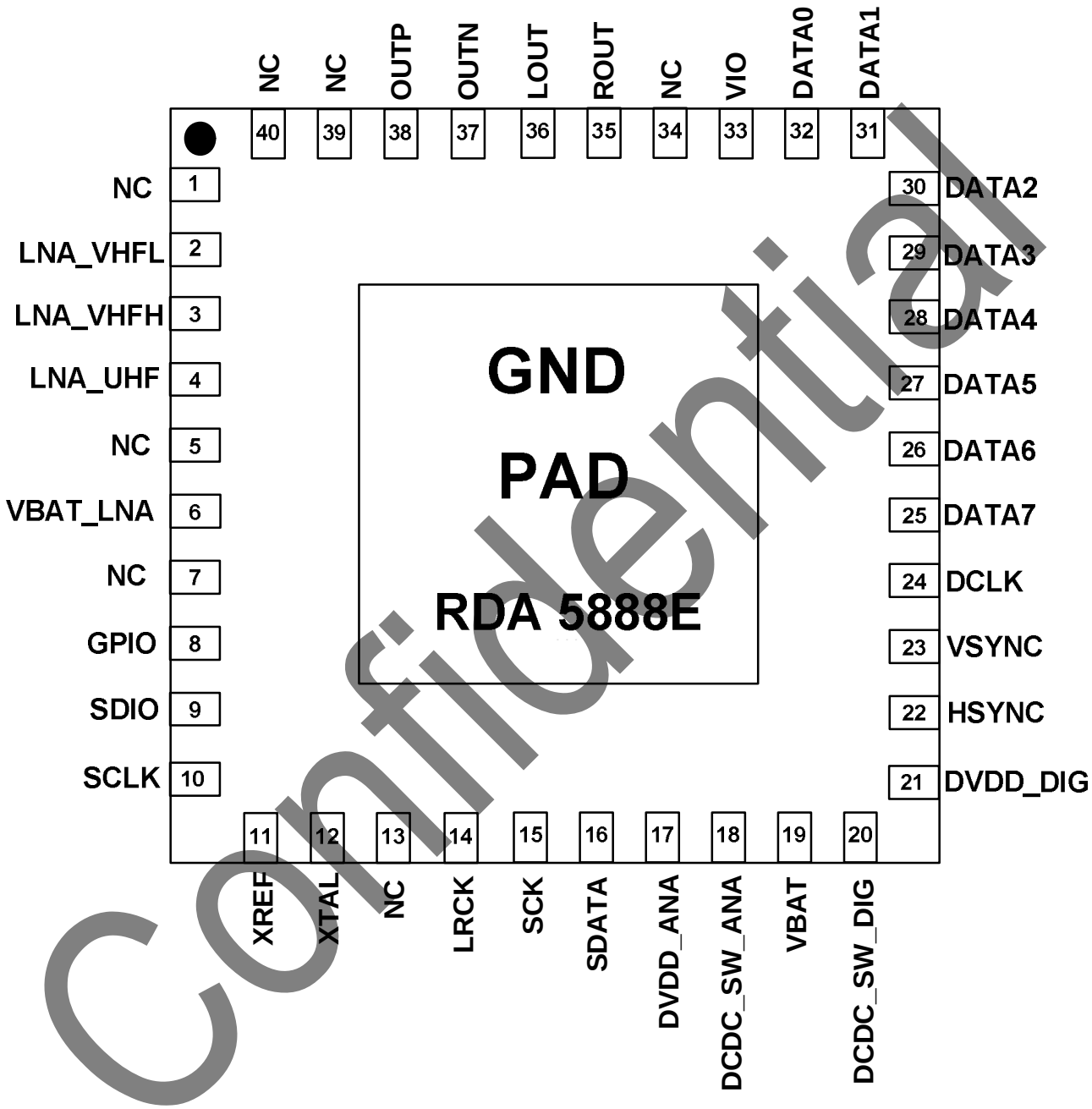


Figure 7. I^2C Interface Read Timing Diagram

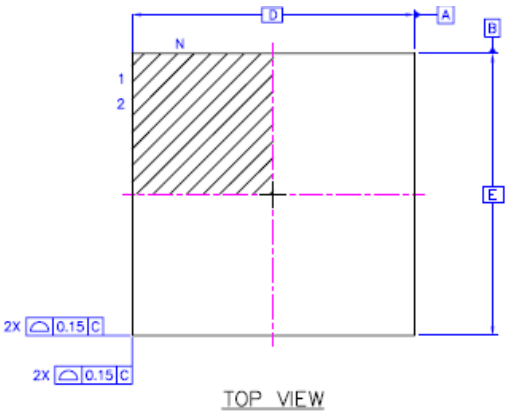
Pin Description



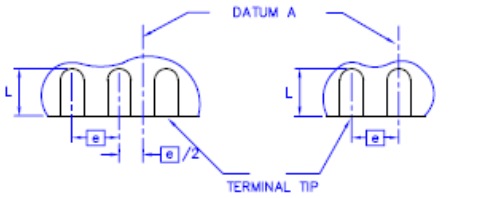
Pin number	Name	I/O	DESCRIPTION
1	NC		No Connect
2	LNA_VHFL	I	VHFL RF input
3	LNA_VHFH	I	VHFH RF input

4	LNA_UHF	I	UHF RF input
5	NC		No Connect
6	VBAT_LNA	I	Battery AVDD for LNA
7	NC		No Connect
8	GPIO	I/O	GPIO
9	SDIO	I/O	I2c Serial data input
10	SCLK	I/O	I2c Serial clock input
11	XREF	I/O	Connect to Crystal (if using external crystal oscillator, this pin connect to the oscillator's output)
12	XTAL	O	Connect to Crystal
13	NC		No Connect
14	LRCK	I/O	Left/right audio sample indicator
15	SCK	I/O	Audio slave clock
16	SDATA	O	I2S data
17	DVDD_ANA	I	DVDD Analog
18	DCDC_SW_ANA	O	DCDC_ Analog output
19	VBAT	I	Battery AVDD
20	DCDC_SW_DIG	O	DCDC_ Digital output
21	DVDD_DIG	I	DVDD Digital
22	HSYNC	O	Hsync line
23	VSYNC	O	Vsync line
24	DCLK	O	data clk output
25	DATA7	O	data output
26	DATA6	O	data output
27	DATA5	O	data output
28	DATA4	O	data output
29	DATA3	O	data output
30	DATA2	O	data output
31	DATA1	O	data output
32	DATA0	O	data output
33	VIO	O	VIO
34	NC		No Connect
35	ROUT	O	Audio analog dac output
36	LOUT	O	Audio analog dac output
37	OUTN	O	Negative Baseband Out
38	OUTP	O	Positive Baseband Out
39	NC		No Connect
40	NC		No Connect

Package Outline

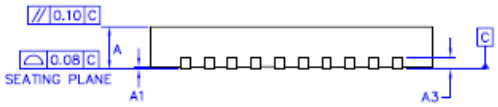


TOP VIEW

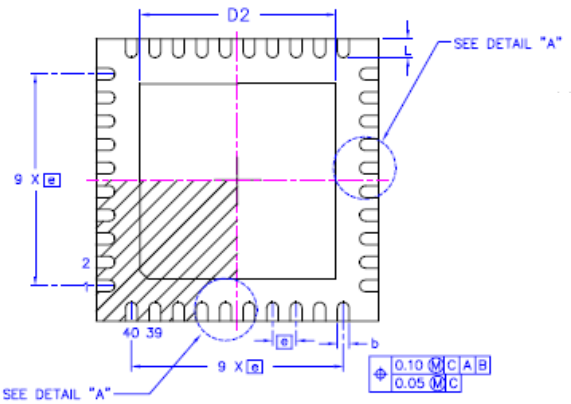


EVEN TERMINAL/SIDE ODD TERMINAL/SIDE

DETAIL "A"



SIDE VIEW

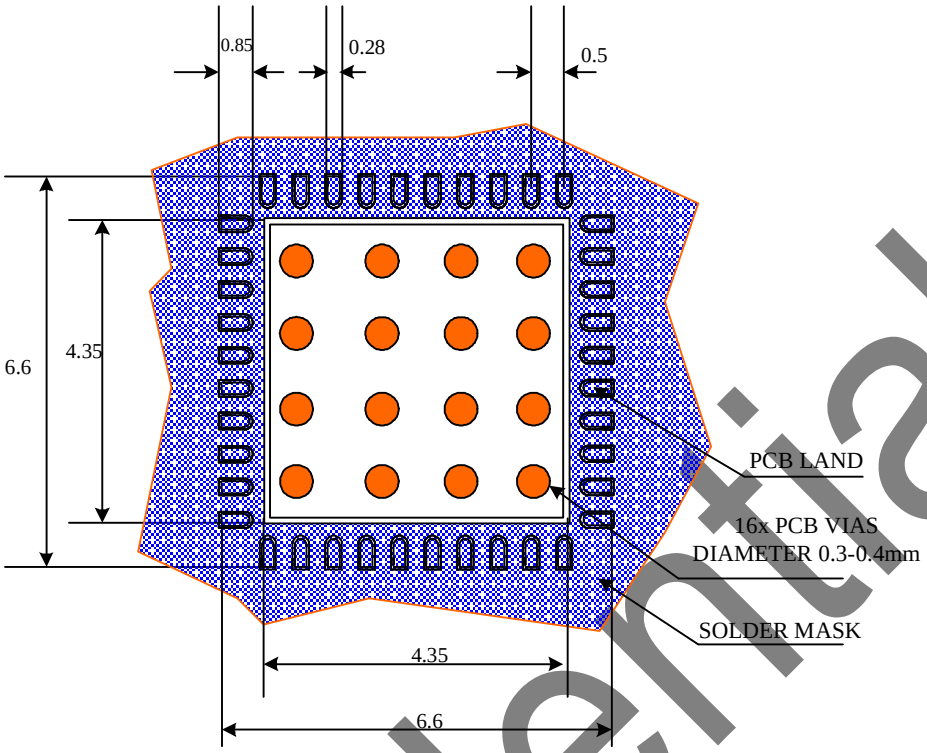


BOTTOM VIEW

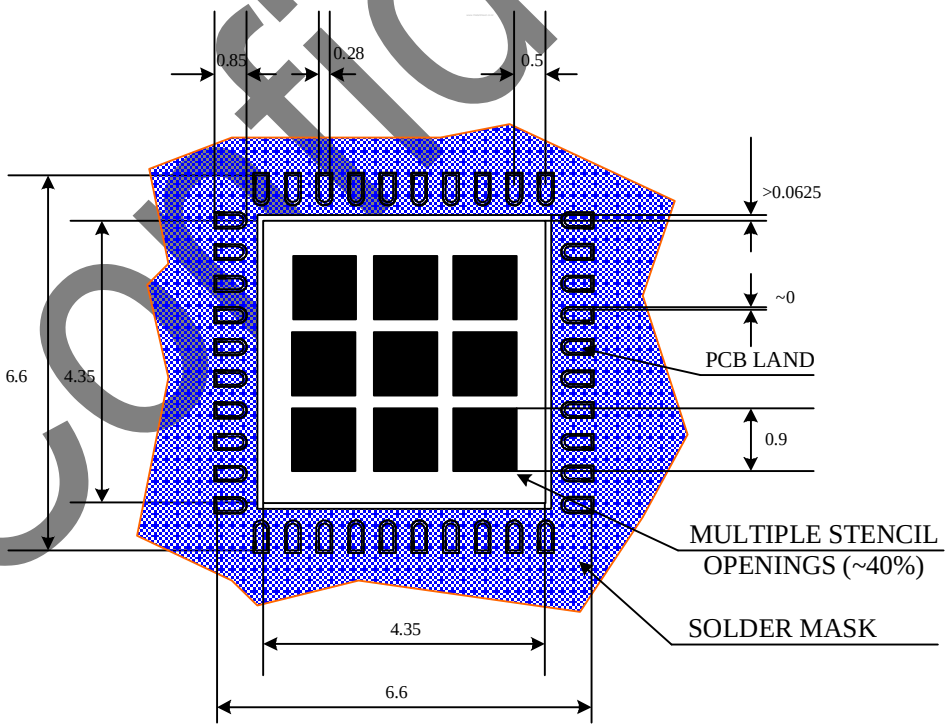
	MIN.	NOM.	MAX.
D		6.00 BSC	
E		6.00 BSC	
D2	4.00	4.15	4.25
E2	4.00	4.15	4.25
e		0.50 BSC	
L	0.30	0.40	0.50
b	0.18	0.25	0.30
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.20 ref	

40-Pin 6x6 Quad Flat No-Lead (QFN)

PCB Land Pattern

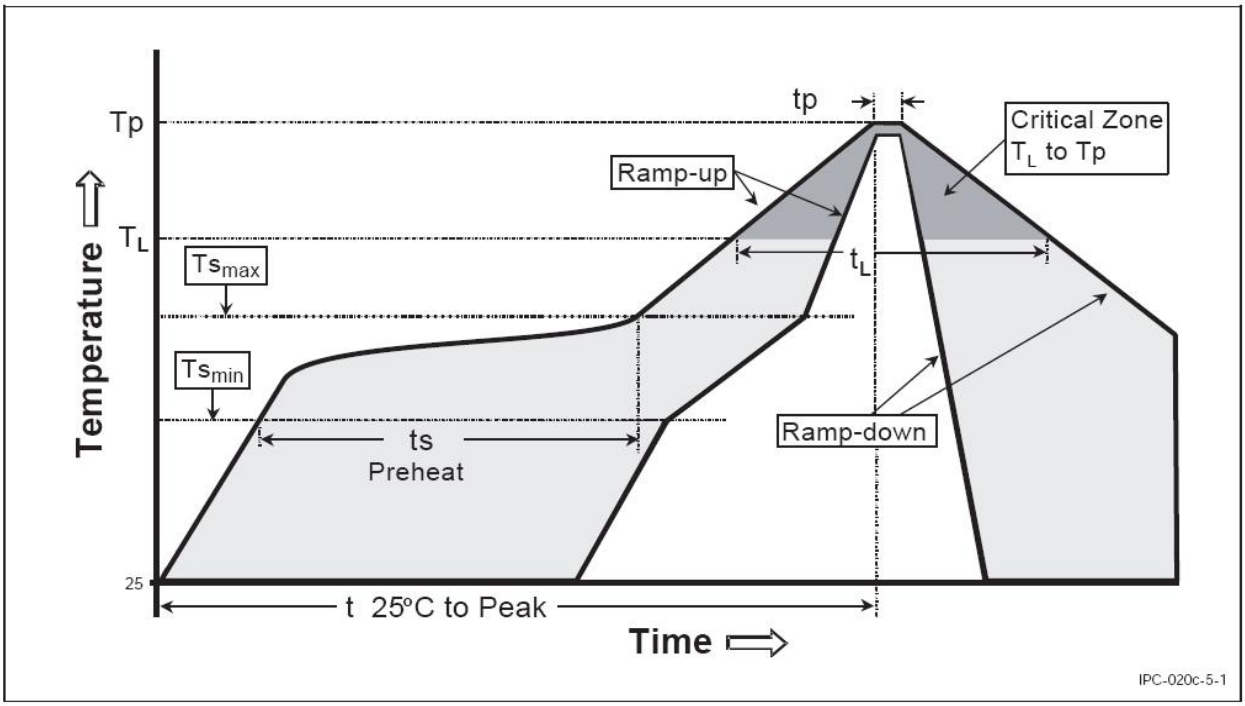


PCB Land Pattern for 40-Pin QFN



PCB Solder Paste Stencil Openings

Solder Mounting Condition



Classification Reflow Profile

Table-I Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate (T_{Smax} to T_p)	3 °C/second max.	3 °C/second max.
Preheat -Temperature Min (T_{smin}) -Temperature Max (T_{smax}) -Time (t_{smin} to t_{smax})	 100 °C 100 °C 60-120 seconds	 150 °C 200 °C 60-180 seconds
Time maintained above: -Temperature (T_L) -Time (t_L)	 183 °C 60-150seconds	 217°C 60-150 seconds
Peak /Classification Temperature(T_p)	See Table-II	See Table-III
Time within 5 °C of actual Peak Temperature (t_p)	10-30 seconds	20-40 seconds
Ramp-Down Rate	6 °C/second max.	6 °C/seconds max.

Time 25 °C to Peak Temperature	6 minutes max.	8 minutes max.

Table – II SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm³ <350	Volume mm³ ≥350
＜2.5mm	240 + 0/-5 °C	225 + 0/-5 °C
≥2.5mm	225 + 0/-5 °C	225 + 0/-5 °C

Table – III Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm³ ＜350	Volume mm³ 350-2000	Volume mm³ ＞2000
＜1.6mm	260 + 0 °C *	260 + 0 °C *	260 + 0 °C *
1.6mm – 2.5mm	260 + 0 °C *	250 + 0 °C *	245 + 0 °C *
≥2.5mm	250 + 0 °C *	245 + 0 °C *	245 + 0 °C *
*Tolerance : The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature(this mean Peak reflow temperature + 0 °C. For example 260+ 0 °C) at the rated MSL Level.			

Note 1: All temperature refer topside of the package. Measured on the package body surface.

Note 2: The profiling tolerance is + 0 °C, - X °C (based on machine variation capability)whatever is required to control the profile process but at no time will it exceed - 5 °C. The producer assures process compatibility at the peak reflow profile temperatures defined in Table –III.

Note 3: Package volume excludes external terminals(balls, bumps, lands, leads) and/or non integral heat sinks.

Note 4: The maximum component temperature reached during reflow depends on package the thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD package may sill exist.

Note 5: Components intended for use in a “lead-free” assembly process **shall** be evaluated using the “lead free” classification temperatures and profiles defined in Table-I II III whether or not lead free.

RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) or polybrominated diphenyl ethers (PBDE), and are therefore considered RoHS compliant.

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electricity. Proper ESD techniques should be used when handling these devices.

Disclaimer

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