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2M x 32 SRAM MODULE

SYS322000ZK-015/020/025

Issue 1.2 : April 1999

Description

The SYS322000ZK is a plastic 64Mbit Static RAM Module offered in a low profile 72 pin ZIP package, organised as 2M x 32. The module utilises sixteen 512K x 8 SRAM's housed in TSOP II packages, surface mounted onto a dual FR4 epoxy PCB construction.

Four chip selects and the highest order address line are used to independently enable the eight bytes as well as the high or low block of addressable memory space. Reading or Writing is executed on individual or any combination of multiple bytes.

The module also incorporates on-board decoupling.

Features

- Access Times of 15/20/25 ns.
- 72 Pin Zig-zag-In-line Package (ZIP).
- 5 Volt Supply ± 10%.
- Operating Power (32bit mode) 7.60W (Max)
  Standby Current (CMOS) 935mW (Max)
- Completely Static Operation.
- Equal Access and Cycle Times.
- All Inputs and Outputs Directly TTL Compatible.
- On-board Supply Decoupling Capacitors.

Block Diagram

See page 7.

Pin Functions

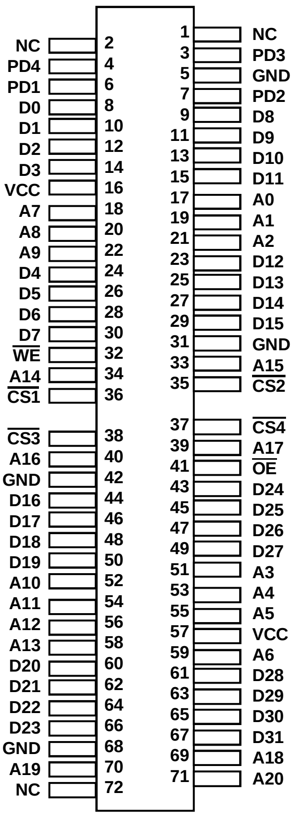
Address Inputs	**A0 - A20**
Data Input/Output	**D0 - D31**
Chip Selects	**$\overline{\text{CS1\~4}}$**
Write Enable	**$\overline{\text{WE}}$**
Output Enable	**$\overline{\text{OE}}$**
No Connect	**NC**
Power (+5V)	**V_{CC}**
Ground	**GND**

Package Details

Plastic 72 Pin ZIP

Pin Definition

TOP VIEW



Signal	Pin	Pin	Signal
		1	NC
NC	2	3	PD3
PD4	4	5	GND
PD1	6	7	PD2
D0	8	9	D8
D1	10	11	D9
D2	12	13	D10
D3	14	15	D11
VCC	16	17	A0
A7	18	19	A1
A8	20	21	A2
A9	22	23	D12
D4	24	25	D13
D5	26	27	D14
D6	28	29	D15
D7	30	31	GND
$\overline{\text{WE}}$	32	33	A15
A14	34	35	$\overline{\text{CS2}}$
$\overline{\text{CS1}}$	36	37	$\overline{\text{CS4}}$
$\overline{\text{CS3}}$	38	39	A17
A16	40	41	$\overline{\text{OE}}$
GND	42	43	D24
D16	44	45	D25
D17	46	47	D26
D18	48	49	D27
D19	50	51	A3
A10	52	53	A4
A11	54	55	A5
A12	56	57	VCC
A13	58	59	A6
D20	60	61	D28
D21	62	63	D29
D22	64	65	D30
D23	66	67	D31
GND	68	69	A18
A19	70	71	A20
NC	72		

PD2 = PD3 = GND
PD1 = PD4 = OPEN

DC OPERATING CONDITIONS

Absolute Maximum Ratings (1)

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Voltage on any pin relative to V_{SS}	V_T(2)	-0.3	-	7.0	V
Power Dissipation	P_T	-	-	16.0	W
Storage Temperature	T_{STG}	-55	-	125	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) V_T can be -2.0V pulse of less than 8ns.

Recommended Operating Conditions

Parameter		*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Supply Voltage		V_{CC}	4.5	5.0	5.5	V
Input High Voltage		V_{IH}	2.2	-	V_{CC}+0.3	V
Input Low Voltage		V_{IL}	-0.3	-	0.8	V
Operating Temperature	(Commercial)	T_A	0	-	70	°C
	(Industrial)	T_{AI}	-40	-	85	°C

DC Electrical Characteristics (V_{CC}=5V±10%) TA 0 to 70 °C

Parameter		*Symbol*	*Test Condition*	*Min*	*Typ*	*max*	*Unit*
I/P Leakage Current	Address,$\overline{OE}$,$\overline{WE}$	I_{LI}	$0V \le V_{IN} \le V_{CC}$	-32	-	32	µA
Output Leakage Current	8-bit mode	I_{LO}	$\overline{CS} = V_{IH}$, $V_{I/O}$ = GND to V_{CC}	-32	-	32	µA
Operating Supply Current	32-bit mode	I_{CC1}	Min. Cycle, $\overline{CS} = V_{IL}, V_{IL} \le V_{IN} \le V_{IH}$	-	-	1380	mA
Standby Supply Current	TTL levels	I_{SB1}	$\overline{CS} = V_{IH}$	-	-	820	mA
	CMOS levels	I_{SB2}	$\overline{CS} \ge V_{CC}$-0.2V, $0.2 \le V_{IN} \le V_{CC}$-0.2V	-	-	170	mA
Output Voltage		V_{OL}	I_{OL} = 8.0mA	-	-	0.4	V
		V_{OH}	I_{OH} = -4.0mA	2.4	-	-	V

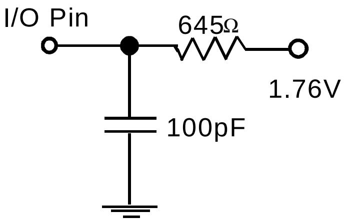
Typical values are at V_{CC}=5.0V,T_A=25°C and specified loading. $\overline{CS}$ above refers to $\overline{CS1\sim4}$.

Capacitance (V_{CC}=5V±10%,T_A=25°C) Note: Capacitance calculated, not measured.

Parameter	*Symbol*	*Test Condition*	*max*	*Unit*
Input Capacitance (Address,$\overline{OE}$,$\overline{WE}$)	C_{IN1}	V_{IN} = 0V	128	pF
I/P Capacitance (other)	C_{IN2}	V_{IN} = 0V	10	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	128	pF

AC Test Conditions Output Load

- * Input pulse levels: 0V to 3.0V
- * Input rise and fall times: 3ns
- * Input and Output timing reference levels: 1.5V
- * Output load: see diagram
- * V_{CC}=5V±10%



Operation Truth Table

$\overline{CS}$	***$\overline{OE}$***	***$\overline{WE}$***	***DATA PINS***	***SUPPLY CURRENT***	***MODE***
H	X	X	High Impedance	I_{SB1} , I_{SB2} , I_{SB3}	Standby
L	L	H	Data Out	I_{CC1}	Read
L	H	L	Data In	I_{CC1}	Write
L	L	L	Data In	I_{CC1}	Write
L	H	H	High-Impedance	I_{SB1} , I_{SB2} , I_{SB3}	High-Z

Notes : H = V_{IH} : L =V_{IL} : X = V_{IH} or V_{IL}

AC OPERATING CONDITIONS

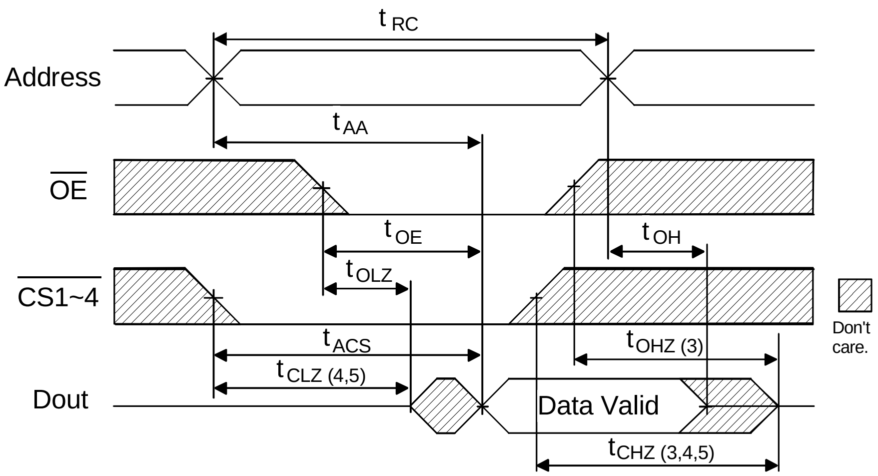
Read Cycle

		015		*020*		*025*	
Parameter	*Symbol*	*min*	*max*	*min*	*max*	*min*	*max*
Read Cycle Time	t_{RC}	15	-	20	-	25	-
Address Access Time	t_{AA}	-	15	-	20	-	25
Chip Select Access Time	t_{ACS}	-	15	-	20	-	25
Output Enable to Output Valid	t_{OE}	-	7	-	9	-	13
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-
Chip Selection to Output in Low Z	t_{CLZ}	3	-	3	-	3	-
Output Enable to Output in Low Z	t_{OLZ}	0	-	0	-	0	-
Chip Deselection to O/P in High Z	t_{CHZ}	0	7	0	9	0	10
Output Disable to Output in High Z	t_{OHZ}	0	7	0	9	0	10

Write Cycle

		015		*020*		*025*	
Parameter	*Symbol*	*min*	*max*	*min*	*max*	*min*	*max*
Write Cycle Time	t_{WC}	15	-	20	-	25	-
Chip Selection to End of Write	t_{CW}	12	-	15	-	20	-
Address Valid to End of Write	t_{AW}	12	-	15	-	20	-
Address Setup Time	t_{AS}	0	-	0	-	0	-
Write Pulse Width	t_{WP}	10	-	12	-	15	-
Write Recovery Time	t_{WR}	0	-	0	-	0	-
Write to Output in High Z	t_{WHZ}	0	7	0	9	0	10
Data to Write Time Overlap	t_{DW}	8	-	10	-	12	-
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-
Output active from end of write	t_{OW}	3	-	3	-	3	-

Read Cycle Timing Waveform (1,2)



AC Read Characteristics Notes

(1) $\overline{WE}$ is High for Read Cycle.

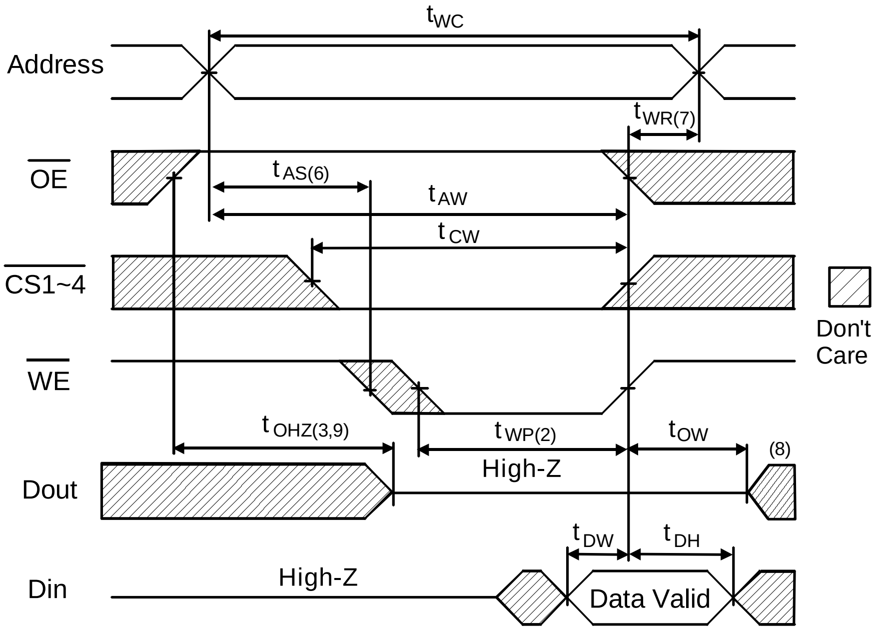
(2) All read cycle timing is referenced from the last valid address to the first transition address.

(3) t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve open circuit conditions and are not referenced to output voltage levels.

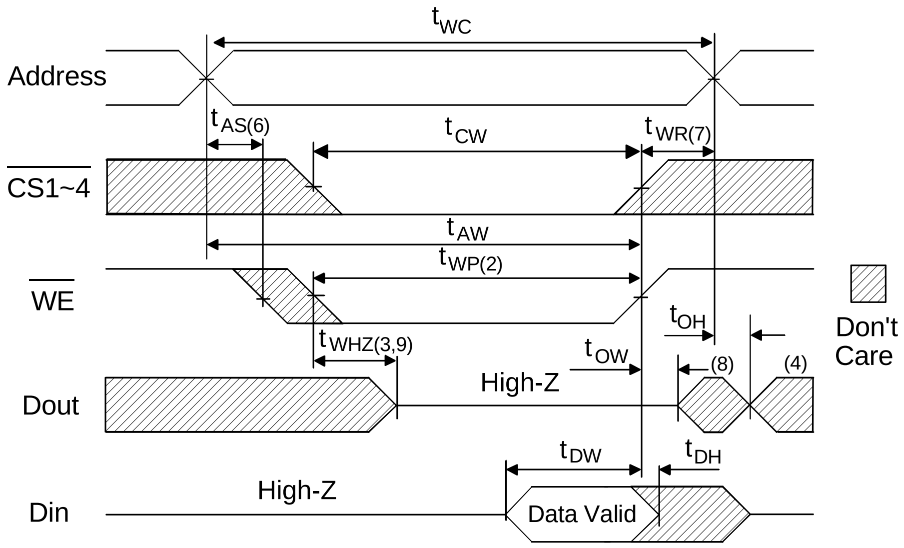
(4) At any given temperature and voltage condition, t_{CHZ} (max) is less than t_{CLZ} (min) both for a given module and from module to module.

(5) These parameters are sampled and not 100% tested.

Write Cycle No.1 Timing Waveform (1,4)



Write Cycle No.2 Timing Waveform (1,5)



AC Write Characteristics Notes

(1) All write cycle timing is referenced from the last valid address to the first transition address.

(2) All writes occur during the overlap of $\overline{\mathrm{CS1{\sim}4}}$ and $\overline{\mathrm{WE}}$ low.

(3) If $\overline{\mathrm{OE}}$, $\overline{\mathrm{CS1{\sim}4}}$, and $\overline{\mathrm{WE}}$ are in the Read mode during this period, the I/O pins are low impedance state. Inputs of opposite phase to the output must not be applied because bus contention can occur.

(4) Dout is the Read data of the new address.

(5) $\overline{\mathrm{OE}}$ is continuously low.

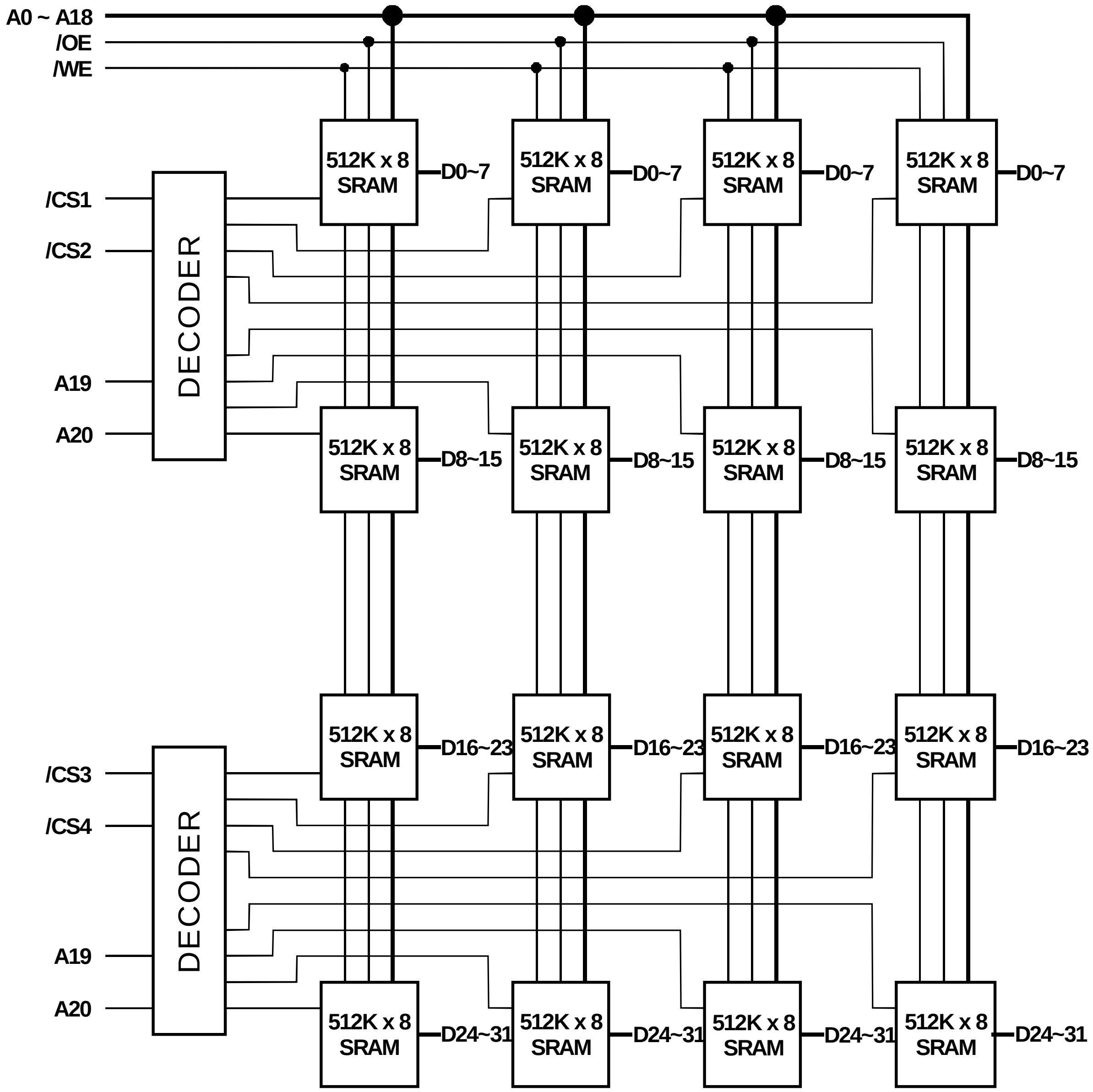
(6) Address is valid prior to or coincident with $\overline{\mathrm{CS1{\sim}4}}$ and $\overline{\mathrm{WE}}$ low, too avoid inadvertant writes.

(7) $\overline{\mathrm{CS1{\sim}4}}$ or $\overline{\mathrm{WE}}$ must be high during address transitions.

(8) When $\overline{\mathrm{CS1{\sim}4}}$ are low : I/O pins are in the output state. Input signals of opposite phase leading to the output should not be applied.

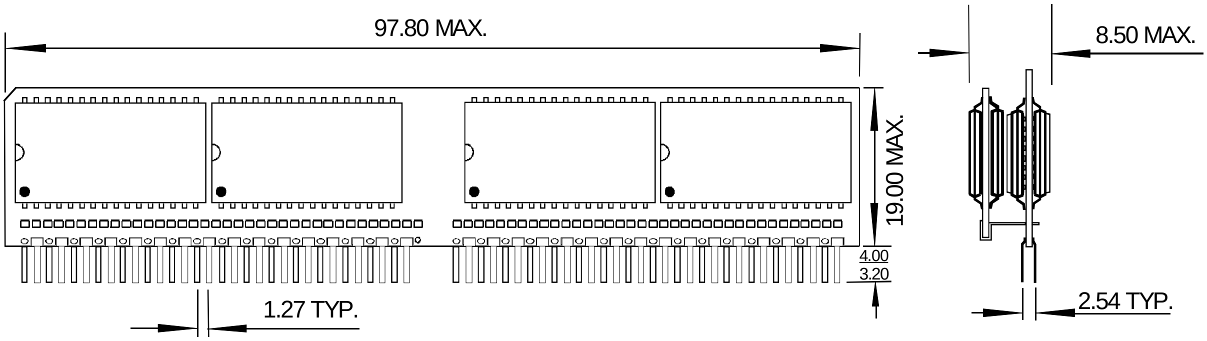
(9) Defined as the time at which the outputs achieve open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.

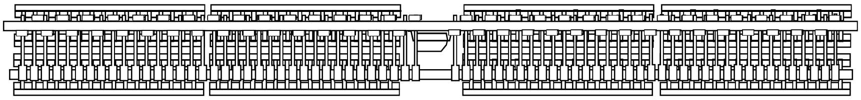
Block Diagram



Package Information Dimensions in mm

Plastic 72 Pin Zig-zag-In-line Package (ZIP)





Ordering Information

SYS322000ZKI-15

Speed
015 = 15 ns
020 = 20 ns
025 = 25 ns

Temperature range
Blank = Commercial Temp.
I = Industrial Temp.

Package
ZK = Plastic 72 Pin ZIP

Organisation
322000 = 2M X 32

Memory Type
SYS = Static RAM