

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC7SZ08F, TC7SZ08FU

2 INPUT AND GATE

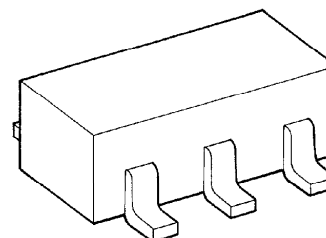
FEATURES

- High Output Drive : ± 24 mA (Typ.)
($V_{CC} = 3$ V)
- Super High Speed Operation : $t_{pD} = 2.7$ ns (Typ.)
($V_{CC} = 5$ V, 50 pF)
- Operation Voltage Range : $V_{CC(opr)} = 1.8 \sim 5.5$ V
- Supply Voltage Data Retention : $V_{CC} = 1.5 \sim 5.5$ V
- 5 V Tolerant Function
- Matches the Performance of TC74LCX Series when Operated at 3.3 V V_{CC}

MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

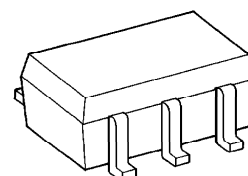
CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 6$	V
DC Input Voltage	V_{IN}	$-0.5 \sim 6$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim 6$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 50	mA
DC V_{CC} /Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	200	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	$^\circ\text{C}$
Lead Temperature (10 s)	T_L	260	$^\circ\text{C}$

TC7SZ08F



SSOP5-P-0.95

TC7SZ08FU



SSOP5-P-0.65A

Weight

SSOP5-P-0.95 : 0.016 g (Typ.)
 SSOP5-P-0.65A : 0.006 g (Typ.)

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● TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.

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DC ELECTRICAL CHARACTERISTICS

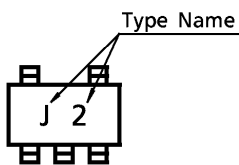
CHARACTERISTIC	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			1.8	$0.88 \times V_{CC}$	—	—	$0.88 \times V_{CC}$	—	V
				2.3~5.5	$0.75 \times V_{CC}$	—	—	$0.75 \times V_{CC}$	—	
Low-Level Input Voltage	V_{IL}			1.8	—	—	$0.12 \times V_{CC}$	—	$0.12 \times V_{CC}$	V
				2.3~5.5	—	—	$0.25 \times V_{CC}$	—	$0.25 \times V_{CC}$	
High-Level Output Voltage	V_{OH}	$V_{IN} = V_{IH}$	$I_{OH} = -100 \mu A$	1.8	1.7	1.8	—	1.7	—	V
				2.3	2.2	2.3	—	2.2	—	
				3.0	2.9	3.0	—	2.9	—	
				4.5	4.4	4.5	—	4.4	—	
			$I_{OH} = -8 \text{ mA}$	2.3	1.9	2.15	—	1.9	—	
			$I_{OH} = -16 \text{ mA}$	3.0	2.4	2.8	—	2.4	—	
			$I_{OH} = -24 \text{ mA}$	3.0	2.3	2.68	—	2.3	—	
			$I_{OH} = -32 \text{ mA}$	4.5	3.8	4.2	—	3.8	—	
Low-Level Output Voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 100 \mu A$	1.8	—	0	0.1	—	0.1	V
				2.3	—	0	0.1	—	0.1	
				3.0	—	0	0.1	—	0.1	
				4.5	—	0	0.1	—	0.1	
			$I_{OL} = 8 \text{ mA}$	2.3	—	0.1	0.3	—	0.3	
			$I_{OL} = 16 \text{ mA}$	3.0	—	0.15	0.4	—	0.4	
			$I_{OL} = 24 \text{ mA}$	3.0	—	0.22	0.55	—	0.55	
			$I_{OL} = 32 \text{ mA}$	4.5	—	0.22	0.55	—	0.55	
Input Leakage Current	I_{IN}	$V_{IN} = 5.5 \text{ V or GND}$		0~5.5	—	—	± 1	—	± 10	μA
Power Off Leakage Current	I_{OFF}	$V_{IN} \text{ or } V_{OUT} = 5.5 \text{ V}$		0.0	—	—	1	—	10	μA
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC} \text{ or GND}$		5.5	—	—	2	—	20	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3\text{ ns}$)

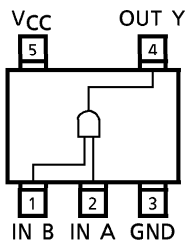
CHARACTERISTIC	SYMBOL	TEST CONDITION	Ta = 25°C				Ta = - 40~85°C		UNIT
			V _{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t _{PLH} t _{PHL}	C _L = 15 pF, R _L = 1 MΩ	1.8	2.0	5.2	10.0	2.0	10.5	ns
			2.5 ± 0.2	0.8	3.4	7.0	0.8	7.5	
			3.3 ± 0.3	0.5	2.6	4.7	0.5	5.0	
			5.0 ± 0.5	0.5	2.2	4.1	0.5	4.4	
		C _L = 50 pF, R _L = 500 Ω	3.3 ± 0.3	1.5	3.3	5.2	1.5	5.5	
			5.0 ± 0.5	0.8	2.7	4.5	0.8	4.8	
Input Capacitance	C _{IN}		0~5.5	—	4	—	—	—	pF
Power Dissipation Capacitance	C _{PD}	(Note 1)	3.3	—	20	—	—	—	pF
			5.5	—	25	—	—	—	

(Note 1) CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation.
 $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

MARKING



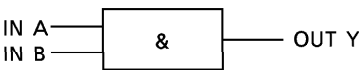
PIN ASSIGNMENT (TOP VIEW)



TRUTH TABLE

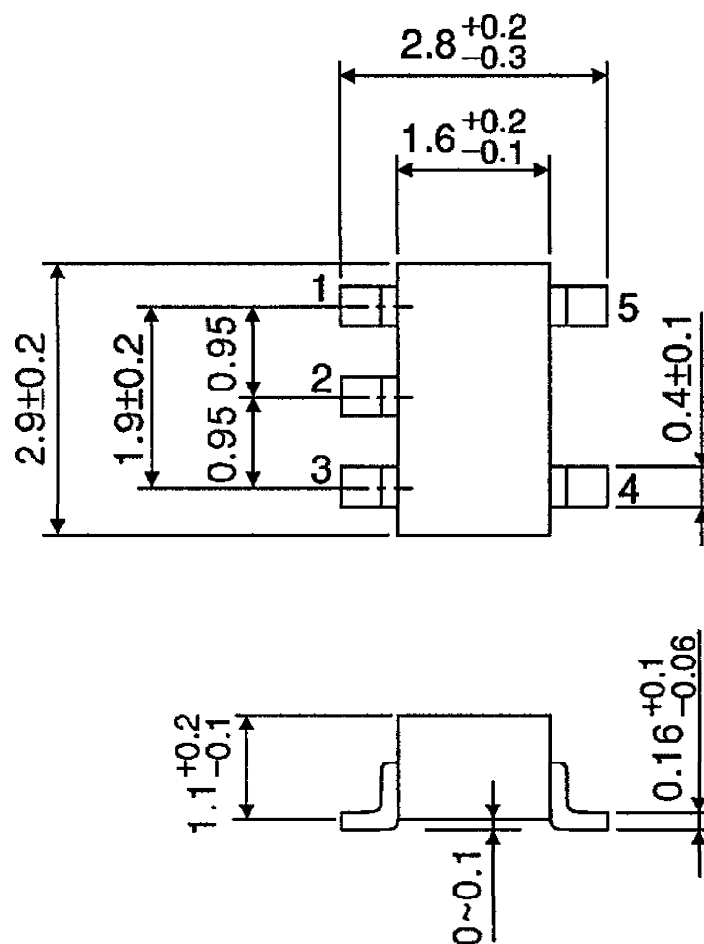
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

LOGIC DIAGRAM



OUTLINE DRAWING
SSOP5-P-0.95

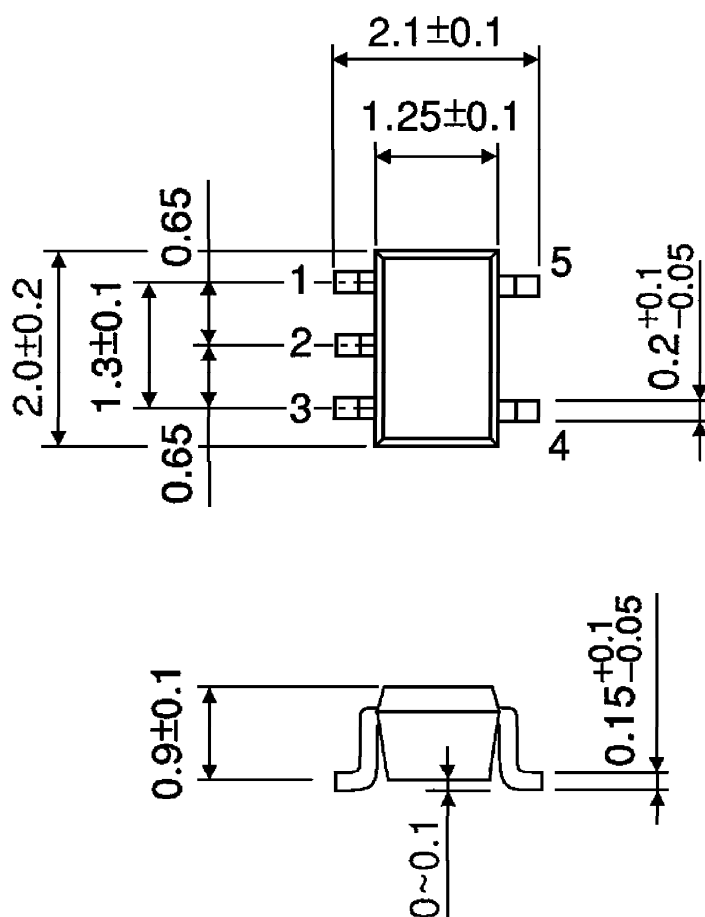
Unit : mm



Weight : 0.016 g (Typ.)

OUTLINE DRAWING
SSOP5-P-0.65A

Unit : mm



Weight : 0.006 g (Typ.)

Tape Packing Specifications for 5-pin Ultra Super-Mini (USV) Package

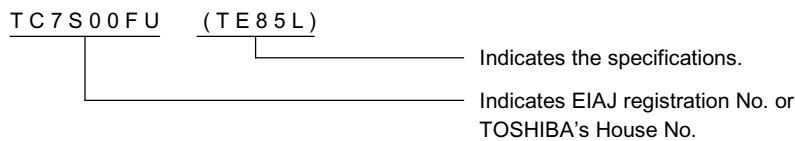
Scope

This specification provides the packaging requirements for 5-pin Ultra Super Mini type transistors, FETs, diodes, L-MOS logics for use in automatic placement machines.

1. Product Naming System

Type of package for shipment is classified by a symbol suffixed to a product name. The method of classification is as below. (this method, however, does not apply to products of which electrical characteristics differ from the TOSHIBA standard specifications.)

[Example]



2. Tape Dimensions

- 2.1 Accumulated pitch tolerance is ± 0.2 mm/10 pitch.
- 2.2 The tape material is plastic.
- 2.3 The tape dimensions are per Figure 1.

Unit: mm

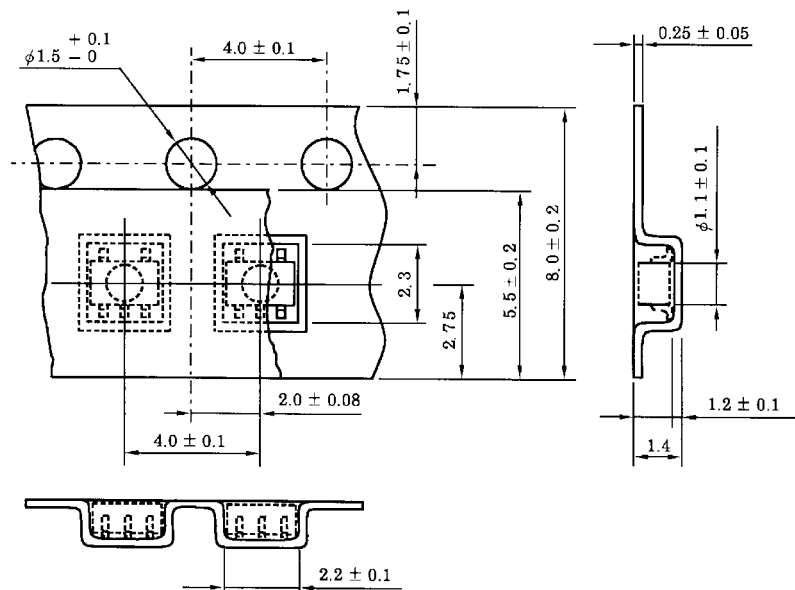


Figure 1

961001EAA1

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2.4 Related Matters

2.4.1 Missing Devices

Except for the leader and trailer portions of the tape there shall be no consecutive missing parts.
The maximum number of missing parts cannot exceed 0.2% per reel.

2.4.2 Electric Characteristics

Electric Characteristics of taping devices are shown in individual Technical Data.

3. Reel

3.1 The reel dimensions are per Figure 2.

Unit: mm

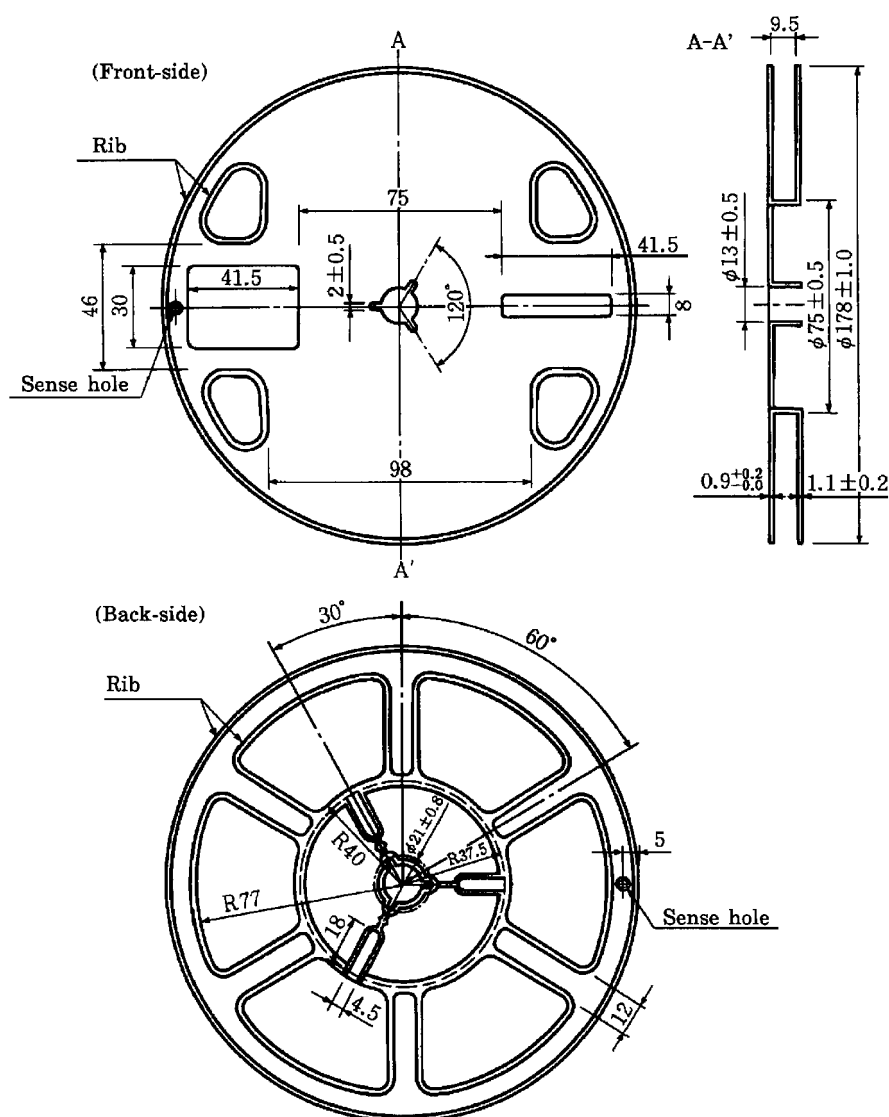


Figure 2

3.2 The reel material is plastic.

4. Packed System

4.1 Packed parts quantity

3000 pcs per reel.

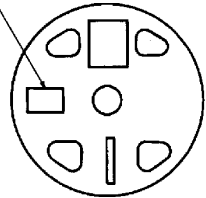
4.2 Indication System

[Example] TC7S00FU (TE85L)

P/N:

TYPE	TC7S00FU		
ADDC	(TE85L)	Q'TY	3,000 pcs
NOTE			

Indicating label position



On special occasion ADD CODE, PART No. etc. are often indicated in indicating label of the reel.

4.3 Part orientation in the carrier tape shall be as shown in Figure 3.

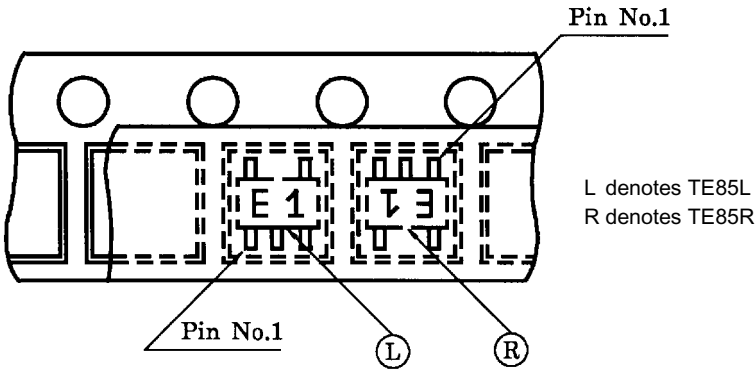
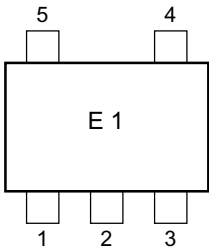


Figure 3

Pin 1 exists on the left below of the marking.

[Example] Top View



5. The leader and trailer portion of the tape shall be as shown in Figure 4.

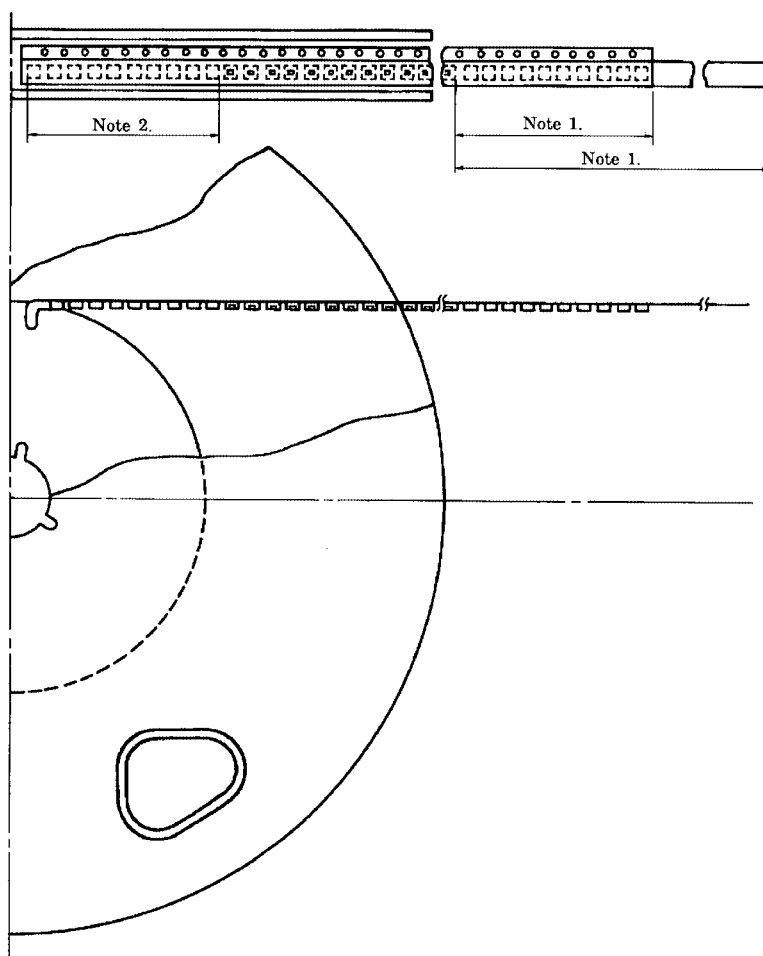


Figure 4

Note1: The leader portion shall consist of a piece of cover tape minimum length of 300 mm and a piece of carrier tape with empty portion of 100 mm minimum.

Note2: The trailer portion shall consist of an empty carrier of more than 10 cavities.