DATA SHEET

SAA8103
Pulse Pattern Generator for Frame Transfer CCD (PPGFT)

Objective specification
File under Integrated Circuits, IC02

2001 Oct 22

Philips
Semiconductors

PHILIPS

Pulse Pattern Generator for Frame Transfer CCD (PPGFT)

SAA8103

CONTENTS

Pulse Pattern Generator for Frame Transfer CCD (PPGFT)

SAA8103

1 FEATURES

- Sync signal generator
- Supports progressive scan operation
- Supports monitoring function
- Supports electronic shutter function
- Supports Frame Transfer CCD (FXA, FTF and FTT) 8×8-kbyte pixels (maximum)
- Supports 1, 2 and 4 output functions with Full Frame CCD type sensor
- Generates the system clock for signal processing
- Base oscillation from 6 to 28 MHz
- I^2C-bus control.

2 APPLICATIONS

- CCD camera
- Digital still camera.

3 GENERAL DESCRIPTION

The SAA8103 is a pulse pattern generator for the Frame Transfer CCD image sensors: FXA1012, FXA1013, FXA1022, FXA1004, FTF2020, FTF3020 and FTT1010 as well as for the front-end analog processing and signal processing circuit.

The circuit generates drive pulses for the CCD, sample-hold pulses for Correlated Double Sampling (CDS), clamp pulses and sync signals.

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDDx}	digital supply voltages: V_{DDD1}, V_{DDD2}, V_{DDD3}, V_{DDD4} and $V_{DD(OSC)}$	3.0	3.3	3.6	V
V_{DDAx}	analog supply voltages: $V_{DDA(BUF1)}$, $V_{DDA(BUF2)}$, $V_{DDA(BUF3)}$, $V_{DDA(DLL1)}$ and $V_{DDA(DLL2)}$	3.0	3.3	3.6	V
$I_{P(tot)}$	total power supply current (f_{CLK} = 25 MHz)	–	65	–	mA
V_{IL}	LOW-level input voltages	–	–	0.8	V
V_{IH}	HIGH-level input voltages	2.3	–	V_{DD}	V
V_{OL}	LOW-level output voltages	–	–	0.5	V
V_{OH}	HIGH-level output voltages	2.3	–	V_{DD}	V
T_{amb}	operating ambient temperature range	–20	+25	+70	°C

5 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA8103HL	LQFP64	plastic low profile quad flat package; 64 leads; body $10 \times 10 \times 1.4$ mm	SOT314-2

6 BLOCK DIAGRAMS

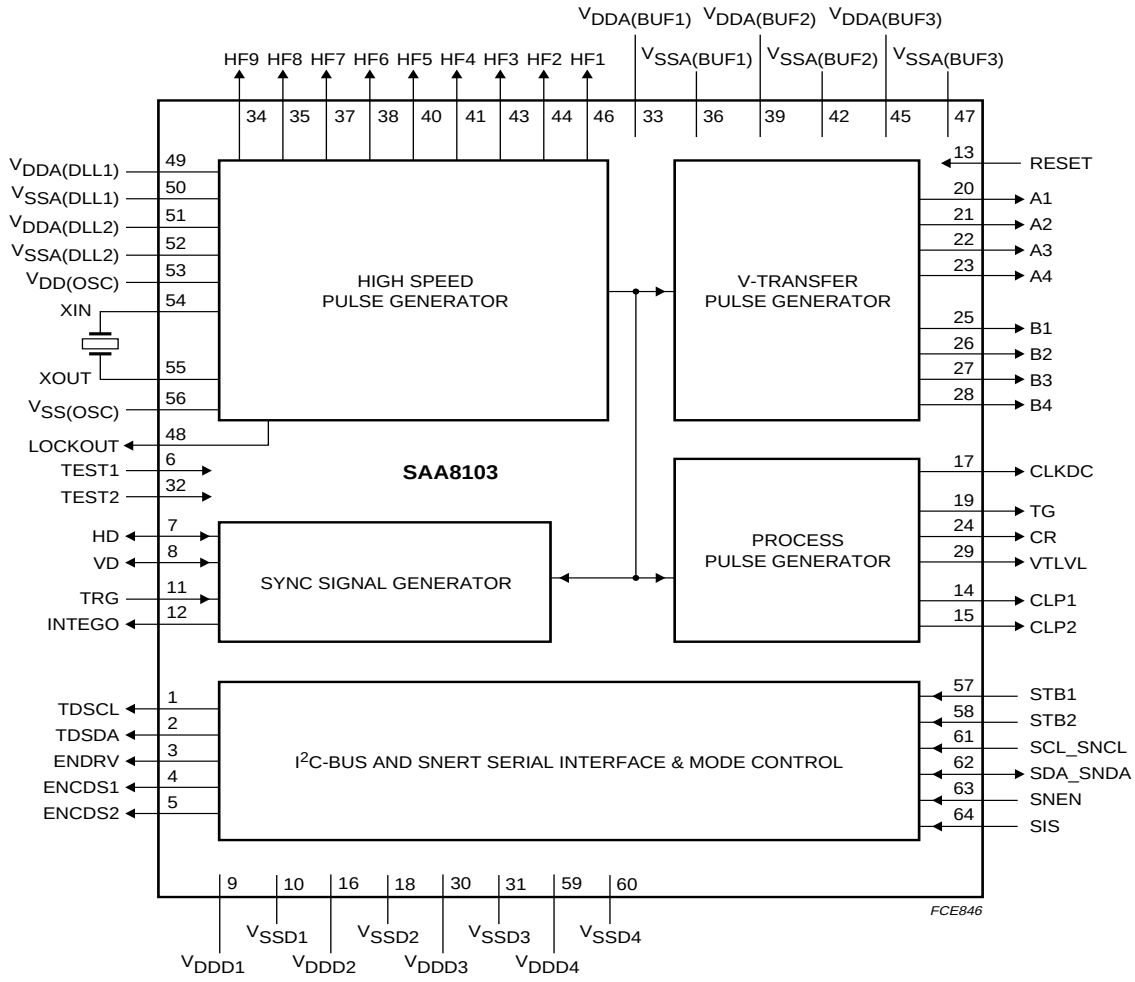
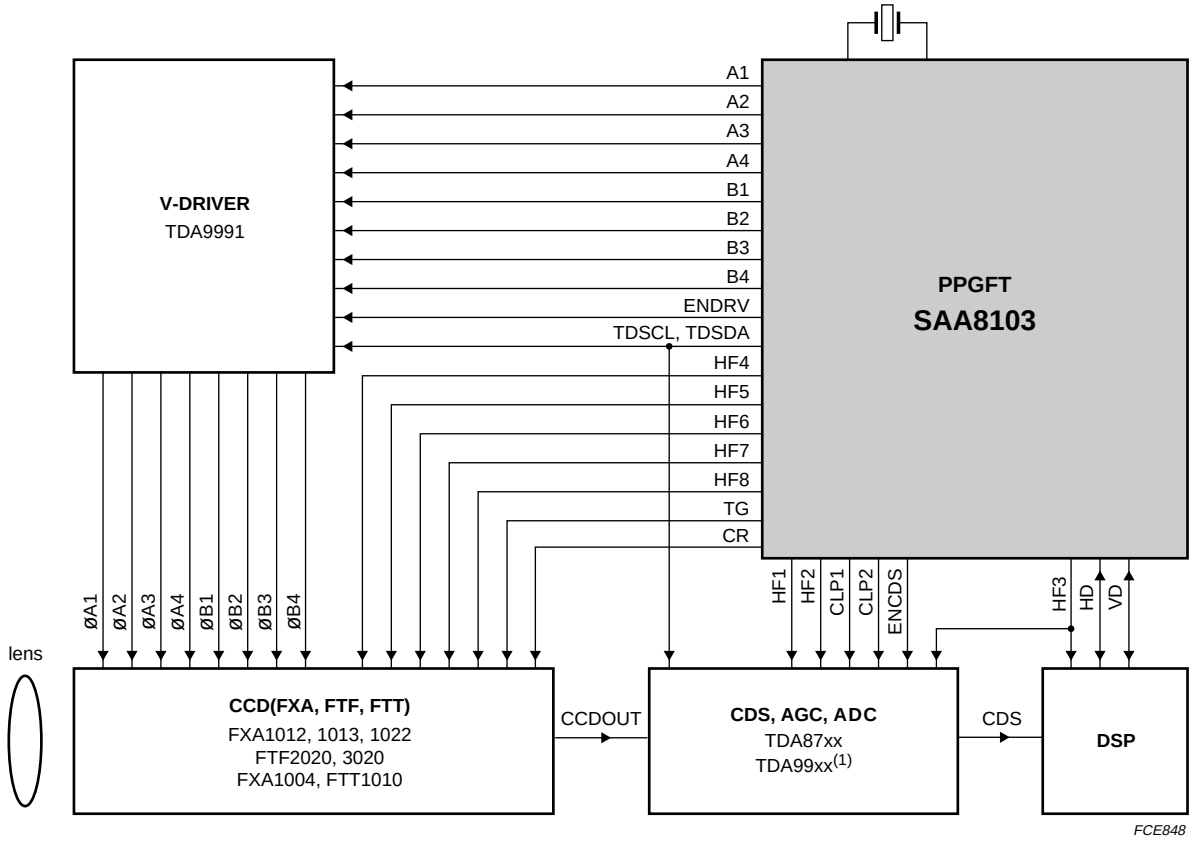


Fig.1 Block diagram.



(1) TDA87xx = TDA8783; TDA8784; TDA8786 and TDA8787A
TDA99xx = TDA9952; TDA9956; TDA9962; TDA9964 and TDA9965

Fig.2 System block diagram.

7 PINNING INFORMATION

7.1 Pinning

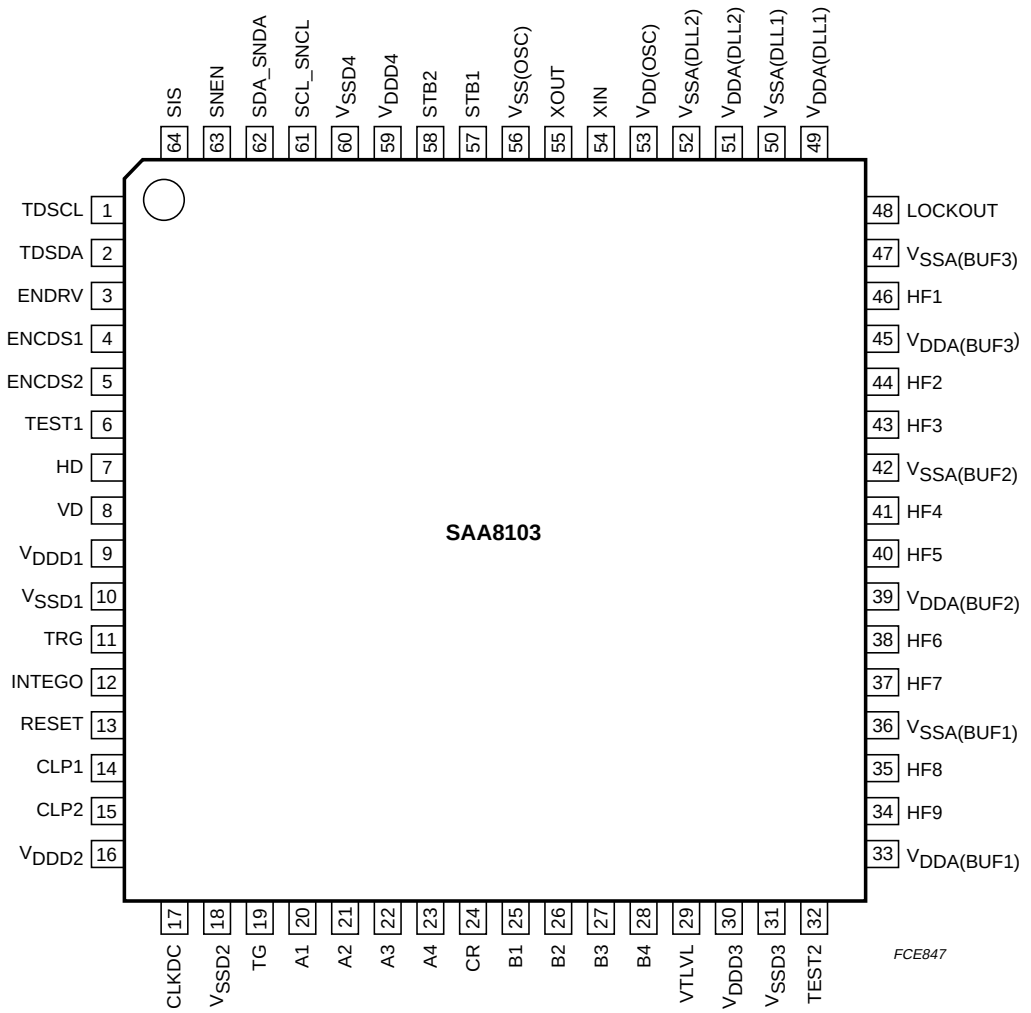


Fig.3 Pin configuration.

7.2 Pin description

Table 1 Pin description for LQFP64 package

SYMBOL	PIN	I/O	DESCRIPTION
TDSCL	1	O	serial interface clock output for CDS/ADC and V-driver
TDSDA	2	O	serial interface data output for CDS/ADC and V-driver
ENDRV	3	O	serial interface enable output for V-driver
ENCDS1	4	O	serial interface enable output 1 for CDS/ADC
ENCDS2	5	O	serial interface enable output 2 for CDS/ADC
TEST1	6	I	test input 1; normally connected to ground
HD	7	I/O	horizontal drive signal input or output; alternative function HREF signal output is controlled by the serial interface; see Chapter 11, address 12
VD	8	I/O	vertical drive signal input or output; alternative function VREF signal output is controlled by the serial interface; see Chapter 11, address 12
V_{DDD1}	9	supply	digital supply voltage 1 for core
V_{SSD1}	10	supply	digital ground 1 for core
TRG	11	I	trigger signal input
INTEGO	12	O	integration time signal output
RESET	13	I	power-on reset, normally connected to ground
CLP1	14	O	optical black clamp control pulse output
CLP2	15	O	clamp control pulse output for the Analog-to-Digital Convertor (ADC)
V_{DDD2}	16	supply	digital supply voltage 2
CLKDC	17	O	clock signal output (for the DC-to-DC convertor of TDA9991)
V_{SSD2}	18	supply	digital ground 2
TG	19	O	transfer gate pulse output
A1	20	O	clock output 1 for CCD vertical register drive
A2	21	O	clock output 2 for CCD vertical register drive
A3	22	O	clock output 3 for CCD vertical register drive
A4	23	O	clock output 4 for CCD vertical register drive
CR	24	O	charge reset pulse output
B1	25	O	clock output 1 for CCD vertical register drive
B2	26	O	clock output 2 for CCD vertical register drive
B3	27	O	clock output 3 for CCD vertical register drive
B4	28	O	clock output 4 for CCD vertical register drive
VTLVL	29	O	vertical transport level pulse output
V_{DDD3}	30	supply	digital supply voltage 3
V_{SSD3}	31	supply	digital ground 3
TEST2	32	I	test input 2; normally connected to ground
$V_{DDA(BUF1)}$	33	supply	analog supply voltage for output buffer 1
HF9	34	O	high frequency output 9
HF8	35	O	high frequency output 8
$V_{SSA(BUF1)}$	36	supply	analog ground for output buffer 1
HF7	37	O	high frequency output 7

SYMBOL	PIN	I/O	DESCRIPTION
HF6	38	O	high frequency output 6
$V_{DDA(BUF2)}$	39	supply	analog supply voltage for output buffer 2
HF5	40	O	high frequency output 5
HF4	41	O	high frequency output 4
$V_{SSA(BUF2)}$	42	supply	analog ground for output buffer 2
HF3	43	O	high frequency output 3
HF2	44	O	high frequency output 2
$V_{DDA(BUF3)}$	45	supply	analog supply voltage for output buffer 3
HF1	46	O	high frequency output 1
$V_{SSA(BUF3)}$	47	supply	analog ground for output buffer 3
LOCKOUT	48	O	lock indication of Delayed Locked Loop (DLL)
$V_{DDA(DLL1)}$	49	supply	analog supply voltage for DLL1 (core)
$V_{SSA(DLL1)}$	50	supply	analog ground for DLL1 (core)
$V_{DDA(DLL2)}$	51	supply	analog supply voltage for DLL2
$V_{SSA(DLL2)}$	52	supply	analog ground for DLL2
$V_{DD(OSC)}$	53	supply	digital supply voltage for crystal oscillator
XIN	54	I/O	inverter input for crystal oscillator
XOUT	55	I/O	inverter output for crystal oscillator
$V_{SS(OSC)}$	56	supply	digital ground for crystal oscillator
STB1	57	I	standby control function inputs; see Section 9.4
STB2	58	I	
V_{DDD4}	59	supply	digital supply voltage 4
V_{SSD4}	60	supply	digital ground 4
SCL_SNCL	61	I	I^2C-bus/SNERT serial interface clock input
SDA_SNDA	62	I/O	I^2C-bus/SNERT serial interface data input/output; 8 mA and 400 kHz
SNEN	63	I	SNERT enable input
SIS	64	I	I^2C-bus/SNERT selection

8 FUNCTIONAL DESCRIPTION

The SAA8103 is a drive pulse generator for the FXA1004, FXA1012, FXA1013, FXA1022, FTF2020, FTF3020 and the FTT1010. The SAA8103 also drives the CDS, ADC front-end, V-driver and the Digital Signal Processor (DSP). The system block diagram is shown in Fig.2.

The SAA8103 generates horizontal and vertical drive signals, summing and reset gate pulses for each CCD, sample-hold pulses and clamp pulses for the front-end devices TDA99xx and TDA87xx(1), and also generates sync signals HD and VD and the reference signals HREF and VREF for the DSP. The SAA8103 can also take sync signals HD and VD as external inputs, the drive signals generated will then be synchronized to these signals.

The SAA8103 is designed to operate with an 8192-line (maximum) $\times$ 8192-pixel (maximum) RGB Bayer CCD (FXA, FTF and FTT). Progressive scan and sub-sampling modes for these CCDs can be used.

The device supports three different modes for the data read-out of each CCD: Normal mode, Shot mode and Preview mode. The SAA8103 also supports electronic shutter function and will provide exact settings of shutter speed and exposure time.

The drive signals for CCD are generated from the main oscillator and range from 6 to 28 MHz. The drive signals are generated by a programmable generator from the main oscillator. The vertical drive signals are provided for the TDA9991, horizontal drive signals are provided for the CCD directly or H-driver, sample-hold pulses and clamp pulses are provided for the TDA99xx or TDA87xx, sync signals HD, VD and reference signals HREF and VREF are provided for the DSP.

The drive pulses are controlled by a microcontroller via one of the serial interfaces (I^2C-bus or SNERT). The SAA8103 takes address and data from the I^2C-bus or SNERT, and decodes these inputs for internal logic. It also decodes these inputs for the SNERT interface of the TDA99xx, TDA87xx and TDA9991.

The basic digital camera system consists of a CCD image sensor, a vertical driver and a Pulse Pattern Generator (PPG) for the CCD, an analog front-end (CDS, AGC and ADC) and Digital Signal Processor.

The high resolution digital camera system can be built using the FTF3020, TDA9965 and TDA9991 devices.

(1) TDA99xx = TDA9952; TDA9956; TDA9962; TDA9964; TDA9965.
TDA87xx = TDA8783; TDA8784; TDA8786; TDA8787A

9 OPERATING MODES

For Full Frame CCD and Frame Transfer CCD there are two modes for data read-out: Shot mode and Preview mode. Shot mode is used to take an image using an external trigger signal; e.g. camera shutter. Preview mode is used to take an image continuously with a fixed (preset) integration; e.g. to show an image on the LCD display of a Digital Still Camera (DSC).

9.1 Full Frame CCD

In the Shot mode, the SAA8103 takes the external input signal TRG, as the trigger signal. After the rising edge of TRG, the charge reset pulses (CR) are generated for the appropriate period. Integration time is held until the falling edge of the TRG signal. A drive signal is generated in each VD period but is not issued until the next event of the TRG signal.

In the Preview mode, the SAA8103 generates a drive signal in every frame. The Preview mode it is not influenced by the TRG signal. The integration time is controlled using the INTTIME command; see Chapter 11, addresses 1 and 2.

The Shot mode and Preview mode for Full Frame CCD is shown in Fig.4.

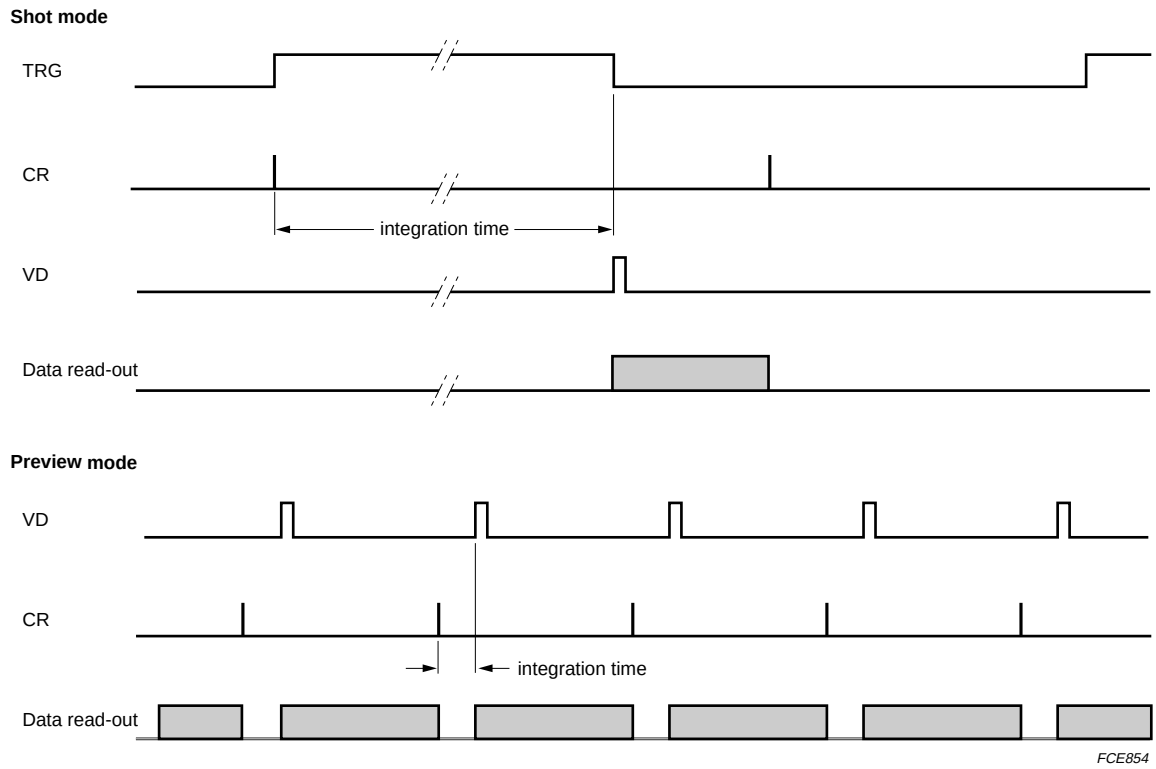


Fig.4 Data read-out of Full Frame CCD.

9.2 Frame Transfer CCD

In the Shot mode, the SAA8103 takes the external input signal TRG, as the trigger signal. After the rising edge of TRG the reset gate pulses (CR) are generated for the appropriate period. Integration time is held until the falling edge of TRG. A drive signal is generated in each VD period but is not issued until the next event of the TRG signal.

In the Preview mode, the SAA8103 generates a drive signal in every frame. The Preview mode is not influenced by the TRG signal.

The integration time is controlled using the INTTIME and EXPTIME command; see Chapter 11, addresses 1, 2, 3 and 4.

The Shot mode and Preview mode for Frame Transfer CCD is shown in Fig.5.

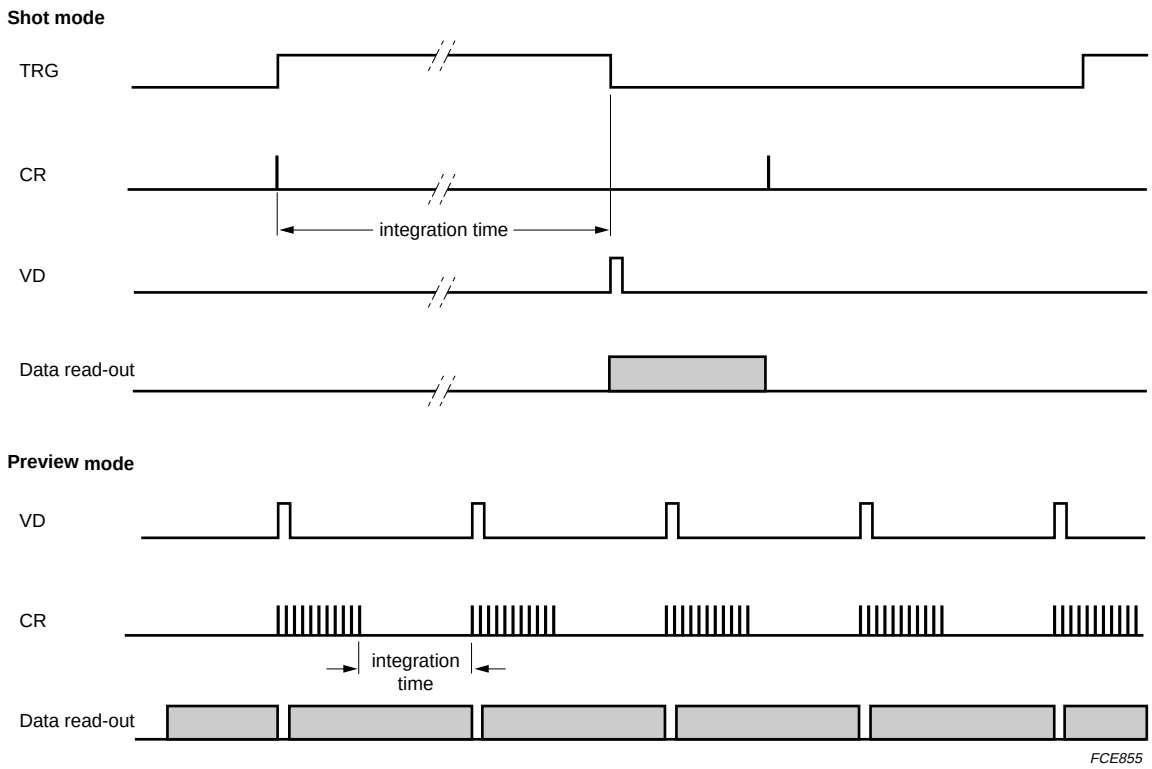


Fig.5 Data read-out of Frame Transfer CCD.

9.3 Standby control function

The SAA8103 has two external inputs STB1 and STB2 which are used to select the Standby control mode, as shown in Table 2.

Table 2 Selection of Standby control mode

STB2	STB1	MODE	CONDITIONS
0	0	Normal	HFEN1 = ON; HFEN2 = ON; VFEN = ON
0	1	Standby mode 1	HFEN1 = OFF; HFEN2 = ON; VFEN = ON
1	0	Standby mode 2	HFEN1 = ON; HFEN2 = OFF; VFEN = ON
1	1	Standby mode 3	HFEN1 = OFF; HFEN2 = OFF; VFEN = OFF

9.4 Standby modes

9.4.1 STANDBY MODE 1

When Standby mode 1 is selected, the internal signal HFEN1 is inactive (OFF-state) and the data for HF1 to HF3 is masked. Consequently, the outputs of HF1 to HF3 are held LOW when Standby mode 1 is active.

9.4.2 STANDBY MODE 2

When Standby mode 2 is selected, the internal signal HFEN2 is inactive (OFF-state) and the data for HF4 to HF9 is masked. Consequently, the outputs HF4 to HF9 are held LOW when Standby mode 2 is active.

9.4.3 STANDBY MODE 3

When Standby mode 3 is selected, the internal signals HFEN1, HFEN2 and VFEN are inactive (OFF-state) and the data for HF1 to HF9 is masked. Consequently, the outputs HF1 to HF9 are held LOW when Standby mode 3 is active. The effect of VFEN being inactive (OFF-state) is described below.

Figure 7 shows the effect of Standby mode 3 on the Preview mode. When the Standby mode 3 is applied on Preview mode, both the V_counter and H_counter are halted. The output signals hold their last state until Standby mode 3 is released. All output signals operate continuously after the release of Standby mode 3. This situation also applies when Standby mode 3 is selected whilst in Shot mode.

Figure 8 shows the effect of an operation change from Preview mode to Shot mode during Standby mode 3. In this situation, both the V_counter and H_counter are reset by the timing of Shot mode detection, and all output signals are reset. The operation is changed to Idle state after the release from Standby mode 3. The SAA8103 is now ready to accept the TRIG signal for Shot mode operation.

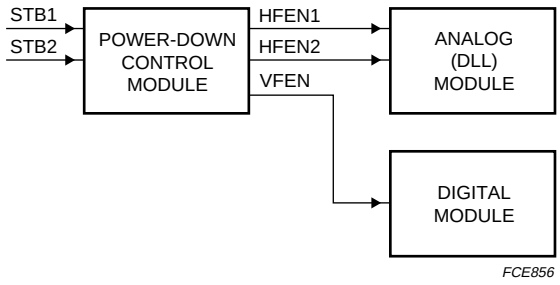


Fig.6 CCD standby control block diagram.

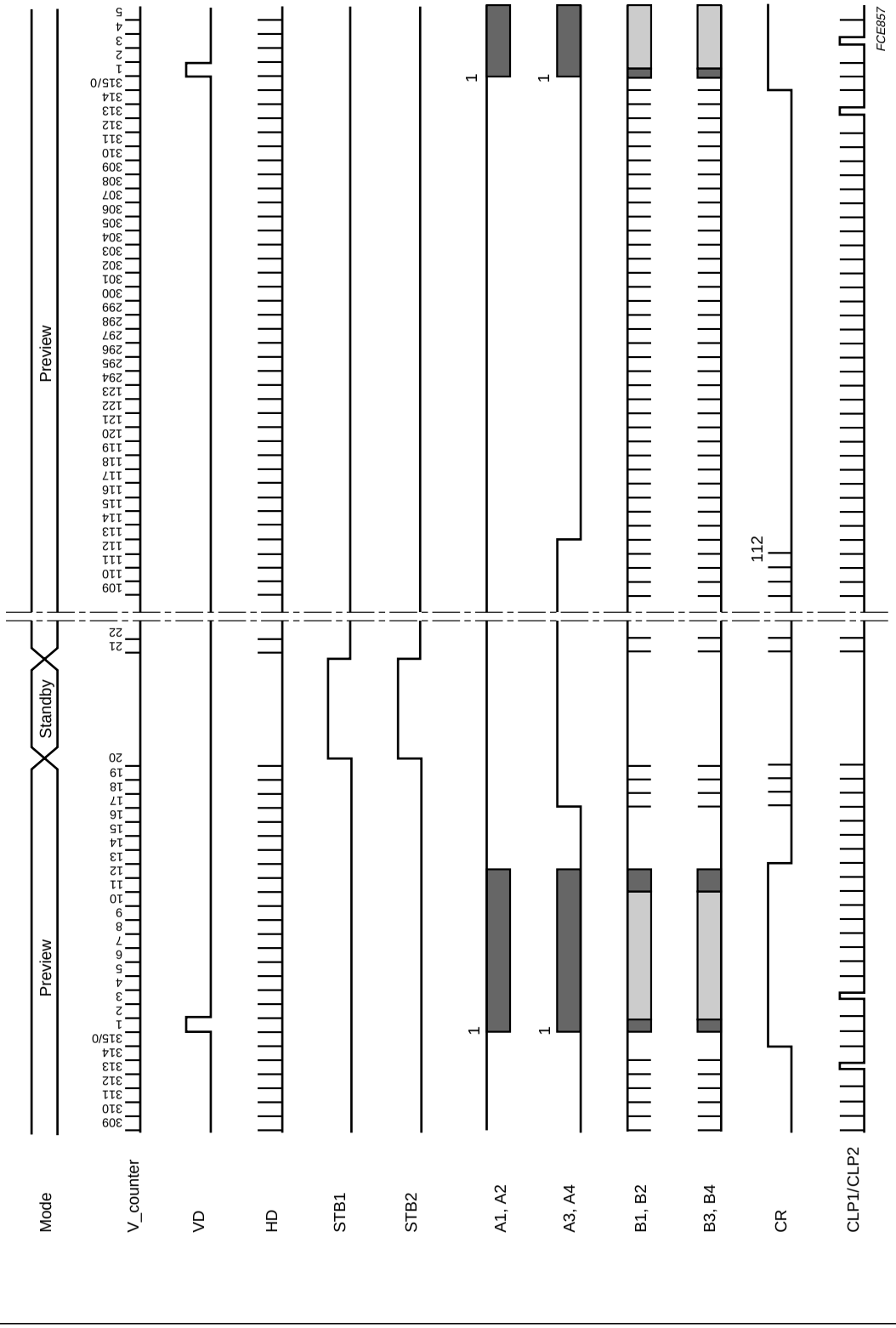


Fig.7 FT CCD V-driver timing in Preview mode with Standby mode 3.

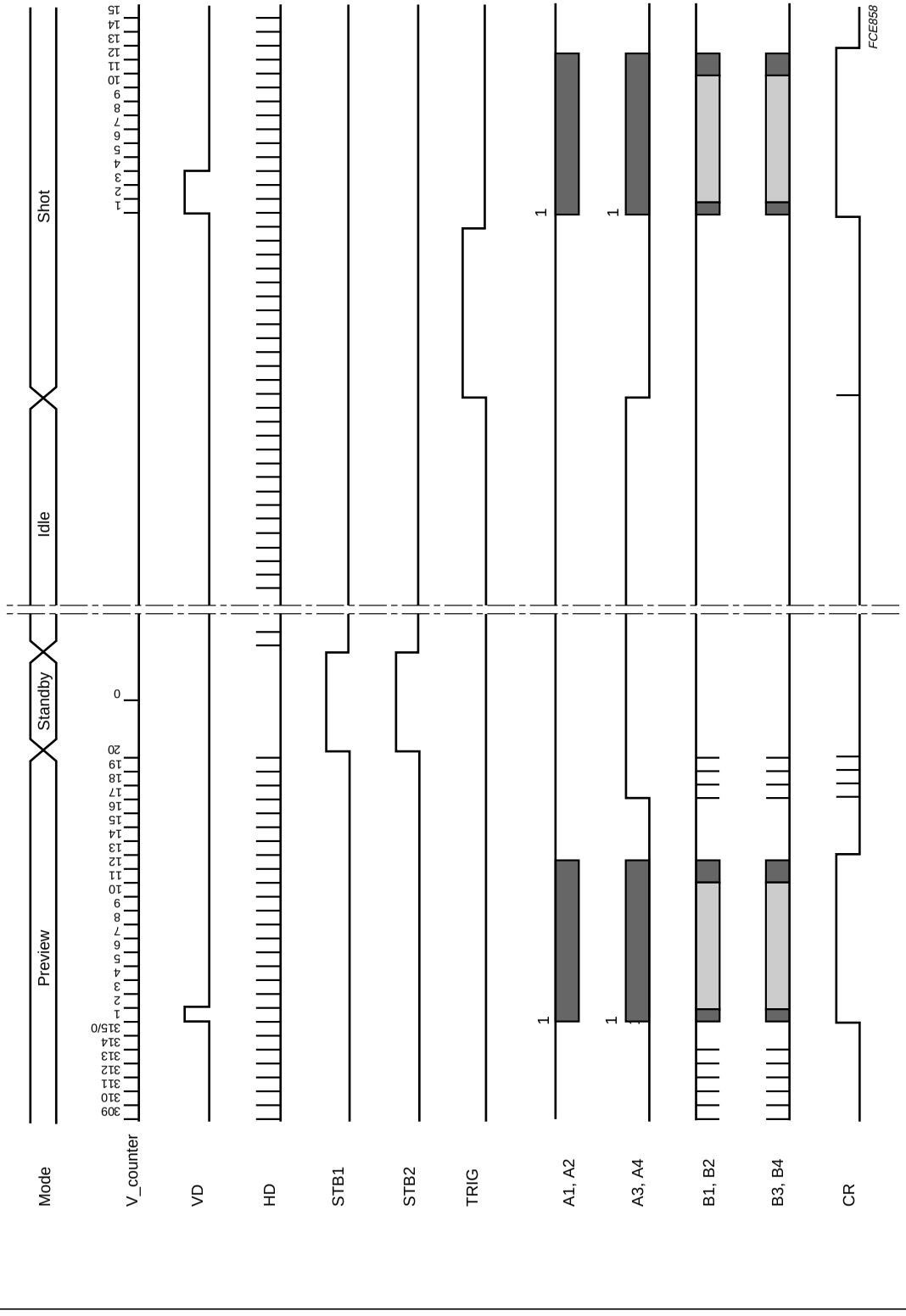


Fig.8 FT CCD V-driver timing during change from Preview to Shot mode with Standby mode 3.

10 SERIAL INTERFACES

The SAA8103 has two means by which it can communicate with a microcontroller: the I²C-bus serial interface and the SNERT serial interface. The selection of the serial interface is determined by the state of the signal on the SIS pin; see Table 3.

The CDS/ADC1, CDS/ADC2 and the V-driver are programmed by a series of commands sent via one of these interfaces. The command list is given in Table 4. Address and data decoding for the internal logic is carried out within the serial interface block.

The CCD transfer pattern data is sent to the serial interface block and is held in one of two registers: Register 0 or Register 1. Register 0 is used to store data when the device is in the Shot mode. Register 1 is used to store data when the device is in the Preview mode. Consequently, before any data can be sent, Register 0 or Register 1 must be selected by writing the appropriate data to address 200. The transfer pattern signal will be loaded by the data read out mode and the TRG signal input. The signal flow between the SAA8103 and the front-end ICs is shown in Fig.9.

Table 3 Serial interface selection

SIS	SDA_SNDA	SCL_SNCL	SNEN	INTERFACE SELECTED
0	I²C-bus data	I²C-bus clock	–	I²C-bus; slave address 4EH
1	SNERT data	SNERT clock	SNERT enable	SNERT

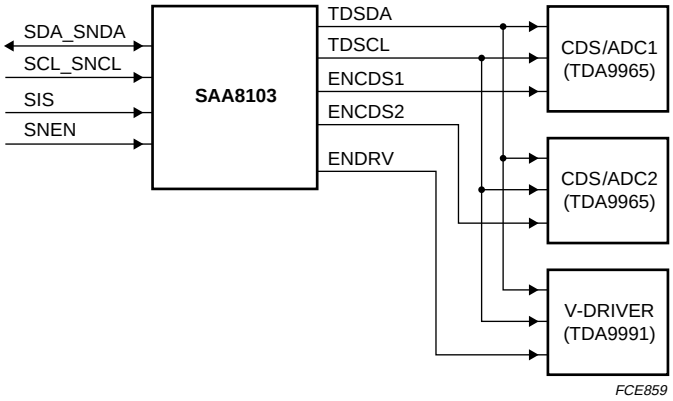


Fig.9 Signal flow between the SAA8103 and front-end ICs.

10.1 Control for V-driver (TDA9991) and CDS or ADC

The SAA8103 can control the V-driver (TDA9991) and the CDS/ADC (TDA99xx and TDA87xx) via the I²C-bus serial interface.

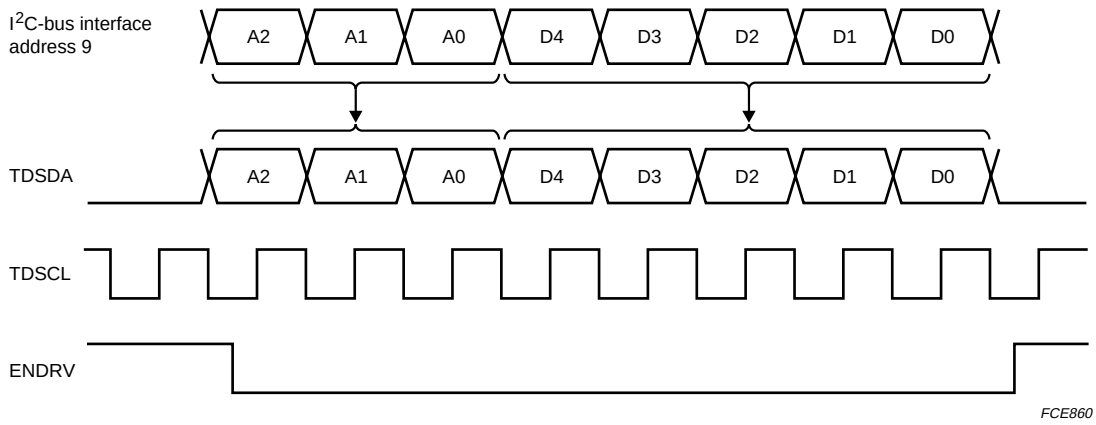


Fig.10 Serial interface for V-driver (TDA9991).

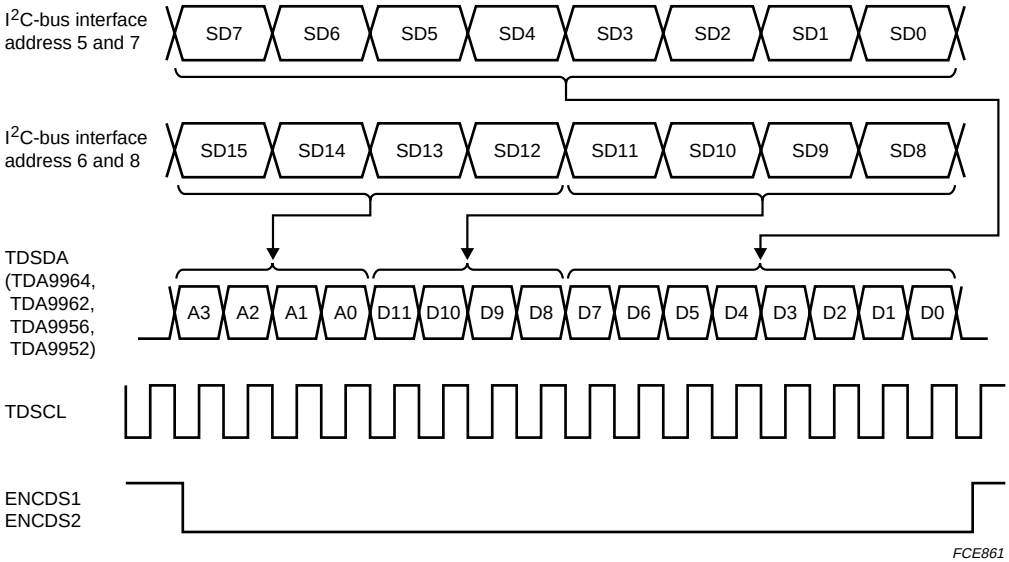


Fig.11 Serial interface timing for CDS or ADC (TDA9964, 62, 56 and 52).

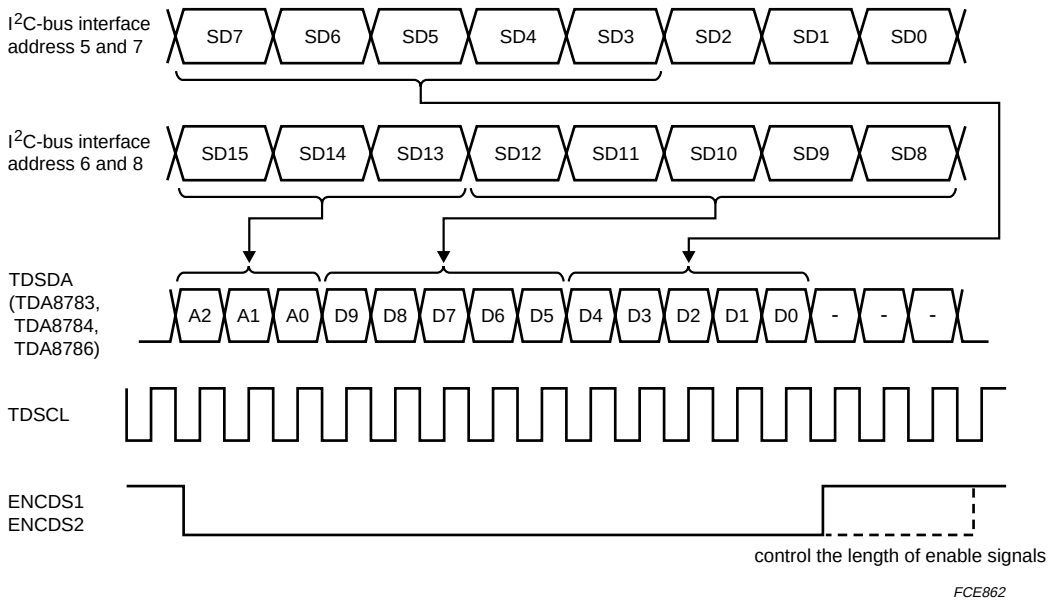


Fig.12 Serial interface timing for CDS or ADC (TDA8783, 84 and 86).

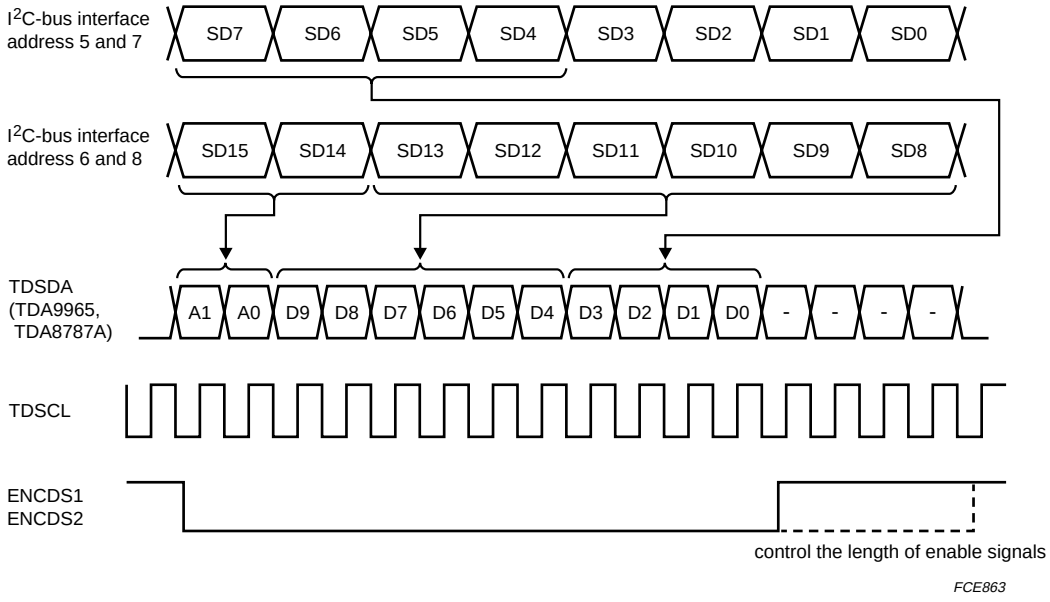


Fig.13 Serial interface timing for CDS or ADC (TDA9965 and TDA8787A).

11 COMMAND LIST

Table 4 The command list for the serial interfaces: I²C-bus and SNERT

ADDRESS	COMMAND BIT	COMMAND DESCRIPTION
Operating settings		
0(1)	0	**Operational mode selection.** 0 = Shot mode selected; default state 1 = Preview mode selected
	1	**CCD type selection.** 0 = FT type CCD 1 = FF type CCD; default state
	2 to 3	These 2 bits are reserved.
	4	**Sub-sampling function enable.** 0 = sub-sampling OFF in FT type CCD; default state 1 = sub-sampling ON in FT type CCD
	5	**Electronic shutter setting (INTTIMEON).** 0 = integration time is ON; default state 1 = integration time is OFF
1(1)	7 to 0	**Integration time setting (INTTIME).** The data provided by these two commands is combined to form the 13-bit integration time setting. The integration time setting has a range from 0 to 8191; the default value is 3. It is calculated by the following expression: Integration time = setting value × HD period
2(1)	4 to 0	
3(1)	7 to 0	**Exposure time setting for FT CCD (EXPTIME).** The data provided by these two commands is combined to form the 13-bit exposure time setting. The exposure time setting has a range from 0 to 8191; the default value is 3. It is calculated by the following expression: Exposure time = VD period − (setting value × HD period)
4(1)	4 to 0	

ADDRESS	COMMAND BIT	COMMAND DESCRIPTION
Setting address, data and enable for serial I/F of analog preprocessing		
5(1)	7 to 0	**Serial data setting for CDS1 and ADC1.** The data provided by these two commands is combined to form the 16-bit serial data setting. The data written to address 5 provides serial data SD7 to SD0. The data written to address 6 provides serial data SD15 to SD8. The default value of both commands is 0.
6(1)	7 to 0	
7(1)	7 to 0	**Serial data setting for CDS2 and ADC2.** The data provided by these two commands is combined to form the 16-bit serial data setting. The data written to address 7 provides serial data SD7 to SD0. The data written to address 8 provides serial data SD15 to SD8. The default value of both commands is 0.
8(1)	7 to 0	
9(1)	4 to 0	**Data setting for V-driver.** These 5 bits (D4 to D0) provide the data setting for the V-driver. The default value is 0.
	7 to 5	**Address setting for V-driver.** These 3 bits (A2 to A0) provide the address for the V-driver. The default value is 0.
10(1)	7 to 0	**Assign the division value of TDSCL generator for TDSCL output (DIVTDSCL).** These 8 bits determine the division value for the TDSCL generator. The default value is 3.
11(1)	0	**Control signal of serial interface data output (TDSDA) for CDS or ADC.** 0 = enable; default state 1 = disable
	1	**Control signal of serial interface clock output (TDSCL) for CDS or ADC.** 0 = enable; default state 1 = disable
	4	**Enable signal for CDS1 and ADC1 (ENCDS1) enable control (CD1ENBON).** 0 = enable; default state 1 = disable
	5	**Enable signal for CDS2 and ADC2 (ENCDS2) enable control (CD2ENBON).** 0 = enable; default state 1 = disable
	6	**Enable signal for V-driver (ENDRV) enable control (DRVENBON).** 0 = enable; default state 1 = disable
	7	**Control signal for 3-wire interface (GATE3WON).** 0 = enable; default state 1 = disable

ADDRESS	COMMAND BIT	COMMAND DESCRIPTION
12[1]	7 to 4	**Control the length of enable signals for ENCDS1, ENCDS2 and ENDRV.** 0000 = 12 bits are generated for CDS; default state 0010 = 13 bits are generated for CDS 0100 = 14 bits are generated for CDS 0110 = 15 bits are generated for CDS 1000 = 16 bits are generated for CDS 0001 = 8 bits are generated for V-driver; default state 0011 = 9 bits are generated for V-driver 0101 = 10 bits are generated for V-driver 0111 = 11 bits are generated for V-driver 1001 = 12 bits are generated for V-driver 1011 = 13 bits are generated for V-driver 1101 = 14 bits are generated for V-driver 1111 = 15 bits are generated for V-driver
	2 to 0	**HD, VD and HREF and VREF polarity (HDVDINT).** 000 = internal mode; negative HD and VD output 001 = internal mode; negative HREF and VREF output 010 = internal mode; positive HD and VD output; default state 011 = internal mode; positive HREF and VREF output 100 = external mode; negative HD input and negative VD output 101 = external mode; negative HD and VD inputs 110 = external mode; positive HD input and positive VD output 111 = external mode; positive HD and VD inputs
Setting the start and stop points for process timing		
13	7 to 0	**Horizontal Sync period (HS).** The data provided by these two commands is combined to form the 13-bit Horizontal Sync period setting. The data written to address 13 provides data D7 to D0. The data written to address 14 provides data D12 to D8. The Horizontal Sync period setting has a range from 0 to 8191. The default value is 3487.
14	4 to 0	
15	7 to 0	**Vertical Sync period (VS).** The data provided by these two commands is combined to form the 13-bit Vertical Sync period setting. The data written to address 15 provides data D7 to D0. The data written to address 16 provides data D12 to D8. The Vertical Sync period setting has a range from 0 to 8191. The default value is 2060.
16	4 to 0	
17	7 to 0	**HD stop (HDSTP)**. The HD stop setting has a range from 0 to 255. The default value is 4. The HD stop value is calculated as shown below. HD stop point = 2 × assigned value
18	7 to 0	**VD stop (VDSTP).** The VD stop setting has a range from 0 to 255. The default value is 4. The VD stop value is calculated as shown below. VD stop point = 2 × assigned value

ADDRESS	COMMAND BIT	COMMAND DESCRIPTION
19	7 to 0	**HREF start (HREFSTR).** The HREF start setting has a range from 0 to 255. The default value is 4. The HREF start value is calculated as shown below. HREF start point = 2 × assigned value
20	7 to 0	**HREF stop (HREFSTP).** The data provided by these two commands is combined to form the 13-bit HREF stop setting. The data written to address 20 provides data D7 to D0. The data written to address 21 provides data D12 to D8. The HREF stop setting has a range from 0 to 8191. The default value is 0.
21	4 to 0	
22	7 to 0	**VREF start (VREFSTR).** The data provided by these two commands is combined to form the 13-bit VREF start setting. The data written to address 22 provides data D7 to D0. The data written to address 23 provides data D12 to D8. The VREF start setting has a range from 0 to 8191. The default value is 4.
23	4 to 0	
24	7 to 0	**VREF stop (VREFSTP).** The data provided by these two commands is combined to form the 13-bit VREF stop setting. The data written to address 24 provides data D7 to D0. The data written to address 25 provides data D12 to D8. The VREF stop setting has a range from 0 to 8191. The default value is 0.
25	4 to 0	
Setting the start and stop points for internal signal SSC		
26	7 to 0	**SSC start (SSCSTR).** The SSC start setting has a range from 0 to 255. The default value is 0. The SSC start value is calculated as shown below. SSC start point = 2 × assigned value
27	7 to 0	**SSC stop (SSCSTP).** The data provided by these two commands is combined to form the 13-bit SSC stop setting. The data written to address 27 provides data D7 to D0. The data written to address 28 provides data D12 to D8. The SSC stop setting has a range from 0 to 8191. The default value is 360.
28	4 to 0	
Setting the start and stop points for clamp timings		
29	7 to 0	**Horizontal direction at the left clamp pulse 1 start (HLCLPSTR1).** The data provided by these two commands is combined to form the 13-bit HLCLPSTR1 setting. The data written to address 29 provides data D7 to D0. The data written to address 30 provides data D12 to D8. The HLCLPSTR1 setting has a range from 0 to 8191. The default value is 371.
30	4 to 0	
31	7 to 0	**Horizontal direction at the left clamp pulse 1 stop (HLCLPSTP1).** The data provided by these two commands is combined to form the 13-bit HLCLPSTP1 setting. The data written to address 31 provides data D7 to D0. The data written to address 32 provides data D12 to D8. The HLCLPSTP1 setting has a range from 0 to 8191. The default value is 383.
32	4 to 0	
33	7 to 0	**Horizontal direction at the right clamp pulse 1 start (HRCLPSTR1).** The data provided by these two commands is combined to form the 13-bit HRCLPSTR1 setting. The data written to address 33 provides data D7 to D0. The data written to address 34 provides data D12 to D8. The HRCLPSTR1 setting has a range from 0 to 8191. The default value is 3470.
34	4 to 0	

ADDRESS	COMMAND BIT	COMMAND DESCRIPTION
35	7 to 0	**Horizontal direction at the right clamp pulse 1 stop (HRCLPSTP1).** The data provided by these two commands is combined to form the 13-bit HRCLPSTP1 setting. The data written to address 35 provides data D7 to D0. The data written to address 36 provides data D12 to D8. The HRCLPSTP1 setting has a range from 0 to 8191. The default value is 3484.
36	4 to 0	
37	7 to 0	**Horizontal direction at the left clamp pulse 2 start (HLCLPSTR2).** The data provided by these two commands is combined to form the 13-bit HLCLPSTR2 setting. The data written to address 37 provides data D7 to D0. The data written to address 38 provides data D12 to D8. The HLCLPSTR2 setting has a range from 0 to 8191. The default value is 371.
38	4 to 0	
39	7 to 0	**Horizontal direction at the left clamp pulse 2 stop (HLCLPSTP2).** The data provided by these two commands is combined to form the 13-bit HLCLPSTP2 setting. The data written to address 39 provides data D7 to D0. The data written to address 40 provides data D12 to D8. The HLCLPSTP2 setting has a range from 0 to 8191. The default value is 383.
40	4 to 0	
41	7 to 0	**Horizontal direction at the right clamp pulse 2 start (HRCLPSTR2).** The data provided by these two commands is combined to form the 13-bit HRCLPSTR2 setting. The data written to address 41 provides data D7 to D0. The data written to address 42 provides data D12 to D8. The HRCLPSTR2 setting has a range from 0 to 8191. The default value is 3470.
42	4 to 0	
43	7 to 0	**Horizontal direction at the right clamp pulse 2 stop (HRCLPSTP2).** The data provided by these two commands is combined to form the 13-bit HRCLPSTP2 setting. The data written to address 43 provides data D7 to D0. The data written to address 44 provides data D12 to D8. The HRCLPSTP2 setting has a range from 0 to 8191. The default value is 3484.
44	4 to 0	
45	7 to 0	**Vertical direction at the top clamp pulse 1 start (VTCLPSTR1).** The VTCLPSTR1 setting has a range from 0 to 255. The default value is 3.
46	7 to 0	**Vertical direction at the top clamp pulse 1 stop (VTCLPSTP1).** The VTCLPSTP1 setting has a range from 0 to 255. The default value is 4.
47	7 to 0	**Vertical direction at the top clamp pulse 1 horizontal start (VTHCLPSTR1).** The data provided by these two commands is combined to form the 13-bit VTHCLPSTR1 setting. The data written to address 47 provides data D7 to D0. The data written to address 48 provides data D12 to D8. The VTHCLPSTR1 setting has a range from 0 to 8191. The default value is 0.
48	4 to 0	
49	7 to 0	**Vertical direction at the top clamp pulse 1 horizontal stop (VTHCLPSTP1).** The data provided by these two commands is combined to form the 13-bit VTHCLPSTP1 setting. The data written to address 49 provides data D7 to D0. The data written to address 50 provides data D12 to D8. The VTHCLPSTP1 setting has a range from 0 to 8191. The default value is 0.
50	4 to 0	
51	7 to 0	**Vertical direction at the bottom clamp pulse 1 start (VBCLPSTR1).** The data provided by these two commands is combined to form the 13-bit VBCLPSTR1 setting. The data written to address 51 provides data D7 to D0. The data written to address 52 provides data D12 to D8. The VTHCLPSTR1 setting has a range from 0 to 8191. The default value is 2060.
52	4 to 0	

ADDRESS	COMMAND BIT	COMMAND DESCRIPTION
53	7 to 0	**Vertical direction at the bottom clamp pulse 1 stop (VBCLPSTP1).** The data provided by these two commands is combined to form the 13-bit VBCLPSTP1 setting. The data written to address 53 provides data D7 to D0. The data written to address 54 provides data D12 to D8. The VBCLPSTP1 setting has a range from 0 to 8191. The default value is 0.
54	4 to 0	
55	7 to 0	**Vertical direction at the bottom clamp pulse 1 horizontal start (VBHCLPSTR1)**. The data provided by these two commands is combined to form the 13-bit VBHCLPSTR1 setting. The data written to address 55 provides data D7 to D0. The data written to address 56 provides data D12 to D8. The VBHCLPSTR1 setting has a range from 0 to 8191. The default value is 0.
56	4 to 0	
57	7 to 0	**Vertical direction at the bottom clamp pulse 1 horizontal stop (VBHCLPSTP1).** The data provided by these two commands is combined to form the 13-bit VBHCLPSTP1 setting. The data written to address 57 provides data D7 to D0. The data written to address 58 provides data D12 to D8. The VBHCLPSTP1 setting has a range from 0 to 8191. The default value is 0.
58	4 to 0	
59	7 to 0	**Vertical direction at the top clamp pulse 2 start (VTCLPSTR2).** The VTCLPSTR2 setting has a range from 0 to 255. The default value is 3.
60	7 to 0	**Vertical direction at the top clamp pulse 2 stop (VTCLPSTP2).** The VTCLPSTP2 setting has a range from 0 to 255. The default value is 4.
61	7 to 0	**Vertical direction at the top clamp pulse 2 horizontal start (VTHCLPSTR2).** The data provided by these two commands is combined to form the 13-bit VTHCLPSTR2 setting. The data written to address 61 provides data D7 to D0. The data written to address 62 provides data D12 to D8. The VTHCLPSTR2 setting has a range from 0 to 8191. The default value is 0.
62	4 to 0	
63	7 to 0	**Vertical direction at the top clamp pulse 2 horizontal stop (VTHCLPSTP2).** The data provided by these two commands is combined to form the 13-bit VTHCLPSTP2 setting. The data written to address 63 provides data D7 to D0. The data written to address 64 provides data D12 to D8. The VTHCLPSTP2 setting has a range from 0 to 8191. The default value is 0.
64	4 to 0	
65	7 to 0	**Vertical direction at the bottom clamp pulse 2 start (VBCLPSTR2).** The data provided by these two commands is combined to form the 13-bit VBCLPSTR2 setting. The data written to address 65 provides data D7 to D0. The data written to address 66 provides data D12 to D8. The VBCLPSTR2 setting has a range from 0 to 8191. The default value is 2060.
66	4 to 0	
67	7 to 0	**Vertical direction at the bottom clamp pulse 2 stop (VBCLPSTP2).** The data provided by these two commands is combined to form the 13-bit VBCLPSTP2 setting. The data written to address 67 provides data D7 to D0. The data written to address 68 provides data D12 to D8. The VBCLPSTP2 setting has a range from 0 to 8191. The default value is 0.
68	4 to 0	
69	7 to 0	**Vertical direction at the bottom clamp pulse 2 horizontal start (VBHCLPSTR2).** The data provided by these two commands is combined to form the 13-bit VBHCLPSTR2 setting. The data written to address 69 provides data D7 to D0. The data written to address 70 provides data D12 to D8. The VBHCLPSTR2 setting has a range from 0 to 8191. The default value is 0.
70	4 to 0	

ADDRESS	COMMAND BIT	COMMAND DESCRIPTION
71	7 to 0	**Vertical direction at the bottom clamp pulse 2 horizontal stop (VBHCLPSTP2).** The data provided by these two commands is combined to form the 13-bit VBHCLPSTP2 setting. The data written to address 71 provides data D7 to D0. The data written to address 72 provides data D12 to D8. The VBHCLPSTP2 setting has a range from 0 to 8191. The default value is 0.
72	4 to 0	
Setting the start and stop points for charge reset timings		
73	7 to 0	**Horizontal direction charge reset pulse start (HCRSTR).** The data provided by these two commands is combined to form the 13-bit HCRSTR setting. The data written to address 73 provides data D7 to D0. The data written to address 74 provides data D12 to D8. The HCRSTR setting has a range from 0 to 8191. The default value is 371.
74	4 to 0	
75	7 to 0	**Horizontal direction charge reset pulse stop (HCRSTP).** The data provided by these two commands is combined to form the 13-bit HCRSTP setting. The data written to address 75 provides data D7 to D0. The data written to address 76 provides data D12 to D8. The HCRSTP setting has a range from 0 to 8191. The default value is 383.
76	4 to 0	
77	7 to 0	**Horizontal direction VTLVL pulse start (HVTLSTR).** The data provided by these two commands is combined to form the 13-bit HVTLSTR setting. The data written to address 77 provides data D7 to D0. The data written to address 78 provides data D12 to D8. The HVTLSTR setting has a range from 0 to 8191. The default value is 371.
78	4 to 0	
79	7 to 0	**Horizontal direction VTLVL pulse stop (HVTLSTP).** The data provided by these two commands is combined to form the 13-bit HVTLSTP setting. The data written to address 79 provides data D7 to D0. The data written to address 80 provides data D12 to D8. The HVTLSTP setting has a range from 0 to 8191. The default value is 383.
80	4 to 0	
81	7 to 0	**Vertical direction at the top charge reset pulse start (VTCRSTR).** The VTCRSTR setting (D7 to D0) has a range from 0 to 255. The default value is 3
82	7 to 0	**Vertical direction at the top charge reset pulse stop (VTCRSTP).** The VTCRSTP setting (D7 to D0) has a range from 0 to 255. The default value is 4.
83	7 to 0	**Vertical direction at the bottom charge reset pulse start (VBCRSTR).** The data provided by these two commands is combined to form the 13-bit VBCRSTR setting. The data written to address 83 provides data D7 to D0. The data written to address 84 provides data D12 to D8. The VBCRSTR setting has a range from 0 to 8191. The default value is 2060.
84	4 to 0	
85	7 to 0	**Vertical direction at the bottom charge reset pulse stop (VBCRSTP).** The data provided by these two commands is combined to form the 13-bit VBCRSTP setting. The data written to address 85 provides data D7 to D0. The data written to address 86 provides data D12 to D8. The VBCRSTP setting has a range from 0 to 8191. The default value is 0.
86	4 to 0	
87	7 to 0	**Vertical direction at the top VTLVL pulse start (VTVTLSTR).** The VTVTLSTR setting (D7 to D0) has a range from 0 to 255. The default value is 3.
88	7 to 0	**Vertical direction at the top VTLVL pulse stop (VTVTLSTP).** The VTVTLSTP setting (D7 to D0) has a range from 0 to 255. The default value is 4.

ADDRESS	COMMAND BIT	COMMAND DESCRIPTION
89	7 to 0	**Vertical direction at the bottom VTLVL pulse start (VBVTLSTR).** The data provided by these two commands is combined to form the 13-bit VBVTLSTR setting. The data written to address 89 provides data D7 to D0. The data written to address 90 provides data D12 to D8. The VBVTLSTR setting has a range from 0 to 8191. The default value is 2060.
90	4 to 0	
91	7 to 0	**Vertical direction at the bottom VTLVL pulse stop (VBVTLSTP).** The data provided by these two commands is combined to form the 13-bit VBVTLSTP setting. The data written to address 91 provides data D7 to D0. The data written to address 92 provides data D12 to D8. The VBVTLSTP setting has a range from 0 to 8191. The default value is 0.
92	4 to 0	
Setting enable for clamp pulse and charge reset pulse		
93	0	**Vertical direction at the top of clamp pulse 1 enable control (VTCLPEN1).** 0 = enable; default state 1 = disable
	1	**Vertical direction at the bottom of clamp pulse 1 enable control (VBCLPEN1).** 0 = enable; default state 1 = disable
	2	**Vertical direction at the top of clamp pulse 2 enable control (VTCLPEN2).** 0 = enable; default state 1 = disable
	3	**Vertical direction at the bottom of clamp pulse 2 enable control (VBCLPEN2).** 0 = enable; default state 1 = disable
	4	**Vertical direction at the top of charge reset pulse enable control (VTCREN).** 0 = enable 1 = disable; default state
	5	**Vertical direction at the bottom of charge reset pulse enable control (VBCREN).** 0 = enable 1 = disable; default state
	6	**Vertical direction at the top of VTLVL pulse enable control (VTVTLEN).** 0 = enable 1 = disable; default state
	7	**Vertical direction at the bottom of VTLVL pulse enable control (VBVTLEN).** 0 = enable 1 = disable; default state

ADDRESS	COMMAND BIT	COMMAND DESCRIPTION
Setting polarity for clamp pulse and charge reset pulse		
94	0	**TRGCRP enable signal (TRGCRPEN).** 0 = disable 1 = enable; default state
	4	**Clamp pulse 1 polarity (CLPPOLA1).** 0 = negative 1 = positive; default state
	5	**Clamp pulse 2 polarity (CLPPOLA2).** 0 = negative 1 = positive; default state
	6	**Charge reset pulse polarity (CRPOLA).** 0 = negative 1 = positive; default state
	7	**VTLVL pulse polarity (VTLVPOLA).** 0 = negative 1 = positive; default state
95	7 to 0	**Data read-out timing control (RDTIMCNT).** The data read out delay control setting has a range 0 to 255. The default value is 0.
Setting for vertical transport signals A[1:4] and B[1:4]		
ASSIGN STATE PATTERN FOR LINE SHIFT STATE MACHINE FOR A PULSES (LUTLSA)		
96	3 to 0	STATE 0; default value = 1
	7 to 4	STATE 1; default value = 3
97	3 to 0	STATE 2; default value = 2
	7 to 4	STATE 3; default value = 6
98	3 to 0	STATE 4; default value = 4
	7 to 4	STATE 5; default value = 12
99	3 to 0	STATE 6; default value = 8
	7 to 4	STATE 7; default value = 9
ASSIGN STATE PATTERN FOR FRAME SHIFT STATE MACHINE FOR A PULSES (LUTFSA)		
100	3 to 0	STATE 0; default value = 1
	7 to 4	STATE 1; default value = 3
101	3 to 0	STATE 2; default value = 2
	7 to 4	STATE 3; default value = 6
102	3 to 0	STATE 4; default value = 4
	7 to 4	STATE 5; default value = 12
103	3 to 0	STATE 6; default value = 8
	7 to 4	STATE 7; default value = 9

ADDRESS	COMMAND BIT	COMMAND DESCRIPTION
ASSIGN STATE PATTERN FOR LINE SHIFT STATE MACHINE FOR B PULSES (LUTLSB)		
104	3 to 0	STATE 0; default value = 0
	7 to 4	STATE 1; default value = 0
105	3 to 0	STATE 2; default value = 0
	7 to 4	STATE 3; default value = 0
106	3 to 0	STATE 4; default value = 0
	7 to 4	STATE 5; default value = 0
107	3 to 0	STATE 6; default value = 0
	7 to 4	STATE 7; default value = 0
ASSIGN STATE PATTERN FOR FRAME SHIFT STATE MACHINE FOR B PULSES (LUTFSB)		
108	3 to 0	STATE 0; default value = 0
	7 to 4	STATE 1; default value = 0
109	3 to 0	STATE 2; default value = 0
	7 to 4	STATE 3; default value = 0
110	3 to 0	STATE 4; default value = 0
	7 to 4	STATE 5; default value = 0
111	3 to 0	STATE 6; default value = 0
	7 to 4	STATE 7; default value = 0
112	5 to 0	**Assign the division value of clock divider for LS sequence for A pulses (DIVLSA).** The DIVLSA setting has a range of 0 to 63. The default value is 2.
113	5 to 0	**Assign the division value of clock divider for LS sequence for B pulses (DIVLSB).** The DIVLSB setting has a range of 0 to 63. The default value is 2.
114	5 to 0	**Assign the division value of clock divider for FS sequence for A and B pulses (DIVFSAB).** The DIVFSAB setting has a range of 0 to 63. The default value is 7.
115	7 to 0	**Assign the up point of start signal for LS sequence for A pulses in horizontal direction (HLSASTR).** The HLSASTR setting has a range of 0 to 255. The default value is 0.
116	7 to 0	**Assign the up point of start signal for LS sequence for B pulses in horizontal direction (HLSBSTR).** The HLSBSTR setting has a range of 0 to 255. The default value is 0.
117	7 to 0	**Assign the up point of start signal for FS sequence for A pulses in horizontal direction (HFSASTR).** The HFSASTR setting has a range of 0 to 255. The default value is 0.
118	7 to 0	**Assign the up point of start signal for FS sequence for B pulses in horizontal direction (HFSBSTR).** The HFSBSTR setting has a range of 0 to 255. The default value is 0.

ADDRESS	COMMAND BIT	COMMAND DESCRIPTION
119	7 to 0	**Assign the up point of start signal 1 for LS sequence for A pulses in vertical direction (VLSASTR1).** The data provided by these two commands is combined to form the 13-bit VLSASTR1 setting. The data written to address 119 provides data D7 to D0. The data written to address 120 provides data D12 to D8. The VLSASTR1 setting has a range from 0 to 8191. The default value is 13.
120	4 to 0	
121	7 to 0	**Assign the down point of stop signal 1 for LS sequence for A pulses in vertical direction (VLSASTP1).** The data provided by these two commands is combined to form the 13-bit VLSASTP1 setting. The data written to address 121 provides data D7 to D0. The data written to address 122 provides data D12 to D8. The VLSASTP1 setting has a range from 0 to 8191. The default value is 200.
122	4 to 0	
123	7 to 0	**Assign the up point of start signal 2 for LS sequence for A pulses in vertical direction (VLSASTR2).** The data provided by these two commands is combined to form the 13-bit VLSASTR2 setting. The data written to address 123 provides data D7 to D0. The data written to address 124 provides data D12 to D8. The VLSASTR2 setting has a range from 0 to 8191. The default value is 1FFFH (disable).
124	4 to 0	
125	7 to 0	**Assign the down point of stop signal 2 for LS sequence for A pulses in vertical direction (VLSASTP2).** The data provided by these two commands is combined to form the 13-bit VLSASTP2 setting. The data written to address 125 provides data D7 to D0. The data written to address 126 provides data D12 to D8. The VLSASTP2 setting has a range from 0 to 8191. The default value is 240.
126	4 to 0	
127	7 to 0	**Assign the up point of start signal 3 for LS sequence for A pulses in vertical direction (VLSASTR3).** The data provided by these two commands is combined to form the 13-bit VLSASTR3 setting. The data written to address 127 provides data D7 to D0. The data written to address 128 provides data D12 to D8. The VLSASTR3 setting has a range from 0 to 8191. The default value is 1FFFH (disable).
128	4 to 0	
129	7 to 0	**Assign the down point of stop signal 3 for LS sequence for A pulses in vertical direction (VLSASTP3).** The data provided by these two commands is combined to form the 13-bit VLSASTP3 setting. The data written to address 129 provides data D7 to D0. The data written to address 130 provides data D12 to D8. The VLSASTP3 setting has a range from 0 to 8191. The default value is 260.
130	4 to 0	
131	7 to 0	**Assign the up point of start signal for LS sequence for B pulses in vertical direction (VLSBSTR).** The data provided by these two commands is combined to form the 13-bit VLSBSTR setting. The data written to address 131 provides data D7 to D0. The data written to address 132 provides data D12 to D8. The VLSBSTR setting has a range from 0 to 8191. The default value is 13.
132	4 to 0	
133	7 to 0	**Assign the down point of stop signal for LS sequence for B pulses in vertical direction (VLSBSTP).** The data provided by these two commands is combined to form the 13-bit VLSBSTP setting. The data written to address 133 provides data D7 to D0. The data written to address 134 provides data D12 to D8. The VLSBSTP setting has a range from 0 to 8191. The default value is 200.
134	4 to 0	

ADDRESS	COMMAND BIT	COMMAND DESCRIPTION
135	7 to 0	**Assign the up point of start signal for FS sequence for A pulses in vertical direction (VFSASTR).** The VFSASTR setting has a range from 0 to 255. The default value is 1.
136	7 to 0	**Assign the up point of start signal for FS sequence for B pulses in vertical direction (VFSBSTR).** The VFSBSTR setting has a range from 0 to 255. The default value is 1.
137	3 to 0	**Assign the count value of LS Counter_A1 for image gate waveform generation (CNTLSA1).** The CNTLSA1 setting has a range from 0 to 15. The default value is 1.
138	3 to 0	**Assign the count value of LS Counter_A2 for image gate waveform generation (CNTLSA2).** The CNTLSA2 setting has a range from 0 to 15. The default value is 1.
139	3 to 0	**Assign the count value of LS Counter_A3 for image gate waveform generation (CNTLSA3).** The CNTLSA3 setting has a range from 0 to 15. The default value is 1.
140	7 to 0	**Assign the count value of FS Counter_A for storage gate waveform generation (CNTFSA).** The data provided by these two commands is combined to form the 13-bit CNTFSA setting. The data written to address 140 provides data D7 to D0. The data written to address 141 provides data D12 to D8. The CNTFSA setting has a range from 0 to 8191. The default value is 0.
141	4 to 0	
142	3 to 0	**Assign the count value of LS Counter_B for storage gate waveform generation (CNTLSB).** The CNTLSB setting has a range of 0 to 15. The default value is 0.
143	7 to 0	**Assign the count value of FS Counter_B for storage gate waveform generation (CNTFSB).** The data provided by these two commands is combined to form the 13-bit CNTFSB setting. The data written to address 143 provides data D7 to D0. The data written to address 141 provides data D12 to D8. The CNTFSB setting has a range from 0 to 8191. The default value is 0.
144	4 to 0	
145	7 to 0	**Assign the up point of TG signal for horizontal direction (HTGSTR).** The data provided by these two commands is combined to form the 13-bit HTGSTR setting. The data written to address 145 provides data D7 to D0. The data written to address 146 provides data D12 to D8. The HTGSTR setting has a range from 0 to 8191. The default value is 0.
146	4 to 0	
147	7 to 0	**Assign the down point of TG signal for horizontal direction (HTGSTP).** The data provided by these two commands is combined to form the 13-bit HTGSTP setting. The data written to address 147 provides data D7 to D0. The data written to address 148 provides data D12 to D8. The HTGSTP setting has a range from 0 to 8191. The default value is 0.
148	4 to 0	
149	7 to 0	**Assign the up point of TG signal for vertical direction (VTGSTR).** The data provided by these two commands is combined to form the 13-bit VTGSTR setting. The data written to address 149 provides data D7 to D0. The data written to address 150 provides data D12 to D8. The VTGSTR setting has a range from 0 to 8191. The default value is 6.
150	4 to 0	

ADDRESS	COMMAND BIT	COMMAND DESCRIPTION
151	7 to 0	**Assign the down point of TG signal for vertical direction (VTGSTP).** The data provided by these two commands is combined to form the 13-bit VTGSTP setting. The data written to address 151 provides data D7 to D0. The data written to address 152 provides data D12 to D8. The VTGSTP setting has a range from 0 to 8191. The default value is 2054.
152	4 to 0	
153	7 to 0	**Assign the up point of START_SP1 signal for sub-sampling waveform generation sequence for B pulse (SPSTR1).** The data provided by these two commands is combined to form the 13-bit SPSTR1 setting. The data written to address 153 provides data D7 to D0. The data written to address 154 provides data D12 to D8. The SPSTR1 setting has a range from 0 to 8191. The default value is 0.
154	4 to 0	
155	7 to 0	**Assign the down point of START_SP1 signal for sub-sampling waveform generation sequence for B pulse (SPSTP1).** The data provided by these two commands is combined to form the 13-bit SPSTP1 setting. The data written to address 155 provides data D7 to D0. The data written to address 156 provides data D12 to D8. The SPSTP1 setting has a range from 0 to 8191. The default value is 0.
156	4 to 0	
157	7 to 0	**Assign the up point of START_SP2 signal for sub-sampling waveform generation sequence for B pulse (SPSTR2).** The data provided by these two commands is combined to form the 13-bit SPSTR2 setting. The data written to address 157 provides data D7 to D0. The data written to address 158 provides data D12 to D8. The SPSTR2 setting has a range from 0 to 8191. The default value is 0.
158	4 to 0	
159	7 to 0	**Assign the down point of START_SP2 signal for sub-sampling waveform generation sequence for B pulse (SPSTP2).** The data provided by these two commands is combined to form the 13-bit SPSTP2 setting. The data written to address 159 provides data D7 to D0. The data written to address 160 provides data D12 to D8. The SPSTP2 setting has a range from 0 to 8191. The default value is 0.
160	4 to 0	
161	7 to 0	**Assign the up point of START_SP3 signal for sub-sampling waveform generation sequence for B pulse (SPSTR3).** The data provided by these two commands is combined to form the 13-bit SPSTR3 setting. The data written to address 161 provides data D7 to D0. The data written to address 162 provides data D12 to D8. The SPSTR3 setting has a range from 0 to 8191. The default value is 0.
162	4 to 0	
163	7 to 0	**Assign the down point of START_SP3 signal for sub-sampling waveform generation sequence for B pulse (SPSTP3).** The data provided by these two commands is combined to form the 13-bit SPSTP3 setting. The data written to address 163 provides data D7 to D0. The data written to address 164 provides data D12 to D8. The SPSTP3 setting has a range from 0 to 8191. The default value is 0.
164	4 to 0	
Define the sub-sampling pattern for SPPATx waveform generation sequence for B pulse (LUTSPx)		
DEFINE THE SUB-SAMPLING PATTERN FOR SPPAT1 WAVEFORM GENERATION SEQUENCE FOR B PULSE (LUTSP1)		
165	7 to 0	The data written to address 165 provides data D7 to D0 of the SPPAT1 setting. The default value is 0.
166	7 to 0	The data written to address 166 provides data D15 to D8 of the SPPAT1 setting. The default value is 0.

ADDRESS	COMMAND BIT	COMMAND DESCRIPTION
167	7 to 0	The data written to address 167 provides data D23 to D16 of the SPPAT1 setting. The default value is 0.
168	7 to 0	The data written to address 168 provides data D31 to D24 for A clock of the SPPAT1 setting. The default value is 0.
DEFINE THE SUB-SAMPLING PATTERN FOR SPPAT2 WAVEFORM GENERATION SEQUENCE FOR B PULSE (LUTSP2)		
169	7 to 0	The data written to address 169 provides data D7 to D0 of the SPPAT2 setting. The default value is 0.
170	7 to 0	The data written to address 170 provides data D15 to D8 of the SPPAT2 setting. The default value is 0.
171	7 to 0	The data written to address 171 provides data D23 to D16 of the SPPAT2 setting. The default value is 0.
172	7 to 0	The data written to address 172 provides data D31 to D24 for A clock of the SPPAT2 setting. The default value is 0.
DEFINE THE SUB-SAMPLING PATTERN FOR SPPAT3 WAVEFORM GENERATION SEQUENCE FOR B PULSE (LUTSP3)		
173	7 to 0	The data written to address 173 provides data D7 to D0 of the SPPAT3 setting. The default value is 0.
174	7 to 0	The data written to address 174 provides data D15 to D8 of the SPPAT3 setting. The default value is 0.
175	7 to 0	The data written to address 175 provides data D23 to D16 of the SPPAT3 setting. The default value is 0.
176	7 to 0	The data written to address 176 provides data D31 to D24 for A clock of the SPPAT3 setting. The default value is 0.
Define sub-sampling pattern shift value		
177	2 to 0	**Define sub-sampling pattern shift value 1 (SPSHIFT1).** The SPSHIFT1 setting has a range from 0 to 7. The default value is 0.
	6 to 4	**Define sub-sampling pattern shift value 2 (SPSHIFT2).** The SPSHIFT2 setting has a range from 0 to 7. The default value is 0.
178	2 to 0	**Define sub-sampling pattern shift value 3 (SPSHIFT3).** The SPSHIFT3 setting has a range from 0 to 7. The default value is 0.
Define pattern length		
179	2 to 0	**Define LSA1 pattern length (RATLSA1).** The RATLSA1 setting has a range from 0 to 7. The default value is 7.
180	2 to 0	**Define LSA2 pattern length (RATLSA2).** The RATLSA2 setting has a range from 0 to 7. The default value is 7.
181	2 to 0	**Define LSA3 pattern length (RATLSA3).** The RATLSA3 setting has a range from 0 to 7. The default value is 7.
182	2 to 0	**Define FSA pattern length (RATFSA).** The RATFSA setting has a range from 0 to 7. The default value is 3.
183	2 to 0	**Define LSB pattern length (RATLSB).** The RATLSB setting has a range from 0 to 7. The default value is 7.
184	4 to 0	**Define FSB pattern length (RATFSB).** The RATFSB setting has a range from 0 to 19. The default value is 3.
185	4 to 0	**Define SP1 pattern length (RATIOSP1).** The RATIOSP1 setting has a range from 0 to 31. The default value is 3.

ADDRESS	COMMAND BIT	COMMAND DESCRIPTION
186	4 to 0	**Define SP2 pattern length (RATIOSP2).** The RATIOSP2 setting has a range from 0 to 31. The default value is 3.
187	4 to 0	**Define SP3 pattern length (RATIOSP3).** The RATIOSP3 setting has a range from 0 to 31. The default value is 3.
Setting polarity for A[1:4] and B[1:4] signals (INVA and INVB)		
188	0	**A[1:4] polarity selection.** 0 = negative polarity 1 = positive polarity; default state
	1	**B[1:4] polarity selection.** 0 = negative polarity 1 = positive polarity; default state
	4	**Setting the priority of the TRIG signal during read-out for FF CCD (TRGPRTY).** 0 = low priority 1 = high priority; default state
Setting for DC-to-DC converter		
189[1]	6	**Control signal of clock signal output for DC-to-DC convertor (CLKDC).** 0 = enable; default state 1 = disable
	5 to 0	**Assign the division value of clock generator for DC-to-DC converter (DIVDC).** The DIVDC setting has a range from 0 to 63. The default value is 3.
Settings for Horizontal Pulse Pattern Generator		
ASSIGN THE ENABLE SIGNALS FOR HF1 AND HF2 PULSES		
190[1]	0	**Define the state during HF1 blanking time (HF1BLK).** 0 = LOW state 1 = HIGH state; default state
	1	**SSC selection (HF1SSC).** 0 = unselect 1 = select; default state
	2	**Define the state when SSC is unselected (HF1EN).** 0 = disable 1 = continuous; default state
	4	**Define the state during HF2 blanking time (HF2BLK).** 0 = LOW state 1 = HIGH state, default state
	5	**SSC selection (HF2SSC).** 0 = unselect 1 = select; default state
	6	**Define the state when SSC is unselected (HF2EN).** 0 = disable 1 = continuous; default state

ADDRESS	COMMAND BIT	COMMAND DESCRIPTION
ASSIGN THE ENABLE SIGNALS FOR HF3 AND HF4 PULSES		
191[1]	0	**Define the state during HF3 blanking time (HF3BLK).** 0 = LOW state 1 = HIGH state, default state
	1	**SSC selection (HF3SSC).** 0 = unselect 1 = select; default state
	2	**Define the state when SSC is unselected (HF3EN).** 0 = disable 1 = continuous; default state
	4	**Define the state during HF4 blanking time (HF4BLK).** 0 = LOW state 1 = HIGH state, default state
	5	**SSC selection (HF4SSC).** 0 = unselect 1 = select; default state
	6	**Define the state when SSC is unselected (HF4EN).** 0 = disable 1 = continuous; default state
ASSIGN THE ENABLE SIGNALS FOR HF5 AND HF6 PULSES		
192[1]	0	**Define the state during HF5 blanking time (HF5BLK).** 0 = LOW state 1 = HIGH state, default state
	1	**SSC selection (HF5SSC).** 0 = unselect 1 = select; default state
	2	**Define the state when SSC is unselected (HF5EN).** 0 = disable 1 = continuous; default state
	4	**Define the state during HF6 blanking time (HF6BLK).** 0 = LOW state 1 = HIGH state, default state
	5	**SSC selection (HF6SSC).** 0 = unselect 1 = select; default state
	6	**Define the state when SSC is unselected (HF6EN).** 0 = disable 1 = continuous; default state

ADDRESS	COMMAND BIT	COMMAND DESCRIPTION
ASSIGN THE ENABLE SIGNALS FOR HF7 AND HF8 PULSES		
193[1]	0	**Define the state during HF7 blanking time (HF7BLK).** 0 = LOW state 1 = HIGH state, default state
	1	**SSC selection (HF7SSC).** 0 = unselect 1 = select; default state
	2	**Define the state when SSC is unselected (HF7EN).** 0 = disable 1 = continuous; default state
	4	**Define the state during HF8 blanking time (HF8BLK).** 0 = LOW state 1 = HIGH state, default state
	5	**SSC selection (HF8SSC).** 0 = unselect 1 = select; default state
	6	**Define the state when SSC is unselected (HF8EN).** 0 = disable 1 = continuous; default state
ASSIGN THE ENABLE SIGNALS FOR HF9 PULSE		
194[1]	0	**Define the state during HF9 blanking time (HF9BLK).** 0 = LOW state 1 = HIGH state, default state
	1	**SSC selection (HF9SSC).** 0 = unselect 1 = select; default state
	2	**Define the state when SSC is unselected (HF9EN).** 0 = disable 1 = continuous; default state
	4	**Stop HF signals in Idle state (HFSTOP).** 0 = disable; default state 1 = enable

ADDRESS	COMMAND BIT	COMMAND DESCRIPTION
TEST control signals setting (TSTSEL)		
195[1]	0	**TSTSEL.** 0 = normal 1 = test; default state
Register selection for CCD transfer data setting in Shot or Preview mode (REGSEL)		
200[1][2]	0	**REGSEL.** 0 = data sent to Register 1 (Shot mode); default state 1 = data sent to Register 2 (Preview mode)
High speed pulse control		
DATA SETTING FOR HF1		
201[1]	2 to 0	Delay data D2 to D0; default value = 0
202[1]	7 to 0	Pattern data D7 to D0; default value = 0
203[1]	7 to 0	Pattern data D15 to D8; default value = 0
204[1]	7 to 0	Pattern data D23 to D16; default value = 0
DATA SETTING FOR HF2		
205[1]	2 to 0	Delay data D2 to D0; default value = 0
206[1]	7 to 0	Pattern data D7 to D0; default value = 0
207[1]	7 to 0	Pattern data D15 to D8; default value = 0
208[1]	7 to 0	Pattern data D23 to D16; default value = 0
DATA SETTING FOR HF3		
209[1]	2 to 0	Delay data D2 to D0; default value = 0
210[1]	7 to 0	Pattern data D7 to D0; default value = 0
211[1]	7 to 0	Pattern data D15 to D8; default value = 0
212[1]	7 to 0	Pattern data D23 to D16; default value = 0
DATA SETTING FOR HF4		
213[1]	2 to 0	Delay data D2 to D0; default value = 0
214[1]	7 to 0	Pattern data D7 to D0; default value = 0
215[1]	7 to 0	Pattern data D15 to D8; default value = 0
216[1]	7 to 0	Pattern data D23 to D16; default value = 0
DATA SETTING FOR HF5		
217[1]	2 to 0	Delay data D2 to D0; default value = 0
218[1]	7 to 0	Pattern data D7 to D0; default value = 0
219[1]	7 to 0	Pattern data D15 to D8; default value = 0
220[1]	7 to 0	Pattern data D23 to D16; default value = 0
DATA SETTING FOR HF6		
221[1]	2 to 0	Delay data D2 to D0; default value = 0
222[1]	7 to 0	Pattern data D7 to D0; default value = 0
223[1]	7 to 0	Pattern data D15 to D8; default value = 0
224[1]	7 to 0	Pattern data D23 to D16; default value = 0

ADDRESS	COMMAND BIT	COMMAND DESCRIPTION
DATA SETTING FOR HF7		
225(1)	2 to 0	Delay data D2 to D0; default value = 0
226(1)	7 to 0	Pattern data D7 to D0; default value = 0
227(1)	7 to 0	Pattern data D15 to D8; default value = 0
228(1)	7 to 0	Pattern data D23 to D16; default value = 0
DATA SETTING FOR HF8		
229(1)	2 to 0	Delay data D2 to D0; default value = 0
230(1)	7 to 0	Pattern data D7 to D0; default value = 0
231(1)	7 to 0	Pattern data D15 to D8; default value = 0
232(1)	7 to 0	Pattern data D23 to D16; default value = 0
DATA SETTING FOR HF9		
233(1)	2 to 0	Delay data D2 to D0; default value = 0
234(1)	7 to 0	Pattern data D7 to D0; default value = 0
235(1)	7 to 0	Pattern data D15 to D8; default value = 0
236(1)	7 to 0	Pattern data D23 to D16; default value = 0
Assign state pattern for Frame shift state machine for B pulses (LUTFSB)		
240	3 to 0	STATE 8; default value = 0
	7 to 4	STATE 9; default value = 0
241	3 to 0	STATE 10; default value = 0
	7 to 4	STATE 11; default value = 0
242	3 to 0	STATE 12; default value = 0
	7 to 4	STATE 13; default value = 0
243	3 to 0	STATE 14; default value = 0
	7 to 4	STATE 15; default value = 0
244	3 to 0	STATE 16; default value = 0
	7 to 4	STATE 17; default value = 0
245	3 to 0	STATE 18; default value = 0
	7 to 4	STATE 19; default value = 0
Assign state pattern for A pulses in Idle state (LUTIDLE)		
246(1)	3 to 0	LUTIDLE; default value = 0

Notes

1. The data sent to these addresses is used in both the Shot and Preview modes.
2. Address 200 for register selection should be assigned first in order to specify the operating settings.

12 TIMING DIAGRAMS

For specifying timing diagrams it is necessary to have a pixel-map available. The timing diagrams are dependent upon pixel count and line count. Timing diagrams and timing software files are available on request; contact your nearest Philips Semiconductors sales office. Please refer to *“Application Note of the SAA8103”.*

13 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDDx}	digital supply voltages: V_{DDD1}, V_{DDD2}, V_{DDD3}, V_{DDD4} and $V_{DD(OSC)}$	–0.5	+5.0	V
V_{DDAx}	analog supply voltages: $V_{DDA(BUF1)}$, $V_{DDA(BUF2)}$, $V_{DDA(BUF3)}$, $V_{DDA(DLL1)}$ and $V_{DDA(DLL2)}$	–0.5	+5.0	V
T_{stg}	storage temperature range	–40	+125	°C
T_{amb}	operating ambient temperature range	–20	+70	°C

14 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	67	K/W

15 DC CHARACTERISTICS

V_{DDDx} = 3.3 V; T_{amb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDDx}	digital supply voltage		3.0	3.3	3.6	V
I_{DDDx}	digital supply current	f_{CLK} = 25 MHz	30	40	50	mA
$V_{DDA(DLLx)}$	analog supply voltage		3.0	3.3	3.6	V
$I_{DDA(DLLx)}$	analog supply current	f_{CLK} = 25 MHz	5	7	9	mA
$V_{DD(BUFx)}$	outputs supply voltage		3.0	3.3	3.6	V
$I_{DD(BUFx)}$	outputs supply current	f_{CLK} = 25 MHz	4	6	8	mA
$V_{DD(OSC)}$	oscillator supply voltage		3.0	3.3	3.6	V
$I_{DD(OSC)}$	oscillator supply current	f_{CLK} = 25 MHz	0.20	0.35	0.50	mA
Data and control inputs						
V_{IL}	LOW-level input voltage		0	–	0.8	V
V_{IH}	HIGH-level input voltage		2.3	–	V_{DD}	V
I_{IL}	LOW-level input current	$V_{IL} = V_{SSD}$	–	–	–1	mA
I_{IH}	HIGH-level input current	$V_{IH} = V_{DDD}$	–	–	1	mA
$t_{su(DI)}$	data input set-up time		4	–	–	ns
$t_{h(DI)}$	data input hold time		4	–	–	ns
Data and control output						
V_{OL}	LOW-level output voltage		0	–	0.5	V
V_{OH}	HIGH-level output voltage		2.3	–	V_{DD}	V
I_{OL}	LOW-level output current		4	–	–	mA
I_{OH}	HIGH-level output current		–	–	–4	mA
$t_{d(DO)}$	data output delay time	C_L = 15 pF	–	2	10	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I^2C-bus signals: SDA_SNDA and SCL_SNCL						
V_{IL}	LOW-level input voltage		0	–	0.8	V
V_{IH}	HIGH-level input voltage		2.3	–	V_{DD}	V
I_I	input current	V_I = LOW or HIGH	–	–	±10	mA
V_{OL}	SDA output voltage	I_O = 3 mA	–	–	0.4	V
I_O	output current	during acknowledge	3	–	–	mA
Crystal oscillator; see Fig.16						
f_{CLK}	clock frequency	C_L = 15 pF	6	–	28	MHz
$t_{r(CLK)}$	clock rising time	f_{CLK} = 25 MHz	–	2.5	10	ns
$t_{f(CLK)}$	clock falling time	f_{CLK} = 25 MHz	–	2.5	10	ns
$T_{cy(CLK)}$	duty cycle at oscillation	f_{CLK} = 25 MHz	40	50	60	%
HF pulse timing; see Fig.15						
$t_{r(HF)}$	HF rising time	C_L = 15 pF; f_{CLK} = 25 MHz; $t_{r(CLK)} = t_{f(CLK)}$ = 1 ns	–	3	10	ns
$t_{f(HF)}$	HF falling time	C_L = 15 pF; f_{CLK} = 25 MHz; $t_{r(CLK)} = t_{f(CLK)}$ = 1 ns	–	3	10	ns
$t_{d(HF)}$	delay time from CLK to HF rising	HF pulse parameter 0F0F0FH; f_{CLK} = 25 MHz	–	–	15	ns
$t_{W(HF)}$	pulse width of HF	HF pulse parameter 0F0F0FH; f_{CLK} = 25 MHz	5	–	–	ns
Reset condition; see Fig.17						
$t_{W(rst)}$	reset pulse width		400	–	–	µs
Interface timing for front-end ICs; see Fig.18						
$t_{f(SCLK)}$	fall time of SCLK		–	3.5	10	ns
$t_{r(SCLK)}$	rise time of SCLK		–	3.5	10	ns
$t_{d(SDATA)}$	data output delay time of SDATA	f_{CLK} = 25 MHz	36	–	–	ns
$t_{h(SDATA)}$	data output hold time of SDATA	f_{CLK} = 25 MHz	36	–	–	ns
$t_{d(SEN)}$	data output delay time of SEN	f_{CLK} = 25 MHz	36	–	–	ns
$t_{h(SEN)}$	data output hold time of SEN	f_{CLK} = 25 MHz	36	–	–	ns
f_{SCLK}	CLK frequency		–	–	5	MHz
$t_{W(SCLK)}$	pulse width of SCLK		–	50	–	%

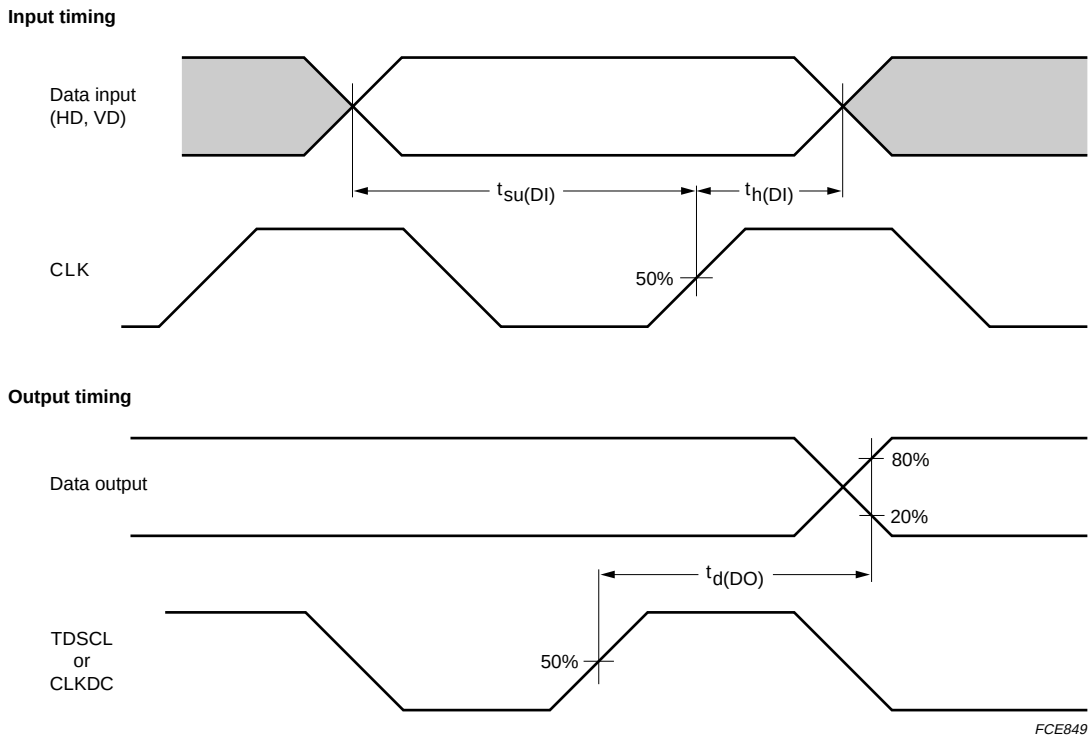


Fig.14 Input and output timing.

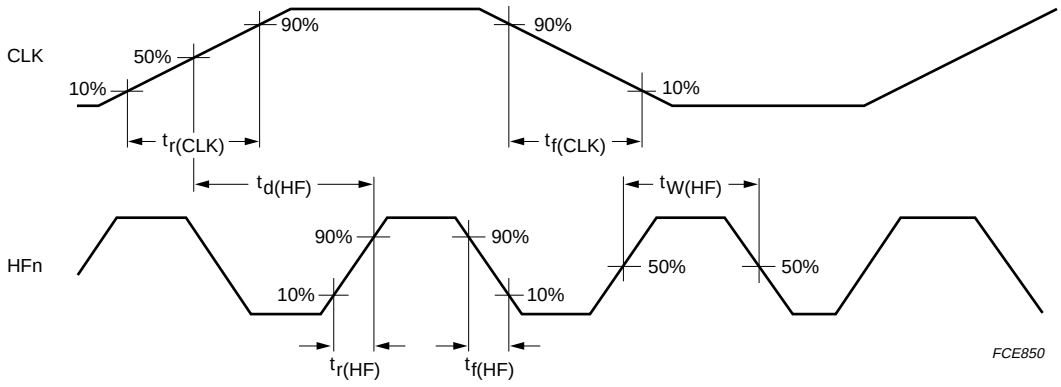


Fig.15 HFn signal output timing (n = 1 to 9).

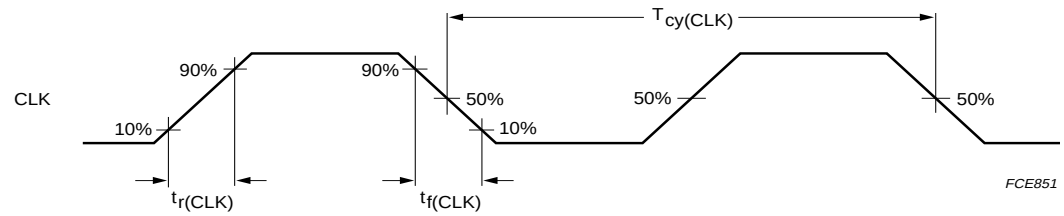


Fig.16 Crystal oscillator output timing.

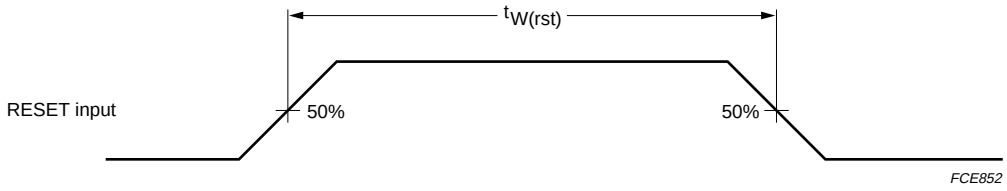


Fig.17 Reset timing.

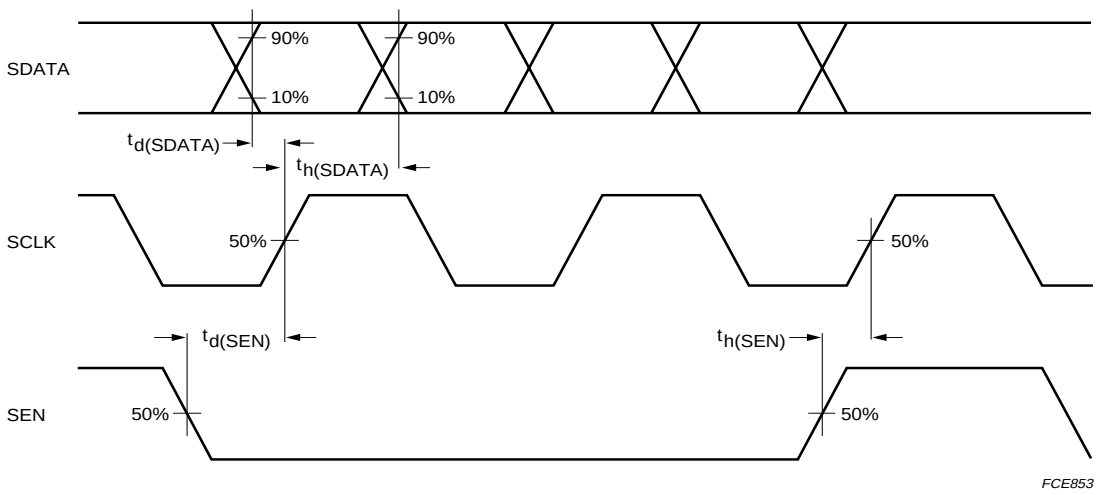
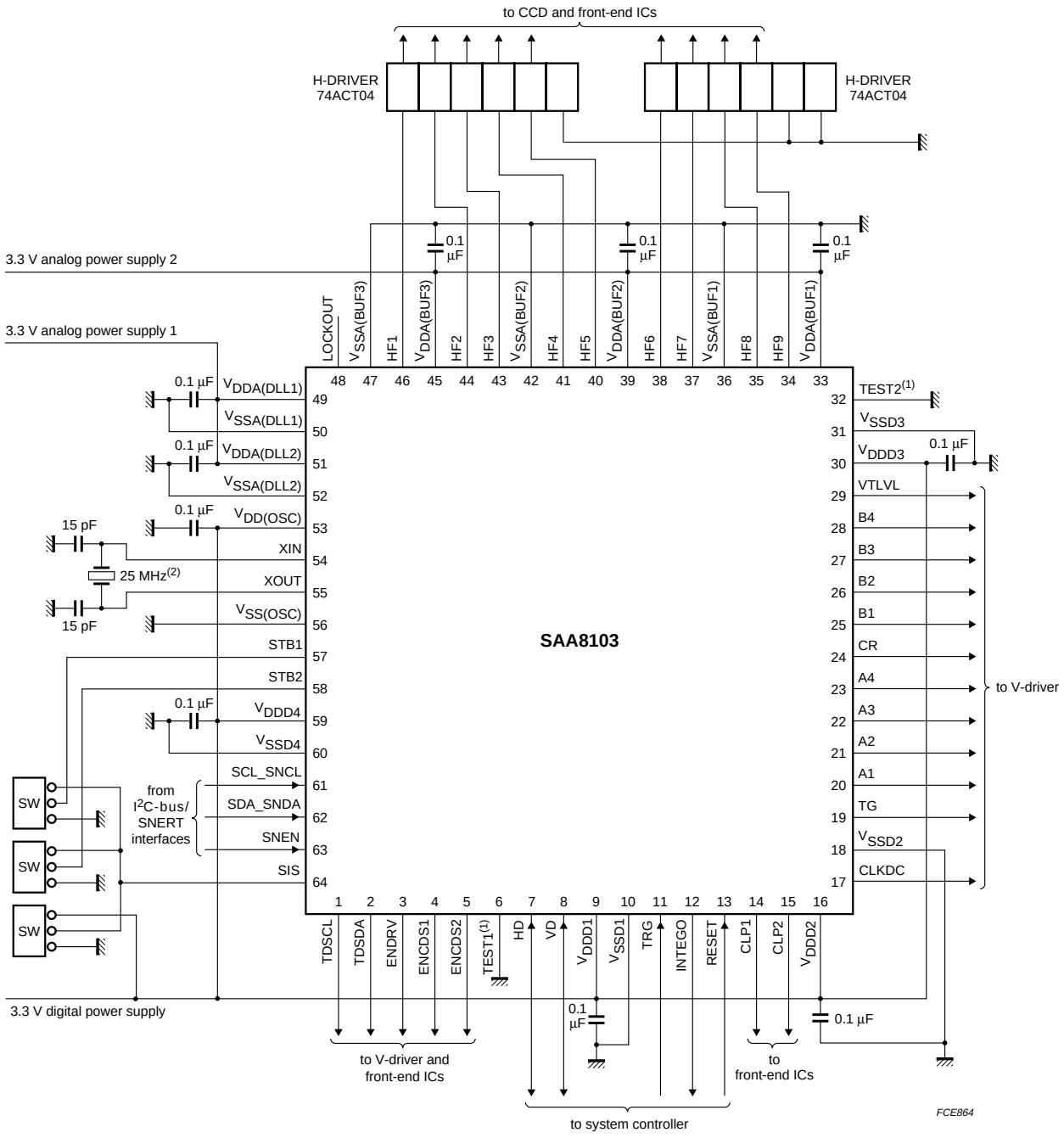


Fig.18 Interface timing for front-end ICs.

16 APPLICATION INFORMATION



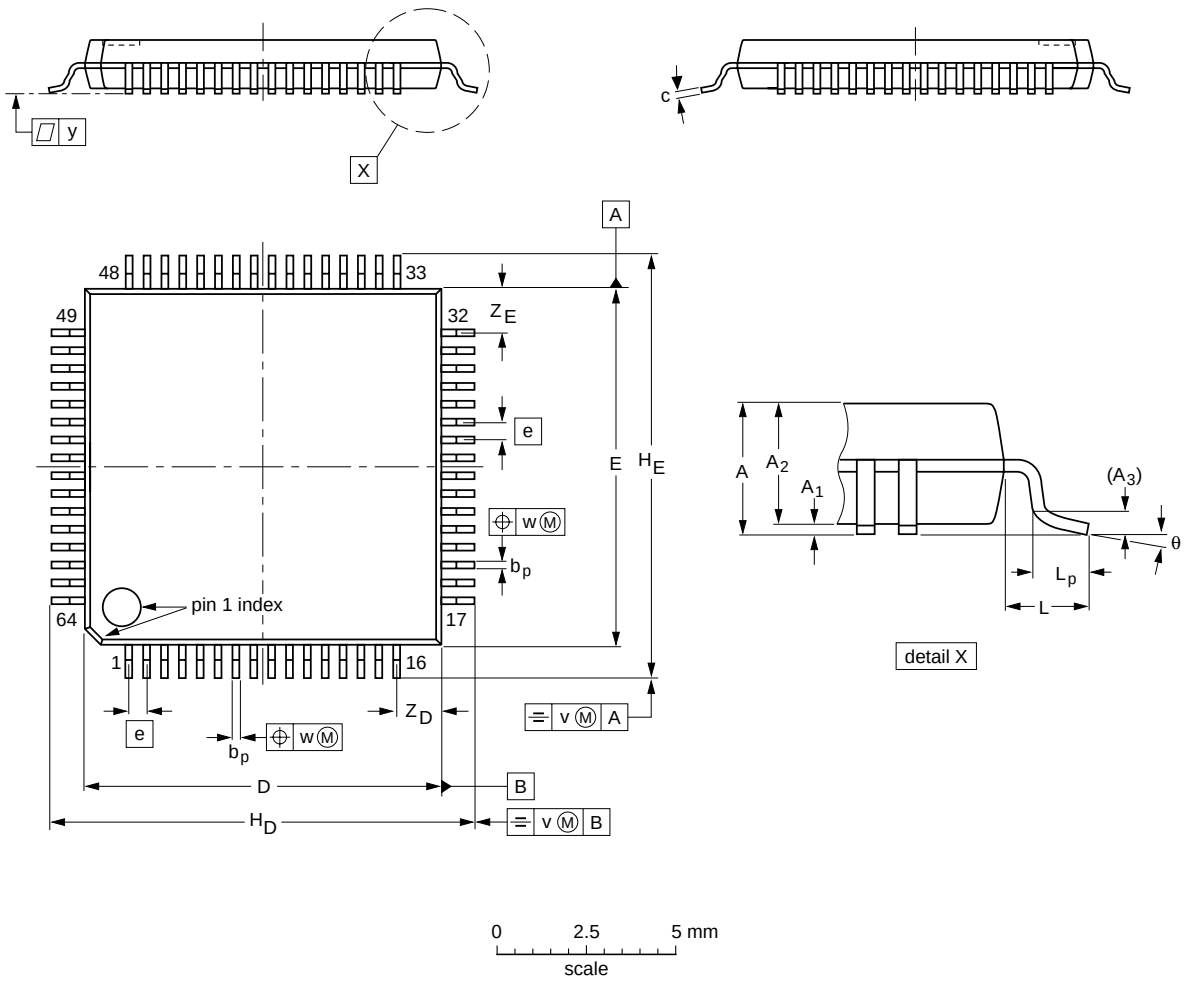
(1) These pins should be connected to the ground line.

(2) Daishinku crystal oscillator.

Fig.19 PPGFT application diagram.

17 PACKAGE OUTLINE

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1.0	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT314-2	136E10	MS-026				~~99-12-27~~ 00-01-19

18 SOLDERING

18.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

18.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

18.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

18.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

18.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW[1]
BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable[2]	suitable
PLCC[3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[3][4]	suitable
SSOP, TSSOP, VSO	not recommended[5]	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

19 DATA SHEET STATUS

DATA SHEET STATUS[1]	PRODUCT STATUS[2]	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

20 DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

21 DISCLAIMERS

Life support applications — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

22 PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

NOTES

Philips Semiconductors – a worldwide company

Contact information

For additional information please visit **http://www.semiconductors.philips.com**. Fax: **+31 40 27 24825**
For sales offices addresses send e-mail to: **sales.addresses@www.semiconductors.philips.com**.

Printed in The Netherlands 753504/01/pp48 Date of release: 2001 Oct 22 Document order number: 9397 750 08514

Let's make things better.

Philips
Semiconductors

PHILIPS