



## 15.0 ELECTRICAL DATA

The following sections describe recommended electrical connections and electrical specifications for the Military Intel486 processor.

### 15.1 Power and Grounding

#### 15.1.1 POWER CONNECTIONS

The Military Intel486 processor is implemented in CHMOS technology and has modest power requirements. However, the high clock frequency output buffers can cause power surges as multiple output buffers drive new signal levels simultaneously. For clean on-chip power distribution at high frequency, multiple  $V_{CC}$  and  $V_{SS}$  pins feed the Military Intel486 processor.

Power and ground connections must be made to all external  $V_{CC}$  and GND pins of the Military Intel486 processor. On the circuit board, all  $V_{CC}$  pins must be connected on a  $V_{CC}$  plane. All  $V_{SS}$  pins must be likewise connected on a GND plane.

#### 15.1.2 MILITARY INTEL486 PROCESSOR POWER DECOUPLING RECOMMENDATIONS

Liberal decoupling capacitance should be placed near the Military Intel486 processor. The Military Intel486 processor, driving its 32-bit parallel address and data buses at high frequencies, can cause transient power surges, particularly when driving large capacitive loads. Low inductance capacitors (i.e., surface-mount capacitors) and interconnects are recommended for the best high-frequency electrical performance. Inductance can be reduced by connecting capacitors directly to the  $V_{CC}$  and  $V_{SS}$  planes, with minimal trace length between the component pads and vias to the plane. These capacitors should be evenly distributed around each component on the  $V_{CC}$  power plane.

Capacitor values should be chosen to ensure they eliminate both low and high frequency noise components.

**The recommendation for the Military Intel486 processor is 9 x 0.01  $\mu$ F and 9 x 0.1  $\mu$ F capacitors.**

The power consumption can transition from a low level of power to a much higher level (or high to low power) very rapidly. A typical example would be entering or exiting the Stop Grant state. Another example would be executing a HALT instruction, causing the Military Intel486 processor to enter the Auto HALT Power Down state, or transitioning from HALT to the Normal state. All of these examples may cause abrupt changes in the power being consumed by the Military Intel486 processor. Bulk storage capacitors with a low ESR (Effective Series Resistance) in the 10 to 100 microfarad range are required to maintain a regulated supply voltage during the interval between the time the current load changes and the point that the regulated power supply output can react to the change in load. In order to reduce the ESR, it may be necessary to place several bulk storage capacitors in parallel. These capacitors should be placed near the Military Intel486 processor (on the processor power plane) to ensure that the supply voltage stays within specified limits during changes in the supply current while in operation.

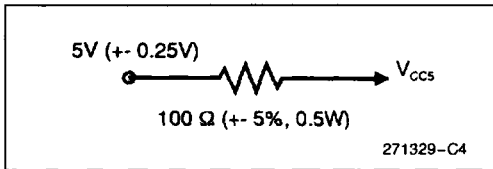
#### 15.1.3 $V_{CC5}$ AND $V_{CC}$ POWER SUPPLY REQUIREMENTS FOR THE INTEL DX4 PROCESSOR

In mixed voltage systems that will be driving IntelDX4 processor inputs in excess of 3.3V, the  $V_{CC5}$  pin must be connected to the system 5V supply. In order to limit current flow into the  $V_{CC5}$  pin, there is a limit to the voltage differential between the  $V_{CC5}$  pin and the other  $V_{CC}$  pins. The voltage differential between the  $V_{CC5}$  pin of the IntelDX4 processor and its 3.3V  $V_{CC}$  pins should never exceed 2.25V. The 2.25V limit applies to power up, power down and steady state operation. Table 15-1 outlines this requirement.

Table 15-1. Dual Power Supply Requirements for the IntelDX4™ Processor

Symbol	Parameter	Min	Max	Unit	Notes
VDIFF	$V_{CC5} - V_{CC}$ Difference		2.25	V	$V_{CC5}$ input should not exceed $V_{CC}$ by more than 2.25V during power-up, power-down or during operation.

Meeting this requirement ensures proper operation of the IntelDX4 processor and guarantees that the current draw into the  $V_{CC5}$  pin will not exceed the  $I_{CC5}$  specification (see section 15.3, "DC Specifications"). If the voltage difference requirement cannot be met due to system design limitations, then an alternate solution may be employed. A minimum of a  $100\Omega$  series resistor may be used to limit the current into the  $V_{CC5}$  pin. This resistor will ensure that current drawn by the  $V_{CC5}$  pin will not exceed the maximum rating of 55 mA for this pin (see section 15.2, "Maximum Ratings").



**Figure 15-1. IntelDX4™ Processor  $V_{CC5}$  Current Limiting Resistor**

Note that this resistor is not necessary if the system can guarantee that the voltage difference between  $V_{CC5}$  and  $V_{CC}$  is always limited to 2.25V, even during power up and power down.

In 3.3V-only systems and systems that will be driving all IntelDX4 processor inputs and I/Os from 3.3V logic, the  $V_{CC5}$  pin should be connected directly to the 3.3V  $V_{CC}$  plane. This will guarantee the voltage difference specification is met and will eliminate the current draw into the  $V_{CC5}$  pin. In a 3.3V-only system, the  $V_{CC5}$  may be connected to the 5V supply as described previously, as long as the voltage differential in Table 15-1 is met, and assuming the current drawn by the  $V_{CC5}$  pin is of little consequence to the system design.

#### 15.1.4 SYSTEM CLOCK RECOMMENDATIONS

It is recommended that the CLK input to the Military Intel486 processor should not be driven until  $V_{CC}$  has reached its normal operating level (either 3.3V or 5V). The CLK input may be grounded or allowed to ramp with  $V_{CC}$  during this period. Once  $V_{CC}$  has reached its normal operating level, the Military Intel486 processor can handle the clock frequency for which it is specified and the oscillator/clock driver should have locked onto its desired frequency.

#### 15.1.5 OTHER CONNECTION RECOMMENDATIONS

NC pins should always remain unconnected. Connection of NC pins to  $V_{CC}$  or  $V_{SS}$  or to any other signal can result in component malfunction or incompatibility with other steppings of the Military Intel486 processor family.

For reliable operation, always connect unused inputs to an appropriate signal level. Active LOW inputs should be connected to  $V_{CC}$  through a pull-up resistor. Pull-ups in the range of 20 k $\Omega$  are recommended. Active HIGH inputs should be connected to GND.

#### 15.2 Maximum Ratings

Table 15-2 is a stress rating only. Functional operation at the maximums is not guaranteed. Function operating conditions are given in Table 15-3 for 3.3V processor DC Specifications, Table 15-5 for 5V DC Specifications, Tables 15-8 and 15-9 for 3.3V processor AC specifications, and Table 15-11 for 5V processor AC specifications.

Extended exposure to the Maximum Ratings may affect device reliability. Furthermore, although the Military Intel486 processor contains protective circuitry to resist damage from static electric discharge, always take precautions to avoid high static voltages or electric fields.

Table 15-2. Absolute Maximum Ratings

Case Temperature under Bias	-65°C to +125°C
Storage Temperature	-65°C to +150°C
DC Voltage on Any Pin with Respect to Ground	-0.5 to $V_{CC} + 0.5V$ -0.5 to $V_{CC5} + 0.5V^{(1)}$
Supply Voltage with Respect to $V_{SS}$	$V_{CC} - 0.5V$ to $+6.5V^{(2)}$ $V_{CC} - 0.5V$ to $+4.6V^{(1)}$ $V_{CC5}^{(1)} - 0.5V$ to $+6.5V^{(1)}$
Transient Voltage on Any Input	-1.6V to $V_{CC5} + 1.6V^{(1,3)}$
Maximum Allowable Current Sink on $V_{CC5}^{(1)}$	55 mA

**NOTES:**

1. For IntelDX4™ processor only.
2. All Military Intel486™ processors except IntelDX4 processor.
3. Maximum voltage on any pin with respect to ground is the lesser of  $V_{CC5} + 1.6V$  or  $6.5V$  for the IntelDX4 processor.

## 15.3 DC Specifications

### 15.3.1 3.3V DC CHARACTERISTICS

Table 15-3 is for IntelDX4 processors.

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**Table 15-3. 3.3V DC Specifications**

Functional operating range:  $V_{CC} = 3.3V \pm 5\%$ ;  $V_{CC5} = 5V \pm 0.25V$  (Note 7);  $T_{CASE} = -55^{\circ}C$  to  $+125^{\circ}C$

Symbol	Parameter	Min	Typ	Max	Unit	Notes
$V_{IL}$	Input LOW Voltage	-0.3		+0.8	V	
$V_{IH}$	Input HIGH Voltage	2.0		$V_{CC5} + 0.3$	V	
$V_{IHC}$	Input HIGH Voltage of CLK	$V_{CC} - 0.6$		$V_{CC} + 0.3$	V	
$V_{OL}$	Output LOW Voltage $I_{OL} = 2.0$ mA $I_{OL} = 100$ $\mu$ A			0.40 0.20 0.45	V V V	
$V_{OH}$	Output HIGH Voltage $I_{OH} = -2.0$ mA	2.4			V	
$I_{CC5}$	$V_{CC5}$ Leakage Current		15	300	$\mu$ A	
$I_{LI}$	Input Leakage Current			$\pm 15$	$\mu$ A	
$I_{IH}$	Input Leakage Current			200	$\mu$ A	
$I_{IL}$	Input Leakage Current			-400	$\mu$ A	
$I_{LO}$	Output Leakage Current			$\pm 15$	$\mu$ A	
$C_{IN}$	Input Capacitance			10	pF	
$C_{OUT}$	Output or I/O Capacitance			14	pF	6
$C_{CLK}$	CLK Capacitance			12	pF	



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**Table 15-4. 3.3V I<sub>CC</sub> Values for IntelDX4™ Processor**

Functional Operating Range: V<sub>CC</sub> = 3.3V ± 5%; V<sub>CC5</sub> = 5V ± 0.25V (Note 7); T<sub>CASE</sub> = -55°C to +125°C

Parameter	Operating Frequency	Typ	Maximum	Notes
I <sub>CC</sub> Active (Power Supply)	100 MHz 75 MHz		1450 mA 1100 mA	1
I <sub>CC</sub> Active (Thermal Design)	100 MHz 75 MHz	1200 mA 900 mA	1300 mA 975 mA	2, 3, 4
I <sub>CC</sub> Stop Grant	100 MHz 75 MHz	50 mA 20 mA	100 mA 75 mA	5
I <sub>CC</sub> Stop Clock	0 MHz	600 μA	1 mA	6

**NOTES:**

1. This parameter is for proper power supply selection. It is measured using the worst case instruction mix at V<sub>CC</sub> = 3.465V.
2. The maximum current column is for thermal design power dissipation. It is measured using the worst case instruction mix at V<sub>CC</sub> = 3.3V.
3. The typical current column is the typical operating current in a system. This value is measured in a system using a typical device at V<sub>CC</sub> = 3.3V, running Microsoft Windows 3.1 at an idle condition. This typical value is dependent upon the specific system configuration.
4. Typical values are not 100% tested.
5. The I<sub>CC</sub> Stop Grant specification refers to the I<sub>CC</sub> value once the Military Intel486 processor enters the Stop Grant or Auto HALT Power Down state.
6. The I<sub>CC</sub> Stop Clock specification refers to the I<sub>CC</sub> value once the processor enters the Stop Clock state. The V<sub>IH</sub> and V<sub>IL</sub> levels must be equal to V<sub>CC</sub> and 0V, respectively, in order to meet the I<sub>CC</sub> Stop Clock specifications.
7. V<sub>CC5</sub> should be connected to 3.3V ± 5% in 3.3V-only systems.

**15.3.2 5V DC CHARACTERISTICS**

Table 15-5 is for Military Intel486™ DX and IntelDX2 Processors.

**Table 15-5. 5V DC Specifications**

 Functional operating range:  $V_{CC} = 5V \pm 0.25V$ ;  $T_{CASE} = -55^{\circ}C$  to  $+125^{\circ}C$ 

Symbol	Parameter	Min	Typ	Max	Unit	Notes
$V_{IL}$	Input LOW Voltage	-0.3		+0.8	V	7
$V_{IH}$	Input HIGH Voltage	2.0		$V_{CC} + 0.3$	V	8
$V_{OL}$	Output LOW Voltage			0.45	V	1
$V_{OH}$	Output HIGH Voltage	2.4			V	2
$I_{LI}$	Input Leakage Current			$\pm 15$	$\mu A$	3
$I_{IH}$	Input Leakage Current			200	$\mu A$	4
$I_{IL}$	Input Leakage Current			-400	$\mu A$	5
$I_{LO}$	Output Leakage Current			$\pm 15$	$\mu A$	
$C_{IN}$	Input Capacitance PGA			20	pF	6
$C_{OUT}$	Output or I/O Capacitance PGA			20	pF	6
$C_{CLK}$	CLK Capacitance PGA			20	pF	6

**1**
**NOTES:**

1. This parameter is measured at: Address, Data, BEn 4.0 mA  
Definition, Control 5.0 mA
2. This parameter is measured at: Address, Data, BEn -1.0 mA  
Definition, Control -0.9 mA
3. This parameter is for inputs without pull-ups or pull-downs and  $0V \leq V_{IN} \leq V_{CC}$ .
4. This parameter is for inputs with pull-downs and  $V_{IH} = 2.4V$ .
5. This parameter is for inputs with pull-ups and  $V_{IL} = 0.45V$ .
6.  $F_C = 1$  MHz; Not 100% tested.
7. Minimum value guaranteed by design characterization but not tested.
8. Maximum value guaranteed by design characterization but not tested.

**Table 15-6. 5V I<sub>CC</sub> Values for Military Intel486™ DX Processor**Functional Operating Range: V<sub>CC</sub> = 5V ± 0.25V; T<sub>CASE</sub> = -55°C to +125°C

Parameter	Operating Frequency	Typ	Maximum	Notes
I <sub>CC</sub> Active (Power Supply)	33 MHz 25 MHz		900 mA 700 mA	1
I <sub>CC</sub> Active (Thermal Supply)	33 MHz 25 MHz	700 mA 550 mA	857 mA 666 mA	2, 3, 4
I <sub>CC</sub> Stop Grant	33 MHz 25 MHz	40 mA 40 mA	80 mA 80 mA	5
I <sub>CC</sub> Stop Clock	0 MHz	200 μA	2 mA	6

**Table 15-7. 5V I<sub>CC</sub> Values for IntelDX2™ Processor**Functional Operating Range: V<sub>CC</sub> = 5V ± 0.25V; T<sub>CASE</sub> = -55°C to +125°C

Parameter	Operating Frequency	Typ	Maximum	Notes
I <sub>CC</sub> Active (Power Supply)	50 MHz 66 MHz		950 mA 1200 mA	1
I <sub>CC</sub> Active (Thermal Supply)	50 MHz 66 MHz	775 mA 975 mA	906 mA 1145 mA	2, 3, 4
I <sub>CC</sub> Stop Grant	50 MHz 66 MHz	35 mA 45 mA	70 mA 90 mA	5
I <sub>CC</sub> Stop Clock	0 MHz	200 μA	2 mA	6

**NOTES:**

1. This parameter is for proper power supply selection. It is measured using the worst case instruction mix at V<sub>CC</sub> = 5.25V.
2. The maximum current column is for thermal design power dissipation. It is measured using the worst case instruction mix at V<sub>CC</sub> = 5V.
3. The typical current column is the typical operating current in a system. This value is measured in a system using a typical device at V<sub>CC</sub> = 5V, running Microsoft Windows 3.1 at an idle condition at room temperature. This typical value is dependent upon the specific system configuration.
4. Typical values are not 100% tested.
5. The I<sub>CC</sub> Stop Grant specification refers to the I<sub>CC</sub> value once the Military Intel486 processor enters the Stop Grant or Auto HALT Power Down state.
6. The I<sub>CC</sub> Stop Clock specification refers to the I<sub>CC</sub> value once the processor enters the Stop Clock state. The V<sub>IH</sub> and V<sub>IL</sub> levels must be equal to V<sub>CC</sub> and 0V, respectively, in order to meet the I<sub>CC</sub> Stop Clock specifications.

## 15.4 AC Specifications

The AC specifications given in the tables in this section consist of output delays, input setup requirements and input hold requirements. All AC specifications are relative to the rising edge of the input system clock (CLK) unless otherwise specified.

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### 15.4.1 3.3V AC CHARACTERISTICS

**Table 15-8. 3.3V AC Characteristics for the 75/25-MHz Intel iDX4™ Processor**

$V_{CC} = 3.3V \pm 5\%$ ;  $V_{CC5} = 5V \pm 0.25V$  (Note 1);  $T_{CASE} = -55^{\circ}C$  to  $+125^{\circ}C$ ;  $C_L = 50$  pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	CLK Frequency	8	25	MHz		2
$t_1$	CLK Period	40	125	ns	15-2	
$t_2$	CLK High Time	14		ns	15-2	at 2V
$t_3$	CLK Low Time	14		ns	15-2	at 0.8V
$t_4$	CLK Fall Time		4	ns	15-2	2V to 0.8V
$t_5$	CLK Rise Time		4	ns	15-2	0.8V to 2V
$t_6$	A2-A31, PWT, PCD, BE0-3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, FERR#, BREQ, HLDA, CACHE#, HITM# Valid Delay	2	19	ns	15-6	
$t_7$	A2-A31, PWT, PCD, BE0-3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, CACHE# Float Delay		28	ns	15-7	3
$t_8$	PCHK# Valid Delay	2	24	ns	15-5	
$t_{8a}$	BLAST#, PLOCK# SMIACK# Valid Delay	2	24	ns	15-6	
$t_9$	BLAST#, PLOCK# Float Delay		28	ns	15-7	3
$t_{10}$	D0-D31, DP0-3 Write Data Valid Delay	2	20	ns	15-6	
$t_{11}$	D0-D31, DP0-3 Write Data Float Delay		28	ns	15-7	3
$t_{12}$	EADS#, INV Setup Time	8		ns	15-3	
$t_{13}$	EADS#, INV Hold Time	3		ns	15-3	
$t_{14}$	KEN#, BS16#, BS8#, WB/WT# Setup Time	8		ns	15-3	
$t_{15}$	KEN#, BS16#, BS8#, WB/WT# Hold Time	3		ns	15-3	
$t_{16}$	RDY#, BRDY# Setup Time	8		ns	15-4	
$t_{17}$	RDY#, BRDY# Hold Time	3		ns	15-4	
$t_{18}$	HOLD, AHOLD Setup Time	8		ns	15-3	
$t_{18a}$	BOFF# Setup Time	8		ns	15-3	
$t_{19}$	HOLD, AHOLD, BOFF# Hold Time	3		ns	15-3	
$t_{20}$	RESET, FLUSH#, A20M#, NMI, INTR, IGNNE# SRESET, STPCLK#, SMI# Setup Time	8		ns	15-3	5
$t_{21}$	RESET, FLUSH#, A20M#, NMI, INTR, IGNNE# SRESET, STPCLK#, SMI# Hold Time	3		ns	15-3	5
$t_{22}$	D0-D31, DP0-3, A4-A31 Read Setup Time	5		ns	15-3, 15-4	
$t_{23}$	D0-D31, DP0-3, A4-A31 Read Hold Time	3		ns	15-3, 15-4	

#### NOTES:

- $V_{CC5}$  should be connected to  $3.3V \pm 5\%$  in 3.3V-only systems.
- 0-MHz operation is guaranteed when the STPCLK# and Stop Grant Acknowledge protocol is used.
- Not 100% tested. Guaranteed by design characterization.
- All timing specifications assume  $C_L = 50$  pF. See capacitive derating charts for additional timing delays due to loading.
- A reset pulse width of 15 CLK cycles is required for warm resets (RESET or SRESET). Power-up resets (cold resets) require RESET to be asserted for at least 1 ms after  $V_{CC}$  and CLK are stable.





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**Table 15-9. 3.3V AC Characteristics for the 100/33-MHz IntelDX4™ Processors**

V<sub>CC</sub> = 3.3V ±5%; V<sub>CC5</sub> = 5V ±0.25V (Note 1); T<sub>CASE</sub> = -55°C to +125°C; C<sub>L</sub> = 50 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	CLK Frequency	8	33	MHz		2
t <sub>1</sub>	CLK Period	30	125	ns	15-2	
t <sub>2</sub>	CLK High Time	11		ns	15-2	at 2V
t <sub>3</sub>	CLK Low Time	11		ns	15-2	at 0.8V
t <sub>4</sub>	CLK Fall Time		3	ns	15-2	2V to 0.8V
t <sub>5</sub>	CLK Rise Time		3	ns	15-2	0.8V to 2V
t <sub>6</sub>	A2-A31, PWT, PCD, BE0-3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, FERR#, BREQ, HLDA, CACHE#, HITM# Valid Delay	2	14	ns	15-6	
t <sub>7</sub>	A2-A31, PWT, PCD, BE0-3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, CACHE# Float Delay		20	ns	15-7	3
t <sub>8</sub>	PCHK# Valid Delay	2	14	ns	15-5	
t <sub>8a</sub>	BLAST#, PLOCK#, SMIACK# Valid Delay	2	14	ns	15-6	
t <sub>9</sub>	BLAST#, PLOCK# Float Delay		20	ns	15-7	3
t <sub>10</sub>	D0-D31, DP0-3 Write Data Valid Delay	2	14	ns	15-6	
t <sub>11</sub>	D0-D31, DP0-3 Write Data Float Delay		20	ns	15-7	3
t <sub>12</sub>	EADS#, INV Setup Time	5		ns	15-3	
t <sub>13</sub>	EADS#, INV Hold Time	3		ns	15-3	
t <sub>14</sub>	KEN#, BS16#, BS8#, WB/WT# Setup Time	5		ns	15-3	
t <sub>15</sub>	KEN#, BS16#, BS8#, WB/WT# Hold Time	3		ns	15-3	
t <sub>16</sub>	RDY#, BRDY# Setup Time	5		ns	15-4	
t <sub>17</sub>	RDY#, BRDY# Hold Time	3		ns	15-4	
t <sub>18</sub>	HOLD, AHOLD Setup Time	6		ns	15-3	
t <sub>18a</sub>	BOFF# Setup Time	7		ns	15-3	
t <sub>19</sub>	HOLD, AHOLD, BOFF# Hold Time	3		ns	15-3	

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**Table 15-9. 3.3V AC Characteristics for the 100/33-MHz IntelDX4™ Processors (Continued)**

V<sub>CC</sub> = 3.3V ±5%; V<sub>CC5</sub> = 5V ±0.25V (Note 1); T<sub>CASE</sub> = -55°C to +125°C; C<sub>L</sub> = 50 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t <sub>20</sub>	RESET, FLUSH#, A20M#, NMI, INTR, IGNNE#, SRESET, STPCLK#, SMI# Setup Time	5		ns	15-3	5
t <sub>21</sub>	RESET, FLUSH#, A20M#, NMI, INTR, IGNNE#, SRESET, STPCLK#, SMI# Hold Time	3		ns	15-3	5
t <sub>22</sub>	D0-D31, DP0-3, A4-A31 Read Setup Time	5		ns	15-3, 15-4	
t <sub>23</sub>	D0-D31, DP0-3, A4-A31 Read Hold Time	3		ns	15-3, 15-4	

**NOTES:**

- V<sub>CC5</sub> should be connected to 3.3V ±5% in 3.3V-only systems.
- 0-MHz operation is guaranteed when the STPCLK# and Stop Grant Acknowledge protocol is used.
- Not 100% tested. Guaranteed by design characterization.
- All timing specifications assume C<sub>L</sub> = 50 pF. See capacitive derating charts for additional timing delays due to loading.
- A reset pulse width of 15 CLK cycles is required for warm resets (RESET or SRESET). Power-up resets (cold resets) require RESET to be asserted for at least 1 ms after V<sub>CC</sub> and CLK are stable.

**Table 15-10. 3.3V IntelDX4™ Processor AC Specifications for the Test Access Port  
(All IntelDX4 Processor Frequencies)**

V<sub>CC</sub> = 3.3V ±5%; V<sub>CC5</sub> = 5V ±0.25V (Note 1); T<sub>CASE</sub> = -55°C to +125°C; C<sub>L</sub> = 50 pF

Symbol	Parameter	Min	Max	Unit	Figure
t <sub>24</sub>	TCK Frequency		25	MHz	
t <sub>25</sub>	TCK Period	40		ns	
t <sub>26</sub>	TCK High Time	10		ns	
t <sub>27</sub>	TCK Low Time	10		ns	
t <sub>28</sub>	TCK Rise Time		4	ns	
t <sub>29</sub>	TCK Fall Time		4	ns	
t <sub>30</sub>	TDI, TMS Setup Time	8		ns	15-8
t <sub>31</sub>	TDI, TMS Hold Time	7		ns	15-8
t <sub>32</sub>	TDO Valid Delay	3	25	ns	15-8
t <sub>33</sub>	TDO Float Delay		30	ns	
t <sub>34</sub>	All Outputs (Non-Test) Valid Delay	3	25	ns	15-8
t <sub>35</sub>	All Outputs (Non-Test) Float Delay		36	ns	15-8
t <sub>36</sub>	All Inputs (Non-Test) Setup Time	8		ns	15-8
t <sub>37</sub>	All Inputs (Non-Test) Hold Time	7		ns	15-8

**NOTES:**

- V<sub>CC5</sub> should be connected to 3.3V ±5% in 3.3V-only systems.
- All inputs and outputs are TTL Level.
- Rise/Fall times are measured between 0.8V and 2.0V. Rise/Fall times can be relaxed by 1 ns per 10-ns increase in TCK period.
- TCK period ≤ CLK period.
- Parameters t<sub>30</sub>-t<sub>37</sub> are measured from TCK.

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15.4.2 5V AC CHARACTERISTICS

Table 15-11 is for 25- and 33-MHz Military Intel486 DX, 50-MHz IntelDX2™ (25-MHz Max.) and 66-MHz IntelDX2 (33-MHz Max.) processors.

**Table 15-11. 5V AC Characteristics**

Functional operating range:  $V_{CC} = 5V \pm 0.25V$ ;  $T_{CASE} = -55^{\circ}C$  to  $+125^{\circ}C$ ;  $C_L = 50$  pF unless otherwise specified. (See also Table 15-12).

Symbol	Parameter	Bus Speed				Unit	Figure	Notes
		25 MHz		33 MHz				
		Min	Max	Min	Max			
	Frequency	8	25	8	33	MHz		1
t <sub>1</sub>	CLK Period	40	125	30	125	ns	15-2	
t <sub>1a</sub>	CLK Period Stability		± 250		± 250	ps	15-2	Adjacent clocks(2)
t <sub>2</sub>	CLK High Time	14		11		ns	15-2	at 2V
t <sub>3</sub>	CLK Low Time	14		11		ns	15-2	at 0.8V(2)
t <sub>4</sub>	CLK Fall Time		4		3	ns	15-2	2V to 0.8V(2)
t <sub>5</sub>	CLK Rise Time		4		3	ns	15-2	0.8V to 2V(2)
t <sub>6</sub>	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, BREQ, HLDA, SMIACK#, FERR# Valid Delay	2	19	2	14	ns	15-6	
t <sub>7</sub>	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, BREQ, HLDA Float Delay		28		20	ns	15-7	2
t <sub>8</sub>	PCHK# Valid Delay	2	24	2	14	ns	15-5	
t <sub>8a</sub>	BLAST#, PLOCK# Valid Delay	2	24	2	14	ns	15-6	
t <sub>9</sub>	BLAST#, PLOCK# Float Delay		28		20	ns	15-7	2
t <sub>10</sub>	D0–D31, DP0–DP3 Write Data Valid Delay	2	20	2	14	ns	15-6	
t <sub>11</sub>	D0–D31, DP0–DP3 Write Data Float Delay		28		20	ns	15-7	2
t <sub>12</sub>	EADS# Setup Time	8		5		ns	15-3	
t <sub>13</sub>	EADS# Hold Time	3		3		ns	15-3	
t <sub>14</sub>	KEN#, BS16#, BS8# Setup Time	8		5		ns	15-3	



**Table 15-11. 5V AC Characteristics (Continued)**

Functional operating range:  $V_{CC} = 5V \pm 0.25V$ ;  $T_{CASE} = -55^{\circ}C$  to  $+125^{\circ}C$ ;  $C_L = 50$  pF unless otherwise specified.

Symbol	Parameter	Bus Speed				Unit	Figure	Notes
		25 MHz		33 MHz				
		Min	Max	Min	Max			
t <sub>15</sub>	KEN#, BS16#, BS8# Hold Time	3		3		ns	15-3	
t <sub>16</sub>	RDY#, BRDY# Setup Time	8		5		ns	15-4	
t <sub>17</sub>	RDY#, BRDY# Hold Time	3		3		ns	15-4	
t <sub>18</sub>	HOLD, AHOLD Setup Time	8		6		ns	15-3	
t <sub>18a</sub>	BOFF# Setup Time	8		7		ns	15-3	
t <sub>19</sub>	HOLD, AHOLD, BOFF# Hold Time	3		3		ns	15-3	
t <sub>20</sub>	FLUSH#, A20M#, NMI, INTR, SMI#, STPCLK#, SRESET, RESET, IGNNE# Setup Time	8		5		ns	15-3	
t <sub>21</sub>	FLUSH#, A20M#, NMI, INTR, SMI#, STPCLK#, SRESET, RESET, IGNNE# Hold Time	3		3		ns	15-3	
t <sub>22</sub>	D0-D31, DP0-DP3, A4-A31 Read Setup Time	5		5		ns	15-3 15-4	
t <sub>23</sub>	D0-D31, DP0-DP3, A4-A31 Read Hold Time	3		3		ns	15-3 15-4	

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**NOTES:**

- 0-MHz operation is guaranteed when the STPCLK# and Stop Grant bus cycle protocol is used.
- Not 100% tested, guaranteed by design characterization.

**Table 15-12. 5V Military Intel486 Processor AC Specifications for the Test Access Port  
(All Processors and Frequencies)**

$V_{CC} = 5V \pm 0.25V$ ;  $T_{CASE} = -55^{\circ}C$  to  $+125^{\circ}C$ ;  $C_L = 50$  pF

Symbol	Parameter	Min	Max	Unit	Notes
t <sub>24</sub>	TCK Frequency		8	MHz	1
t <sub>25</sub>	TCK Period	125		ns	
t <sub>26</sub>	TCK High Time	40		ns	@ 2.0V
t <sub>27</sub>	TCK Low Time	40		ns	@ 0.8V
t <sub>28</sub>	TCK Rise Time		8	ns	2
t <sub>29</sub>	TCK Fall Time		8	ns	2
t <sub>30</sub>	TDI, TMS Setup Time	8		ns	3
t <sub>31</sub>	TDI, TMS Hold Time	10		ns	3
t <sub>32</sub>	TDO Valid Delay	2	30	ns	3
t <sub>33</sub>	TDO Float Delay		36	ns	3
t <sub>34</sub>	All Outputs (Non-Test) Valid Delay	2	30	ns	3
t <sub>35</sub>	All Outputs (Non-Test) Float Delay		36	ns	3
t <sub>36</sub>	All Inputs (Non-Test) Setup Time	8		ns	3
t <sub>37</sub>	All Inputs (Non-Test) Hold Time	10		ns	3

**NOTES:**

1. TCK period  $\leq$  CLK period.
2. Rise/Fall times are measured between 0.8V and 2.0V. Rise/Fall times can be relaxed by 1 ns per 10-ns increase in TCK period.
3. Parameters t<sub>30</sub>-t<sub>37</sub> are measured from TCK.
4. Refer to Figure 15-18 for signal waveforms.

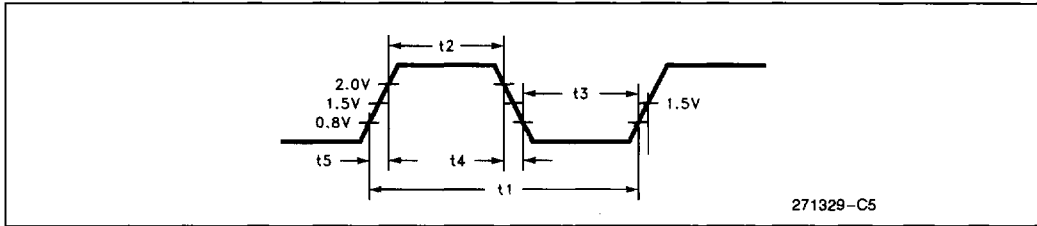


Figure 15-2. CLK Waveforms

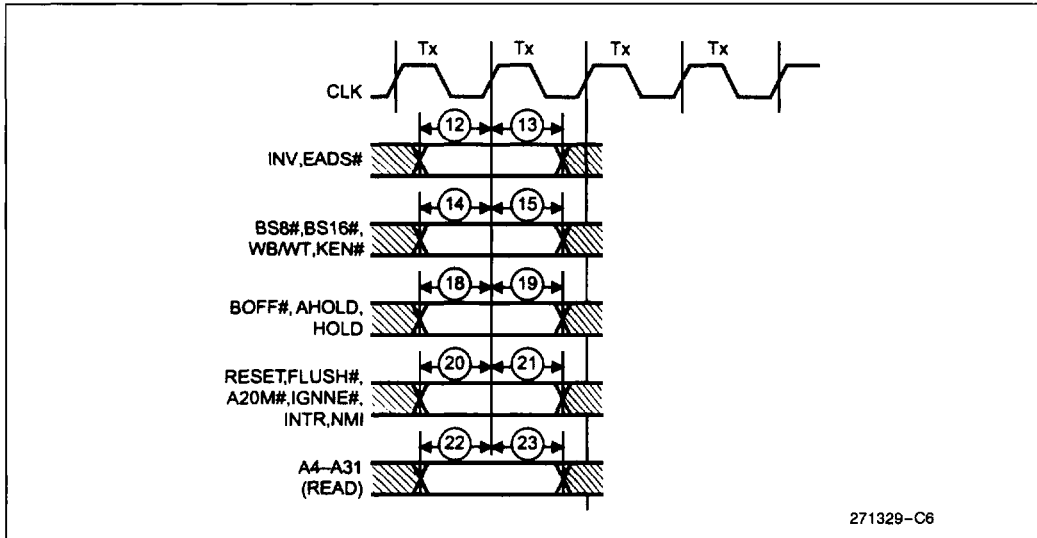


Figure 15-3. Input Setup and Hold Timing

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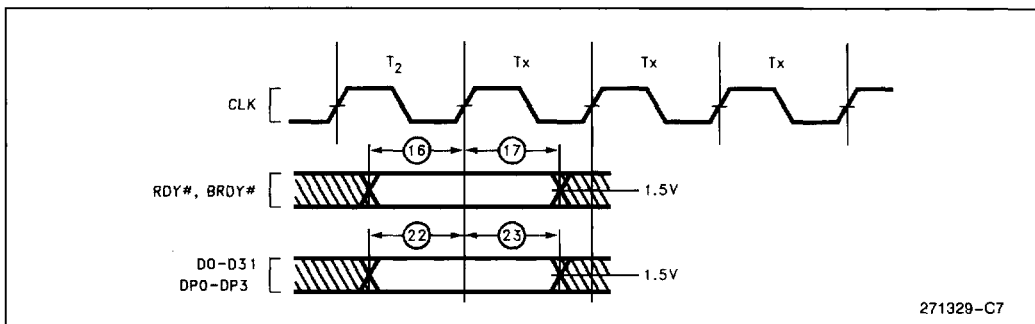


Figure 15-4. Input Setup and Hold Timing

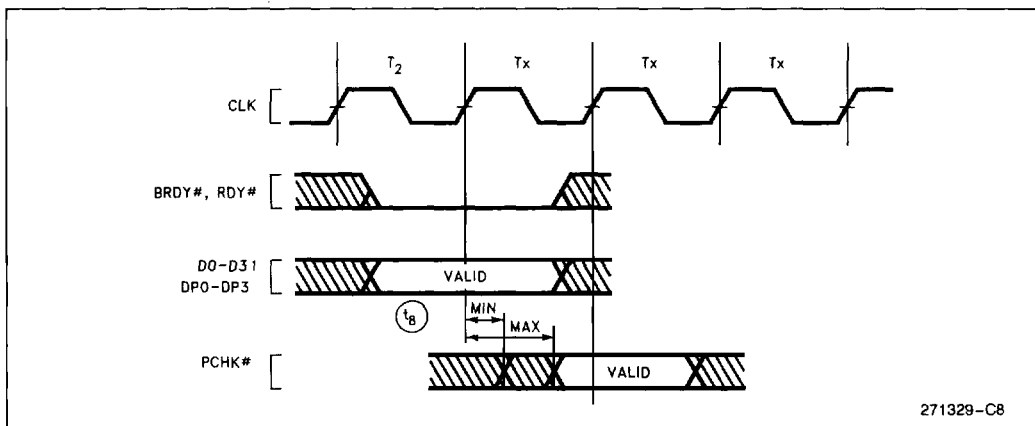


Figure 15-5. PCHK# Valid Delay Timing

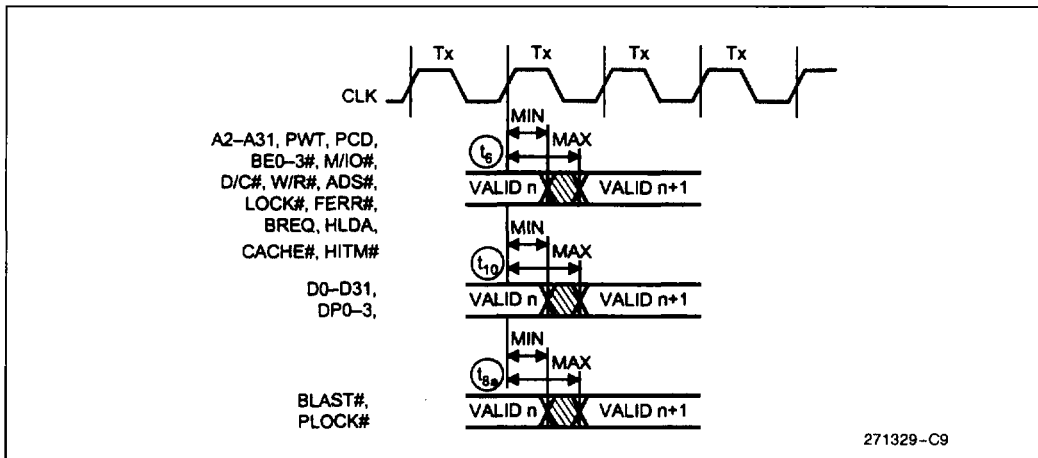


Figure 15-6. Output Valid Delay Timing

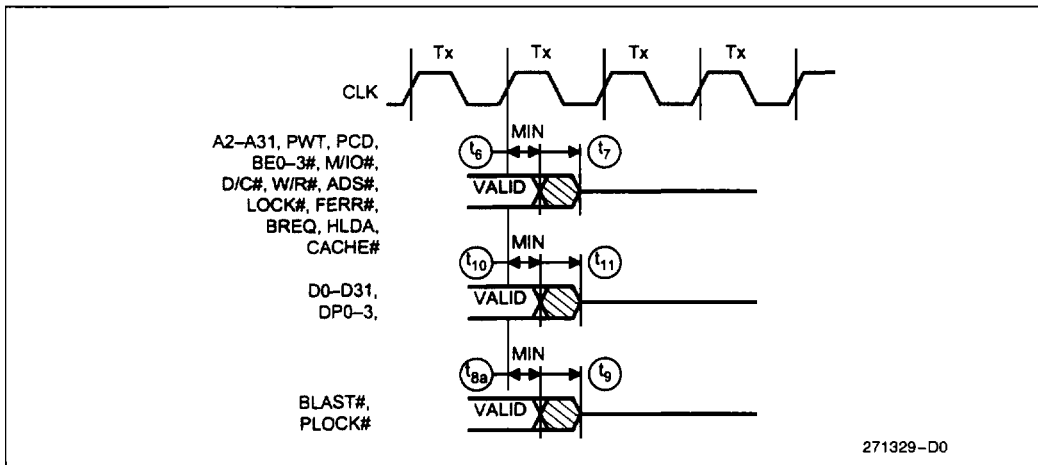


Figure 15-7. Maximum Float Delay Timing

1



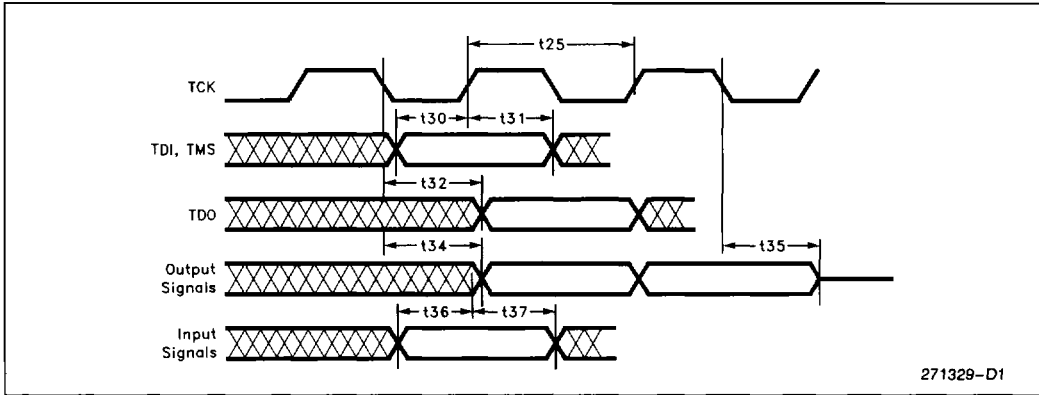
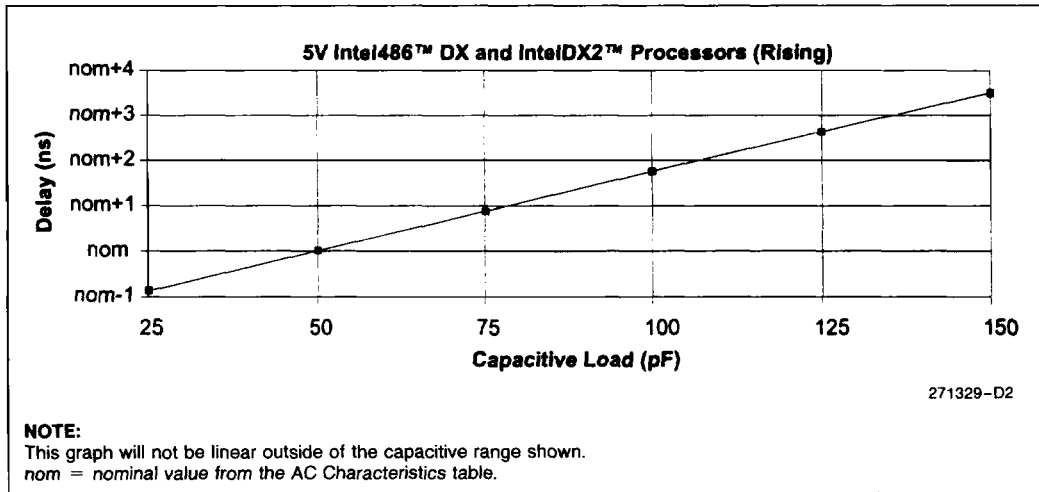


Figure 15-8. Test Signal Timing Diagram

### 15.5 Capacitive Derating Curves

The capacitive derating curves illustrate output delay versus capacitive load for 5V Military Intel486 processors. The derating curves show the delays for the rising and falling edges under worst-case conditions. Figure 15-9 and Figure 15-10 apply to 5V Military

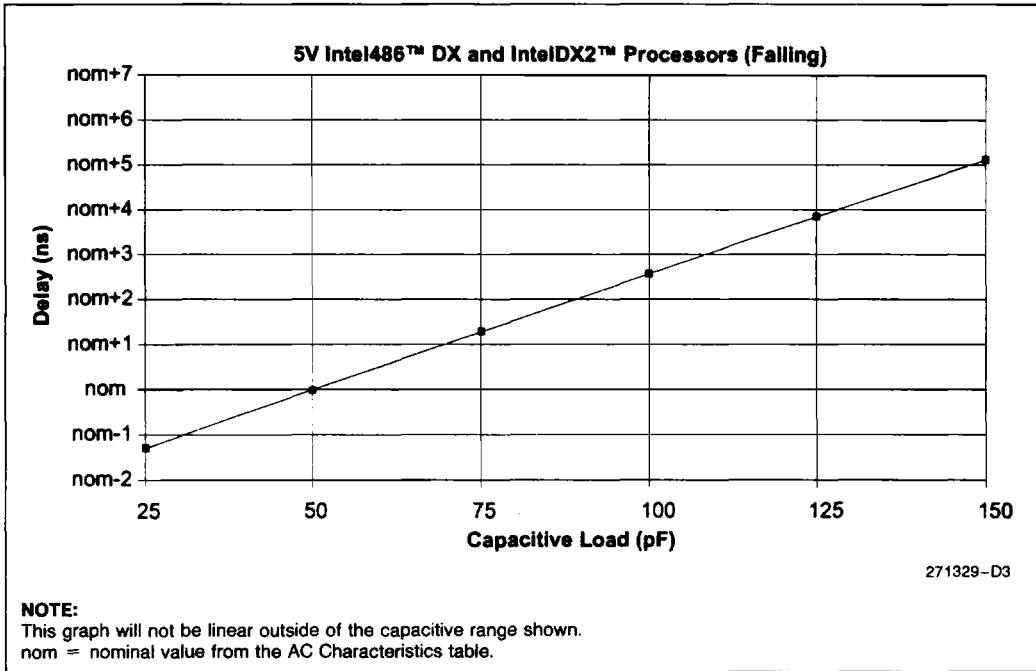
Intel486 DX and IntelDX2 processors. Figures 15-11, 15-12 and 15-13 apply to the IntelDX4 processor. The figures apply to all frequencies specified for each corresponding product. Refer to Appendix B for bus frequencies above 33 MHz for Military Intel486 processors.



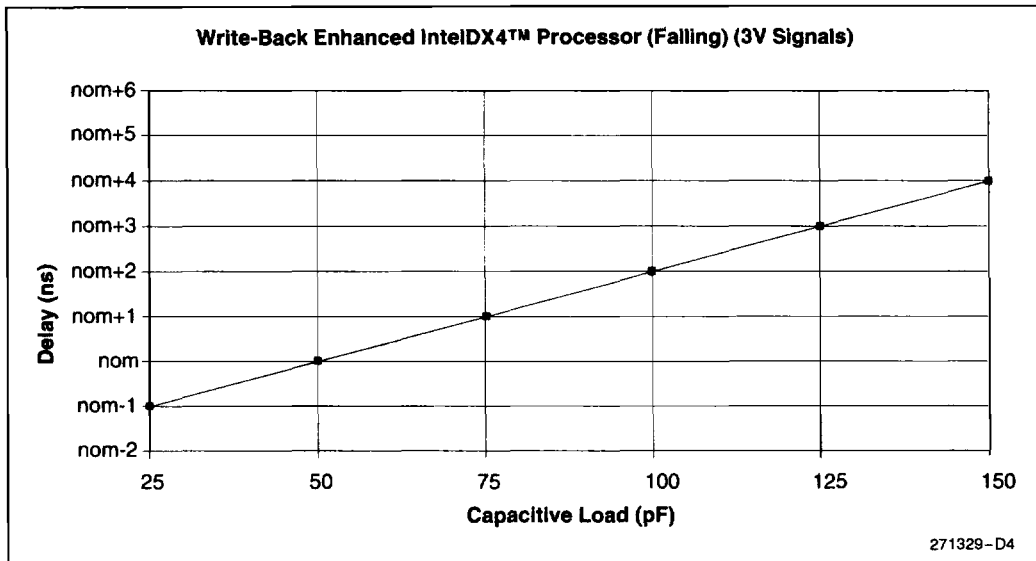
**NOTE:**  
This graph will not be linear outside of the capacitive range shown.  
nom = nominal value from the AC Characteristics table.

Figure 15-9. Typical Loading Delay versus Load Capacitance under Worst-Case Conditions for a Low-to-High Transition

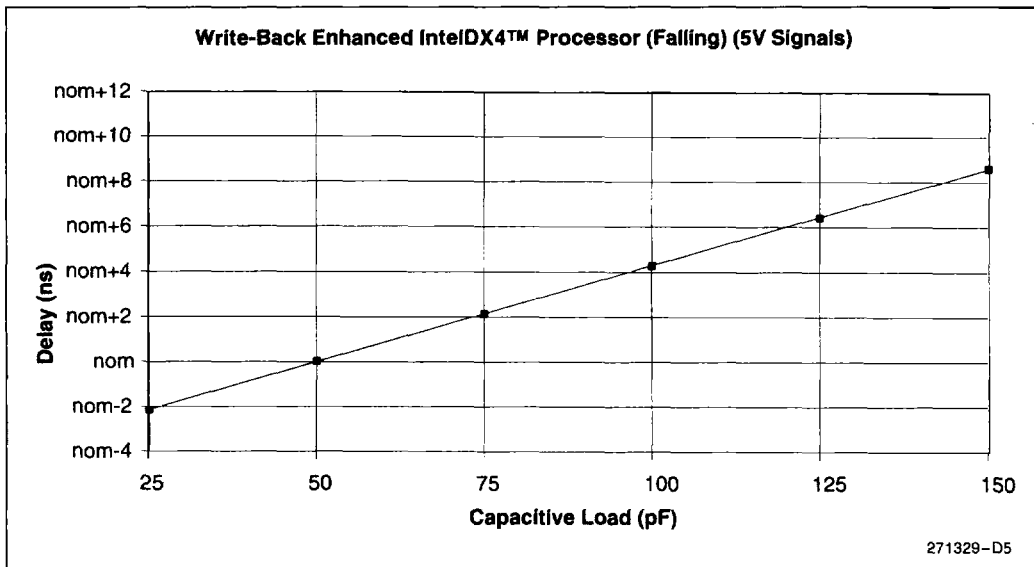
1



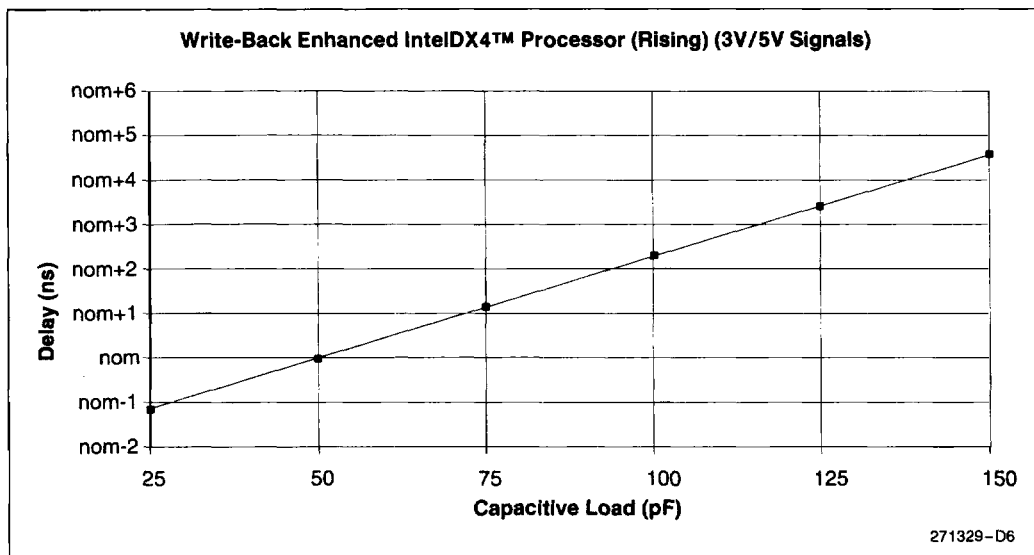
**Figure 15-10. Typical Loading Delay versus Load Capacitance under Worst-Case Conditions for a High-to-Low Transition**



**Figure 15-11. Write-Back Enhanced IntelDX4™ Processor (Falling) (3V Signals)**



**Figure 15-12. Write-Back Enhanced IntelDX4™ Processor (Falling) (5V Signals)**



**Figure 15-13. Write-Back Enhanced IntelDX4™ Processor (Rising) (3V/5V Signals)**