NEC

PRELIMINARY DATA SHEET

V850E/DL3, V850E/DJ3

32-Bit Single-Chip Microcontrollers

Hardware

μPD70F3420, μPD703420,
μPD70F3421, μPD703421,
μPD70F3422, μPD703422,
μPD70F3423,
μPD70F3424,
μPD70F3425,
μPD70F3426,
μPD70F3427

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Chapter 1 Overview

The V850E/DJ3/DL3 is a product in NECEL's V850 family of single-chip microcontrollers designed for Automotive applications.

1.1 General

The V850E/DJ3/DL3 single-chip microcontroller, is a member of NECEL's V850 32-bit RISC family, which match the performance gains attainable with RISC-based controllers to the needs of embedded control applications. The V850 CPU offers easy pipeline handling and programming, resulting in compact code size comparable to 16-bit CISC CPUs.
The V850E/DJ3/DL3 provides an excellent combination of general purpose peripheral functions, like serial communication interfaces (UART, clocked SI), Timers and measurement inputs (A/D converter), with dedicated CAN network support. Control and driver for 6 stepper motors are included.
The device offers power-saving modes to manage the power consumption effectively under varying conditions.
Thus equipped, the V850E/DJ3/DL3 is ideally suited for automotive applications, like dashboard or body. It is also an excellent choice for other applications where a combination of sophisticated peripheral functions and CAN network support is required.

This specification covers the following devices of the family:

Family Code	Part Number	Internal Flash	Internal RAM	LCD	Peripherals
DL3	µPD70F3427GD	1024 kbyte	60 kbytes	LCD I/F	Full set
DJ3	µPD70F3426GJ	2048 kbyte	84 kbytes	LCD I/F	Full set
DJ3	µPD70F3425GJ	1024 kbyte	32 kbytes	LCD I/F	Full set
DJ3	µPD70F3424GJ	512 kbyte	24 kbytes	LCD I/F	Full set
DJ3	µPD70F3423GJ	512 kbyte	20 kbytes	LCD I/F, LCD C/D	Reduced set
DJ3	µPD70F3422GJ	384 kbyte	16 kbytes	LCD I/F, LCD C/D	Reduced set
DJ3	µPD703422GJ	384 kbyte ROM	16 kbytes	LCD I/F, LCD C/D	Reduced set
DJ3	µPD70F3421GJ	256 kbyte	12 kbytes	LCD I/F, LCD C/D	Reduced set
DJ3	µPD703421GJ	256 kbyte ROM	12 kbytes	LCD I/F, LCD C/D	Reduced set
DJ3	µPD70F3420GJ	128 kbyte	6 kbytes	LCD I/F, LCD C/D	Reduced set
DJ3	µPD703420GJ	128kbyte ROM	6 kbytes	LCD I/F, LCD C/D	Reduced set

The following table gives a more detailed overview of the different derivates and their major features.

Table 1-1: DJ3 Family Overview (1/2)

Series name		V850E/DL3	V850E/DJ3	V850E/DJ3	V850E/DJ3	V850E/DJ3	V850E/DJ3	V850E/DJ3	V850E/DJ3	V850E/DJ3	V850E/DJ3	V850E/DJ3
Part Number		uDP70F3427	uDP70F3426	uDP70F3425	uDP70F3424	uDP70F3423	uDP70F3422	uDP703422	uPD70F3421	uPD703421	uDP70F3420	uDP703420
Technology		MF2 (Flash)						MF2 (ROM)	MF2 (Flash)	MF2 (ROM)	MF2 (Flash)	MF2 (ROM)
Internal memory	Flash	1MB	2MB[NOTE1]	1MB	512kB		384kB	None	256kB	None	128kB	None
	ROM	None						384kB	None	256kB	None	128kB
	RAM	60k	84k[NOTE2]	32kB	24kB	20kB	16kB		12kB		6kB	
DMA		4ch										
Operating Clock	Main (internal)	64MHz typ.				32MHz typ.		24MHz typ.	32MHz typ.	24MHz typ.	32MHz typ.	24MHz typ.
	Ring-OSC	240kHz typ.										
	Subclock	32kHz typ.										
I/O ports		101	98									
Input ports		16										
A/D converter		16 ch				12 ch						
Timers	TMZ	10 ch				6 ch						
	TMP	4 ch										
	TMG	3 ch				2 ch						
	WDT	provided										
	Watch	provided										
	Watch calibration	provided										
Serial interfaces	AFCAN	2 ch										
	UARTA	2 ch										
Serial interfaces	CSIB	3 ch				2 ch						
	IIC	2 ch										

Table 1-1: DJ3 Family Overview (2/2)

Series name		V850E/DL3	V850E/DJ3	V850E/DJ3	V850E/DJ3	V850E/DJ3	V850E/DJ3	V850E/DJ3	V850E/DJ3	V850E/DJ3	V850E/DJ3	V850E/DJ3
Part Number		uDP70F3427	uDP70F3426	uDP70F3425	uDP70F3424	uDP70F3423	uDP70F3422	uDP703422	uPD70F3421	uPD703421	uDP70F3420	uDP703420
Interrupts	External	8				7						
	Internal	91				76						
	NMI	2 ch										
Other functions	ROM-correction	8ch (DBTRAP)										
	POC	Provided										
	Voltage comparator	2 ch										
	Clock supervision	Provided										
	Sound generator	1 ch										
	Stepper motor C/D	6 ch										
	LCD C/D	none				40 x 4						
	LCD I/F	Provided										
	Auxilliary frequency output	Provided										
	On-Chip debug	Provided										
	External Mem.-I/F	Provided	none									
Operating voltage		3.2v to 5.5V for core functions, ADC and StepperMotor C/D, 3.0V to 5.5V for all other I/O Full operation in range from 4.0V to 5.5V due to POC function (see chapter 8.2 on page 80)										
Package		208-pin QFP	144-pin QFP									

Notes: 1. For the DJ3 derivative µPD70F3426, the upper 1MB of the flash memory is connected to the internal system bus (VSB). In case performing consecutive accesses to that part of the flash-memory, a 32-bit data access requires two cycles.

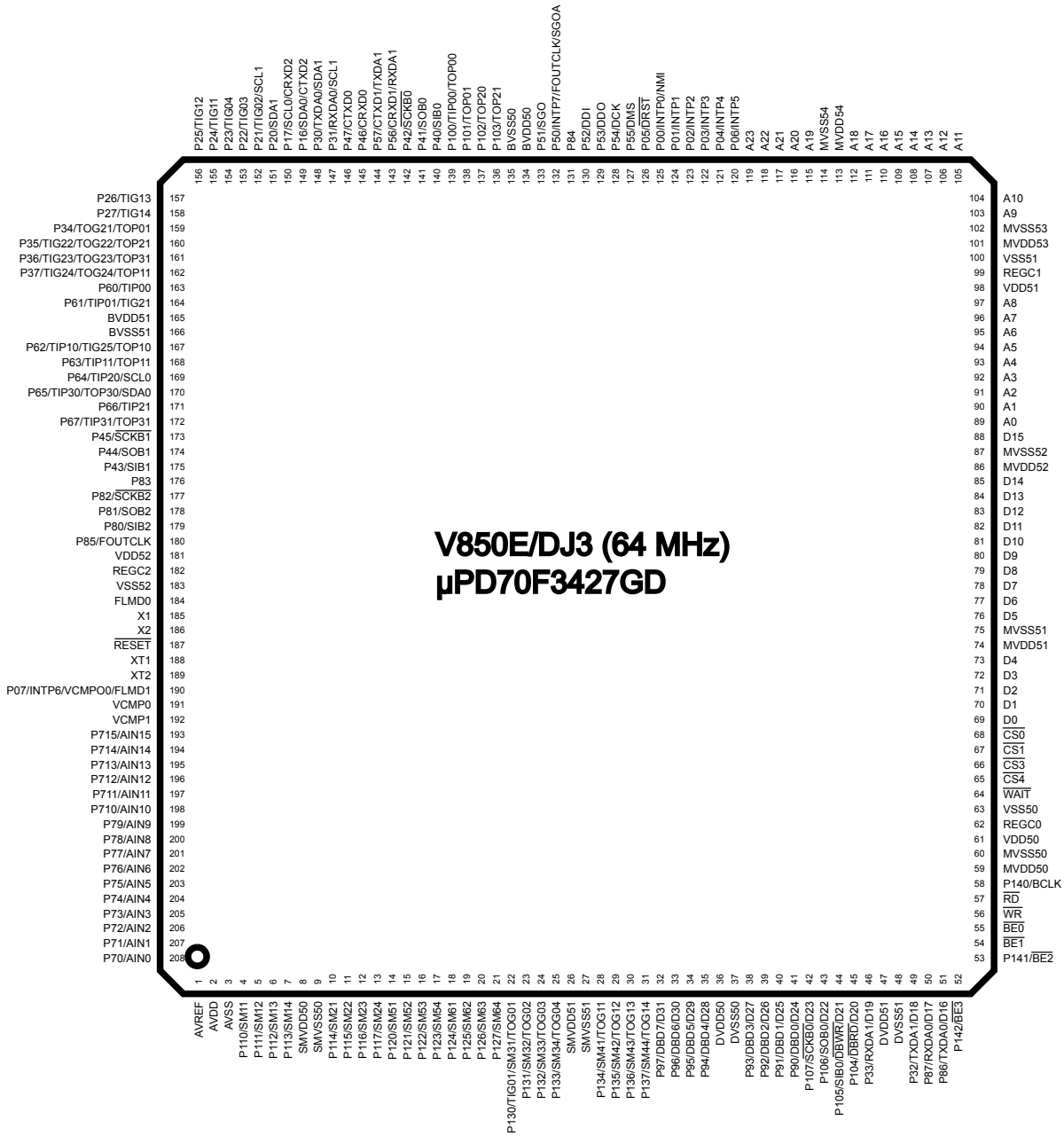
2. For the DJ3 derivative µPD70F3426, the upper 24kB of the internal RAM is connected to the internal system bus (VSB). In case performing consecutive accesses to that part of the internal RAM, a 32-bit data access requires two cycles.

Chapter 2 Pinout Information

2.1 Pinconfiguration µPD70F3427

- µPD70F3427GJ

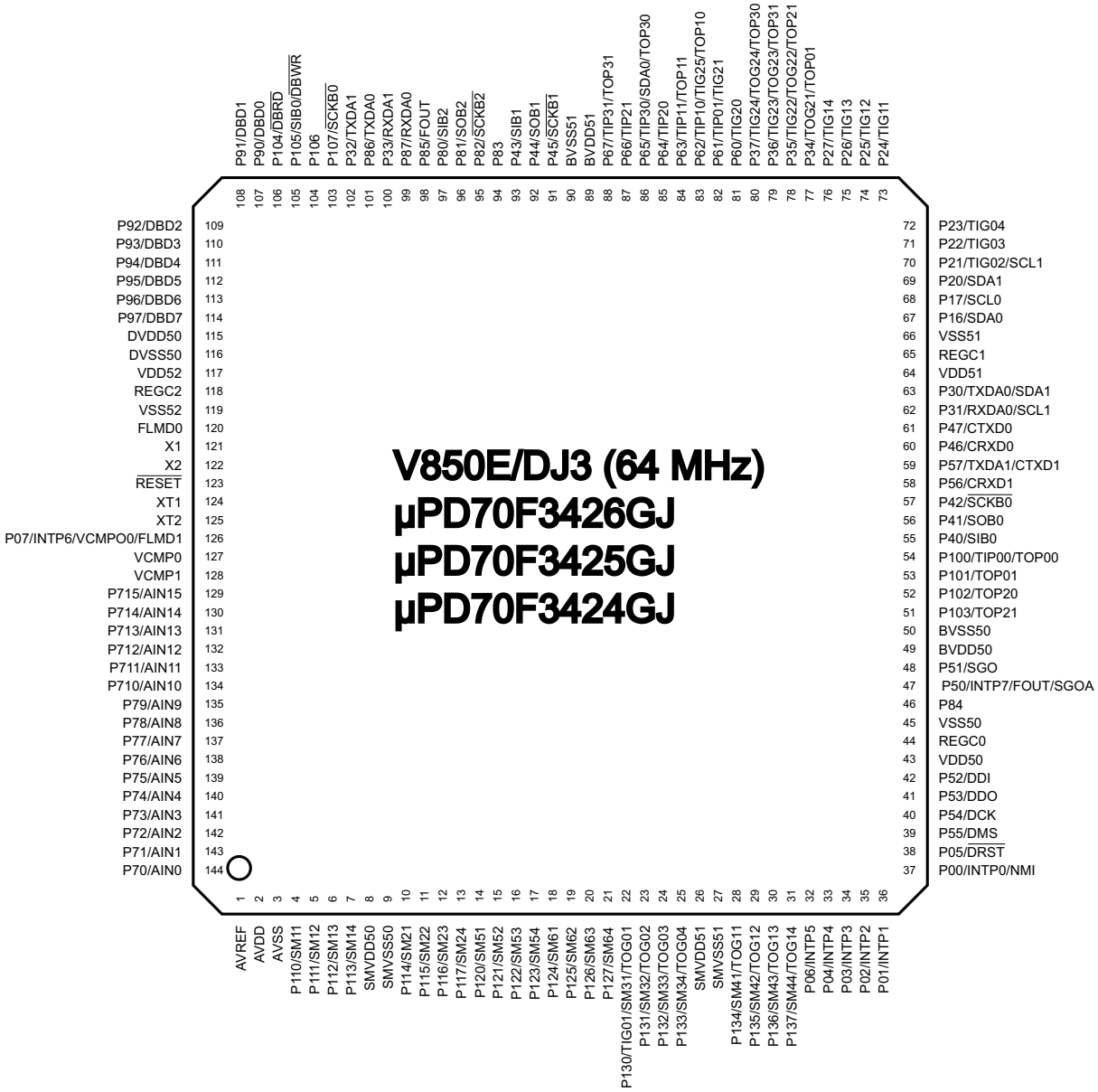
Figure 2-1: Pin Configuration µPD70F3427



2.2 Pinconfiguration µPD70F3426, µPD70F3425, µPD70F3424

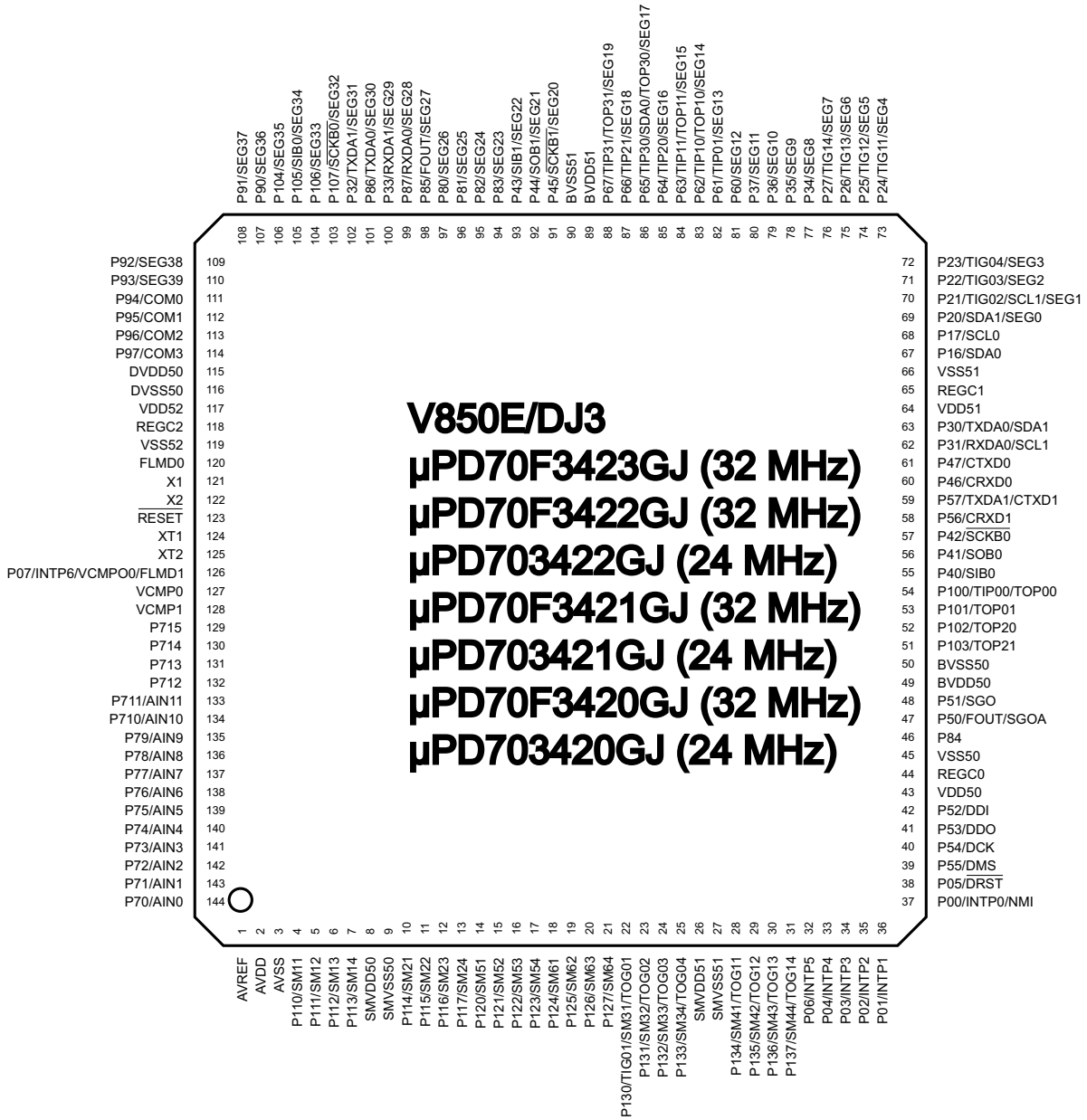
- µPD70F3426GJ,
- µPD70F3425GJ,
- µPD70F3424GJ

Figure 2-2: Pin Configuration µPD70F3426, µPD70F3425, µPD70F3424



2.3 Pinconfiguration µPD70F3423, µPD70F3422, µPD703422, µPD70F3421, µPD703421, µPD70F3420, µPD703420

- µPD70F3423GJ,
- µPD70F3422GJ,
- µPD703422GJ,
- µPD70F3421GJ,
- µPD703421GJ,
- µPD70F3420GJ,
- µPD703420GJ



2.4 Pin Group information

- Pin Groups 1x: Pins supplied by BV_{DD5}**Note1**
  1A: (P00-06, P50-55, P84)
  1B: (P16-17, P30-31, P40-42, P46-47, P56-57, P100-103)
  1C: (P20-27, P34-37, P60-67)
  1D: (P43-45, P80-83, P85)
- Pin Groups 1x: Pins supplied by BV_{DD5}**Note2**
  1A: (P00-06, P50-55, P84)
  1B: (P16-17, P30-31, P40-42, P46-47, P56-57, P100-103)
  1C: (P20-27, P34-37, P60-61)
  1D: (P62-67, P43-45, P80-83, P85)
- Pin Group 2: Pins supplied by V_{DD5}
  2: ($\overline{\text{RESET}}$, FLMD0, P07)
- Pin Group 3**Note1**: GPIO and LCD Bus interface supplied by DV_{DD5}
  3: (P32-33, P86-87, P90-97, P104-107)
- Pin Group 3**Note2**: GPIO and LCD Bus and external memory interface supplied by DV_{DD5}
  3: (P32-33, P86-87, P90-97, P104-107, P141-142)
  3A: (P94-97)
  3B: (P90-93)
  3C: (P33, P104-107)
  3D: (P32, P86-87, P141-142)
- Pin Group 4: Stepper Motor outputs supplied by SMV_{DD5}
  4A: (P110-117, P120-123)
  4B: (P124-127, P130-137)
- Pin Group 5: ADC Inputs supplied by AV_{DD}
  5: (P70…P715)
- Pin Group 6**Note2**: External memory Interface supplied by MV_{DD5}
  6: (A0-23, D0-15, $\overline{\text{CS}}$0-1, $\overline{\text{CS}}$3-4, $\overline{\text{WAIT}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{BE}}$0-1, P140)
  6A: ($\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{BE}}$0-1 , P140)
  6B: ($\overline{\text{CS}}$0-1, $\overline{\text{CS}}$3-4 , $\overline{\text{WAIT}}$)
  6C: (D0-4)
  6D: (D5-9)
  6E: (D10-14)
  6F: (D15, A0-3)
  6G: (A4-18)
  6H: (A9-13)
  6I: (A14-18)
  6J: (A19-23)
- Pin Group 8: Voltage Comparator Inputs supplied by AV_{DD}
  8: (VCMP0-1)

Notes: 1. µPD70F3426, µPD70F3425, µPD70F3424, µPD70F3423, µPD70F3422, µPD703422, µPD70F3421, µPD703421, µPD70F3420, µPD703420

2. µPD70F3427

Chapter 3 Absolute Maximum Ratings

Condition 1:
T_A = -40 ... +85°C,
Operation Modes: RUN, HALT, IDLE
Power dissipation: < 1.3W (µPD70F3427, µPD70F3426, µPD70F3425, µPD70F3424)
< 1.0W (µPD70F3423, µPD70F3422, µPD703422, µPD70F3421, µPD703421, µPD70F3420, µPD703420)
Duration: 15000 hours
V_{SS5} = 0V

Condition 2:
T_A = -40 ... +85°C,
Operation Modes: WATCH, Sub-WATCH, STOP, Sub-Clock CPU Operation
Power dissipation: < 0.5W
Duration: 15 years
V_{SS5} = 0V

Table 3-1: Absolute maximum ratings

Parameter		Symbol	Test Conditions	Ratings [a]	Unit
Supply voltage		V_{DD5}		-0.5 ~ +6.5	V
		AV_{DD}		-0.5 ~ +6.5	V
		AV_{REF}		-0.5 ~ +6.5	V
		BV_{DD5}		-0.5 ~ +6.5	V
		DV_{DD5}		-0.5 ~ +6.5	V
		SMV_{DD5}		-0.5 ~ +6.5	V
		MV_{DD5} [b]		-0.5 ~ +6.5	V
		AV_{SS}		-0.5 ~ +0.5	V
		BV_{SS5}		-0.5 ~ +0.5	V
		DV_{SS5}		-0.5 ~ +0.5	V
		SMV_{SS5}		-0.5 ~ +0.5	V
		MV_{SS5} [b]		-0.5 ~ +0.5	V
Input voltage	Group 1	V_{I1}	$V_{I1} < BV_{DD5} + 0.5$ V	-0.5 ~ + 6.5	V
	Group 2	V_{I2}	$V_{I2} < V_{DD5} + 0.5$ V	-0.5 ~ + 6.5	V
	Group 3	V_{I3}	$V_{I3} < DV_{DD5} + 0.5$ V	-0.5 ~ + 6.5	V
	Group 4	V_{I4}	$V_{I4} < SMV_{DD5} + 0.5$ V	-0.5 ~ + 6.5	V
	Group 5, 8 AVREF	V_{IA}	$V_{IA} < AV_{DD} + 0.5$ V	-0.5 ~ + 6.5	V
	Group 6 [b]	V_{I6}	$V_{IM} < MV_{DD5} + 0.5$ V	-0.5 ~ + 6.5	V

Table 3-1: Absolute maximum ratings (Continued)

Parameter		Symbol	Test Conditions	Ratings [a]	Unit
Special [c]	X1, X2, XT1, XT2, REGC0-2	V_{IS}		-0.5 ~ + 3.6	V
Output voltage		V_O		-0.5 ~ +6.5	V
Operating temperature (ambient)		T_{OPR}		-40 ~ +85	°C
Storage temperature		T_{STGB}		-40 ~ +150	°C

a. Currents are average current over the given life time. Transient currents are not relevant as long as the average of transient is below the given value.

b. µPD70F3427 only.

c. These pins are for special use only and should not be used for other connections than specified. Pins operate with the internal generated core voltage.

Note: See “Pinout Information” on page 11. for pin to group association.

V_{DD5} is the supply voltage for the internal voltage regulators applied to pins V_{DD5x}.
V_{SS5} is the ground for the internal logic applied to pins $V_{SS5x.}$
A_{VDD} is the supply for analog part of the A/D converter.
A_{VSS} is the ground for the analog part of the A/D converter.
BV_{DD5} is the supply voltage for the I/O buffers applied to pins $BV_{DD5x.}$
BV_{SS5} is the ground for the I/O buffers applied to pins $BV_{SS5x.}$
DV_{DD5} is the supply voltage for the I/O buffers that support the LCD bus I/F applied to pins $DV_{DD5x.}$
DV_{SS5} is the ground for the I/O buffers that support the LCD bus I/F applied to pins $DV_{SS5x.}$
SMV_{DD5} is the supply voltage for the I/O buffers of the stepper motor drivers applied to pins $SMV_{DD5x.}$
SMV_{SS5} is the ground for the I/O buffers of the stepper motor drivers applied to pins $SMV_{SS5x.}$
MV_{DD5} is the supply voltage for the I/O buffers of the external memory interface applied to pins $MV_{DD5x.}$
MV_{SS5} is the ground for the I/O buffers of the external memory interface applied to pins $MV_{SS5x.}$

Condition 1:
T_A = -40 ... +85°C,
Operation Modes: RUN, HALT, IDLE
Power dissipation: < 1.3W (µPD70F3427, µPD70F3426, µPD70F3425, µPD70F3424)
< 1.0W (µPD70F3423, µPD70F3422, µPD703422, µPD70F3421, µPD703421, µPD70F3420, µPD703420)
Duration: 15000 hours
V_{SS5} = 0V

Condition 2:
T_A = -40 ... +85°C,
Operation Modes: WATCH, Sub-WATCH, STOP, Sub-Clock CPU Operation
Power dissipation: < 0.5W
Duration: 15 years
V_{SS5} = 0V

Table 3-2: Absolute maximum ratings currents

Parameter		Symbol	Test Conditions	Ratings average [a]	Ratings peak [b]	Unit
Output current low	1 pin	I_{OL1}	Groups 1A, 1B, 1C, 1D	30	40	mA
	All pins	I_{OLA1A}	Group 1A	40	60	mA
	All pins	I_{OLA1B}	Group 1B	40	60	mA
	All pins	I_{OLA1AB}	Sum of Groups 1A, 1B	60	100	mA
	All pins	I_{OLA1C}	Group 1C	40	60	mA
	All pins	I_{OLA1D}	Group 1D	40	60	mA
	All pins	I_{OLA1CD}	Sum of Groups 1C, 1D	60	100	mA
	1 pin	I_{OL2}	Group 3[c]	30	40	mA
	All pins	I_{OLA2}	Groups 3A, 3B, 3C, 3D[d]	40	60	mA
	All pins	$I_{OLA2SAB}$	Sum of Groups 3A, 3B [d]	60	100	mA
	All pins	$I_{OLA2SCD}$	Sum of Groups 3C, 3D [d]	60	100	mA
	1 pin	I_{OL3}	Group 4A	45	55	mA
	All pins	I_{OLA3}		200	270	mA
	1 pin	I_{OL4}	Group 4B	45	55	mA
	All pins	I_{OLA4}		200	270	mA
	1 pin	I_{OL6}	Groups 6A-6J [d]	30	40	mA
	All pins	I_{OLA6}		60	100	mA

Table 3-2: Absolute maximum ratings currents (Continued)

Parameter		Symbol	Test Conditions	Ratings average [a]	Ratings peak [b]	Unit
Output current high	1 pin	I_{OH1}	Groups 1A, 1B, 1C, 1D	-30	-40	mA
	All pins	I_{OHA1A}	Group 1A	-40	-60	mA
	All pins	I_{OHA1B}	Group 1B	-40	-60	mA
	All pins	I_{OHA1AB}	Sum of Groups 1A, 1B	-60	-100	mA
	All pins	I_{OHA1C}	Group 1C	-40	-60	mA
	All pins	I_{OHA1D}	Group 1D	-40	-60	mA
	All pins	I_{OHA1CD}	Sum of Groups 1C, 1D	-60	-100	mA
	1 pin	I_{OH2}	Group 3 [c]	-30	-40	mA
	All pins	I_{OHA2}	Groups 3A, 3B, 3C, 3D [d]	-40	-60	mA
	All pins	$I_{OHA2SAB}$	Sum of Groups 3A, 3B [d]	-60	-100	mA
	All pins	$I_{OHA2SCD}$	Sum of Groups 3C, 3D [d]	-60	-100	mA
	1 pin	I_{OH3}	Group 4A	-45	-55	mA
	All pins	I_{OHA3}		-200	-270	mA
	1 pin	I_{OH4}	Group 4B	-45	-55	mA
	All pins	I_{OHA4P}		-200	-270	mA
	1 pin	I_{OH6}	Groups 6A-6J [d]	-30	-40	mA
	All pins	I_{OHA6}		-60	-100	mA

a. Average currents are average current over the given life time. Transient currents are not relevant as long as the average of transient is below the given value.

b. The peak current sets the limit for short term current flows.

c. µPD70F3426, µPD70F3425, µPD70F3424, µPD70F3423, µPD70F3422, µPD703422, µPD70F3421, µPD703421, µPD70F3420, µPD703420

d. µPD70F3427 only

Chapter 4 General Characteristics

4.1 Requirements for external connections

The user have to ensure a low resistive connection of all VSS pins on the PCB. This specification denotes this as:

$V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = MV_{SS5}$ (µPD70F3427) = $AV_{SS} = 0$ V

in the further text.

The user has to ensure a low resistive connection of all V_{DD5x} pins.

The user has to ensure a low resistive connection of all BV_{DD5x} pins.

The user has to ensure a low resistive connection of all SMV_{DD5x} pins.

The user has to ensure a low resistive connection of all DV_{DD5x} pins.

The user has to ensure a low resistive connection of all MV_{DD5x} pins (µPD70F3427).

4.2 Capacitance connected to REGCx

The Device requires to connect capacitors with the following parameters to each of the pins REGC0, REGC1 and REGC2 individually.

The pins REGC0, REGC1, REGC2 must not be connected externally.

Table 4-1: External Capacitance Requirement

Parameter	Symbol	Test Conditions	Min.	Typ	Max.	Unit
Capacitance	C_{REG}		3.3	4.7	10	µF
ESR of capacitance	C_{ESR}	F0 = 100kHz			0.6	Ω

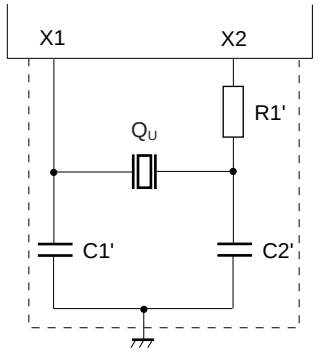
4.3 Main Oscillator Characteristics

T_A = -40 ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427)
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
V_{DD5} = 3.2 V ~ 5.5 V, (see “Power On Clear” on page 80 for further functional restriction),
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} (µPD70F3427) = 0 V

A ceramic or crystal resonator has to be connected to the main clock input pins as shown in figure 4-1.

Note: External clock supply not possible in user mode due to oscillator circuit limitation.

Figure 4-1: Recommended Main Oscillator Circuit



Note: Values of C_1, C_2 and R depend on the used crystal or resonator and must be specified in cooperation with crystal/resonator manufacturer.

Cautions: 1. External clock input is prohibited.

2. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figure to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

Table 4-2: Main Oscillator Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Oscillation stabilization time	T_{OST}	OSC MODE			16 [a]	ms
X1, X2 Oscillator Frequency	f_{OSC}		3.6	4.0	4.4	MHz

a. T_{OST} depends on the external crystal. Value might be improved after evaluation

Remark: This value is valid only for crystal operation.

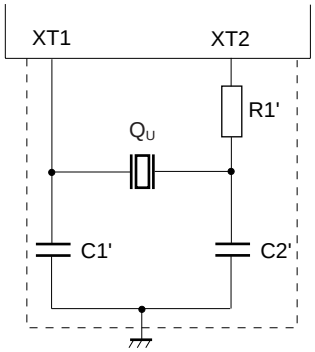
4.4 Sub-Oscillator Characteristics

T_A = -40 ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427)
V_{DD5} = 3.2 V ~ 5.5 V, (see “Power On Clear” on page 80 for further functional restriction),
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} (µPD70F3427) = 0V

A crystal resonator has to be connected to the sub clock input pins as shown in figure 4-2.

Note: External clock supply not possible in user mode due to oscillator circuit limitation.

Figure 4-2: Recommended Sub Oscillator Circuit



Note: Values of C_{S1}, C_{S2} and R_S depend on the used crystal and must be specified in cooperation with crystal manufacturer.

Cautions: 1. External clock input is prohibited.

2. When using the sub system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figure to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

Table 4-3: Sub Oscillator Characteristics

Parameter	Symbol	Test Conditions	Min.	Typ	Max	Unit
XT1,XT2 Oscillator Frequency	f_{SOSC}		32	32.768	35	KHz
Sub oscillator stabilization time	T_{SOST}				5 [a]	s

a. T_{SOST} depends on the external crystal. Value might be improved after evaluation

Remark: These values are valid only for crystal operation.

4.5 Peripheral PLL Characteristics

T_A = -40 ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427)
V_{DD5} = 3.2 V ~ 5.5 V, (see “Power On Clear” on page 80 for further functional restriction),
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427)

Table 4-4: Peripheral PLL Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
PLL Startup Time	T_{PST}	OSC MODE			1.2	ms
PLL Output period jitter [a]	T_{PJ}	Peak to peak			1	ns
PLL Long term jitter [a]	T_{LJ}	Time = 20µs			2	ns

a. Not tested in production. Specified by design.

4.6 Spread Spectrum PLL Characteristics

T_A = -40 ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427)
V_{DD5} = 3.2 V ~ 5.5 V, (see “Power On Clear” on page 80 for further functional restriction),
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427)

Table 4-5: Spread Spectrum PLL Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
SSCG Startup Time	T_{SSCGST}	OSC MODE			1.2	ms
SSCG Frequency modulation range [a]	DITHER	OSC MODE	0		±5	%
SSCG center frequency during dithering [a]	f_{DITHER}			1.0 * $f_{nominal}$		
SSCG modulation frequency [a]	f_{Mod}	SCFMC2-0 = [b] 000 001 010 011 100		 20 30 40 50 60		kHz

a. Not tested in production. Specified by design.

b. The typical modulation frequency can be selected by register SCFMC.

4.7 Ring Oscillator Characteristics

T_A = -40 ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427)
V_{DD5} = 3.2 V ~ 5.5 V, (see “Power On Clear” on page 80 for further functional restriction),
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427)

Table 4-6: Ring Oscillator Characteristics

Parameter	Symbol	Test Conditions	Min.	Typ	Max	Unit
Ring Oscillator Frequency	f_{RING}		200	240	300	KHz
Ring oscillator Stabilization Time [a]	T_{ROST}				20	µs

a. Not tested in production. Specified by design.

4.8 I/O Capacitances

T_A = -40 ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427)
V_{DD5} = 3.2 V ~ 5.5 V, (see “Power On Clear” on page 80 for further functional restriction),
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427)

Table 4-7: I/O Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz Unmeasured pins returned to 0 V			10	pF
Input/output capacitance, all I/O pins except group 4	C_{IO}				15	pF
Input/output capacitance Group 4	C_{IO4}				30	pF

Chapter 5 Operation Conditions

5.1 CPU Clock

T_A = -40 ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427)
V_{DD5} = 3.2 V ~ 5.5 V, (see “Power On Clear” on page 80 for further functional restriction),
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427)

Table 5-1: CPU Clock Frequencies

Clock Mode	Prescale	Operation Mode	Device	CPU Operation Clock Frequency [MHz]
OSC mode	n/a	all modes	all	4
OSC mode, PLL x8	1/2			16
OSC mode, PLL x8	n/a		µPD70F3427, µPD70F3426, µPD70F3425, µPD70F3424, µPD70F3423, µPD70F3422, µPD70F3421, µPD70F3420	32
OSC mode, SSCG x12	1/6		all	8
OSC mode, SSCG x16	1/4			16
OSC mode, SSCG x12	1/2			24
OSC mode, SSCG x16	1/2		µPD70F3427, µPD70F3426, µPD70F3425, µPD70F3424, µPD70F3423, µPD70F3422, µPD70F3421, µPD70F3420	32
OSC mode, SSCG x12	1/1		µPD70F3427, µPD70F3426, µPD70F3425, µPD70F3424	48
OSC mode, SSCG x16	1/1		µPD70F3427, µPD70F3426, µPD70F3425, µPD70F3424	64
OSC mode, Ring OSC	n/a		all	0.2
OSC mode, Sub OSC	n/a			0.032

5.2 Peripheral Clock

T_A = -40 ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427)
V_{DD5} = 3.2 V ~ 5.5 V, (see “Power On Clear” on page 80 for further functional restriction),
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427)

Table 5-2: Peripheral Clock Frequencies

Clock	Clock Source	Max	Unit
PCLK0 - 1	Main OSC	4	MHz
	Main OSC, PLL x 8	16, 8	MHz
PCLK2 - 15	Main OSC	4, 2, ... , 1/2048	MHz
IICLK	Main OSC	4	MHz
	Main OSC, PLL x8	32	MHz
SPCLK0 - 1	Main OSC	4	MHz
	Main OSC, PLL x8	16, 8	MHz
SPCLK2 - 15	Main OSC	4, 2 ... 1/2048	MHz
FOUT (CLKOUT)	Main OSC, PLL x8	32	MHz
	Main OSC, SSCG	32	MHz
	Main OSC	4	MHz
	Sub-OSC	0.032	MHz
	Ring-OSC	0.2	MHz
LCDCLK	Main OSC	4	MHz
	Ring OSC	0.2	MHz
	Sub OSC	0.032	MHz
WTCLK	Main OSC	4	MHz
	Ring OSC	0.2	MHz
	Sub OSC	0.032	MHz
WDTCLK	Main OSC	4	MHz
	Ring OSC	0.2	MHz
	Sub OSC	0.032	MHz
WCTCLK	Main OSC	4	MHz
	PCLK1	see PCLK1	MHz

Chapter 6 DC Characteristics

6.1 General DC Characteristics

T_A = -40 ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427)
V_{DD5} = 3.2 V ~ 5.5 V, (see “Power On Clear” on page 80 for further functional restriction),
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427)

Table 6-1: DC General Specs

Parameter	Pin Group	Symbol	Test Conditions	Min.	Typ	Max.	Unit
Input leakage	1	I_{LI1}	0 <= V_I <= BV_{DD5}	-1		+1	µA
	2	I_{LI2}	0 <= V_I <= V_{DD52}	-1		+1	µA
	3	I_{LI3}	0 <= V_I <= DV_{DD5}	-1		+1	µA
	5	I_{LIA}	0 <= V_I <= AV_{DD}	-0.2		+0.2	µA
	8	I_{LIAD}	0 <= V_I <= AV_{DD}	-2		+1	µA
	4	I_{LIS}	0 <= V_I <= SMV_{DD5}	-10		+10	µA

6.2 Pin Group 1

Pin Groups 1x: Pins supplied by BV_{DD5}

- 1A: (P00-06, P50-55, P84)
  1B: (P16-17, P30-31, P40-42, P46-47, P56-57, P100-103)
  1C: (P20-27, P34-37, P60-67)
  1D: (P43-45, P80-83, P85)

T_A = -40 ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 4.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427)
V_{DD5} = 3.2 V ~ 5.5 V, (see “Power On Clear” on page 80 for further functional restriction),
$V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS}$ = 0 V
MV_{SS5} = 0 V (µPD70F3427)

Table 6-2: Pin Group 1 Normal Operating Range

Parameter	Pin mode[a]	Pin Group	Symbol	Test Conditions	Min.	Typ	Max.	Unit
Input voltage high	Schmitt1	1	V_{IH1}		0.7 BV_{DD5}		BV_{DD5}	V
	Schmitt2	P80-85	V_{IH2}		0.8 BV_{DD5}		BV_{DD5}	V
	CMOS1	1	V_{IH3}		0.7 BV_{DD5}		BV_{DD5}	V
	CMOS2	P80-85	V_{IH4}		0.8 BV_{DD5}		BV_{DD5}	V
Input voltage low	Schmitt1	1	V_{IL1}		0		0.3 BV_{DD5}	V
	Schmitt2	P80-85	V_{IL2}		0		0.4 BV_{DD5}	V
	CMOS1	1	V_{IL3}		0		0.3 BV_{DD5}	V
	CMOS2	P80-85	V_{IL4}		0		0.4 BV_{DD5}	V
Input hysteresis [b]	Schmitt1	1	V_{HY1}		150			mV
	Schmitt2	P80-85	V_{HY2}		150			mV
Output voltage high	Limit1	1	V_{OH}	I_{OH} = -2.0 mA	BV_{DD5} - 0.45			V
	Limit2	1	V_{OH}	I_{OH} = -5.0 mA	BV_{DD5} - 0.45			V
Output voltage low	Limit1	1	V_{OL}	I_{OL} = 2.0 mA			0.45	V
	Limit2	1	V_{OL}	I_{OL} = 5.0 mA			0.45	V
Maximum output short circuit current high	Limit1	1	I_{OHM1}	V_{OH} = 0 V	-2		-12	mA
	Limit2		I_{OHM2}		-5		-30	mA
Maximum output short circuit current low	Limit1		I_{OLM1}	V_{OL} = BV_{DD5}	2		12	mA
	Limit2		I_{OLM2}		5		30	mA

a. CMOS1, CMOS2, Schmitt1 and Schmitt2 denote the non-schmitt and the two schmitt trigger input characteristics of the device pins. This characteristic can be selected bitwise by software. CMOS2 and SCHMITT2 are only available on Port P8.
Limit1 and Limit2 denote the two output characteristics with current limit functionality of the device pins. The characteristic can be selected bitwise by software.

b. Not tested in production. Specified by design.

T_A = -40 ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 4.0 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427)
V_{DD5} = 3.2 V ~ 5.5 V, (see “Power On Clear” on page 80 for further functional restriction),
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427)

Table 6-3: Pin Group 1 Low Voltage Operating Range

Parameter	Pin mode [a]	Pin Group	Symbol	Test Conditions	Min.	Typ	Max.	Unit
Input voltage high	Schmitt1	1	V_{IH1}		0.7 BV_{DD5}		BV_{DD5}	V
	Schmitt2	P80-85	V_{IH2}		0.8 BV_{DD5}		BV_{DD5}	V
	CMOS1	1	V_{IH3}		0.7 BV_{DD5}		BV_{DD5}	V
	CMOS2	P80-85	V_{IH4}		0.8 BV_{DD5}		BV_{DD5}	V
Input voltage low	Schmitt1	1	V_{IL1}		0		0.3 BV_{DD5}	V
	Schmitt2	P80-85	V_{IL2}		0		0.35 BV_{DD5}	V
	CMOS1	1	V_{IL3}		0		0.3 BV_{DD5}	V
	CMOS2	P80-85	V_{IL4}		0		0.4 BV_{DD5}	V
Input hysteresis [b]	Schmitt1	1	V_{HY1}		100			mV
	Schmitt2	P80-85	V_{HY2}		100			mV
Output voltage high	Limit1	1	V_{OH}	I_{OH} = -1.0 mA	BV_{DD5} - 0.45			V
	Limit2	1	V_{OH}	I_{OH} = -2.0 mA	BV_{DD5} - 0.45			V
Output voltage low	Limit1	1	V_{OL}	I_{OL} = 1.0 mA			0.45	V
	Limit2	1	V_{OL}	I_{OL} = 2.0 mA			0.45	V
Maximum output short circuit current high	Limit1	1	I_{OHM1}	V_{OH} = 0 V	-1			mA
	Limit2		I_{OHM2}		-2			mA
Maximum output short circuit current low	Limit1		I_{OLM1}	V_{OL} = BV_{DD5}	1			mA
	Limit2		I_{OLM2}		2			mA

a. CMOS1, CMOS2, Schmitt1 and Schmitt2 denote the non-schmitt and the two schmitt trigger input characteristics of the device pins. This characteristic can be selected bitwise by software. CMOS2 and SCHMITT2 are only available on Port P8.
Limit1 and Limit2 denote the two output characteristics with current limit functionality of the device pins. The characteristic can be selected bitwise by software.

b. Not tested in production. Specified by design.

T_A = -40 ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427)
V_{DD5} = 3.2 V ~ 5.5 V, (see “Power On Clear” on page 80 for further functional restriction),
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427)

Table 6-4: Pin P05 pulldown resistor

Parameter	Pin mode	Pin Group	Symbol	Test Conditions	Min.	Typ	Max.	Unit
Pull down resistor		P05	V_{PD}		14	28	56	kΩ

6.3 Pin group 2: $\overline{\text{RESET}}$ and FLMD0

T_A = -40 ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427)
V_{DD5} = 3.2 V ~ 5.5 V, (see “Power On Clear” on page 80 for further functional restriction),
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427)

Table 6-5: Pin Group 2 (except P07) Normal Operating Range

Parameter	Pin mode	Pin Group	Symbol	Test Conditions	Min.	Typ	Max.	Unit
Input voltage high	Schmitt1	2	V_{IH1}		0.7 V_{DD52}		V_{DD52}	V
Input voltage low	Schmitt1	2	V_{IL1}		0		0.3 V_{DD52}	V

6.4 Pin group 2: P07

T_A = -40 ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427)
V_{DD5} = 4.0 V ~ 5.5 V, (see "Power On Clear" on page 80 for further functional restriction),
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427)

Table 6-6: P07 Normal Voltage Operating Range

Parameter	Pin mode [a]	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage High	Schmitt1	V_{IH1}		0.7 V_{DD52}		V_{DD52}	V
	CMOS1	V_{IH3}		0.7 V_{DD52}		V_{DD52}	V
Input Voltage Low	Schmitt1	V_{IL1}		0		0.3 V_{DD52}	V
	CMOS1	V_{IL3}		0		0.3 V_{DD52}	V
Input Voltage Hysteresis [b]	Schmitt1	V_{HI1}		150			mV
Output voltage high	Limit1	V_{OH}	I_{OH} = -2.0 mA	V_{DD52} - 0.45			V
	Limit2	V_{OH}	I_{OH} = -5.0 mA	V_{DD52} - 0.45			V
Output voltage low	Limit1	V_{OL}	I_{OL} = 2.0 mA			0.45	V
	Limit2	V_{OL}	I_{OL} = 5.0 mA			0.45	V
Maximum output short circuit current high	Limit1	I_{OHM1}	V_{OH} = 0 V	-2			mA
	Limit2	I_{OHM2}		-5			mA
Maximum output short circuit current low	Limit1	I_{OLM1}	V_{OL} = V_{DD52}	2			mA
	Limit2	I_{OLM2}		5			mA

a. CMOS1 and Schmitt1 denote the non-schmitt trigger and the schmitt trigger input characteristics of the device pins. This characteristic can be selected bitwise by software.

b. Not tested in production. Specified by design.

T_A = -40 ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427)
V_{DD5} = 3.2 V ~ 4.0 V, (see “Power On Clear” on page 80 for further functional restriction),
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427)

Table 6-7: P07 Low Voltage Operating Range

Parameter	Pin mode [a]	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage High	Schmitt 1	V_{IH1}		0.7 V_{DD52}		V_{DD52}	V
	CMOS1	V_{IH3}		0.7 V_{DD52}		V_{DD52}	V
Input Voltage Low	Schmitt1	V_{IL1}		0		0.3 V_{DD52}	V
	CMOS1	V_{IL3}		0		0.3 V_{DD52}	V
Input Voltage Hysteresis [b]	Schmitt1	V_{HI1}		100			mV
Output voltage high	Limit1	V_{OH}	I_{OH} = -1.0 mA	V_{DD52} - 0.45			V
	Limit2	V_{OH}	I_{OH} = -2.0 mA	V_{DD52} - 0.45			V
Output voltage low	Limit1	V_{OL}	I_{OL} = 1.0 mA			0.45	V
	Limit2	V_{OL}	I_{OL} = 2.0 mA			0.45	V
Maximum output short circuit current high	Limit1	I_{OHM1}	V_{OH} = 0 V	-1			mA
	Limit2	I_{OHM2}		-2			mA
Maximum output short circuit current low	Limit1	I_{OLM1}	V_{OL} = V_{DD52}	1			mA
	Limit2	I_{OLM2}		2			mA

a. CMOS1 and Schmitt1 denote the non-schmitt trigger and the schmitt trigger input characteristics of the device pins. This characteristic can be selected bitwise by software.

b. Not tested in production. Specified by design.

6.5 ADC Input

This chapter describes the digital functions available at the pins supplied by AVDD. The number of available analog conversion channels differ between the devices.

Pin Group 5: Pins supplied by AV_{DD}
5: (P70 .. P715)
Digital buffer function is only available for P70..P715.

T_A = -40 ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.2 V ~ 5.5 V (µPD70F3427)
V_{DD5} = 3.2 V ~ 5.5 V, (see “Power On Clear” on page 80 for further functional restriction),
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427)

Table 6-8: Pin Group 5 Normal Operating Range

Parameter	Pin mode [a]	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage High	Schmitt1	V_{IH1}		0.7 AV_{DD5}		AV_{DD5}	V
Input Voltage Low	Schmitt1	V_{IL1}		0		0.3 AV_{DD5}	V
Input Voltage Hysteresis [b]	Schmitt1	V_{HI1}		150			mV

a. Schmitt1 denote the schmitt trigger input characteristics of the device pins.

b. Not tested in production. Specified by design.

6.6 Pin Group 3: GPIO and LCD Bus Interface (µPD70F3426, µPD70F3425, µPD70F3424, µPD70F3423, µPD703423, µPD70F3422, µPD703422, µPD70F3421, µPD703421, µPD70F3420, µPD703420)

Pin Group 3: GPIO and LCD Bus interface supplied by DV_{DD5}
3: (P32-33, P86-87, P90-97, P104-107)
LCD bus function on these pins is not available in µPD70F3423, µPD70F3422, µPD703422, µPD70F3421, µPD703421, µPD70F3420 and µPD703420.

T_A = -40 ~ +85°C,
DV_{DD5} = 4.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
V_{DD5} = 3.2 V ~ 5.5 V, (see “Power On Clear” on page 80 for further functional restriction),
$V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS}$ = 0 V

Table 6-9: Pin Group 3 Normal Operating Range

Parameter	Pin mode[a]	Pin Group	Symbol	Test Conditions	Min.	Typ	Max.	Unit
Input voltage high	Schmitt1	3	V_{IH1}		0.7 DV_{DD5}		DV_{DD5}	V
	Schmitt2	P86-87	V_{IH2}		0.8 DV_{DD5}		DV_{DD5}	V
	CMOS1	3	V_{IH3}		0.7 DV_{DD5}		DV_{DD5}	V
	CMOS 2	P86-87	V_{IH4}		0.8 DV_{DD5}		DV_{DD5}	V
Input voltage low	Schmitt1	3	V_{IL1}		0		0.3 DV_{DD5}	V
	Schmitt2	P86-87	V_{IL2}		0		0.4 DV_{DD5}	V
	CMOS1	3	V_{IL3}		0		0.3 DV_{DD5}	V
	CMOS2	P86-87	V_{IL4}		0		0.4 DV_{DD5}	V
Input hysteresis [b]	Schmitt1	3	V_{HY1}		150			mV
	Schmitt2	P86-87	V_{HY2}		150			mV
Output voltage high	Limit1	3	V_{OH}	I_{OH} = -2.0 mA	DV_{DD5} - 0.45			V
	Limit2	3	V_{OH}	I_{OH} = -5.0 mA	DV_{DD5} - 0.45			V
Output voltage low	Limit1	3	V_{OL}	I_{OL} = 2.0 mA			0.45	V
	Limit2	3	V_{OL}	I_{OL} = 5.0 mA			0.45	V
Maximum output short circuit current high	Limit1	3	I_{OHM1}	V_{OH} = 0 V	-2		-12	mA
	Limit2		I_{OHM2}		-5		-30	mA
Maximum output short circuit current low	Limit1		I_{OLM1}	$V_{OL} = DV_{DD5}$	2		12	mA
	Limit2		I_{OLM2}		5		30	mA

a. CMOS1, CMOS2, Schmitt1 and Schmitt2 denote the non-schmitt and the two schmitt trigger input characteristics of the device pins. This characteristic can be selected bitwise by software. CMOS2 and SCHMITT2 are only available on Port P8.
Limit1 and Limit2 denote the two output characteristics with current limit functionality of the device pins. The characteristic can be selected bitwise by software.

b. Not tested in production. Specified by design.

T_A = -40 ~ +85°C,
DV_{DD5} = 3.0 V ~ 4.0 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
V_{DD5} = 3.2 V ~ 5.5 V, (see “Power On Clear” on page 80 for further functional restriction),
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V

Table 6-10: Pin Group 3 Low Voltage Operating Range

Parameter	Pin mode [a]	Pin Group	Symbol	Test Conditions	Min.	Typ	Max.	Unit
Input voltage high	Schmitt1	3	V_{IH1}		0.7 DV_{DD5}		DV_{DD5}	V
	Schmitt2	P86-87	V_{IH2}		0.8 DV_{DD5}		DV_{DD5}	V
	CMOS1	3	V_{IH3}		0.7 DV_{DD5}		DV_{DD5}	V
	CMOS2	P86-87	V_{IH4}		0.8 DV_{DD5}		DV_{DD5}	V
Input voltage low	Schmitt1	3	V_{IL1}		0		0.3 DV_{DD5}	V
	Schmitt2	P86-87	V_{IL2}		0		0.35 DV_{DD5}	V
	CMOS1	3	V_{IL3}		0		0.3 DV_{DD5}	V
	CMOS2	P86-87	V_{IL4}		0		0.4 DV_{DD5}	V
Input hysteresis [b]	Schmitt1	3	V_{HY1}		100			mV
	Schmitt2	P86-87	V_{HY2}		100			mV
Output voltage high	Limit1	3	V_{OH}	I_{OH} = -1.0 mA	DV_{DD5} - 0.45			V
	Limit2	3	V_{OH}	I_{OH} = -2.0 mA	DV_{DD5} - 0.45			V
Output voltage low	Limit1	3	V_{OL}	I_{OL} = 1.0 mA			0.45	V
	Limit2	3	V_{OL}	I_{OL} = 2.0 mA			0.45	V
Maximum output short circuit current high	Limit1	3	I_{OHM1}	V_{OH} = 0 V	-1			mA
	Limit2		I_{OHM2}		-2			mA
Maximum output short circuit current low	Limit1		I_{OLM1}	V_{OL} = DV_{DD5}	1			mA
	Limit2		I_{OLM2}		2			mA

a. CMOS1, CMOS2, Schmitt1 and Schmitt2 denote the non-schmitt and the two schmitt trigger input characteristics of the device pins. This characteristic can be selected bitwise by software. CMOS2 and SCHMITT2 are only available on Port P8.
Limit1 and Limit2 denote the two output characteristics with current limit functionality of the device pins. The characteristic can be selected bitwise by software.

b. Not tested in production. Specified by design.

6.7 Pin Group 3: GPIO and LCD Bus and external Memory Interface (µPD70F3427)

Pin Group 3: GPIO and LCD Bus interface and external memory interface supplied by DV_{DD5}
3: (P32-33, P86-87, P90-97, P104-107, P141-142)
LCD bus function on these pins is not available in µPD70F3423, µPD70F3422, µPD703422, µPD70F3421, µPD703421, µPD70F3420 and µPD703420.

T_A = -40 ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427)
V_{DD5} = 3.2 V ~ 5.5 V, (see “Power On Clear” on page 80 for further functional restriction),
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427)

Table 6-11: Pin Group 3 Normal Operating Range

Parameter	Pin mode[a]	Pin Group	Symbol	Test Conditions	Min.	Typ	Max.	Unit
Input voltage high	CMOS1	3	V_{IH3}		0.7 DV_{DD5}		DV_{DD5}	V
Input voltage low	CMOS1	3	V_{IL3}		0		0.3 DV_{DD5}	V
Output voltage high	No Limit	3	V_{OH}	I_{OH} = -5.0 mA	DV_{DD5} - 0.45			V
Output voltage low	No Limit	3	V_{OL}	I_{OL} = 5.0 mA			0.45	V

a. CMOS1 denotes the fixed non-schmitt input characteristics of these device pins. This pin group does not support current limitation.

6.8 Pin Group 6: External Memory Interface (µPD70F3427)

Pin Group 6: External Memory Interface supplied by MV_{DD5} .
6: (A0-23, D0-15, $\overline{CS0\text{-}1}$, $\overline{CS3\text{-}4}$, $\overline{WAIT}$, $\overline{RD}$, $\overline{WR}$, $\overline{BE0\text{-}1}$, P140)

T_A = -40 ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V, MV_{DD5} = 3.0 V ~ 5.5 V
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
V_{DD5} = 3.2 V ~ 5.5 V, (see “Power On Clear” on page 80 for further functional restriction),
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = MV_{SS5} = AV_{SS} = 0 V

Table 6-12: Pin Group 3 Normal Operating Range

Parameter	Pin mode[a]	Pin Group	Symbol	Test Conditions	Min.	Typ	Max.	Unit
Input voltage high	CMOS1	6	V_{IH6}		0.7 MV_{DD5}		MV_{DD5}	V
Input voltage low	CMOS1	6	V_{IL6}		0		0.3 MV_{DD5}	V
Output voltage high	No Limit	6	V_{OH}	I_{OH} = -5.0 mA	MV_{DD5} - 0.45			V
Output voltage low	No Limit	6	V_{OL}	I_{OL} = 5.0 mA			0.45	V

a. CMOS1 denotes the fixed non-schmitt input characteristics of the device pins. This pin group does not support current limitation.

6.9 LCD Common and Segment Lines

The LCD common and segment function is only available in µPD70F3423, µPD70F3422, µPD703422, µPD70F3421, µPD703421, µPD70F3420 and µPD703420.

T_A = -40 ~ +85°C,
DV_{DD5} = 4.5 V ~ 5.5 V, BV_{DD5} = 4.5 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
V_{DD5} = 3.2 V ~ 5.5 V, (see “Power On Clear” on page 80 for further functional restriction),
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V

Table 6-13: DC Characteristics LCD Common and Segment Lines

Parameter	Symbol	TestConditions	Min.	Typ	Max	Unit
LCD Segment Output Voltage (unloaded)	V_{ODS}	IO = ±1µA	V_{LCDn} - 0.2	V_{LCDn}[a]	V_{LCDn} + 0.2	V
LCD Common Output Voltage (unloaded)	V_{ODC}	IO = ±1µA	V_{LCDn} - 0.2	V_{LCDn}	V_{LCDn} + 0.2	V
LCD split voltage[b]	V_{LC0}	IO = ±1.5 mA	V_{LCD0} - 0.1	V_{LCD0}	V_{LCD0} + 0.1	V
	V_{LC1}	IO = ±1.0 mA	V_{LCD1} - 0.1	V_{LCD1}	V_{LCD1} + 0.1	V
	V_{LC2}	IO = ±1.0 mA	V_{LCD2} - 0.1	V_{LCD2}	V_{LCD2} + 0.1	V
	V_{LC3}	IO = ±1.5 mA	V_{LCD3} - 0.1	V_{LCD3}	V_{LCD3} + 0.1	V
LCD Series resistance[c]	R_{LCDS}	Segment lines, V_{LCDn} to pin			1.8	kΩ
	R_{LCDC}	Common lines, V_{LCDn} to pin			1.8	kΩ
LCD operation current	IDD_{LCD}	tbd.			tbd.	µA

a. VLCDn (n= 0..3) represents one of the four possible voltage levels at the LCD pins. See table below for reference.

b. The split voltage is an internal design value. Direct measurement is not possible.

c. The Series resistance is an internal design value. Direct measurement is not possible.

Note: The power supply configuration is restricted, when the LCD is used.
The LCD voltages are generated centrally. Since the LCD output buffers are supplied by different supplies (BV_{DD5} and DV_{DD5}) it is necessary that BV_{DD5} is equal to DV_{DD5}.

Note: Do not operate buffers of pin group 3 in current limit state, when the LCD function is used. Failing to do so may lead to a decreased accuracy of the LCD waveforms.

6.10 Stepper Motor Driver IO

Pin Group 4: Stepper Motor outputs supplied by SMV_{DD5}
4A: (P110-117, P120-123)
4B: (P124-127, P130-137)

T_A = -40 ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 4.0 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427)
V_{DD5} = 3.2 V ~ 5.5 V, (see “Power On Clear” on page 80 for further functional restriction),
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427)

Table 6-14: DC Characteristics Stepper Motor Driver Input Normal Voltage Operation

Parameter	Pin mode [a]	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage High	Schmitt1	V_{IH1}		0.7 SMV_{DD5}		SMV_{DD5}	V
	CMOS1	V_{IH3}		0.7 SMV_{DD5}		SMV_{DD5}	V
Input Voltage Low	Schmitt1	V_{IL1}		0		0.3 SMV_{DD5}	V
	CMOS1	V_{IL3}		0		0.3 SMV_{DD5}	V
Input Voltage Hysteresis [b]	Schmitt1	V_{HI1}		150			mV

a. CMOS1 and Schmitt1 denote the non-schmitt trigger and the two schmitt trigger input characteristics of the device pins. This characteristic can be selected bitwise by software.

b. Not tested in production. Specified by design.

T_A = -40 ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 4.0 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427)
V_{DD5} = 3.2 V ~ 5.5 V, (see “Power On Clear” on page 80 for further functional restriction),
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427)

Table 6-15: DC Characteristics Stepper Motor Driver Input Low Voltage Operation

Parameter	Pin mode [a]	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage High	Schmitt1	V_{IH1}		0.7 SMV_{DD5}		SMV_{DD5}	V
	CMOS1	V_{IH3}		0.7 SMV_{DD5}		SMV_{DD5}	V
Input Voltage Low	Schmitt1	V_{IL1}		0		0.3 SMV_{DD5}	V
	CMOS1	V_{IL3}		0		0.3 SMV_{DD5}	V
Input Voltage Hysteresis [b]	Schmitt1	V_{HI1}		100			mV

a. CMOS1 and Schmitt1 denote the non-schmitt trigger and the two schmitt trigger input characteristics of the device pins. This characteristic can be selected bitwise by software.

b. Not tested in production. Specified by design.

T_A = -40 ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 4.75 V ~ 5.25 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427)
V_{DD5} = 3.2 V ~ 5.5 V, (see “Power On Clear” on page 80 for further functional restriction),
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427)

Table 6-16: DC Characteristics Stepper Motor Driver Output Normal Operation

Parameter	Pin mode	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage High		V_{OH}	I_{OH} = -40 mA, T_A= -40°C	SMV_{DD5} - 0.5		SMV_{DD5}	V
		V_{OH}	I_{OH} = -30 mA, T_A= +25°C	SMV_{DD5} - 0.5		SMV_{DD5}	V
		V_{OH}	I_{OH} = -27 mA, T_A= +85°C	SMV_{DD5} - 0.5		SMV_{DD5}	V
Output Voltage Low		V_{OL}	I_{OL} = 40 mA, T_A= -40°C	0		0.5	V
		V_{OL}	I_{OL} = 30 mA, T_A= +25°C	0		0.5	V
		V_{OL}	I_{OL} = 27 mA, T_A= +85°C	0		0.5	V
Output voltage deviation [a]		V_{DEV}		0		50	mV
Output Slew rate [b]		t_{RF}	10% - 90%	12	25	70	ns
Peak Cross Current[c]		I_{CROSS}				50	mA
Output Pulse width[d]		t_{MO}		125			ns
Output Pulse length deviation[e]		t_{SMDEV}		-10	+5	+45	ns

a. Output voltage deviation defines the difference of the outputs levels of the same stepper motor.
V_{DEV} = max (| V_{OHx} - V_{OHy} | , | V_{OLx} - V_{OLy} |) @ I_{OHx} = I_{OHy}, I_{OLx}=I_{OLy}.
x and y denote any combination of two pins of the following pin groups: (P110-P113, P114-117, P120-123, P124-P127, P130-P133, P134-P137)

b. The slew rate is not tested, but derived from simulation.

c. The slew rate control generates a cross current in the output stage to control the energy of the external inductive load. The cross current flows only during the output transistion time t_{RF}. It flows in addition to the output current. The cross current is not tested, but derived from simulation.

d. The output buffer can not generate high or low pulses shorter than this time, because of its slew rate control system. This value is not tested, but derived from simulation.

e. The slew rate control function causes a deviation of output pulse time compared to the ideal selected output pulse setting. This value is not tested, but derived from simulation.

Note: The stepper output drivers have no current limitation and are not protected regarding short circuit.

T_A = -40 ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 4.75 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427)
V_{DD5} = 3.2 V ~ 5.5 V, (see “Power On Clear” on page 80 for further functional restriction),
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427)

Table 6-17: DC Characteristics Stepper Motor Driver Output Low Voltage Operation

Parameter	Pin mode	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage High		V_{OH}	I_{OH} = -5 mA,	SMV_{DD5} - 0.5		SMV_{DD5}	V
Output Voltage Low		V_{OL}	I_{OL} = +5 mA,	0		0.5	V

6.11 Current Limit Function of I/O buffers

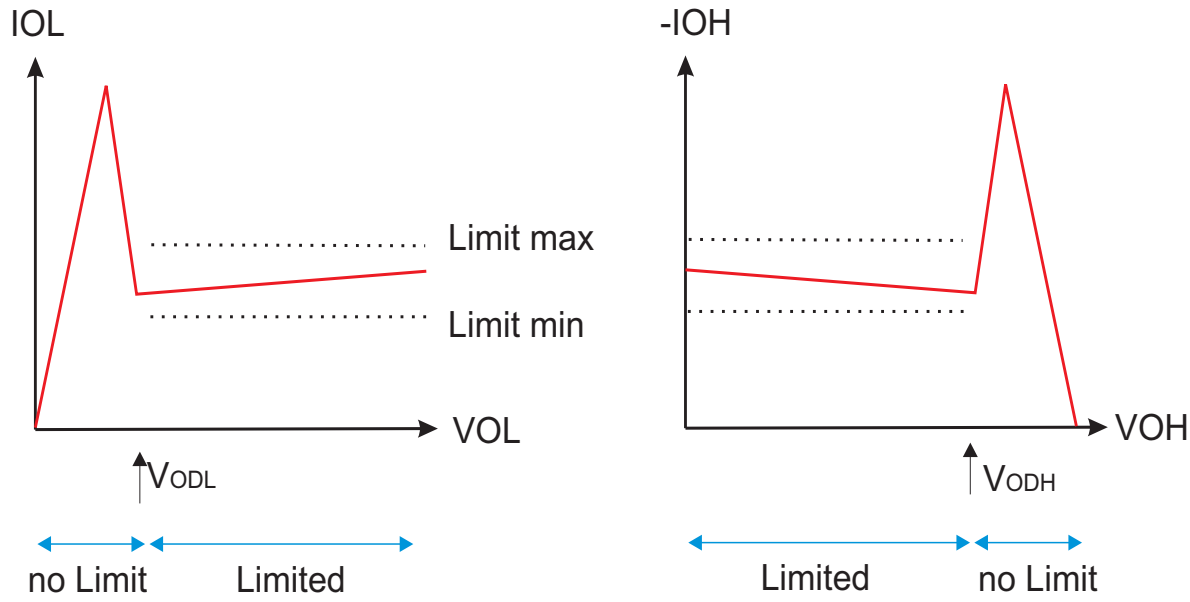
The output buffers of the pin groups 1 and 3 incorporate a current limiting function. This function limits the output current of the buffer to a certain value during output signal switching.
The limit is disabled when the buffer output voltage is near to its target voltage, thus providing full drivability. During full drivability the current may reach values given in absolute maximum ratings for a single pin.
The user can select different limit ranges by software (see Functional Target Specification for details).

The limit function is independant from the operation mode of the device.

A permanent short circuit of outputs is not permitted.

The stepper motor driver outputs do not support a current limiting function.

Figure 6-1: Current Limit Function Principle



Note: The current limit function of the I/O buffers needs additional bias current to control the output stage. The additional bias current depend on the status of each buffer. Each buffer with either high or low output and in the stage of current limiting will draw this bias current.

T_A = -40 ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427)
V_{DD5} = 3.2 V ~ 5.5 V, (see “Power On Clear” on page 80 for further functional restriction),
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427)

Table 6-18: DC Characteristics of Current Limiting Function [a]

Parameter	Pin mode	Symbol	Test Conditions	Min	Typ	Max	Unit
Limit disable threshold voltage for V_{OH}		V_{ODH}		VDDx[b] - 1.6		VDDx - 1.1	V
Limit disable threshold voltage for V_{OL}		V_{ODL}		1.1		1.6	V
Supply Current per buffer for current limitation [c]	Limit1	I_{DDCL1}				0.8	mA
	Limit2	I_{DDCL2}				1.7	mA

a. These values are not tested. They are given based on design simulation

b. VDDx denotes the corresponding voltage supply of the pin.

c. This current need not be considered during absolute maximum current calculation.

Note: The function of the current limiting operation is sensitive against inductive loads under a certain condition:

- The load of the pin is below the selected current limit and the device could reach a sufficient output voltage. The device changed to full drivability.
- The external circuitry sinks/sources more and more current.
- The current creates an increasing voltage drop in the output stage of the device.
- The increasing voltage drop enables the current limiting function.
- The enabling of the current limit together with an external inductance may lead to an oscillation of the output between the limited and unlimited state. The external inductance creates voltage peaks that change the state of the output buffers current limiting function.
- Recommendation: keep external inductance small (keep external wiring short).

The current limit function of pin group 3 is only available for the derivatives µPD70F3426, µPD70F3425, µPD70F3424, µPD70F3423, µPD70F3422, µPD703422, µPD70F3421, µPD703421, µPD70F3420, µPD703420. The pin group 3 of the derivative µPD70F3427 does not contain a current limit function.

6.12 Supply Current

T_A = -40 ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427)
V_{DD5} = 3.2 V ~ 5.5 V, (see “Power On Clear” on page 80 for further functional restriction),
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427)

Table 6-19: DC Characteristics Supply Current µPD70F3426 [a]

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply current	I_{DD10}	Operating (f_{CPU} = 64 MHz; SSCG,PLL: on)		100	130	mA
	I_{DD11}	Operating (f_{CPU} = 48 MHz; SSCG,PLL: on)		77	100	mA
	I_{DD12}	Operating (f_{CPU} = 32 MHz; SSCG,PLL: on)		57	75	mA
	I_{DD13}	Operating (f_{CPU} = 24 MHz; SSCG,PLL: on)		46	60	mA
	I_{DD13}	Operating (f_{CPU} = 16 MHz; SSCG,PLL: on)		35	45	mA
	I_{DD13}	Operating (f_{CPU} = 8 MHz; SSCG,PLL: on)		24	30	mA
	I_{DD14}	Operating (f_{CPU} = 4 MHz; SSCG,PLL: off)		15	19	mA
	I_{DD15}	Operating (f_{CPU} = 32 kHz; SSCG,PLL: off)		1	1.3	mA
	I_{DD16}	Operating (f_{CPU} = RingOSC; SSCG,PLL: off)		8.1	11	mA
	I_{DD20}	HALT Mode (f_{PLL} = 64 MHz; SSCG,PLL: on)		48	65	mA
	I_{DD21}	HALT Mode (f_{PLL} = 48 MHz; SSCG,PLL: on)		39	50	mA
	I_{DD30}	IDLE Mode (f_{PLL} = 64 MHz; SSCG,PLL: on)		5	7	mA

Table 6-19: DC Characteristics Supply Current µPD70F3426 [a] (Continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply current	I_{DD31}	IDLE Mode (f_{PLL} = 48 MHz; SSCG,PLL: on)		5	7	mA
	I_{DD5}	STOP		10	190	µA
	I_{DD6}	WATCH		350	500	µA
	I_{DD6A}	WATCH Monitored		330	530	µA
	I_{DD7}	SUB WATCH		50	200	µA
	I_{DD7A}	SUB WATCH Monitored		65	215	µA
	I_{DD7B}	SUB WATCH on Ring-Osc		65	215	µA

a. These values are target values without current consumption due to external circuitry at the IO-pins.

Table 6-20: DC Characteristics Supply Current µPD70F3427 [a]

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply current	I_{DD10}	Operating (f_{CPU} = 64 MHz; SSCG,PLL: on)		108	140	mA
	I_{DD11}	Operating (f_{CPU} = 48 MHz; SSCG,PLL: on)		85	110	mA
	I_{DD12}	Operating (f_{CPU} = 32 MHz; SSCG,PLL: on)		62	80	mA
	I_{DD13}	Operating (f_{CPU} = 24 MHz; SSCG,PLL: on)		50	65	mA
	I_{DD13}	Operating (f_{CPU} = 16 MHz; SSCG,PLL: on)		38	50	mA
	I_{DD13}	Operating (f_{CPU} = 8 MHz; SSCG,PLL: on)		26	35	mA
	I_{DD14}	Operating (f_{CPU} = 4 MHz; SSCG,PLL: off)		15	20	mA
	I_{DD15}	Operating (f_{CPU} = 32 kHz; SSCG,PLL: off)		1	1.3	mA
	I_{DD16}	Operating (f_{CPU} = RingOSC; SSCG,PLL: off)		5	6.6	mA
	I_{DD20}	HALT Mode (f_{PLL} = 64 MHz; SSCG,PLL: on)		70	90	mA
	I_{DD21}	HALT Mode (f_{PLL} = 48 MHz; SSCG,PLL: on)		54	70	mA
	I_{DD30}	IDLE Mode (f_{PLL} = 64 MHz; SSCG,PLL: on)		5	7	mA
	I_{DD31}	IDLE Mode (f_{PLL} = 48 MHz; SSCG,PLL: on)		5	7	mA
	I_{DD5}	STOP		10	190	µA
	I_{DD6}	WATCH		350	500	µA
	I_{DD6A}	WATCH Monitored		330	530	µA
	I_{DD7}	SUB WATCH		50	200	µA

Table 6-20: DC Characteristics Supply Current µPD70F3427 [a] (Continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply current	I_{DD7A}	SUB WATCH Monitored		65	215	µA
	I_{DD7B}	SUB WATCH on Ring-OSC		65	215	µA

a. These values are target values without current consumption due to external circuitry at the IO-pins.

Table 6-21: DC Characteristics Supply Current µPD70F3425, µPD70F3424 [a]

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply current	I_{DD10}	Operating (f_{CPU} = 64MHz; SSCG,PLL: on)		82	123	mA
	I_{DD11}	Operating (f_{CPU} = 48 MHz; SSCG,PLL: on)		65	98	mA
	I_{DD12}	Operating (f_{CPU} = 32 MHz; SSCG,PLL: on)		48	72	mA
	I_{DD13}	Operating (f_{CPU} = 24 MHz; SSCG,PLL: on)		40	60	mA
	I_{DD13}	Operating (f_{CPU} = 16 MHz; SSCG,PLL: on)		32	48	mA
	I_{DD13}	Operating (f_{CPU} = 8 MHz; SSCG,PLL: on)		24	36	mA
	I_{DD14}	Operating (f_{CPU} = 4 MHz; SSCG,PLL: off)		10	15	mA
	I_{DD15}	Operating (f_{CPU} = 32 kHz; SSCG,PLL: off)		0.2	1.2	mA
	I_{DD16}	Operating (f_{CPU} = RingOSC; SSCG,PLL: off)		3.3	6	mA
	I_{DD20}	HALT Mode (f_{PLL} = 64 MHz; SSCG,PLL: on)		40	60	mA
	I_{DD21}	HALT Mode (f_{PLL} = 48 MHz; SSCG,PLL: on)		32	48	mA
	I_{DD30}	IDLE Mode (f_{PLL} = 64 MHz; SSCG,PLL: on)		6	9	mA
	I_{DD31}	IDLE Mode (f_{PLL} = 48 MHz; SSCG,PLL: on)		5	7.5	mA
	I_{DD5}	STOP		10	190	µA
	I_{DD6}	WATCH		250	500	µA
	I_{DD6A}	WATCH Monitored		265	530	µA
	I_{DD7}	SUB WATCH		50	200	µA

Table 6-21: DC Characteristics Supply Current µPD70F3425, µPD70F3424 [a] (Continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply current	I_{DD7A}	SUB WATCH Monitored		65	215	µA
	I_{DD7B}	SUB WATCH on Ring-OSC		65	215	µA

a. These values are target values without current consumption due to external circuitry at the IO-pins.

Table 6-22: DC Characteristics Supply Current µPD70F3423, µPD70F3422, µPD70F3421, µPD70F3420[a]

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply current	I_{DD12}	Operating (f_{CPU} = 32 MHz; SSCG,PLL: on)		48	72	mA
	I_{DD13}	Operating (f_{CPU} = 24 MHz; SSCG,PLL: on)		40	60	mA
	I_{DD13}	Operating (f_{CPU} = 16 MHz; SSCG,PLL: on)		32	48	mA
	I_{DD13}	Operating (f_{CPU} = 8 MHz; SSCG,PLL: on)		24	36	mA
	I_{DD14}	Operating (f_{CPU} = 4 MHz; SSCG,PLL: off)		10	15	mA
	I_{DD15}	Operating (f_{CPU} = 32 kHz; SSCG,PLL: off)		0.2	1.2	mA
	I_{DD16}	Operating (f_{CPU} = RingOSC = 300 kHz; SSCG,PLL: off)		3.3	6	mA
	I_{DD20}	HALT Mode (f_{PLL} = 32 MHz; SSCG,PLL: on)		24	36	mA
	I_{DD20}	HALT Mode (f_{PLL} = 24 MHz; SSCG,PLL: on)		20	30	mA
	I_{DD21}	HALT Mode (f_{PLL} = 16 MHz; SSCG,PLL: on)		16	24	mA
	I_{DD30}	IDLE Mode (f_{PLL} = 32 MHz; SSCG,PLL: on)		3.8	5.7	mA
	I_{DD30}	IDLE Mode (f_{PLL} = 24 MHz; SSCG,PLL: on)		3.5	5.3	mA
	I_{DD31}	IDLE Mode (f_{PLL} = 16 MHz; SSCG,PLL: on)		3.2	4.8	mA
	I_{DD5}	STOP		10	190	µA
	I_{DD6}	WATCH		250	500	µA
	I_{DD6A}	WATCH Monitored		265	530	µA

Table 6-22: DC Characteristics Supply Current µPD70F3423, µPD70F3422, µPD70F3421, µPD70F3420[a] (Continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply current	I_{DD7}	SUB WATCH		50	200	µA
	I_{DD7A}	SUB WATCH Monitored		65	215	µA
	I_{DD7B}	SUB WATCH on RingOSC		65	215	µA

a. These values are target values without current consumption due to external circuitry at the IO-pins.

Table 6-23: DC Characteristics Supply Current µPD703422, µPD703421, µPD703420 [a]

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply current	I_{DD12}	Operating (f_{CPU} = 32 MHz; SSCG,PLL: on)		48	72	mA
	I_{DD13}	Operating (f_{CPU} = 24 MHz; SSCG,PLL: on)		40	60	mA
	I_{DD13}	Operating (f_{CPU} = 16 MHz; SSCG,PLL: on)		32	48	mA
	I_{DD13}	Operating (f_{CPU} = 8 MHz; SSCG,PLL: on)		24	36	mA
	I_{DD14}	Operating (f_{CPU} = 4 MHz; SSCG,PLL: off)		10	15	mA
	I_{DD15}	Operating (f_{CPU} = 32 kHz; SSCG,PLL: off)		0.2	1.2	mA
	I_{DD16}	Operating (f_{CPU} = RingOSC = 300 kHz; SSCG,PLL: off)		3.3	6	mA
	I_{DD20}	HALT Mode (f_{PLL} = 32 MHz; SSCG,PLL: on)		24	36	mA
	I_{DD20}	HALT Mode (f_{PLL} = 24 MHz; SSCG,PLL: on)		20	30	mA
	I_{DD21}	HALT Mode (f_{PLL} = 16 MHz; SSCG,PLL: on)		16	24	mA
	I_{DD30}	IDLE Mode (f_{PLL} = 32 MHz; SSCG,PLL: on)		3.8	5.7	mA
	I_{DD30}	IDLE Mode (f_{PLL} = 24 MHz; SSCG,PLL: on)		3.5	5.3	mA
	I_{DD31}	IDLE Mode (f_{PLL} = 16 MHz; SSCG,PLL: on)		3.2	4.8	mA
	I_{DD5}	STOP		10	190	µA
	I_{DD6}	WATCH		250	500	µA
	I_{DD6A}	WATCH Monitored		265	530	µA
	I_{DD7}	SUB WATCH		50	200	µA

Table 6-23: DC Characteristics Supply Current µPD703422, µPD703421, µPD703420 [a] (Contin-

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply current	I_{DD7A}	SUB WATCH Monitored		65	215	µA
	I_{DD7B}	SUB WATCH on RingOSC		65	215	µA

a. These values are target values without current consumption due to external circuitry at the IO-pins.

The low current modes (STOP, WATCH, SUB WATCH) are tested under the following conditions:

- Operation modes setting as described in table below.
- All functional pins with output possibility are set to output with alternating high and low output levels.
- Testequipment is disconnected from output pins.
- IDD is the total sum of currents to the device supply pins V_{DD5}, BV_{DD5}, DV_{DD5}, SMV_{DD5}, AV_{DD}
  - Device drives its own leakage currents by its output stages.
  - The leakage current is included in the given IDD values.

Table 6-24: Operational conditions for measurement

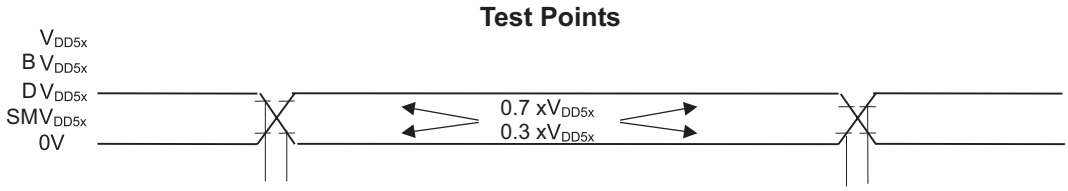
Unit	Watch	Watch monitored	Sub Watch	Sub Watch on RingOSC	Sub Watch monitored	STOP
Main-oscillator	running	running	stopped	stopped	stopped	stopped
Sub-oscillator	stopped (XT1 clamped)	stopped (XT1 clamped)	running	stopped (XT1 clamped)	running	stopped
Ring-oscillator	stopped	running	stopped	running	running	stopped
SSCG	stopped	stopped	stopped	stopped	stopped	stopped
PLL	stopped	stopped	stopped	stopped	stopped	stopped
CPU system	stopped	stopped	stopped	stopped	stopped	stopped
IICCLK	stopped	stopped	stopped	stopped	stopped	stopped
PCLK0, PCLK1	stopped	stopped	stopped	stopped	stopped	stopped
PCLK2…PCLK15	stopped	stopped	stopped	stopped	stopped	stopped
SPCLK0, SPCLK1	stopped	stopped	stopped	stopped	stopped	stopped
SPCLK2…SPCLK15	stopped	stopped	stopped	stopped	stopped	stopped
FOUT	stopped	stopped	stopped	stopped	stopped	stopped
WTCLK	running	running	running	running	running	stopped
WDTCLK	stopped	stopped	stopped	stopped	stopped	stopped
TM0CLK	stopped	stopped	stopped	stopped	stopped	stopped
LCD	disabled	disabled	disabled	disabled	disabled	disabled
ADC	disabled	disabled	disabled	disabled	disabled	disabled
VCOMP	disabled	disabled	disabled	disabled	disabled	disabled
Regulator[a]	Standby	Standby	Standby	Standby	Standby	Standby

a. Regulator in standby: STBCTL = 0x03

Chapter 7 AC Characteristics

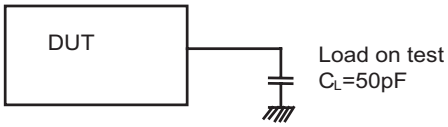
7.1 AC Test Input/Output Waveform

Figure 7-1: AC Test Input/Output Waveform



7.2 AC Test Load Condition

Figure 7-2: AC Test Load Condition



7.3 Reset

T_A = -40 ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427)
V_{DD5} = 3.2 V ~ 5.5 V, (see “Power On Clear” on page 80 for further functional restriction),
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427)

Table 7-1: Reset AC Characteristics

Parameter	Symbol	Test Conditions	MIN.		MAX.	Unit
$\overline{\text{RESET}}$ high-level width [a]	t_{WRSH}		500			ns
$\overline{\text{RESET}}$ low-level width [b]	t_{WRSL}		500			ns
$\overline{\text{RESET}}$ Pulse rejection [c]	t_{WRRJ}		50			ns

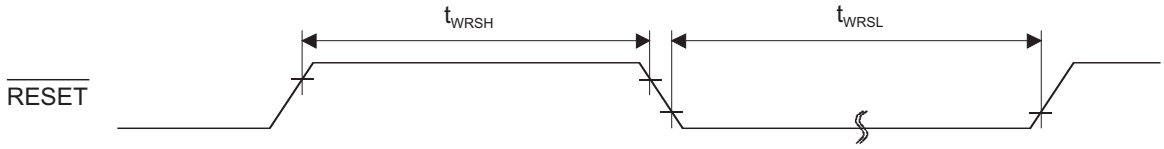
a. This signal high time is needed to ensure that the internal RESET release operation starts.

b. This signal low time is needed to ensure that the internal RESET is activated.

c. The RESET input incorporates an analog filter. Pulses shorter than this minimum will be ignored. Not tested in production.

Note: Reset pulses shorter than the given value may not be recognized by the device, they do not cause undefined states of the device.

Figure 7-3: Reset Timing



7.4 Interrupt Timing

T_A = -40 ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427)
V_{DD5} = 3.2 V ~ 5.5 V, (see “Power On Clear” on page 80 for further functional restriction),
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427)

Table 7-2: Interrupt AC Characteristics

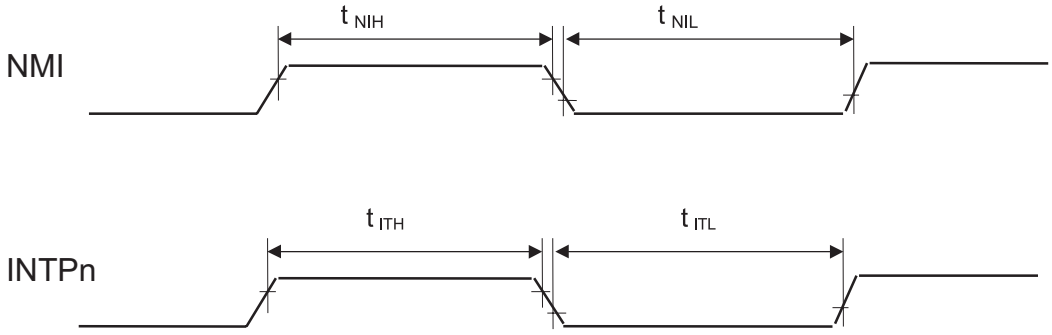
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
NMI high-level width [a]	t_{NIH}		360			ns
NMI low-level width [a]	t_{NIL}		360			ns
NMI pulse rejection [b]	t_{NIRJ}		50		360	ns
INTPn[c] high-level width [a]	t_{ITH}		360			ns
INTPn[c] low-level width [a]	t_{ITL}		360			ns
INTPn[c] pulse rejection [b]	t_{ITRJ}		50		360	ns

a. Pulses longer than this value will pass the input filter.

b. Pulses shorter than this value do not pass the input filters. not tested in production.

c. n = 7…0

Figure 7-4: Interrupt Timing



Note: Interrupt timing is generated by analog delay elements. Delay characteristics have a wide range in production.

7.5 Peripheral Function Characteristics

The following conditions are valid for all peripheral function characteristics unless otherwise noted.

T_A = -40 ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427)
V_{DD5} = 3.2 V ~ 5.5 V, (see “Power On Clear” on page 80 for further functional restriction),
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427)

7.5.1 Timer P

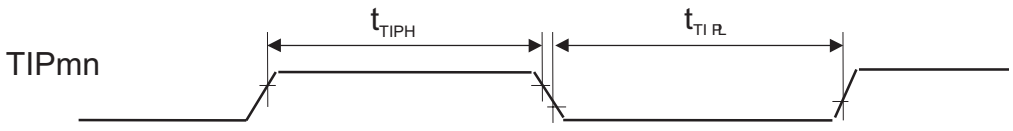
Table 7-3: Timer P AC Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
TIPmn[a] high-level width	t_{TIPHD}	Digital filter	45 +3/f_{PCLK0}[b]			ns
	t_{TIPHNB}	No digital filter, react on both edge	45 +2/f_{PCLK0}			ns
	t_{TIPHNS}	No digital filter, react on single edge	45 +1/f_{PCLK0}			ns
TIPmn [a] low-level width	t_{TIPL}	Digital filter	45 +3/f_{PCLK0}			ns
	t_{TIPLNB}	No digital filter, react on both edge	45 +2/f_{PCLK0}			ns
	t_{TIPLNS}	No digital filter, react on single edge	45 +1/f_{PCLK0}			ns

a. m = 3…0, n = 1…0

b. f_{PCLK0} is the clock frequency of the digital filter connected to the input pin.

Figure 7-5: Timer P Input Timing



7.5.2 Timer G

Table 7-4: Timer G Input Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
TIGmn[a] high-level width	t_{TIGH1}	Digital filter, f_{PCLK0}[b] = f_{CCLK}[c]	45 + 3/f_{PCLK0}			ns
	t_{TIGH2}	Digital filter, $f_{PCLK0} > f_{CCLK}$	45 + 2/f_{CCLK}			ns
	t_{TIGH0}	No digital filter	45 + 2/f_{CCLK}			ns
TIGmn[a] low-level width	t_{TIGL1}	Digital filter, $f_{PCLK0} = f_{CCLK}$	45 + 3/f_{PCLK0}			ns
	t_{TIGL2}	Digital filter, $f_{PCLK0} > f_{CCLK}$	45 + 2/f_{CCLK}			ns
	t_{TIGL0}	No digital filter	45 + 2/f_{CCLK}			ns

a. m = 0…1: n = 1…4; m = 2: n = 0...5

b. f_{SPCLK0} is the clock frequency of the digital filter connected to the input pin.

c. f_{CCLK} is the count clock frequency of the Timer G.

7.5.3 UARTA

Table 7-5: UARTA AC Characteristics

Parameter	Symbol	Test Conditions	Min.	Max	Unit
Transfer rate	T_{UARTA}		0.3	1000	Kbps

7.5.4 CAN

Table 7-6: CAN AC Characteristics

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Transfer rate	T_{FCAN}	f_{CAN}[a] ≥ 8 MHz		1	Mbps

a. f_{CAN} is the CAN macro clock frequency. For CAN clock selection refer to functional specification of the CAN.

7.5.5 CSI B (High Voltage Operation)

T_A = -40 ~ +85°C,
DV_{DD5} = 4.5 V ~ 5.5 V, BV_{DD5} = 4.5 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
V_{DD5} = 3.2 V ~ 5.5 V, (see “Power On Clear” on page 80 for further functional restriction),
MV_{DD5} = 3.0 V ~ 3.6 V,
$V_{SS5} = BV_{SS5} = DV_{SS5} = MV_{SS5} = SMV_{SS5} = AV_{SS}$ = 0 V

(1) CSIB Master Mode

(a) With Digital Filter

Table 7-7: CSIB Master Mode AC Characteristics with Digital Filter

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{\text{SCKBn}}$ cycle time	t_{KCY1}		$8/f_{PCLK0}$		ns
$\overline{\text{SCKBn}}$ high level width	t_{KH1}		0.5 t_{KCY1} - 15		ns
$\overline{\text{SCKBn}}$ low level width	t_{KL1}		0.5 t_{KCY1} - 15		ns
SIBn setup time (to $\overline{\text{SCKBn}}$)	t_{SIK1}		$50 + 4/f_{PCLK0}$[a]		ns
SIBn hold time (from $\overline{\text{SCKBn}}$)	t_{KSI1}		$-31 - 4/f_{PCLK0}$		ns
Delay time from $\overline{\text{SCKBn}}$ to SOBn	t_{KSO1}			6	ns

a. f_{PCLK0} is the clock frequency of the digital filter connected to the input pin.

(b) Without Digital Filter

Table 7-8: CSIB Master Mode AC Characteristics without Digital Filter

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{\text{SCKBn}}$ cycle time	t_{KCY1}		125		ns
$\overline{\text{SCKBn}}$ high level width	t_{KH1}		0.5 t_{KCY1} - 15		ns
$\overline{\text{SCKBn}}$ low level width	t_{KL1}		0.5 t_{KCY1} - 15		ns
SIBn setup time (to $\overline{\text{SCKBn}}$)	t_{SIK1}		50		ns
SIBn hold time (from $\overline{\text{SCKBn}}$)	t_{KSI1}		-31		ns
Delay time from $\overline{\text{SCKBn}}$ to SOBn	t_{KSO1}			6	ns

(2) CSIB Slave Mode

(a) With Digital Filter

Table 7-9: CSIB Slave Mode AC Characteristics with Digital Filter

Parameter	Symbol	Test Conditions	Min	Max	Unit
$\overline{\text{SCKBn}}$ cycle time	t_{KCY1}		$8/f_{PCLK0}$		ns
$\overline{\text{SCKBn}}$ high level width	t_{KH1}		$0.5\ t_{KCY1} - 5$		ns
$\overline{\text{SCKBn}}$ low level width	t_{KL1}		$0.5\ t_{KCY1} - 5$		ns
SIBn setup time (to $\overline{\text{SCKBn}}$)	t_{SIK1}		$15 + 2/f_{PCLK0}$[a]		ns
SIBn hold time (from $\overline{\text{SCKBn}}$)	t_{KSI1}		$5 + 2/f_{PCLK0}$		ns
Delay time from $\overline{\text{SCKBn}}$ to SOBn	t_{KSO1}			$45 + 3/f_{PCLK0}$	ns

a. f_{PCLK0} is the clock frequency of the digital filter connected to the input pin.

(b) Without Digital Filter

Table 7-10: CSIB Slave Mode AC Characteristics without Digital Filter

Parameter	Symbol	Test Conditions	Min	Max	Unit
$\overline{\text{SCKBn}}$ cycle time	t_{KCY1}		125		ns
$\overline{\text{SCKBn}}$ high level width	t_{KH1}		50		ns
$\overline{\text{SCKBn}}$ low level width	t_{KL1}		50		ns
SIBn setup time (to $\overline{\text{SCKBn}}$)	t_{SIK1}		15		ns
SIBn hold time (from $\overline{\text{SCKBn}}$)	t_{KSI1}		5		ns
Delay time from $\overline{\text{SCKBn}}$ to SOBn	t_{KSO1}			45	ns

Note: n = 2…0

Figure 7-6: CSI Master/Slave Mode Timing

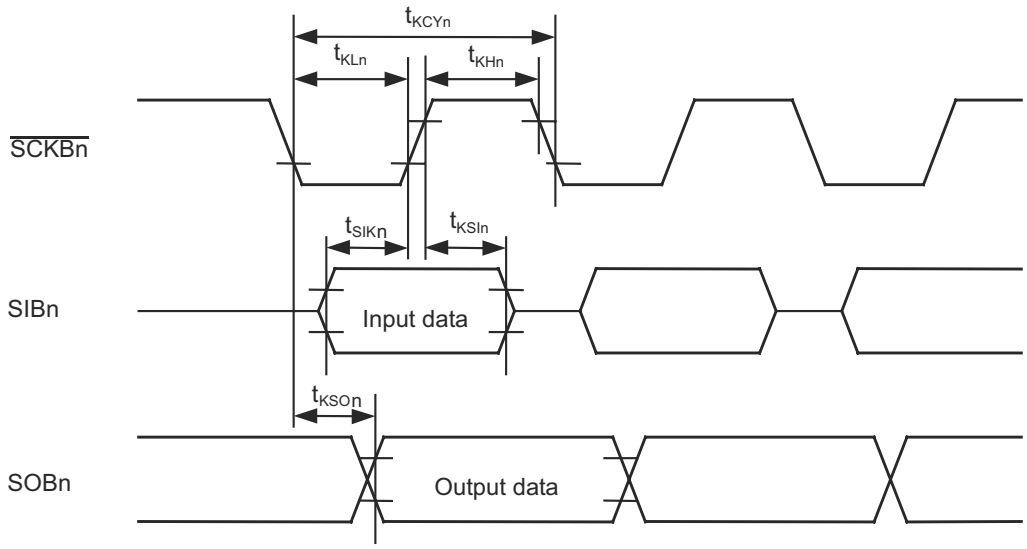
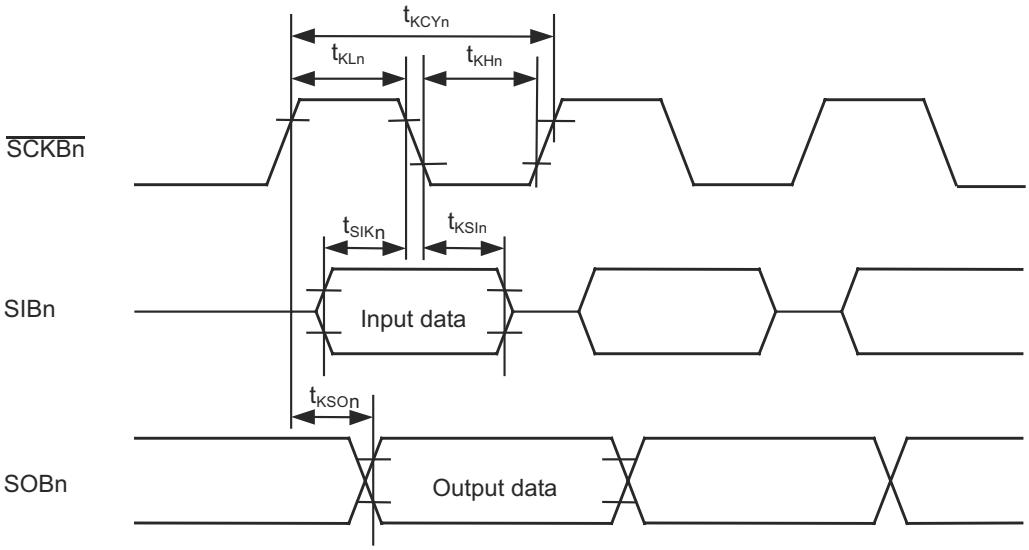


Figure 7-7: CSI Master/Slave Mode Timing Inverted Clock



7.5.6 CSI B (Low Voltage Operation)

T_A = -40 ~ +85°C,
DV_{DD5} = 3.15 V ~ 4.5 V, BV_{DD5} = 3.15 V ~ 4.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
V_{DD5} = 3.2 V ~ 5.5 V, (see “Power On Clear” on page 80 for further functional restriction),
MV_{DD5} = 3.0 V ~ 3.6 V,
V_{SS5} = BV_{SS5} = DV_{SS5} = MV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V

(1) CSIB Master Mode

(a) With Digital Filter

Table 7-11: CSIB Master Mode AC Characteristics with Digital Filter

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{\text{SCKBn}}$ cycle time	t_{KCY1}		$8/f_{PCLK0}$		ns
$\overline{\text{SCKBn}}$ high level width	t_{KH1}		0.5 t_{KCY1} - 15		ns
$\overline{\text{SCKBn}}$ low level width	t_{KL1}		0.5 t_{KCY1} - 15		ns
SIBn setup time (to $\overline{\text{SCKBn}}$)	t_{SIK1}		$-93 + 4/f_{PCLK0}$ [a]		ns
SIBn hold time (from $\overline{\text{SCKBn}}$)	t_{KSI1}		$-49 - 4/f_{PCLK0}$		ns
Delay time from $\overline{\text{SCKBn}}$ to SOBn	t_{KSO1}			45	ns

a. f_{PCLK0} is the clock frequency of the digital filter connected to the input pin.

(b) Without Digital Filter

Table 7-12: CSIB Master Mode AC Characteristics without Digital Filter

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{\text{SCKBn}}$ cycle time	t_{KCY1}		125		ns
$\overline{\text{SCKBn}}$ high level width	t_{KH1}		0.5 t_{KCY1} - 80		ns
$\overline{\text{SCKBn}}$ low level width	t_{KL1}		0.5 t_{KCY1} - 80		ns
SIBn setup time (to $\overline{\text{SCKBn}}$)	t_{SIK1}		-93		ns
SIBn hold time (from $\overline{\text{SCKBn}}$)	t_{KSI1}		-49		ns
Delay time from $\overline{\text{SCKBn}}$ to SOBn	t_{KSO1}			45	ns

(2) CSIB Slave Mode

(a) With Digital Filter

Table 7-13: CSIB Slave Mode AC Characteristics with Digital Filter

Parameter	Symbol	Test Conditions	Min	Max	Unit
$\overline{\text{SCKBn}}$ cycle time	t_{KCY1}		$8/f_{PCLK0}$		ns
$\overline{\text{SCKBn}}$ high level width	t_{KH1}		$4/f_{PCLK0} - 5$		ns
$\overline{\text{SCKBn}}$ low level width	t_{KL1}		$4/f_{PCLK0} - 5$		ns
SIBn setup time (to $\overline{\text{SCKBn}}$)	t_{SIK1}		$15 + 2/f_{PCLK0}$ [a]		ns
SIBn hold time (from $\overline{\text{SCKBn}}$)	t_{KSI1}		$5 + 2/f_{PCLK0}$		ns
Delay time from $\overline{\text{SCKBn}}$ to SOBn	t_{KSO1}			$100 + 3/f_{PCLK0}$	ns

a. f_{PCLK0} is the clock frequency of the digital filter connected to the input pin.

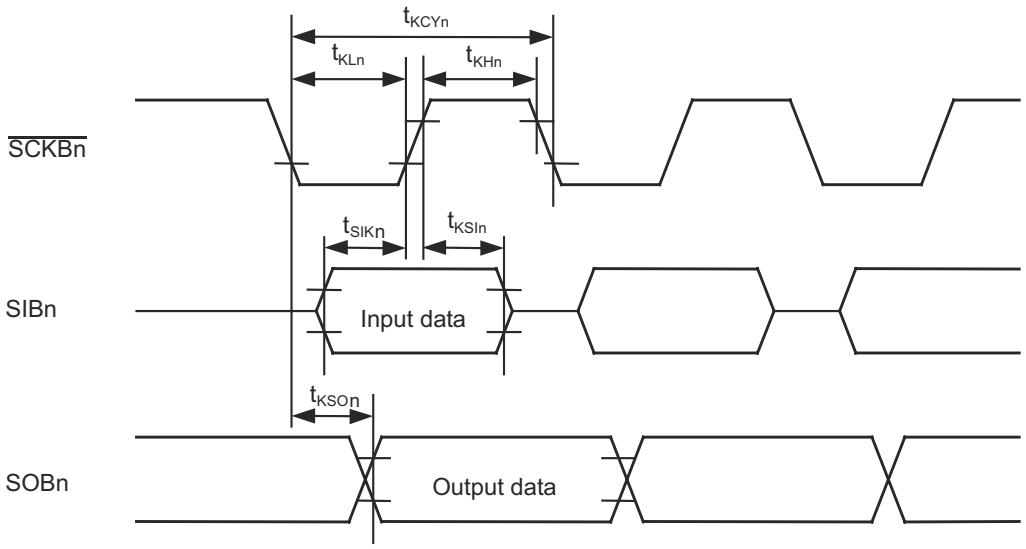
(b) Without Digital Filter

Table 7-14: CSIB Slave Mode AC Characteristics without Digital Filter

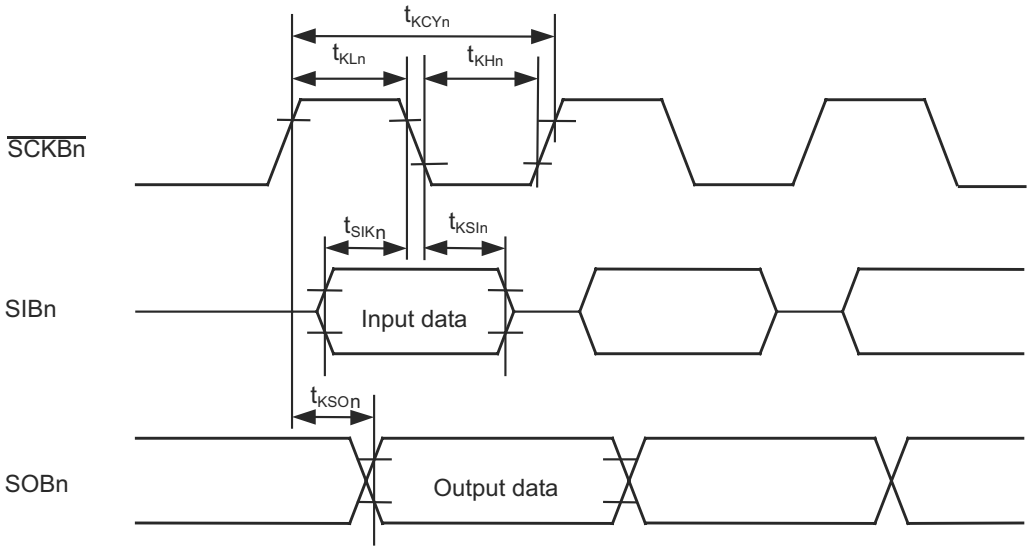
Parameter	Symbol	Test Conditions	Min	Max	Unit
$\overline{\text{SCKBn}}$ cycle time	t_{KCY1}		125		ns
$\overline{\text{SCKBn}}$ high level width	t_{KH1}		50		ns
$\overline{\text{SCKBn}}$ low level width	t_{KL1}		50		ns
SIBn setup time (to $\overline{\text{SCKBn}}$)	t_{SIK1}		15		ns
SIBn hold time (from $\overline{\text{SCKBn}}$)	t_{KSI1}		5		ns
Delay time from $\overline{\text{SCKBn}}$ to SOBn	t_{KSO1}			100	ns

Note: n = 2…0

Figure 7-8: CSI Master/Slave Mode Timing



CSI Master/Slave Mode Timing Inverted Clock



7.5.7 I²C

Table 7-15: I²C AC Characteristics

Parameter		Symbol	Normal Mode		Fast-speed Mode		Unit
			min	max	min	max	
SCL0 clock frequency		f_{CLK}	0	100	0	400	kHz
Bus-free time (between stop/start conditions)		t_{BUF}	4.7	—	1.3	—	µs
Hold time[a]		$t_{HD:STA}$	4.0	—	0.6	—	µs
SCL0 clock low-level width		t_{LOW}	4.7	—	1.3	—	µs
SCL0 clock high-level width		t_{HIGH}	4.0	—	0.6	—	µs
Setup time for start/restart conditions		$t_{SU:STA}$	4.7	—	0.6	—	µs
Data hold time	CBUS compatible master	$t_{HD:DAT}$	5.0	—	—	—	µs
	I²C mode		0[b]	3.45 [c]	0[Note b]	0.9[c]	µs
Data setup time		$t_{SU:DAT}$	250	—	100[d]	—	ns
STOP condition setup time		$t_{SU:STO}$	4.0	—	0.6	—	µs
Noise suppression [e]		t_{SP}				t_{IICLK}[f]	ns
Capacitive load of each bus line		C_b	—	400	—	400	pF

a. At the start condition, the first clock pulse is generated after the hold time

b. The system requires a minimum of 300ns hold time Internally for the SDA signal (at V_{IHmin} of SCL0 signal) in order to occupy the undefined area at the falling edge of SCL0.

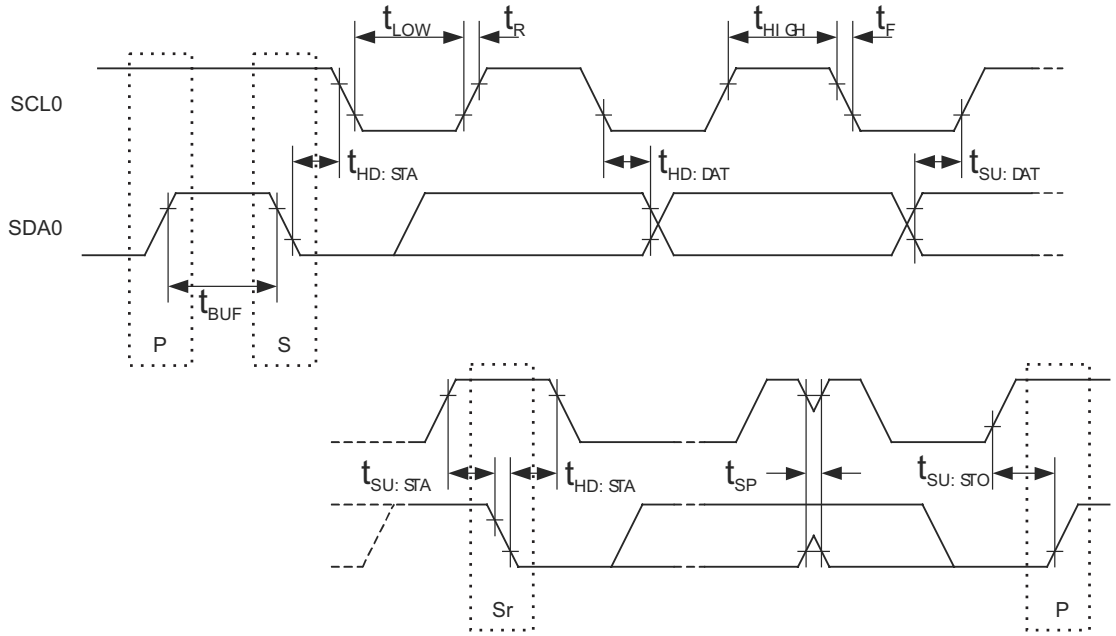
c. If the system does not extend the SCL0 signal low hold time (t_{low}), only the maximum data hold time ($t_{HD:DAT}$) needs to be satisfied.

d. The fast-speed-mode IIC bus can be used In a normal-mode IIC bus system.
In this case, set the fast-speed-mode IIC bus so that It meets the following conditions:
- If the system does not extend the SCL0n signal's low state hold time: tSU:DAT>/=250ns
- If the system extends the SCL0n signal's low state hold time:
Transmit the following data bit to the SDA0 line prior to releasing the SCL0 line (t_{Rmax}.+$t_{SU:DAT}$=1000+250=1250ns: Normal mode IIC bus specification).

e. Noise suppression is only available in Fast-speed mode.

f. t_{IICLK} is the period of the IICLK supplied by the clock controller.

Figure 7-9: I^2C Timing



Remarks: **1.** P: Stop condition

2. S: Start condition

3. Sr: Restart condition

4. Rise and Fall time depend on the actual load of the signal and the selected output current limit. For a capacitive load the time can be roughly calculated from:
($t_R = V_{OH} / I_{OH} * C_L$),
($t_F = V_{OH} / I_{OL} * C_L$)

7.6 LCD Bus Interface

T_A = -40 ~ +85°C,
DV_{DD5} = 3.15 V ~ 4.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
V_{DD5} = 3.2 V ~ 5.5 V, (see “Power On Clear” on page 80 for further functional restriction),
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427)
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427)

The following tables give the timing for Pin Group 3 used as LCD Bus Interface with Schmitt1 input characteristic and unlimited output current.

Table 7-16: LCD Bus Interface AC Characteristics

Parameter	Symbol	Cond.	Min.[a]	Max.	Unit
Cycle Time	t_{CYC}		CYC x T - 5	-	ns
Control LOW-Pulse Width	t_{CL}		(WST+1)T - 50	-	ns
Enable Active Pulse Width	t_{ELH}		(WST+1)T - 35	-	ns
Control Setup Time	t_{RWS}		0.5 T + 2	-	ns
Control Hold Time	t_{RWH}		0.5 T	-	ns
Data Output Setup Time	t_{DOS}		0.5 T - 20	0.5 T + 12	ns
Data output Hold Time	t_{DOH}		[CYC-(WST+1.5)] T - 88	-	ns
Data Input Setup Time	t_{DIS}		117	-	ns
Data Input Hold Time	t_{DIH}		0	-	ns
Output Disable Time	t_{OD}		0.5 T + 5	-	ns

a. T: $1/f_{LCD}$ (LCD Bus Interface macro clock frequency)
For clock selection refer to functional specification of the LCD Bus Interface
Always keep CYC $\geq$ 2
Always keep WST $\leq$ (CYC-2)

Figure 7-10: LCD Bus Interface Motorola Mode Timing

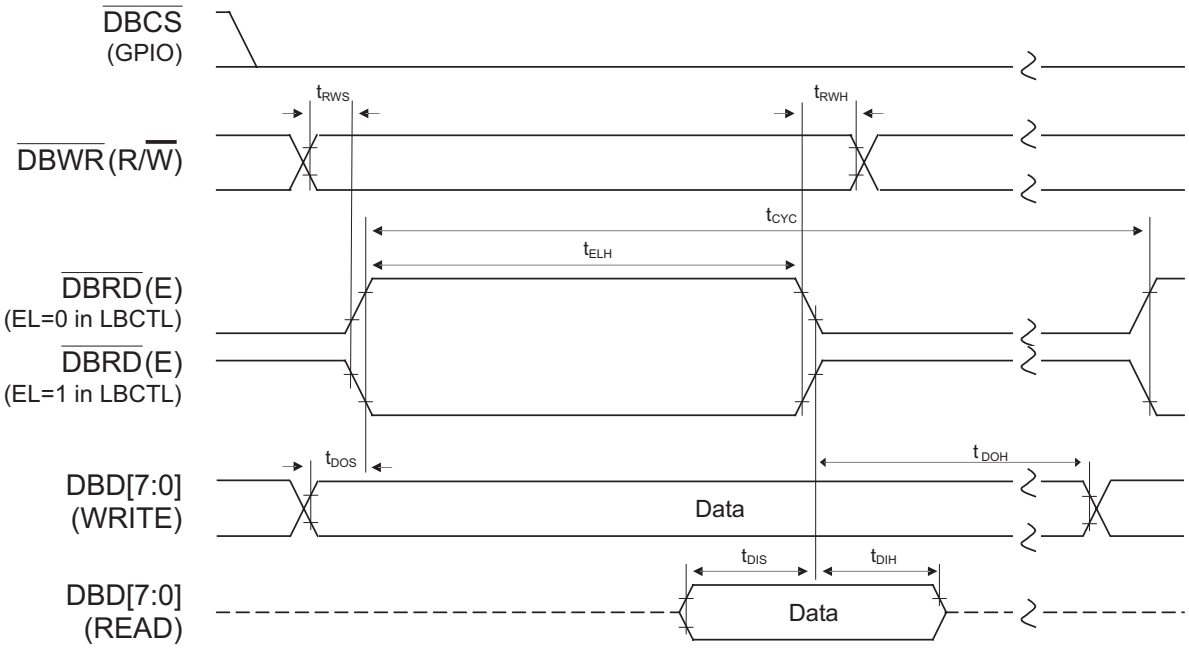


Figure 7-11: LCD Bus Interface Intel Mode Timing

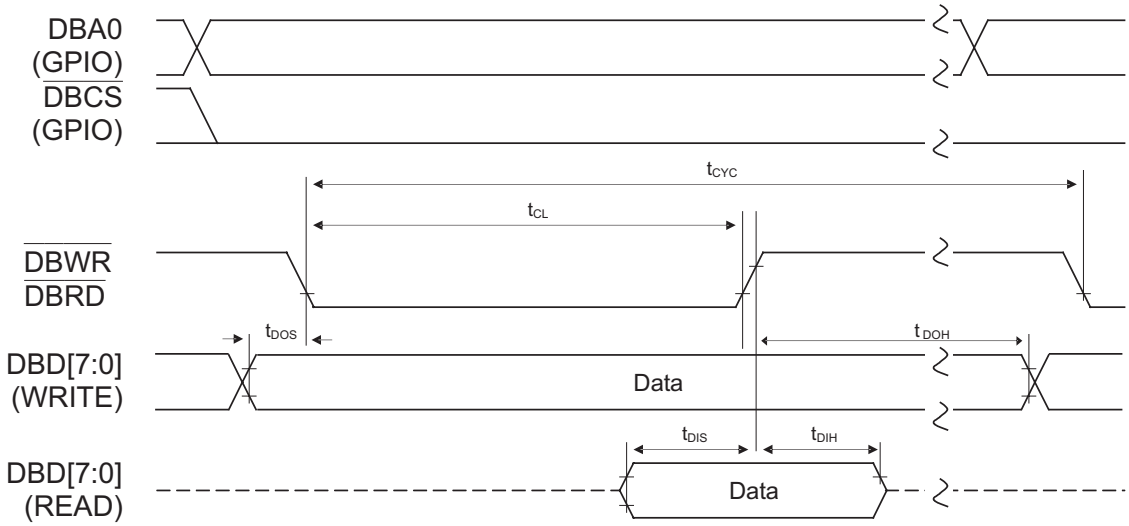


Figure 7-12: LCD Bus Interface Motorola Mode Turnaround Timing

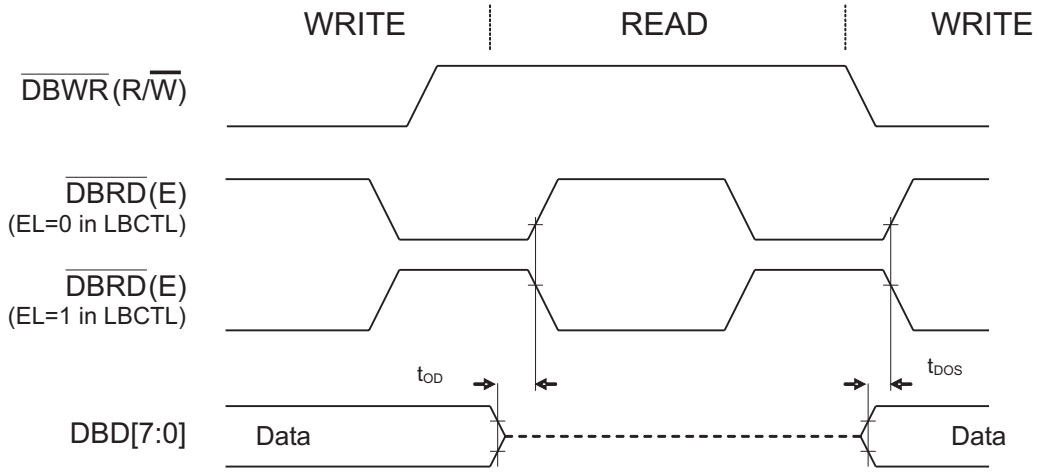
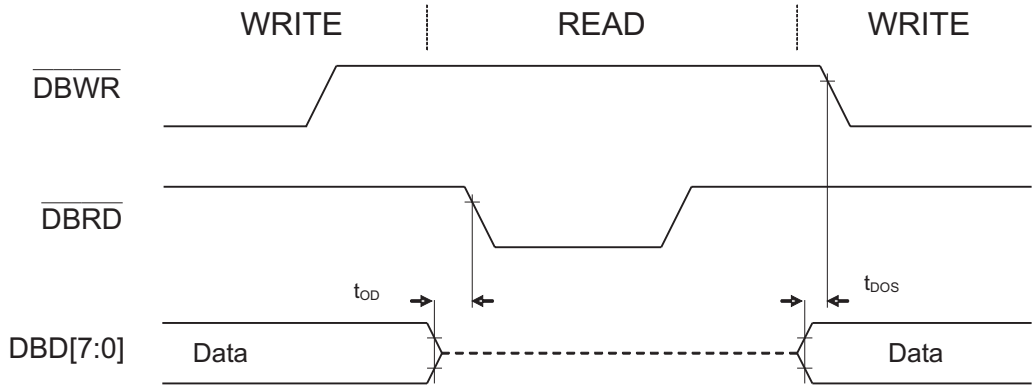


Figure 7-13: LCD Bus Interface Intel Mode Turnaround Timing



7.7 External Memory Access (µPD70F3427)

T_A = -40 ~ +85°C,
DV_{DD5} = 3.0 V ~ 3.6 V, (if used as ext. mem. I/F, DV_{DD5} = 3.0 V ~ 5.5 V otherwise)
MV_{DD5} = 3.0 V ~ 3.6 V,
BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
V_{DD5} = 3.2 V ~ 5.5 V, (see “Power On Clear” on page 80 for further functional restriction),
V_{SS5} = BV_{SS5} = DV_{SS5} = MV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V

Output pin load capacitance: C_L = 50pF

Table 7-17: External Memory Access Asynchronous Read Timing

Parameter	Symbol		Condi-tions	Min	Max	Unit
Data input set up time D0-D15 (vs.address)	<10>	T_{SAID}			$(2.0+W_T)T-22$	ns
Data input set up time D0-D15 (vs. $\overline{RD}\downarrow$)	<11>	T_{SRDID}			$(1.5+W_D)T-21$	ns
Data input set up time D16-D31 (vs.address)	<10>	T_{SAID}			$(2.0+W_T)T-27$	ns
Data input set up time D16-D31 (vs. $\overline{RD}\downarrow$)	<11>	T_{SRDID}			$(1.5+W_D)T-26$	ns
$\overline{RD}$ Low level width	<12>	T_{WRDL}		$(1.5+W_D)T-12$		ns
$\overline{RD}$ Low level width (delayed RD)	<12a>	T_{WRDL}		$(2+W_D)T-12$		ns
$\overline{RD}$ High level width	<13>	T_{WRDH}		$(1.5+W_{AS}+i)T-12$		ns
$\overline{RD}$ High level width (delayed RD)	<13a>	T_{WRDH}		$(1+W_{AS}+i)T-12$		ns
Address to $\overline{RD}$ delay time	<14>	T_{DARD}		$(0.5+W_{AS)}T-3$		ns
$\overline{CSn}$ to $\overline{RD}$ delay time	<14a>	T_{DCRD}		$(0.5+W_{AS})T-3$		ns
$\overline{RD}$ address delay time	<15>	T_{DRDA}		iT-7		ns
$\overline{RD}$ address delay time (delayed RD)	<15a>	T_{DRDA}		(-0.5+i)T-7		ns
Data input hold time (vs. $\overline{RD}\uparrow$)	<16>	T_{HRDID}		-11		ns
Data input hold time (vs. delayed $\overline{RD}\uparrow$)	<16a>	T_{HRDID}		-0.5T-11		ns
Write data output delay time after $\overline{RD}\uparrow$	<17>	T_{DRDOD}		(1+i)T-12		ns
Write data output delay time after delayed $\overline{RD}\uparrow$	<17a>	T_{DRDOD}		(0.5+i)T-12		ns

Note: T: 1 / fCPU (= frequency of system clock)
i: Number of idle states specified by BCC register
W_T: Total Number of waits, $W_T = W_{AS}+W_D$
W_{AS}: Number of waits specified by ASC register
W_D: Number of waits specified by DWC0, DWC1 register in SRAM mode and during off-page access in page mode. PRC register during on-page access in page mode.

Figure 7-14: SRAM Asynchronous Read Timing

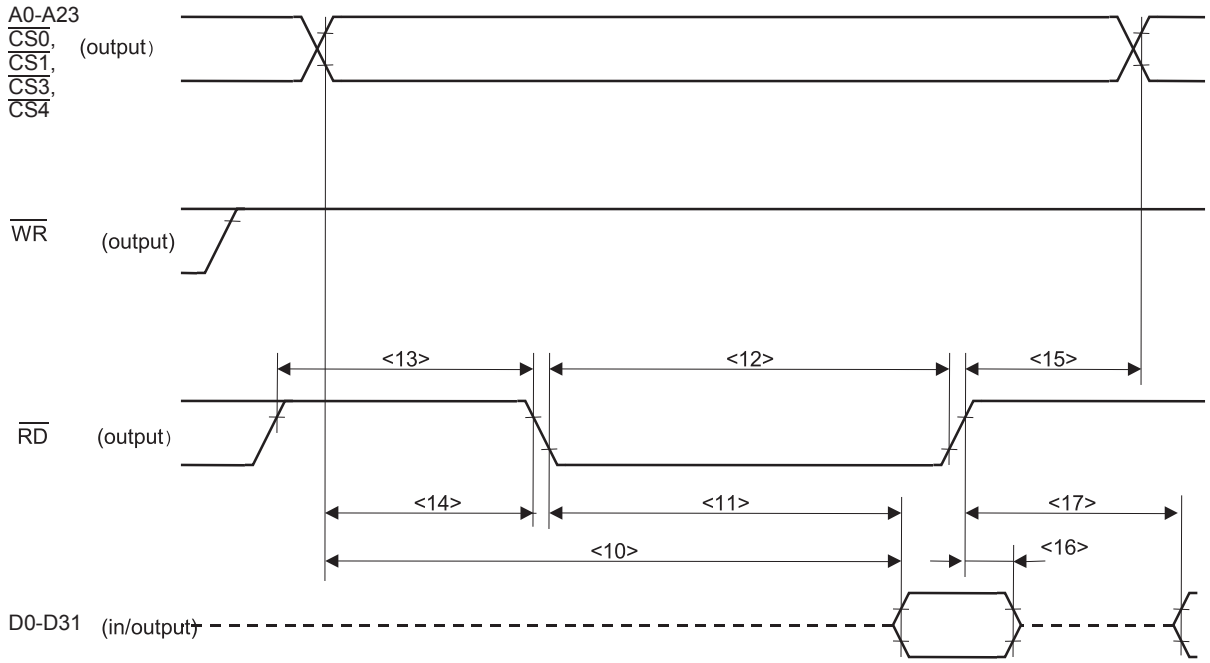
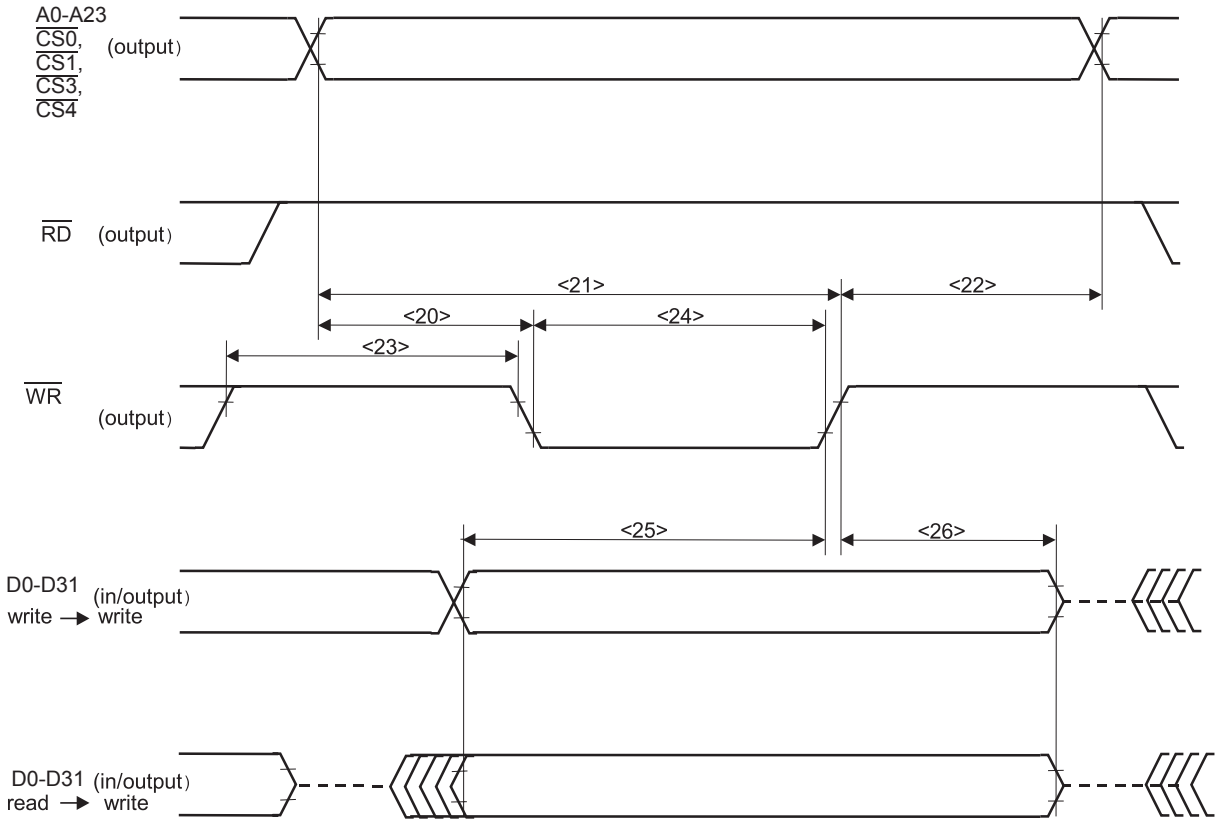


Table 7-18: External Memory Access Asynchronous Write Timing

Parameter	Symbol		Condi-tions	Min	Max	Unit
Address, $\overline{WR}$ delay time	<20>	T_{DAWR}		$(0.5+W_{AS})T-4$		ns
$\overline{CSn}$, $\overline{WR}$ delay time	<20a>	T_{DAWR}		$(0.5+W_{AS})T-4$		ns
Address set up (vs. $\overline{WR}\uparrow$)	<21>	T_{SAWR}		$(1.5+W_T)T-4$		ns
$\overline{WR}$ address delay time	<22>	T_{DWRA}		$(0.5+i)T-8$		ns
$\overline{WR}$ $\overline{CSn}$ delay time	<22a>	T_{DWRA}		$(0.5+i)T-8$		ns
$\overline{WR}$ High level width	<23>	T_{WWRH}		$(1+ i +W_{AS})T-12$		ns
$\overline{WR}$ Low level width	<24>	T_{WWRL}		$(1+W_D)T-8$		ns
Data output set up time D0-15 (vs. $\overline{WR}\uparrow$)	<25>	T_{SODWR}		$(1+W_T)T-10$		ns
Data output hold time D0-D15 (vs. $\overline{WR}\uparrow$)	<26>	T_{HWROD}		0.5iT+2		ns
Data output set up time D16-31 (vs. $\overline{WR}\uparrow$)	<25>	T_{SODWR}		$(1+W_T)T-15$		ns
Data output hold time D16-D31 (vs. $\overline{WR}\uparrow$)	<26>	T_{HWROD}		iT+2		ns

Note: T: 1 / fCPU (= frequency of system clock)
i: Number of idle states specified by BCC register
W_T: Total Number of waits, $W_T = W_{AS}+W_D$
W_{AS}: Number of waits specified by ASC register
W_D: Number of waits specified by DWC1, DWC2 register

Figure 7-15: SRAM Asynchronous Write Timing



Chapter 8 Analog Functions

8.1 A/D Converter

The number of available input channels depends on the device:
µPD70F3427, µPD70F3426, µPD70F3425, µPD70F3424: 16 channel input P70..P715.
µPD70F3423, µPD70F3422, µPD703422, µPD70F3421, µPD703421, µPD70F3420, µPD703420: 12 channel input P70..P711.

T_A = -40 ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.2 V ~ 5.5 V (µPD70F3427)
V_{DD5} = 3.2 V ~ 5.5 V, (see "Power On Clear" on page 80 for further functional restriction),
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427)

Table 8-1: A/D Converter Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Resolution	-			10		Bit
Reference voltage	AVREF		AV_{SS}		AV_{DD}	V
Overall error [a]	-	$AV_{SS} \le AIN \le AV_{REF}$, $4.5V \le (AV_{REF} = AV_{DD}) \le 5.5V$			+/- 3.5	LSB
	-	$AV_{SS} \le AIN \le AV_{REF}$, $3.5V = AV_{REF}$, $4.0V \le AV_{DD} \le 5.5V$			+/- 10	LSB
Additional error due to disturbance by digital read of P70..P715 [b]	DRERR				2	LSB
Conversion time [c]	T_{CONV}		3.88		15.50	µs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{DD}	V
Analogue supply current	I_{AVDD}				10	mA
Analog input equivalent circuit resistance[b]	R_{INA}		0.3		2.55	kΩ
Analog input equivalent circuit capacitance[b]	C_{INA}		4.0		8.0	pF
Analogue supply current	I_{AVDD}				10	mA
Reference voltage supply current [d]	I_{AVREF}				350	µA

a. Quantization error of ±0.5 LSB is not included

b. This value is not tested during production.

c. T_{CONV} depends on register setting

d. The reference current is mainly a transient current that is influenced by the conversion time. The given value is the maximum value. Value is not tested during production.

8.2 Power On Clear

T_A = -40 ~ +85°C,
V_{DD5} = 0 ~ 5.5 V,
V_{SS} = 0 V

Table 8-2: Power On Clear Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Threshold Voltage [a]	V_{IP}		3.2		4.0	V
Detection time [b]	T_{DETP}	V_{DD5} slope > 25mV/µs			2	µs

a. These are target values. Final values are fixed after device evaluation.

b. Not tested in production.

Note: The POC ensures that the devices stops operation (RESET condition) when the device is outside the operation voltage range, under the condition that the supply voltage slope on V_{DD5} is ≤ 25mV/µs.

Note: Full device operation is only available, when the supply voltage is above the maximum threshold voltage. The device may stop operation due to reset condition generated by POC, if the supply voltage dropps below the given max threshold voltage.

8.3 Voltage Comparator

The voltage comparator is supplied by A_{VDD}.

T_A = -40 ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
V_{DD5} = 3.2 V ~ 5.5 V, (see “Power On Clear” on page 80 for further functional restriction),
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427)
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427)

Table 8-3: Voltage Comparator Characteristics[a]

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Threshold Voltage (uncalibrated)	V_{IV}	TRMA = 15	1.56	1.73 [b]	1.92	V
Threshold Voltage (calibrated) [c]	V_{IV}		1.73 -0.065	1.73	1.73 +0.065	V
Detection Time [d]	T_{DETV2}	step = 100mV, overdrive = 5mV			2	µs
Stabilization Time	T_S				2	ms

a. These are target values. Final values are fixed after device evaluation.

b. The voltage will be decided after evaluation of the device.

c. The Voltage comparator has a cailbration capability. The application has to identify a calibration value for TRMA during production. This value must then be used by the application to overwrite the initial value of TRAM after RESET. The flow and conditions for the calibration will be defined in a separate document after device evaluation.

d. Not tested in production.

Chapter 9 Memory Characteristics

9.1 Basic Characteristics

T_A = -40 ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427)
V_{DD5} = 3.2 V ~ 5.5 V, (see “Power On Clear” on page 80 for further functional restriction),
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427)

Table 9-1: Memory Operation Characteristics

Parameter	Symbol	Device	Min	Typ	Max	Unit
Operation Frequency	f_{CPU}	µPD70F3427, µPD70F3426, µPD70F3425, µPD70F3424	32k		64M	Hz
		µPD70F3423, µPD70F3422, µPD70F3421, µPD70F3420	32k		32M	Hz
		µPD703422, µPD703421, µPD703420	32k		24M	Hz

The above maximum operation frequency specification lists the center frequency of the SSCG. The maximum dithering range of the SSCG is assured for this center frequency.

9.2 Flash Memory Characteristics

T_A = -40 ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427)
V_{DD5} = 4.5 V ~ 5.5 V, (see “Power On Clear” on page 80 for further functional restriction),
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427)

Table 9-2: Flash Memory Selfprogramming Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Number of Rewrites	C_{WRT}				1000	times
Data retention	t_{RET}		15			years
Blank Check Time[a]	t_{IVBL}			450	450	µs
Erase Time	t_{IERT4k}	One memory block (4k)[b]		25	250	ms
	$t_{IERT256k}$	64 memory blocks (256k)		64	640	ms
Write Time	t_{IWRT}	Write to words[c]		300	2800	µs
	t_{IWRT4k}	One memory block (4k)		45	tbd.	ms
Verify Time	t_{IVRT}			16	20	ms
Erase/Write Current [d]	I_{DDFL}			1	3	mA
Programming Temperature[e]	t_{PRG}		-40		+65	°C
		maximum power dissipation 0.8W	-40		+85	°C

a. Blank check of one memory block (4 kB).

b. Erase of one memory block (4kB).

c. The corresponding library call is configured for 2 word-write per call.

d. Additional current that is only needed during erase or write of flash.

e. The power dissipation may be reduced by disabling some functionality or reducing the CPU operation speed.

9.3 Special Conditions for End-of-Line Programming

T_A = +15 ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427)
V_{DD5} = 4.8 V ~ 5.15 V, (see “Power On Clear” on page 80 for further functional restriction),
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427)

(1) Flash Memory End-of-Line Programming Characteristics (PG-FP4)

Table 9-3: Flash Memory End-of-Line Programming Characteristics (PG-FP4: CSI)

Parameter	Symbol	Device	Test Conditions	Min	Typ	Max	Unit
Blank Check	t_{IVBL}	All	W/E cycles ≤ 5		1	1	s
Erase Time [a]	t_{IWRT}				1	1	s
Write Time [b]	t_{IERT}	µPD70F3426, µPD70F3425			20	32	s
		µPD70F3424, µPD70F3423			10	16	s
		µPD70F3421			5	8	s
Verify Time	t_{IVRT}	µPD70F3426, µPD70F3425			16	20	s
		µPD70F3424, µPD70F3423			8	10	s
		µPD70F3421			5	7	s

a. Erase of all flash-memory blocks (0 .. 255)

b. Write of complete flash area.

Table 9-4: Flash Memory End-of-Line Programming Characteristics (PG-FP4: UART)

Parameter	Symbol	Device	Test Conditions	Min	Typ	Max	Unit
Blank Check	t_{IVBL}	All	W/E cycles ≤ 5		1	1	s
Erase Time [a]	t_{IWRT}				1	1	s
Write Time [b]	t_{IERT}	µPD70F3426			230	300	s
		µPD70F3425			115	150	s
		µPD70F3424, µPD70F3423			60	80	s
		µPD70F3421			30	40	s
Verify Time	t_{IVRT}	µPD70F3426			230	300	s
		µPD70F3425			115	150	s
		µPD70F3424, µPD70F3423			60	80	s
		µPD70F3421			30	40	s

a. Erase of all flash-memory blocks (0 .. 255)

b. Write of complete flash area.

(2) Flash Memory End-of-Line Programming Characteristic (Flash-Selfprogramming)

Table 9-5: Flash Memory End-of-Line Programming Characteristics (Flash-Selfprogramming)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Blank Check[a]	t_{IVBL}	W/E cycles ≤ 5		450	450	µs
Erase Time one memory block (4k)	t_{IWRT4k}			25	50	ms
Erase Time 64 memory blocks (256k)	$t_{IWRT256k}$			64	128	ms
Write Time (Write two words)[b]	t_{IERT}			300	600	µs
Write Time (One memory block 4k)	t_{IERT4k}			45	tbd.	ms
Verify Time	t_{IVRT}			tbd.	tbd.	s

a. Blank check of one memory block (4kB).

b. The corresponding library call is configured for 2 word per call.

9.4 Serial Write Operation Characteristics

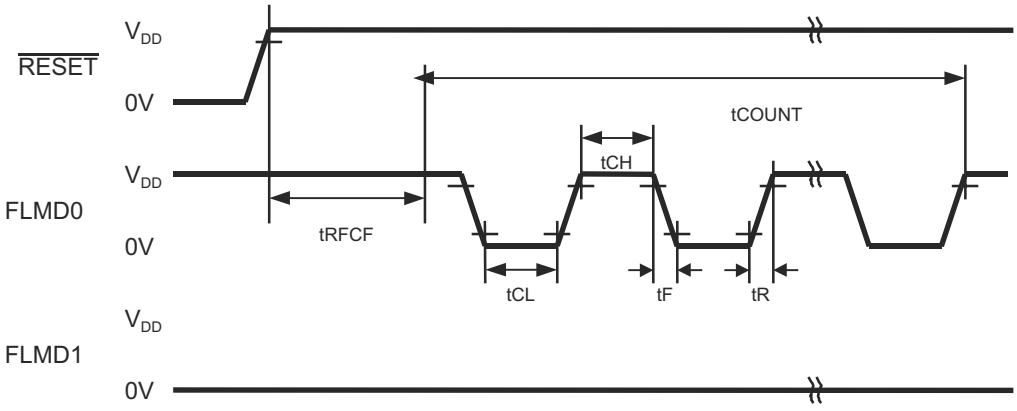
T_A = -40 ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427)
V_{DD5} = 4.5 V ~ 5.5 V, (see “Power On Clear” on page 80 for further functional restriction),
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427)

Table 9-6: Flash Memory AC Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Count start time from rising edge of $\overline{\text{RESET}}$ to FLMD0	t_{RFCF}		5			ms
Count ending time from rising edge of $\overline{\text{RESET}}$ to FLMD0	t_{COUNT}				20	ms
FLMD0 counter High/Low level width	t_{CH},t_{CL}		10		100	µs
FLMD0 counter rise/fall time	t_R,t_F				50	ns

Note: FLMD1 is a shared function of the P07 pin.

Figure 9-1: Flash Memory Timing



Chapter 10 Special Conditions for Device Operation at extended Operating Temperature Range (T_A = -40°C ... +105°C)

Caution: For any device's operation within the extended operating temperature range (T_A = -40 °C ... +105°C), the device's total power consumption must be reduced. The following tables within this chapter describe additional device conditions securing the requested decrease of the device's power consumption.

In case any device may operate within the extended operating temperature range (T_A = -40°C ... +105°C) all of the below mentioned conditions must never be exceeded at any time.

All of the below mentioned device conditions must be applied in addition to any other parameter that is described within this document.

Condition 1 (µPD70F3427):
T_A = -40 ... +105°C,
Operation Modes: RUN, HALT, IDLE
Power dissipation:
< 1.0 W

Duration: 15000 hours
V_{SS5} = 0V

Condition 2:
T_A = -40 ... +105°C,
Operation Modes: WATCH, Sub-WATCH, STOP, Sub-Clock CPU Operation
Power dissipation: < 0.5W
Duration: 15 years
V_{SS5} = 0V

Table 10-1: Absolute maximum ratings currents 105°C (µPD70F3427)

Parameter		Symbol	Test Conditions		Ratings average	Unit
Output current low	All pins	I_{OLA}	Sum of Groups 1, 2, 3, 5, 6, 7, 8	f_{SYS}= 48 MHz	70	mA
Output current high		I_{OHA}			-70	mA
Number of active stepper					4	
Output current low	All pins	I_{OLA}	Sum of Groups 1, 2, 3, 5, 6, 7, 8	f_{SYS}= 24 MHz	250	mA
Output current high		I_{OHA}			-250	mA
Number of active stepper					6	

Condition 1 (µPD70F3426):
T_A = -40 ... +105°C,
Operation Modes: RUN, HALT, IDLE
Power dissipation:
< 1.0 W

Duration: 15000 hours
V_{SS5} = 0V

Condition 2:
T_A = -40 ... +105°C,
Operation Modes: WATCH, Sub-WATCH, STOP, Sub-Clock CPU Operation
Power dissipation: < 0.5W
Duration: 15 years
V_{SS5} = 0V

Table 10-2: Absolute maximum ratings currents 105°C (µPD70F3426)

Parameter		Symbol	Test Conditions		Ratings average	Unit
Output current low	All pins	I_{OLA}	Sum of Groups 1, 2, 3, 5, 6, 7, 8	f_{SYS}= 48 MHz	40	mA
Output current high		I_{OHA}			-40	mA
Number of active stepper					6	
Output current low	All pins	I_{OLA}	Sum of Groups 1, 2, 3, 5, 6, 7, 8	f_{SYS}= 24 MHz	250	mA
Output current high		I_{OHA}			-250	mA
Number of active stepper					6	

Condition 1 (µPD70F3425):
T_A = -40 ... +105°C,
Operation Modes: RUN, HALT, IDLE
Power dissipation:
< 0.9 W

Duration: 15000 hours
V_{SS5} = 0V

Condition 2:
T_A = -40 ... +105°C,
Operation Modes: WATCH, Sub-WATCH, STOP, Sub-Clock CPU Operation
Power dissipation: < 0.5W
Duration: 15 years
V_{SS5} = 0V

Table 10-3: Absolute maximum ratings currents 105°C (µPD70F3425)

Parameter		Symbol	Test Conditions		Ratings average	Unit
Output current low	All pins	I_{OLA}	Sum of Groups 1, 2, 3, 5, 6, 7, 8	f_{SYS}= 48 MHz	135	mA
Output current high		I_{OHA}			-135	mA
Number of active stepper					6	
Output current low	All pins	I_{OLA}	Sum of Groups 1, 2, 3, 5, 6, 7, 8	f_{SYS}= 32 MHz	250	mA
Output current high		I_{OHA}			-250	mA
Number of active stepper					6	

Condition 1 (µPD70F3424):
T_A = -40 ... +105°C,
Operation Modes: RUN, HALT, IDLE
Power dissipation:
< 0.88 W

Duration: 15000 hours
V_{SS5} = 0V

Condition 2:
T_A = -40 ... +105°C,
Operation Modes: WATCH, Sub-WATCH, STOP, Sub-Clock CPU Operation
Power dissipation: < 0.5W
Duration: 15 years
V_{SS5} = 0V

Table 10-4: Absolute maximum ratings currents 105°C (µPD70F3424)

Parameter		Symbol	Test Conditions		Ratings average	Unit
Output current low	All pins	I_{OLA}	Sum of Groups 1, 2, 3, 5, 6, 7, 8	f_{SYS}= 48 MHz	180	mA
Output current high		I_{OHA}			-180	mA
Number of active stepper					6	
Output current low	All pins	I_{OLA}	Sum of Groups 1, 2, 3, 5, 6, 7, 8	f_{SYS}= 32 MHz	250	mA
Output current high		I_{OHA}			-250	mA
Number of active stepper					6	

Condition 1 (µPD703420, µPD703421, µPD70F3421, µPD703422, µPD70F3422, µPD70F3423):
T_A = -40 ... +105°C,
Operation Modes: RUN, HALT, IDLE
Power dissipation:
< 0.86 W

Duration: 15000 hours
V_{SS5} = 0V

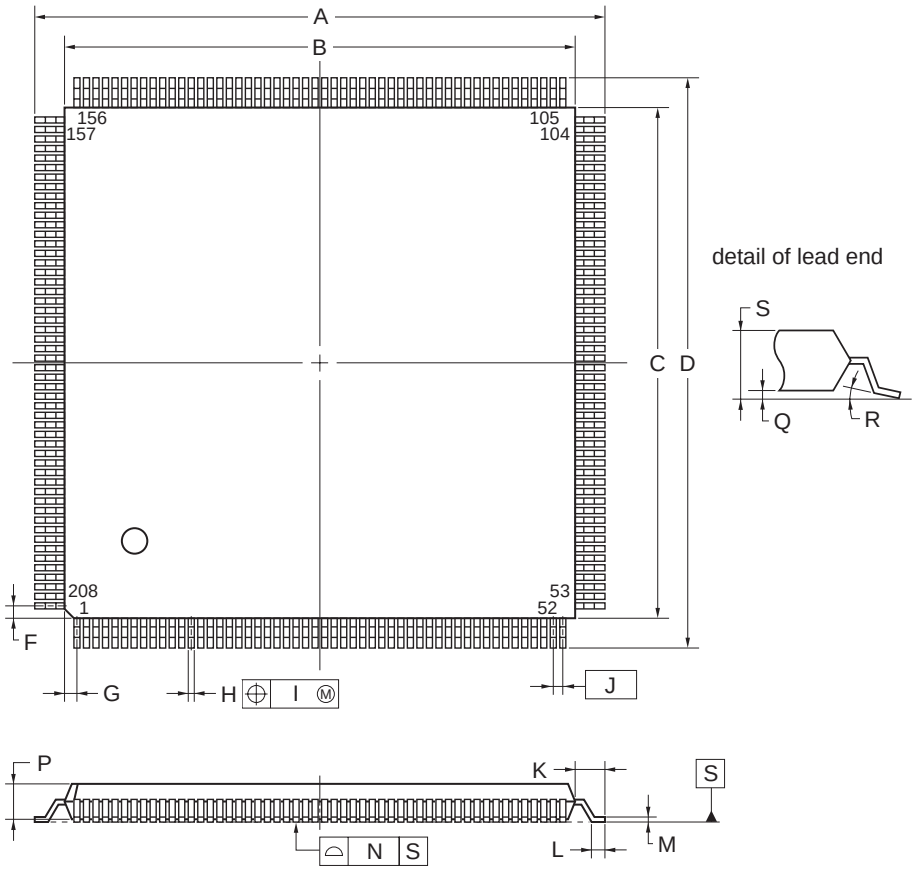
Condition 2:
T_A = -40 ... +105°C,
Operation Modes: WATCH, Sub-WATCH, STOP, Sub-Clock CPU Operation
Power dissipation: < 0.5W
Duration: 15 years
V_{SS5} = 0V

Note: No additional condition must be followed.

Chapter 11 Package

11.1 Package Drawing µPD70F3427GD

208-PIN PLASTIC QFP (FINE PITCH) (28x28)



NOTE

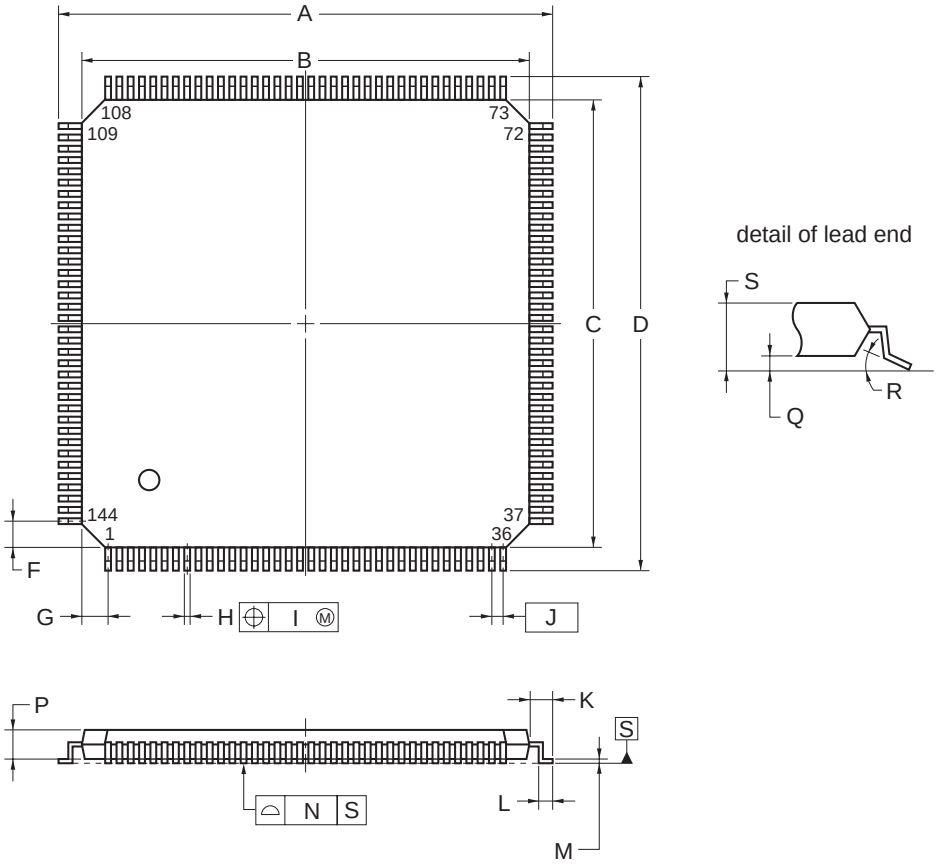
Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	30.6±0.2
B	28.0±0.2
C	28.0±0.2
D	30.6±0.2
F	1.25
G	1.25
H	$0.22^{+0.05}_{-0.04}$
I	0.10
J	0.5 (T.P.)
K	1.3±0.2
L	0.5±0.2
M	$0.17^{+0.03}_{-0.07}$
N	0.10
P	3.2±0.1
Q	0.4±0.1
R	5°±5°
S	3.8 MAX.

P208GD-50-LML,MML,SML,WML-7

11.2 Package Drawing μPD70F3426GJ, μPD70F3425GJ, μPD70F3424GJ, μPD70F3423GJ, μPD70F3422GJ, μPD703422GJ, μPD70F3421GJ, μPD703421GJ, μPD70F3420GJ, μPD703420GJ

144-PIN PLASTIC LQFP (FINE PITCH) (20x20)



NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	22.0±0.2
B	20.0±0.2
C	20.0±0.2
D	22.0±0.2
F	1.25
G	1.25
H	0.22±0.05
I	0.08
J	0.5 (T.P.)
K	1.0±0.2
L	0.5±0.2
M	$0.17^{+0.03}_{-0.07}$
N	0.08
P	1.4
Q	0.10±0.05
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.5±0.1

S144GJ-50-UEN

Chapter 12 Revision History

Item	Date published	Document No.	Comment
1	July 5th , 2005	EASE-PL-8007-0V1	First release of this document
2	August 3rd, 2005	EASE-PL-8007-0V2	Second release of this document
3	December 13th, 2005	EASE-PL-8007-0V3	Update of document
			Overview: - Included the derivatives µPD70F3427, µPD70F3426, µPD70F3422, µPD703422. - Included a note describing the expansion of flash and RAM for the derivative µPD70F3426. - Included the LCD I/F to the reduced peripheral set.
			DC characteristics: - Added typical operating current for 48MHz. - Changed VCOMP0/1 to VCMP0/1. - Corrected the table 6-15.
			Pinout Information: - Included the Pinconfiguration of the new derivatives µPD70F3427 and µPD70F3426. - Introduced the pin-group 6 representing the external memory-interface of the new derivative µPD70F3427. - Introduced the pin-group 8 representing the voltage comparator input pins.
			Absolute Maximum Ratings: - Included the DJ3 derivatives µPD70F3427, µPD70F3426, µPD70F3422, µPD703422. - Included the concerned parameters for the µPD70F3427's memory interface.
			General Characteristics: - Included the concerned information regarding the external memory interface of the derivative µPD70F3427.
			Operation Conditions: - Included the DJ3 derivatives µPD70F3427 and µPD70F3426 for the corrseponding CPU clock frequencies 32 MHz and 48 MHz.
			DC-Characteristics: - Included the DJ3 derivatives µPD70F3427 and µPD70F3426. - Separated the characteristics of pin-group 3 for µPD70F3427 and the remaining devices. - Included the characteristics of pin-group 6 for the device µPD70F3427. - Included the supply-currents for added derivatives µPD70F3427 and µPD70F3426. - Added a note regarding current limit function of the derivative µPD70F3427. - Review of chapter "LCD Common and Segment Lines".
			AC-Characteristics: - Included the derivatives µPD70F3427 and µPD70F3426. - Included the external memory access specification for the derivative µPD70F3427.

Item	Date published	Document No.	Comment
3	December 13th, 2005	EASE-PL-8007-0V3	Analog Functions: - POC characteristics. Included a note.
			Flash Memory: - Included the derivatives µPD70F3427 and µPD70F3426.
			Package: - Included the derivatives µPD70F3427 and µPD70F3426 - Added the package drawings for the derivatives µPD70F3427 and µPD70F3426.
4	September 4th, 2006	EASE-PL-8007-1V0	Redefinition of that document "Electrical Target Specification" to "Preliminary Data Sheet".
			Family Overview: - Updated operating clock.
			Operation Conditions: - Update the CPU clock frequencies.
			DC-Characteristics: - Updated the supply-currents for all derivatives. - Completion of table 6-23.
			AC-Characteristics: - Updated the AC-Characteristics for the ext. mem. I/F (µPD70F3427).
5	January 18th, 2007	EASE-PL-8007-1V1	DC-Characteristics: - Included the values for the LCD split voltages - Updated the supply-currents for the derivatives µPD70F3424, µPD70F3426 and µPD70F3427.
			AC- Characteristics: - CSIB updated and expanded characteristics. - LCD Bus Interface updated. - External memory access updated.
			Analog Functions: - Added the Voltage Comparator Characteristics stabilization time.
			Flash Memory: - Updated parameters for End-of-Line programming. Included parameters for missing derivatives.
			Special Conditions for Device Operation at extended Operating Temperature Range (T_A = -40°C ... +105°C) - Included a new chapter describing the operating conditions when device is operating within the extened operating temperature range.

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