

# ACT-S128K32 High Speed 4 Megabit SRAM Multichip Module

## Features

- 4 Low Power CMOS 128K x 8 SRAMs in one MCM
- Overall configuration as 128K x 32
- Input and Output TTL Compatible
- 17, 20, 25, 35, 45 & 55ns Access Times, 15ns Available by Special Order
- Full Military (-55°C to +125°C) Temperature Range
- +5V Power Supply
- Choice of 6 Hermetically sealed Co-fired Packages:
  - 68-Lead, Low Profile CQFP (F1), 1.56"SQ x .140"max
  - 68-Lead, Dual-Cavity CQFP (F2), .88"SQ x .20"max (.18"max thickness available, contact factory for details) (*Drops into the 68 Lead JEDEC .99"SQ CQFJ footprint*)
  - 66-Lead, PGA-Type (P2,P6 with/without shoulders), 1.185"SQ x .245"max
  - 66-Lead, PGA-Type (P7,P3 with/without shoulders), 1.08"SQ x .160"max
- Internal Decoupling Capacitors
- DESC SMD# 5962-93187 Released (P2,P3,P6,P7)  
5962-95595 Released (F1,F2)



## General Description

The ACT-S128K32 is a High Speed 4 megabit CMOS SRAM Multichip Module (MCM) designed for full temperature range, military, space, or high reliability mass memory and fast cache applications.

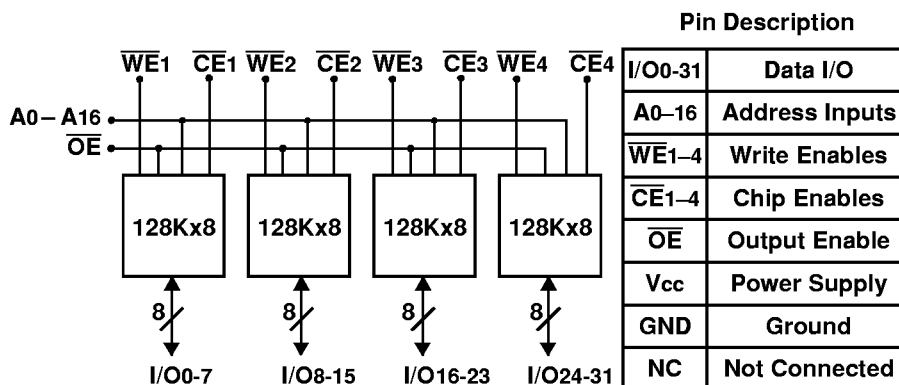
The MCM can be organized as a 128K x 32 bits, 256K x 16 bits or 512k x 8 bits device and is input and output TTL compatible. Writing is executed when the write enable ( $\overline{WE}$ ) and chip enable ( $\overline{CE}$ ) inputs are low. Reading is accomplished when  $\overline{WE}$  is high and  $\overline{CE}$  and output enable ( $\overline{OE}$ ) are both low. Access time grades of 17ns, 20ns, 25ns, 35ns, 45ns and 55ns maximum are standard.

The +5 Volt power supply version is standard and the +3.3 Volt low power model is available (See ACT-S128K32V data sheet).

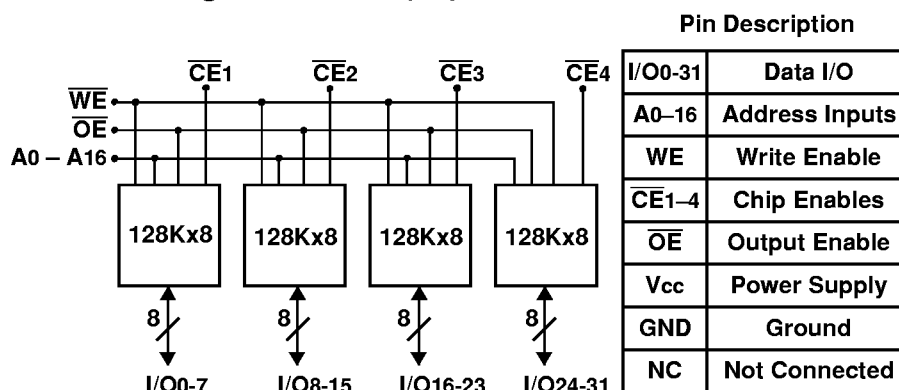
The products are designed for operation over the temperature range of -55°C to +125°C and screened under the full military environment. DESC Standard Military Drawing (SMD) part numbers are released and available.

The ACT-S128K32 is manufactured in Aeroflex's 80,000ft<sup>2</sup> MIL-PRF-38534 certified facility in Plainview, N.Y.

Block Diagram – PGA Type Package(P2,P7) & CQFP(F2)



Block Diagram – CQFP(F1)



## Absolute Maximum Ratings

Symbol	Rating	Range	Units
$T_C$	Case Operating Temperature	-55 to +125	°C
$T_{STG}$	Storage Temperature	-65 to +150	°C
$P_D$	Maximum Package Power Dissipation		
	F1, P2/P6, P3/P7 Packages	4.4	W
	F2 Package	3.3	W
$\theta_{J-C}$	Hottest Die, Max Thermal Resistance - Junction to Case		
	F1, P2/P6, P3/P7 Packages	2.0	°C/W
	F2 Package	8.0	°C/W
$V_G$	Maximum Signal Voltage to Ground	-0.5 to +7	V
$T_L$	Maximum Lead Temperature (10 seconds)	300	°C

## Normal Operating Conditions

Symbol	Parameter	Minimum	Maximum	Units
$V_{CC}$	Power Supply Voltage	+4.5	+5.5	V
$V_{IH}$	Input High Voltage	+2.2	$V_{CC} + 0.3$	V
$V_{IL}$	Input Low Voltage	-0.5	+0.8	V

## Truth Table

Mode	CE	OE	WE	Data I/O	Power
Standby	H	X	X	High Z	Standby (deselect/power down)
Read	L	L	H	Data Out	Active
Read	L	H	H	High Z	Active (deselected)
Write	L	X	L	Data In	Active

## Capacitance

(f = 1MHz,  $T_C = 25^\circ\text{C}$ )

Symbol	Parameter	Maximum	Units
$C_{AD}$	A <sub>0</sub> – A <sub>16</sub> Capacitance	50	pF
$C_{OE}$	$\overline{OE}$ Capacitance	50	pF
$C_{WE}$	CQFP(F1) Package	50	pF
	PGA(P2,P3,P6,P7) and CQFP(F2) Packages	20	pF
$C_{CE}$	Chip Enable Capacitance	20	pF
$C_{I/O}$	I/O <sub>0</sub> – I/O <sub>31</sub> Capacitance	20	pF

Capacitance is guaranteed by design but not tested.

## DC Characteristics

(4.5Vdc ≤ V<sub>CC</sub> ≤ 5.5Vdc, V<sub>SS</sub> = 0V, T<sub>C</sub> = -55°C to +125°C, Unless otherwise specified)

Parameter	Sym	Conditions	-017 & -020		-025 & -035		-045 & -055		Units
			Min	Max	Min	Max	Min	Max	
Input Leakage Current	$I_{LI}$	V <sub>CC</sub> = Max, V <sub>IN</sub> = 0 or V <sub>CC</sub>		10		10		10	μA
Output Leakage Current	$I_{LO}$	$\overline{CE} = V_{IH}, \overline{OE} = V_{IH},$ V <sub>OUT</sub> = 0 or V <sub>CC</sub>		10		10		10	μA
Operating Supply Current 32 Bit Mode	$I_{CCX32}$	$\overline{CE} = V_{IL}, \overline{OE} = V_{IH},$ f = 5 MHz, V <sub>CC</sub> = Max, CMOS Compatible		600		600		600	mA

### DC Characteristics (Continued)

( $4.5V_{dc} \leq V_{CC} \leq 5.5V_{dc}$ ,  $V_{SS} = 0V$ ,  $T_C = -55^{\circ}C$  to  $+125^{\circ}C$ , Unless otherwise specified)

Parameter	Sym	Conditions	-017 & -020		-025 & -035		-045 & -055		Units
			Min	Max	Min	Max	Min	Max	
Standby Current	$I_{SB}$	$\overline{CE} = V_{IH}$ , $\overline{OE} = V_{IH}$ , $f = 5 \text{ MHz}$ , $V_{CC} = \text{Max}$ , CMOS Compatible		80		60		60	mA
Output Low Voltage	$V_{OL}$	$I_{OL} = 8 \text{ mA}$ , $V_{CC} = \text{Min}$		0.4		0.4		0.4	V
Output High Voltage	$V_{OH}$	$I_{OH} = -4.0 \text{ mA}$ , $V_{CC} = \text{Min}$	2.4		2.4		2.4		V

### AC Characteristics

( $V_{CC} = 5.0V$ ,  $V_{SS} = 0V$ ,  $T_C = -55^{\circ}C$  to  $+125^{\circ}C$ )

#### Read Cycle

Parameter	Sym	-017		-020		-025		-035		-045		-055		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	$t_{RC}$	17		20		25		35		45		55		ns
Address Access Time	$t_{AA}$		17		20		25		35		45		55	ns
Chip Enable Access Time	$t_{ACE}$		17		20		25		35		45		55	ns
Output Hold from Address Change	$t_{OH}$	0		0		0		0		0		0		ns
Output Enable to Output Valid	$t_{OE}$		9		12		15		20		25		30	ns
Chip Enable to Output in Low Z*	$t_{CLZ}$	3		3		3		3		3		3		ns
Output Enable to Output in Low Z*	$t_{OLZ}$	0		0		0		0		0		0		ns
Chip Deselect to Output in High Z*	$t_{CHZ}$		12		12		12		15		20		20	ns
Output Disable to Output in High Z*	$t_{OHZ}$		10		11		12		15		20		20	ns

\* Parameters guaranteed by design but not tested

#### Write Cycle

Parameter	Sym	-017		-020		-025		-035		-045		-055		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	$t_{WC}$	17		20		25		35		45		55		ns
Chip Enable to End of Write	$t_{CW}$	12		15		20		25		30		40		ns
Address Valid to End of Write	$t_{AW}$	12		15		20		25		30		40		ns
Data Valid to End of Write	$t_{DW}$	10		12		15		18		20		20		ns
Write Pulse Width	$t_{WP}$	13		15		20		25		30		40		ns
Address Setup Time	$t_{AS}$	0		0		0		0		0		0		ns
Output Active from End of Write *	$t_{OW}$	3		3		3		4		4		4		ns
Write to Output in High Z *	$t_{WHZ}$		10		10		10		15		15		15	ns
Data Hold from Write Time	$t_{DH}$	0		0		0		0		0		0		ns
Address Hold Time	$t_{AH}$	0		0		0		0		0		0		ns

\* Parameters guaranteed by design but not tested

### Data Retention Electrical Characteristics (Special Order Only)

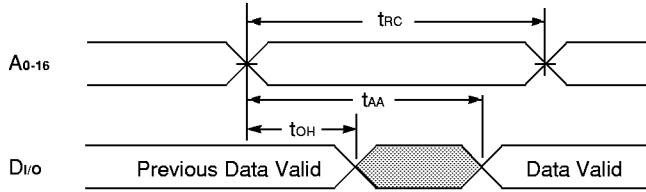
( $T_C = -55^{\circ}C$  to  $+125^{\circ}C$ )

Parameter	Sym	Test Conditions	All Speeds		Units
			Min	Max	
$V_{CC}$ for Data Retention	$V_{DR}$	$\overline{CE} \geq V_{CC} - 0.2V$	2	5.5	V
Data Retention Current	$I_{CCDR1}$	$V_{CC} = 3V$ , 17-55ns		10.4	mA

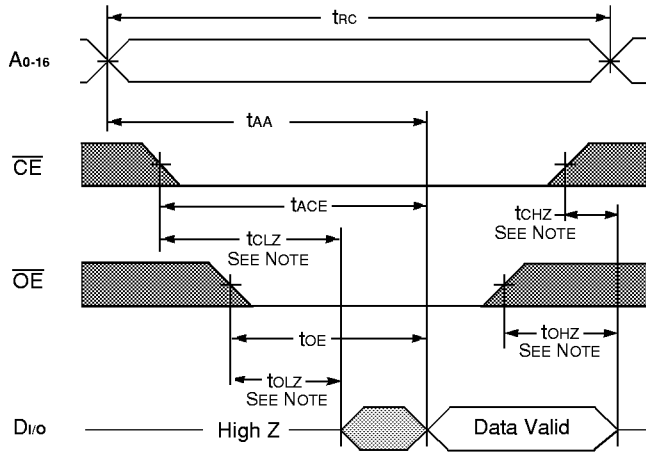
## Timing Diagrams

### Read Cycle Timing Diagrams

**Read Cycle 1 ( $\overline{CE} = \overline{OE} = V_{IL}$ ,  $\overline{WE} = V_{IH}$ )**



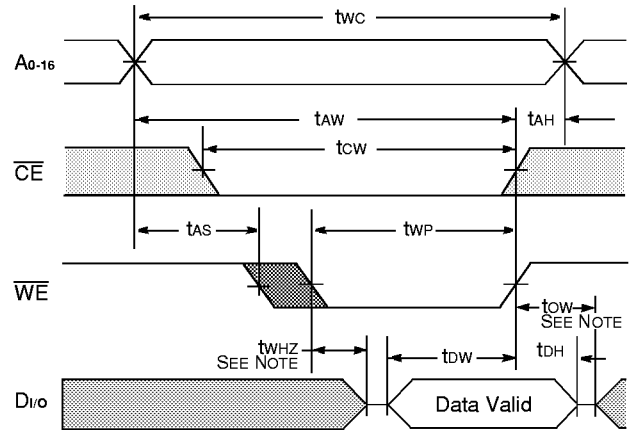
**Read Cycle 2 ( $\overline{WE} = V_{IH}$ )**



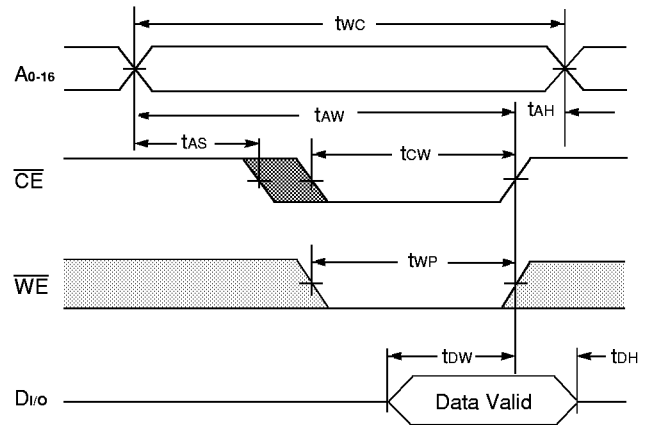
Note: Guaranteed by design, but not tested.

### Write Cycle Timing Diagrams

**Write Cycle 1 ( $\overline{WE}$  Controlled,  $\overline{OE} = V_{IL}$ )**

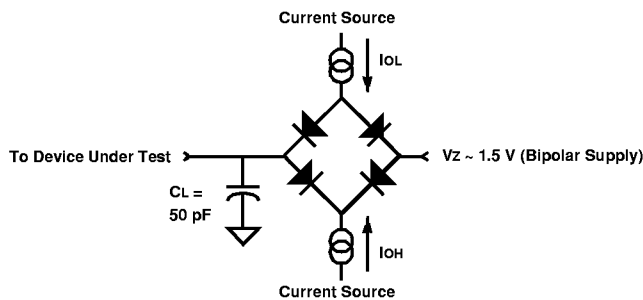


**Write Cycle 2 ( $\overline{CE}$  Controlled,  $\overline{OE} = V_{IH}$ )**



Note: Guaranteed by design, but not tested.

### AC Test Circuit



**Notes:**

- 1)  $V_Z$  is programmable from -2V to +7V. 2)  $I_{OL}$  and  $I_{OH}$  programmable from 0 to 16 mA. 3) Tester Impedance  $Z_O = 75\Omega$ . 4)  $V_Z$  is typically the midpoint of  $V_{OH}$  and  $V_{OL}$ . 5)  $I_{OL}$  and  $I_{OH}$  are adjusted to simulate a typical resistance load circuit. 6) ATE Tester includes jig capacitance.

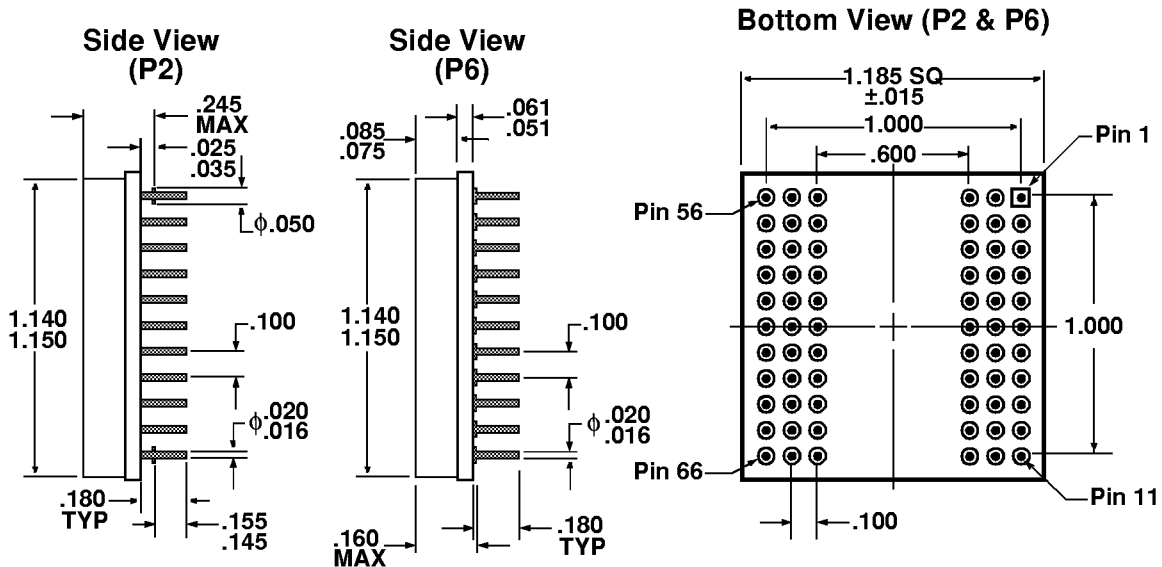
Parameter	Typical	Units
Input Pulse Level	0 – 3.0	V
Input Rise and Fall	5	ns
Input and Output Timing Reference Level	1.5	V
Output Lead Capacitance	50	pF

## Pin Numbers & Functions

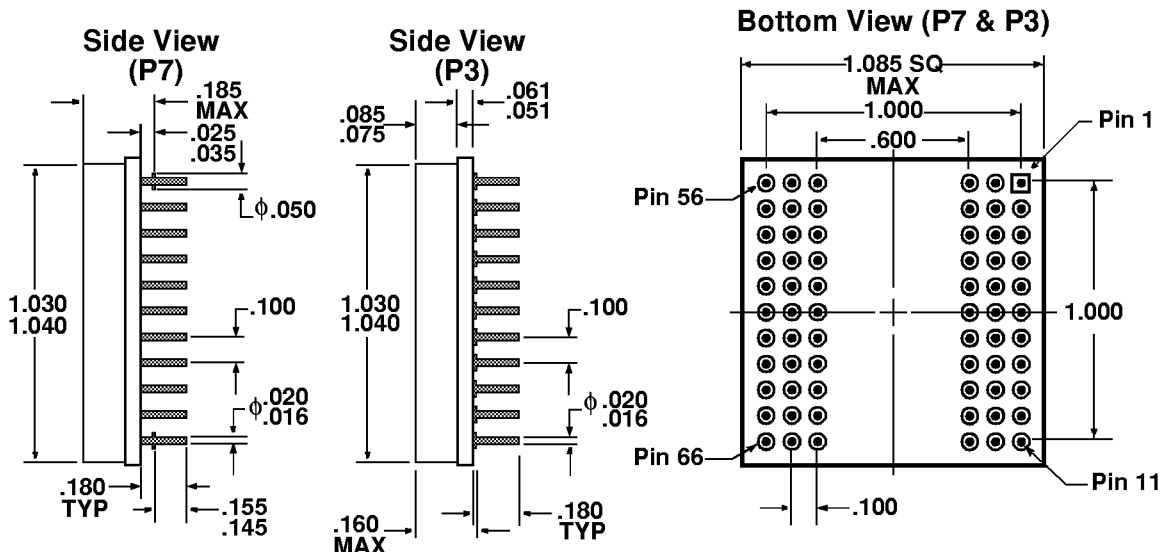
66 Pins — PGA-Type													
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	I/O8	11	I/O2	21	NC	31	I/O6	41	A9	51	A5	61	A1
2	I/O9	12	$\overline{WE}_2$	22	I/O3	32	I/O5	42	I/O16	52	$\overline{WE}_3$	62	A2
3	I/O10	13	$\overline{CE}_2$	23	I/O15	33	I/O4	43	I/O17	53	$\overline{CE}_3$	63	I/O23
4	A13	14	GND	24	I/O14	34	I/O24	44	I/O18	54	GND	64	I/O22
5	A14	15	I/O11	25	I/O13	35	I/O25	45	V <sub>CC</sub>	55	I/O19	65	I/O21
6	A15	16	A10	26	I/O12	36	I/O26	46	$\overline{CE}_4$	56	I/O31	66	I/O20
7	A16	17	A11	27	OE	37	A6	47	$\overline{WE}_4$	57	I/O30		
8	NC	18	A12	28	NC	38	A7	48	I/O27	58	I/O29		
9	I/O0	19	V <sub>CC</sub>	29	$\overline{WE}_1$	39	NC	49	A3	59	I/O28		
10	I/O1	20	$\overline{CE}_1$	30	I/O7	40	A8	50	A4	60	A0		

**Note:** Pins 8, 21, 28, & 39 normally not connected, and can be connected to ground by specifying pinout Option "C".

**"P2" — 1.185" SQ PGA Type Package Standard (with shoulders on Pins 1, 11, 56 & 66)**  
**"P6" — 1.185" SQ PGA Type Special Order Package (without shoulders)**



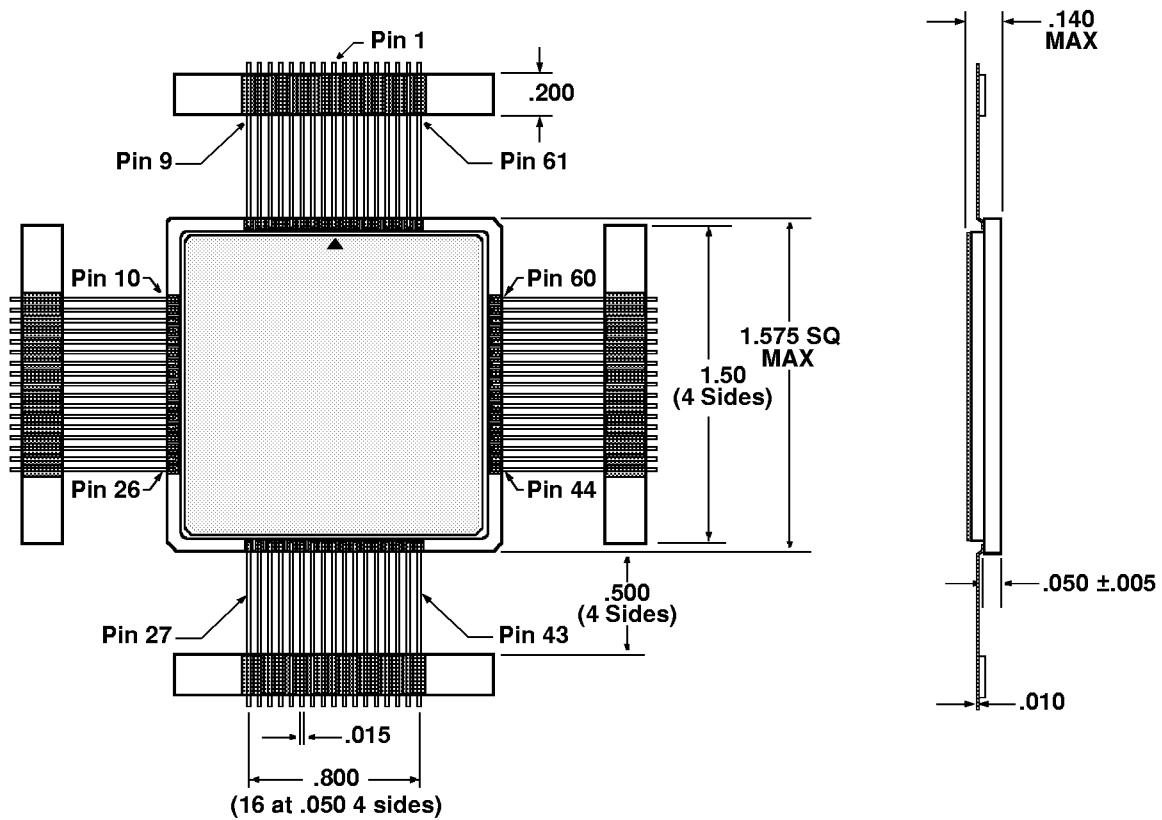
**"P7" — 1.08" SQ PGA Type Package Standard (with shoulders on Pins 1, 11, 56 & 66)**  
**"P3" — 1.08" SQ PGA Type Special Order Package (without shoulders)**



## Pin Numbers & Functions

68 Pins — CQFP							
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	GND	18	GND	35	$\overline{OE}$	52	GND
2	$\overline{CE1}$	19	I/O8	36	$\overline{CE4}$	53	I/O23
3	A5	20	I/O9	37	NC	54	I/O22
4	A4	21	I/O10	38	NC	55	I/O21
5	A3	22	I/O11	39	NC	56	I/O20
6	A2	23	I/O12	40	NC	57	I/O19
7	A1	24	I/O13	41	NC	58	I/O18
8	A0	25	I/O14	42	NC	59	I/O17
9	NC	26	I/O15	43	NC	60	I/O16
10	I/O0	27	V <sub>CC</sub>	44	I/O31	61	V <sub>CC</sub>
11	I/O1	28	A11	45	I/O30	62	A10
12	I/O2	29	A12	46	I/O29	63	A9
13	I/O3	30	A13	47	I/O28	64	A8
14	I/O4	31	A14	48	I/O27	65	A7
15	I/O5	32	A15	49	I/O26	66	A6
16	I/O6	33	A16	50	I/O25	67	$\overline{WE}$
17	I/O7	34	$\overline{CE2}$	51	I/O24	68	$\overline{CE3}$

### Package Outline — CQFP "F1"



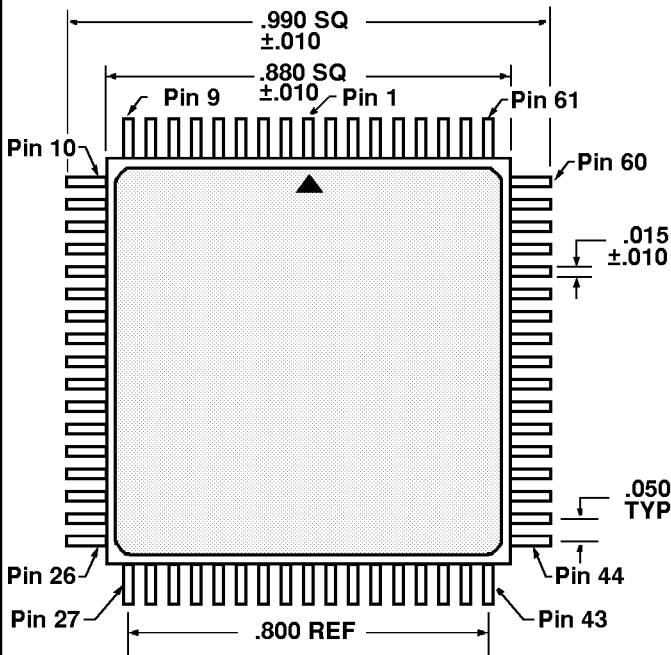
All dimensions in inches

## Pin Numbers & Functions

68 Pins — Dual-Cavity CQFP							
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	GND	18	GND	35	$\overline{OE}$	52	GND
2	$\overline{CE}_3$	19	I/O <sub>8</sub>	36	$\overline{CE}_2$	53	I/O <sub>23</sub>
3	A <sub>5</sub>	20	I/O <sub>9</sub>	37	NC	54	I/O <sub>22</sub>
4	A <sub>4</sub>	21	I/O <sub>10</sub>	38	$\overline{WE}_2$	55	I/O <sub>21</sub>
5	A <sub>3</sub>	22	I/O <sub>11</sub>	39	$\overline{WE}_3$	56	I/O <sub>20</sub>
6	A <sub>2</sub>	23	I/O <sub>12</sub>	40	$\overline{WE}_4$	57	I/O <sub>19</sub>
7	A <sub>1</sub>	24	I/O <sub>13</sub>	41	NC	58	I/O <sub>18</sub>
8	A <sub>0</sub>	25	I/O <sub>14</sub>	42	NC	59	I/O <sub>17</sub>
9	NC	26	I/O <sub>15</sub>	43	NC	60	I/O <sub>16</sub>
10	I/O <sub>0</sub>	27	V <sub>cc</sub>	44	I/O <sub>31</sub>	61	V <sub>cc</sub>
11	I/O <sub>1</sub>	28	A <sub>11</sub>	45	I/O <sub>30</sub>	62	A <sub>10</sub>
12	I/O <sub>2</sub>	29	A <sub>12</sub>	46	I/O <sub>29</sub>	63	A <sub>9</sub>
13	I/O <sub>3</sub>	30	A <sub>13</sub>	47	I/O <sub>28</sub>	64	A <sub>8</sub>
14	I/O <sub>4</sub>	31	A <sub>14</sub>	48	I/O <sub>27</sub>	65	A <sub>7</sub>
15	I/O <sub>5</sub>	32	A <sub>15</sub>	49	I/O <sub>26</sub>	66	A <sub>6</sub>
16	I/O <sub>6</sub>	33	A <sub>16</sub>	50	I/O <sub>25</sub>	67	$\overline{WE}_1$
17	I/O <sub>7</sub>	34	$\overline{CE}_1$	51	I/O <sub>24</sub>	68	$\overline{CE}_4$

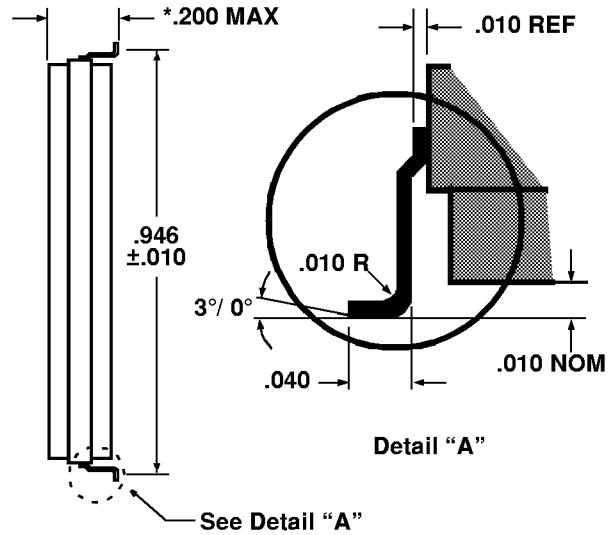
### Package Outline "F2" — Dual-Cavity CQFP

#### Top View



All dimensions in inches

(\* $.180 \text{ MAX}$  available, call factory for details)



Note: Metallic lids and walls – both sides

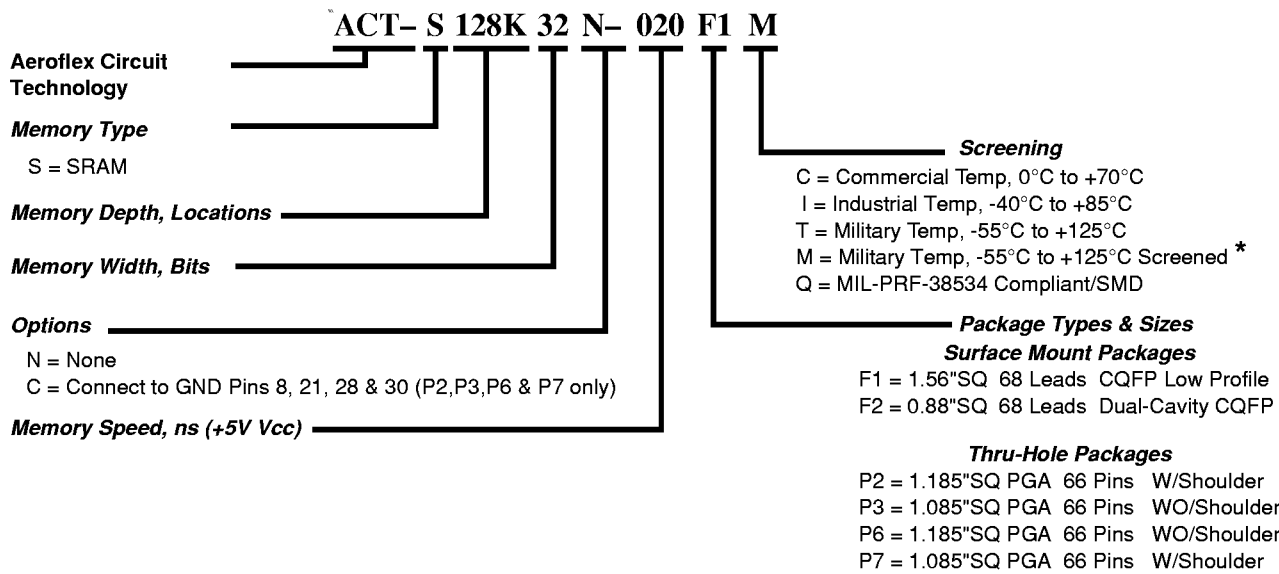
## DESC Ordering Information

Model Number	DESC Part Number	Speed	Package
ACT-S128K32N-017F1Q	5962-9559510HYX	17ns	1.56"sq CQFP
ACT-S128K32N-020F1Q	5962-9559509HYX	20ns	1.56"sq CQFP
ACT-S128K32N-025F1Q	5962-9559508HYX	25ns	1.56"sq CQFP
ACT-S128K32N-035F1Q	5962-9559507HYX	35ns	1.56"sq CQFP
ACT-S128K32N-045F1Q	5962-9559506HYX	45ns	1.56"sq CQFP
ACT-S128K32N-055F1Q	5962-9559505HYX	55ns	1.56"sq CQFP
ACT-S128K32N-017F2Q	5962-9559510HZX	17ns	.88"sq CQFP
ACT-S128K32N-020F2Q	5962-9559509HZX	20ns	.88"sq CQFP
ACT-S128K32N-025F2Q	5962-9559508HZX	25ns	.88"sq CQFP
ACT-S128K32N-035F2Q	5962-9559507HZX	35ns	.88"sq CQFP
ACT-S128K32N-045F2Q	5962-9559506HZX	45ns	.88"sq CQFP
ACT-S128K32N-055F2Q	5962-9559505HZX	55ns	.88"sq CQFP
ACT-S128K32N-017P2Q	5962-9318710HTX	17ns	1.185"sq PGA-Type
ACT-S128K32N-020P2Q	5962-9318709HTX	20ns	1.185"sq PGA-Type
ACT-S128K32N-025P2Q	5962-9318708HTX	25ns	1.185"sq PGA-Type
ACT-S128K32N-035P2Q	5962-9318707HTX	35ns	1.185"sq PGA-Type
ACT-S128K32N-045P2Q	5962-9318706HTX	45ns	1.185"sq PGA-Type
ACT-S128K32N-055P2Q	5962-9318705HTX	55ns	1.185"sq PGA-Type
ACT-S128K32C-017P2Q	5962-9318710HTX	17ns	1.185"sq PGA-Type
ACT-S128K32C-020P2Q	5962-9318709HTX	20ns	1.185"sq PGA-Type
ACT-S128K32C-025P2Q	5962-9318708HTX	25ns	1.185"sq PGA-Type
ACT-S128K32C-035P2Q	5962-9318707HTX	35ns	1.185"sq PGA-Type
ACT-S128K32C-045P2Q	5962-9318706HTX	45ns	1.185"sq PGA-Type
ACT-S128K32C-055P2Q	5962-9318705HTX	55ns	1.185"sq PGA-Type
ACT-S128K32N-017P7Q	5962-9318710H4X	17ns	1.085"sq PGA-Type
ACT-S128K32N-020P7Q	5962-9318709H4X	20ns	1.085"sq PGA-Type
ACT-S128K32N-025P7Q	5962-9318708H4X	25ns	1.085"sq PGA-Type
ACT-S128K32N-035P7Q	5962-9318707H4X	35ns	1.085"sq PGA-Type
ACT-S128K32N-045P7Q	5962-9318706H4X	45ns	1.085"sq PGA-Type
ACT-S128K32N-055P7Q	5962-9318705H4X	55ns	1.085"sq PGA-Type
ACT-S128K32C-017P7Q	5962-9318710H5X	17ns	1.085"sq PGA-Type
ACT-S128K32C-020P7Q	5962-9318709H5X	20ns	1.085"sq PGA-Type
ACT-S128K32C-025P7Q	5962-9318708H5X	25ns	1.085"sq PGA-Type
ACT-S128K32C-035P7Q	5962-9318707H5X	35ns	1.085"sq PGA-Type
ACT-S128K32C-045P7Q	5962-9318706H5X	45ns	1.085"sq PGA-Type
ACT-S128K32C-055P7Q	5962-9318705H5X	55ns	1.085"sq PGA-Type





## Part Number Breakdown



\* Screened to the individual test methods of MIL-STD-883

Specifications subject to change without notice

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