ANALOG DEVICES

DSP Microcomputer

ADSP-2105

FEATURES

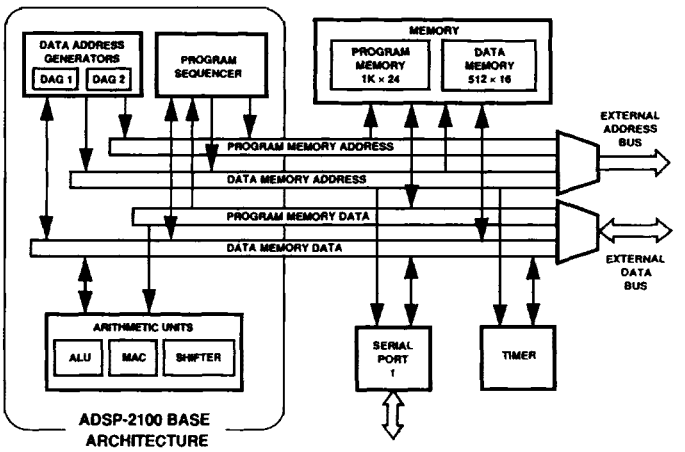
Complete DSP Microcomputer
100 ns Instruction Cycle Time from 10 MHz Crystal
ADSP-2100 Code- & Function-Compatible
ADSP-2101 Pin-Compatible
1K Words of On-Chip Program Memory RAM
512 Words of On-Chip Data Memory RAM
Dual Purpose Program Memory for Both Instruction and Data Storage
Separate Program and Data Buses On-Chip
Three Computation Units: ALU, Multiplier/ Accumulator and Barrel Shifter
Two Independent Data Address Generators
Powerful Program Sequencer
Zero Overhead Looping
Conditional Arithmetic Instruction Execution
Double-Buffered Serial Port with Companding Hardware and Automatic Data Buffering
Programmable 16-Bit Interval Timer with Prescaler
Programmable Wait State Generation
Automatic Boot of Internal Program Memory from Byte-Wide External Memory, e.g., EPROM
Provisions for Multiprecision Computation and Saturation Logic
Single-Cycle Instruction Execution
Single-Cycle Context Switch
Multifunction Instructions
Three Edge- or Level-Sensitive External Interrupts
80 mW Maximum Power Dissipation in Standby Mode
68-Lead PLCC

GENERAL DESCRIPTION

The ADSP-2105 is a single-chip microcomputer optimized for digital signal processing (DSP) and other high-speed numeric processing applications. Its instruction set is a fully compatible superset of the ADSP-2100 instruction set. It combines the complete ADSP-2100 architecture (three computational units, data address generators and a program sequencer) with a serial port, a programmable timer, extensive interrupt capabilities and on-chip program and data memory RAM. The ADSP-2105 has 512 words of (16-bit) data memory RAM and 1K words of (24-bit) program memory RAM on chip.

The ADSP-2105 is an architectural subset of Analog Devices' ADSP-2101. It is pin-for-pin and code compatible with the ADSP-2101. The ADSP-2105 is the industry's leading cost/ performance DSP. It is an ideal choice in applications needing the performance advantages of a DSP processor at the cost of today's standard microcontrollers.

FUNCTIONAL BLOCK DIAGRAM



The ADSP-2105 offers a direct upgrade path to more highly integrated and higher performance DSP processors such as the ADSP-2101 and ADSP-2111. Designers selecting the ADSP-2105 will be able to preserve their investment in ADSP-21XX development tools in future programs requiring the added features found on the ADSP-2101 and other members of the ADSP-2100 family.

The ADSP-2105 is feature- and instruction-set compatible with the ADSP-2101. The only differences are the sizes of on-chip memories (half the size of the ADSP-2101's), the number of serial ports (one instead of two) and processor speed. The ADSP-2105 serial port (SPORT) is identical to SPORT1 of the ADSP-2101. The specifics of these differences are documented on page 22 of this data sheet.

Fabricated in a high-speed double-layer metal CMOS process, the ADSP-2105 operates with a 100 ns instruction cycle time. Every instruction executes in a single cycle. Fabrication in CMOS results in low power dissipation. The ADSP-2105 dissipates less than 1 W under all conditions and no more than 80 mW under standby conditions.

The ADSP-2105's flexible architecture and comprehensive instruction set support a high degree of operational parallelism. In one cycle the ADSP-2105 can:

- generate the next program address
- fetch the next instruction
- perform one or two data moves
- update one or two data address pointers
- perform a computational operation
- receive or transmit data via the serial port

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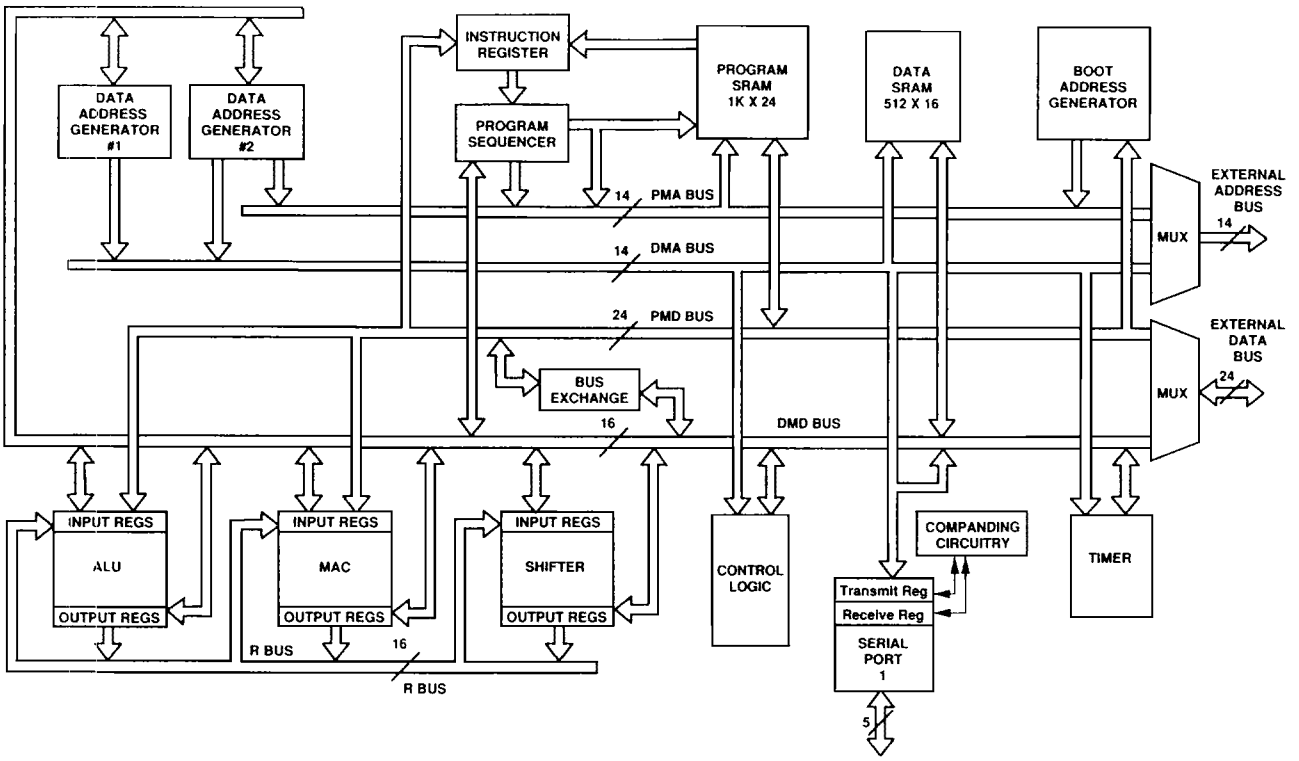

Figure 1. ADSP-2105 Block Diagram

Development System

The ADSP-2105 is supported by a complete set of tools for software and hardware system development. The development software is a set of modules that supports all the ADSP-2100 family processors. The System Builder provides a high-level method for defining the architecture of systems under development. The Assembler produces object code and the Linker combines object modules and library calls into an executable file. The Simulator provides an interactive instruction-level simulation with a reconfigurable user interface. A PROM Splitter generates PROM burner compatible files. The C Compiler generates ADSP-21XX assembly source code.

ADSP-2101 emulators aid in the hardware debugging of ADSP-2105 systems. The full-featured emulator performs a full range of emulation functions including trace and triggering. EZ-Tools are low cost, easy-to-use hardware tools. The EZ-ICE® emulator provides basic functions like changing register values and setting breakpoints. The EZ-LAB® demonstration board is a complete ADSP-2101-based system that executes its own example programs. The EZ-Kit package is a starter kit that contains an EZ-LAB board, development software, books and example programs.

Additional Information

Because the ADSP-2105 is an architectural subset of the ADSP-2101, the same documentation and development tools support both devices.

For additional information on the architecture and instruction set of the processor, refer to the *ADSP-2100 Family User's Manual*. For more information about the Development System and programmer's reference information, refer to the *ADSP-2100 Family Development Software Manuals* and the *ADSP-2101 Emulator Manual*.

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ARCHITECTURE OVERVIEW

Figure 1 is an overall block diagram of the ADSP-2105.

The processor contains three independent computational units: the ALU, the multiplier/accumulator (MAC) and the shifter. The computational units process 16-bit data directly and have provisions to support multiprecision computations. The ALU performs a standard set of arithmetic and logic operations; division primitives are also supported. The MAC performs single-cycle multiply, multiply/add and multiply/subtract operations. The shifter performs logical and arithmetic shifts, normalization, denormalization, and derive exponent operations. The shifter can be used to efficiently implement numeric format control including multiword floating-point representations.

The internal result (R) bus directly connects the computational units so that the output of any unit may be the input of any unit on the next cycle.

A powerful program sequencer and two dedicated data address generators ensure efficient use of these computational units. The sequencer supports conditional jumps, subroutine calls and returns in a single cycle. With internal loop counters and loop stacks, the ADSP-2105 executes looped code with zero overhead; no explicit jump instructions are required to maintain the loop.

The data address generators (DAGs) handle address pointer updates. Each DAG maintains four address pointers. Whenever the pointer is used to access data (indirect addressing), it is post-modified by the value of a specified modify register. A length value may be associated with each pointer to implement automatic modulo addressing for circular buffers. With two independent DAGs, the processor can generate two data addresses simultaneously for dual operand fetches. The circular buffering feature is also used by the serial port for automatic data transfers.

Efficient data transfer is achieved with the use of five internal buses.

- Program Memory Address (PMA) Bus
- Program Memory Data (PMD) Bus
- Data Memory Address (DMA) Bus
- Data Memory Data (DMD) Bus
- Result (R) Bus

The two address buses (PMA and DMA) share a single external address bus, and the two data buses (PMD and DMD) share a single external data bus. The $\overline{BMS}$, $\overline{DMS}$ and $\overline{PMS}$ signals indicate which memory space the external buses are being used for.

Program memory can store both instructions and data, permitting the ADSP-2105 to fetch two operands in a single cycle, one from program memory and one from data memory. The ADSP-2105 can fetch an operand from on-board program memory and the next instruction in the same cycle.

The memory interface supports slow memories and memory-mapped peripherals with programmable wait state generation. External devices can gain control of buses with bus request/grant signals ($\overline{BR}$ and $\overline{BG}$). One execution mode allows the ADSP-2105 to continue running from internal memory. A second execution mode requires the processor to halt while buses are granted.

The ADSP-2105 can respond to up to three external interrupts, configured as edge or level sensitive. Internal interrupts can be generated by the timer and the serial port (SPORT1). There is also a master $\overline{RESET}$ signal.

The serial port provides a complete synchronous serial interface with optional companding in hardware and a wide variety of framed and frameless data transmit and receive modes of operation. The port can generate an internal programmable serial clock or accept an external serial clock. Note that this serial port (SPORT1) does not have the multichannel capability of the ADSP-2101's (and ADSP-2111's) SPORT0.

Boot circuitry provides for loading on-chip program memory automatically from byte-wide external memory. After $\overline{RESET}$ three wait states are automatically generated. This allows, for example, a 100 ns ADSP-2105 to use an external 250 ns EPROM as boot memory. Multiple programs can be selected and loaded from the EPROM with no additional hardware.

A programmable interval timer can generate periodic interrupts. A 16-bit count register (TCOUNT) is decremented every *n* cycles, where *n–1* is a scaling value stored in an 8-bit register (TSCALE). When the value of the count register reaches zero, an interrupt is generated and the count register is reloaded from a 16-bit period register (TPERIOD).

The ADSP-2105 instruction set provides flexible data moves and multifunction (one or two data moves with a computation) instructions. Every instruction can be executed in a single processor cycle. The ADSP-2105 assembly language uses an algebraic syntax for ease of coding and readability. A comprehensive set of development tools supports program development.

Pin Description

The ADSP-2105 is available in a 68-lead PLCC.

Table I. ADSP-2105 Pin List

Pin Group Name	# of Pins	Function
Address	14	Address Output for Program, Data and Boot Memory Spaces.
Data	24	Data I/O pins for program and data memories. Input only for Boot memory space, with two MSBs used for Boot space addresses.
$\overline{RESET}$	1	Processor Reset Input.
$\overline{IRQ2}$	1	External Interrupt Request #2 Input.
$\overline{BR}$	1	External Bus Request Input.
$\overline{BG}$	1	External Bus Grant Output.
$\overline{PMS}$	1	External Program Memory Select.
$\overline{DMS}$	1	External Data Memory Select.
$\overline{BMS}$	1	Boot Memory Select.
$\overline{RD}$	1	External Memory Read Enable Output.
$\overline{WR}$	1	External Memory Write Enable Output.
MMAP	1	Memory Map Select.
CLKIN, XTAL	2	External Clock or Quartz Crystal Input.
CLKOUT	1	Processor Clock Output.
SPORT1 or Flags and Interrupts		
TFS1/$\overline{IRQ1}$	1	Transmit Frame Sync/External Interrupt Request #1 Input.
RFS1/$\overline{IRQ0}$	1	Receive Frame Sync/External Interrupt Request #0 Input.
SCLK1	1	Programmable Clock.
DT1/FO	1	Data Transmit/Flag Output.
DR1/FI	1	Data Receive/Flag Input.
GND	4	Ground Pins.
V_{DD}	3	Power Supply.
N/C	5	No Connect.

Serial Port

The ADSP-2105 incorporates a complete synchronous serial port (SPORT1) for serial communications and multiprocessor communication.

The serial port has a 5-pin interface consisting of the following signals. This port is identical to SPORT1 on the ADSP-2101.

Signal Name	Function
SCLK1	Serial Clock I/O
RFS1	Receive Frame Sync I/O
TFS1	Transmit Frame Sync I/O
DR1	Serial Data Receive
DT1	Serial Data Transmit

Here is a brief list of the capabilities of the ADSP-2105 SPORT:

- Bidirectional: the SPORT has separate transmit and receive sections.
- Double-buffered: each SPORT section (both receive and transmit) has a data register accessible to the user and an internal transfer register. The double-buffering provides additional time to service the SPORT.
- Flexible clocking: the SPORT can use an external serial clock (from 0 Hz to the processor frequency) or generate its own (up to 1/2 the processor frequency).
- Flexible framing: framings for the receive and transmit sections are independent. Each section can run in a frameless mode, with internally generated or externally generated frame synchronization signals, with active high or inverted frame signals, with either of two pulse widths/timings. The receive and transmit sections share the same serial clock.
- Flexible word length: the SPORT supports serial data word lengths from three to sixteen bits.
- Companding in hardware: the SPORT provides optional A-law and μ-law companding according to CCITT recommendation G.711.
- Flexible interrupt scheme: each SPORT section (receive and transmit) can generate a unique interrupt upon completing a data word transfer or after transferring an entire buffer (see next item).
- Auto-buffering with single-cycle overhead: using the ADSP-2105 DAGs, the SPORT can receive and/or transmit an entire circular buffer of data with an overhead of only one cycle per data word. Transfers to and from the SPORT and the circular buffer are automatic in this mode and do not require additional programming. An interrupt is generated only when the receive buffer is full or the transmit buffer is empty.
- Alternate configuration: the SPORT can be configured as two external interrupt inputs ($\overline{IRQ0}$ and $\overline{IRQ1}$) and the Flag In and Flag Out signals. The internally generated serial clock may still be used in this configuration.

Note that this serial port (SPORT1) does not offer the multichannel feature of the ADSP-2101's (and ADSP-2111's) SPORT0.

Interrupts

The interrupt controller works the same way as that of the ADSP-2101. Because the ADSP-2105 has one serial port instead of two, there are four interrupts rather than six. The processor responds to the four possible interrupts with a minimum of overhead. The ADSP-2105 provides up to three external interrupt input pins, $\overline{IRQ0}$, $\overline{IRQ1}$ and $\overline{IRQ2}$. $\overline{IRQ2}$ is always available as a dedicated pin; $\overline{IRQ1}$ and $\overline{IRQ0}$ may be alternately configured as part of the serial port. The ADSP-2105 also supports internal interrupts from the timer and the serial port. The interrupt levels are internally prioritized and individually maskable. The input pins can be programmed to be either level- or edge-sensitive. The priorities of the interrupts are shown in Table II.

Table II. Interrupt Priority & Interrupt Vector Addresses

Source of Interrupt	Interrupt Vector Address
$\overline{IRQ2}$ (external pin)	0004 (*highest priority*)
SPORT1 Transmit (internal) or $\overline{IRQ1}$ (external)	0010
SPORT1 Receive (internal) or $\overline{IRQ0}$ (external)	0014
Timer (internal)	0018 (*lowest priority*)

The ADSP-2105 supports a vectored interrupt scheme: when an interrupt is acknowledged, the processor shifts program control to the interrupt vector address corresponding to the interrupt level. Interrupts can optionally be nested so that a higher priority interrupt can preempt the currently executing interrupt service routine. Each interrupt vector location is four instructions in length, so that simple service routines can be coded entirely in this space. Longer routines require an additional JUMP or CALL instruction.

Individual interrupt requests are logically ANDed with the bits in IMASK; the highest priority unmasked interrupt is then selected.

The interrupt control register, ICNTL, allows the external interrupts to be set as either edge- or level-sensitive. Depending on Bit 4 in ICNTL, interrupt routines can either be nested with higher priority interrupts taking precedence or processed sequentially with only one interrupt service active at a time.

The 12-bit interrupt force and clear register, IFC, is a write-only register that contains a force bit and a clear bit for each of the four interrupts.

When responding to an interrupt, the status registers ASTAT, MSTAT, IMASK are pushed onto the status stack and the PC counter is loaded with the appropriate vector address. The status stack is seven levels deep to allow interrupt nesting. The stack is automatically popped when a return from the interrupt is executed.

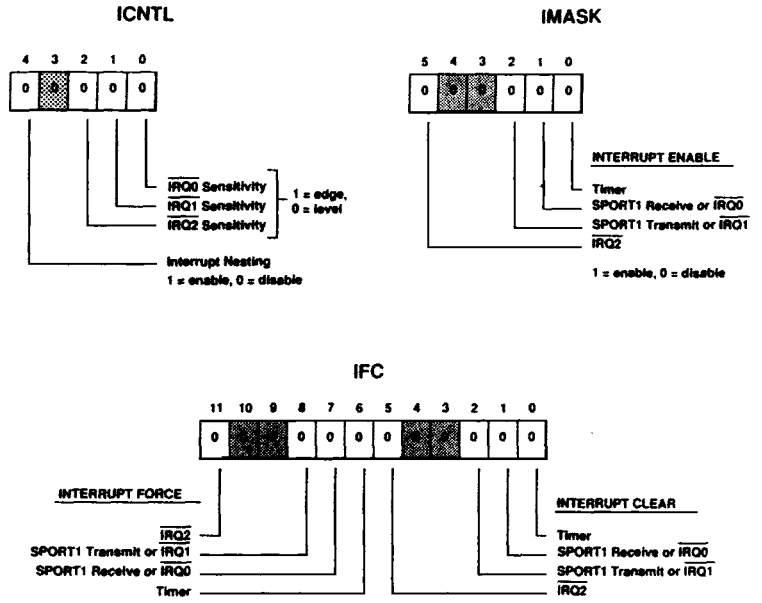
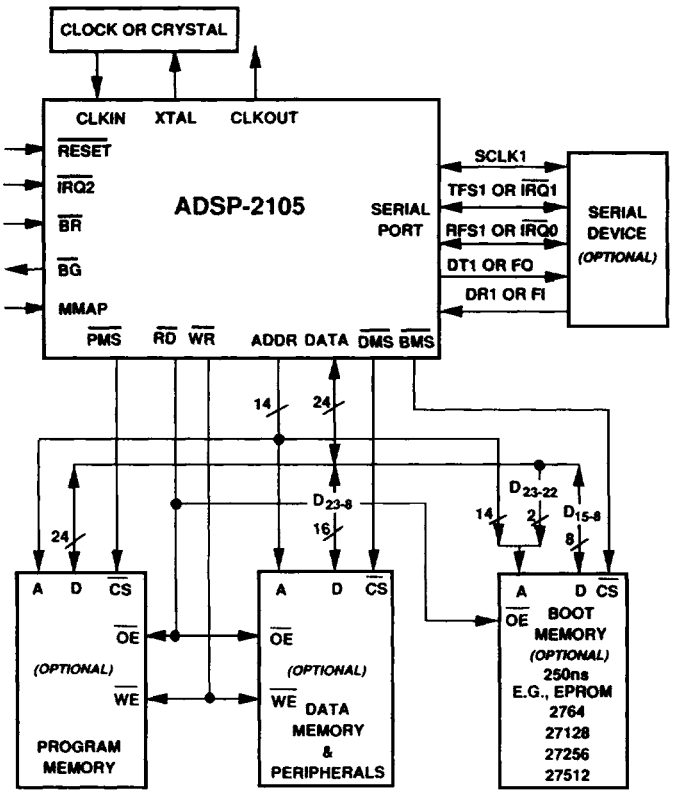


Figure 2. Interrupt Registers



NOTE: THE TWO MSBs OF THE BOOT EPROM ADDRESS ARE ALSO THE TWO MSBs OF THE DATA BUS. THIS IS ONLY REQUIRED FOR THE 27256 AND 27512.

Figure 3. ADSP-2105 Basic System Configuration

SYSTEM INTERFACE

Figure 3 shows a typical system configuration with the ADSP-2105, a serial codec, a boot EPROM and optional external program and data memories. This configuration allows an easy upgrade to the ADSP-2101. Up to 14.5K words of data memory and 15K words of program memory can be supported. Programmable wait state generation allows the processor to interface easily to slow memories.

The ADSP-2105 also provides one external interrupt and a serial port or three external interrupts.

Clock Signals

The ADSP-2105 may be clocked by either a crystal or a TTL-compatible clock signal.

The CLKIN input may not be halted, changed during operation, or operated below the specified frequency.

If an external clock is used, it should be a TTL-compatible signal running at the instruction rate. The signal is connected to the processors's CLKIN input. When an external clock is used, the XTAL input *must* be left unconnected.

Because the ADSP-2105 includes an on-chip oscillator circuit, an external crystal may be used. The crystal should be connected across the CLKIN and XTAL pins, with two capacitors connected as shown in Figure 2. A parallel-resonant, fundamental frequency microprocessor grade crystal should be used.

A clock output (CLKOUT) signal is generated by the processor, synchronized to the processor's internal cycles.

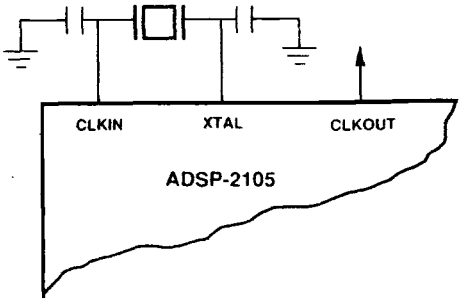


Figure 4. External Crystal Connections

Bus Interface

The ADSP-2105 can relinquish control of the data and address buses to an external device. When the external device requires access to memory, it asserts the bus request ($\overline{BR}$) signal. If the ADSP-2105 is not performing an external memory access, then it responds to the active $\overline{BR}$ input in the same cycle by:

- tristating the data and address buses and the $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ output drivers,
- asserting the bus grant ($\overline{BG}$) signal, and
- halting program execution.

If the Go mode is set, however, the ADSP-2105 will not halt program execution until it encounters an instruction that requires an external memory access.

If the ADSP-2105 is performing an external memory access when the external device asserts the $\overline{BR}$ signal, then it will not tristate the memory interfaces or assert the $\overline{BG}$ signal until the cycle after the access completes, up to eight cycles later depending on the number of wait states. The instruction does not need to be completed when the bus is granted; the ADSP-2105 will grant the bus in between two memory accesses if an instruction requires more than one external memory access.

When the $\overline{BR}$ signal is released, the processor releases the $\overline{BG}$ signal, re-enables the output drivers and continues program execution from the point where it stopped.

The bus request feature operates at all times, including when the processor is booting and when $\overline{RESET}$ is active.

Program Memory Interface

The on-chip program memory address bus (PMA) and the on-chip program memory data bus (PMD) are multiplexed with on-chip DMA and DMD buses, creating a single external data bus and a single external address bus. The 14-bit address bus directly addresses up to 15K words, of which 1K are on-chip. The data bus is bidirectional and 24 bits wide to external program memory. Program memory may contain code and data.

The program memory data lines are bidirectional. The Program Memory Select ($\overline{PMS}$) signal indicates access to the Program Memory and can be used as a chip select signal. The Write ($\overline{WR}$) signal indicates a write operation and is used as a write strobe. The Read ($\overline{RD}$) signal indicates a read operation and is used as a read strobe or output enable signal.

The ADSP-2105 writes data from its 16-bit registers to the 24-bit program memory using the PX register to provide the lower eight bits. When it reads data (not instructions) from 24-bit program memory to a 16-bit data register, the lower eight bits are placed in the PX register.

Program Memory Maps

Program memory can be mapped in two ways, depending on the state of the MMAP pin. Figure 5 shows the two configurations. When MMAP = 0, internal RAM occupies 1K words beginning at address 0000; external program memory uses the 14K words beginning at address H#0800. In this configuration, the boot loading sequence (described below) is automatically initiated when $\overline{RESET}$ is released.

When MMAP = 1, 14K words of external program memory begin at address 0000 and internal RAM is located in 1K words at addresses H#3800 to H#3BFF. In this configuration, program memory is not loaded although it can be written to and read from under program control.

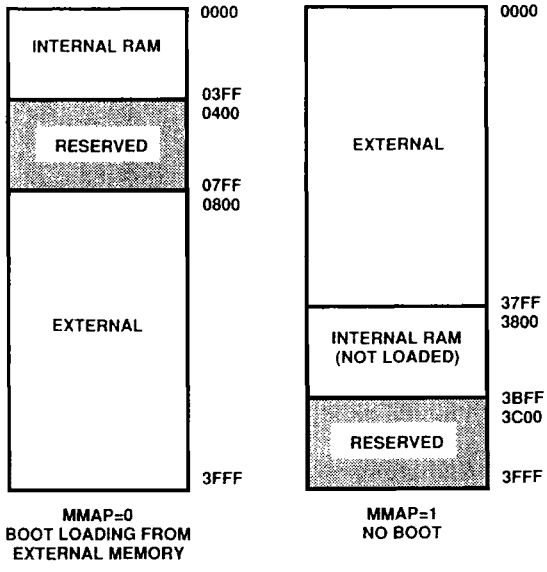


Figure 5. ADSP-2105 Program Memory Maps

The program memory interface can generate 0 to 7 wait states for external memory devices; default is to 7 wait states after $\overline{RESET}$.

Data Memory Interface

The data memory address (DMA) bus is 14 bits wide. The bidirectional external data bus is 24 bits wide, with the upper 16 bits used for data memory data (DMD) transfers.

The Data Memory Select ($\overline{DMS}$) signal indicates access to the Data Memory and can be used as a chip select signal. The Write ($\overline{WR}$) signal indicates a write operation and can be used as a write strobe. The Read ($\overline{RD}$) signal indicates a read operation and can be used as a read strobe or output enable signal.

The ADSP-2105 supports memory-mapped I/O, with the peripherals memory mapped into the data memory address space and accessed by the processor in the same manner as data memory.

Data Memory Map

The on-chip data memory RAM resides in the 512 words of data memory beginning at address H#3800, as shown in Figure 6. In addition, data memory locations from H#3A00 to the end of

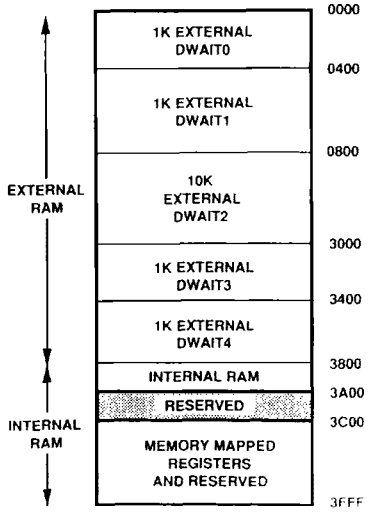


Figure 6. ADSP-2105 Data Memory Map

data memory at H#3FFF are reserved. Control registers for the system, timer, wait state configuration and serial port operations are located in this region of memory.

The remaining 14K of data memory is external. External data memory is divided into five zones each associated with its own wait state generator. This allows slower peripherals to be memory mapped into data memory for which wait states are specified. By mapping peripherals into different zones, you can accommodate peripherals with different wait state requirements. All zones default to 7 wait states after $\overline{\text{RESET}}$.

Boot Memory Interface

The Boot memory space consists of an external 32K by 8 space, divided into eight separate 4K by 8 pages. Three bits in the system control register select which page is loaded by the Boot memory interface. Another bit in the system control register allows the user to force a boot loading sequence under software control. Boot loading from page 0 after $\overline{\text{RESET}}$ is initiated automatically if MMAP = 0.

The boot memory interface can generate 0 to 7 wait states; it defaults to 3 wait states after $\overline{\text{RESET}}$. This allows an ADSP-2105 running with a 100 ns instruction cycle to use a slow, low-cost EPROM for program storage. Program memory is loaded a byte at a time and converted to 24-bit words.

The $\overline{\text{BMS}}$ and $\overline{\text{RD}}$ signals are used to select and strobe the boot memory interface. Only 8-bit data is read over the data bus, on pins D8–D15. To accommodate up to eight pages of boot memory, the two MSBs of the data bus are used in the boot memory interface as the two MSBs of the boot space address.

$\overline{\text{BR}}$ is recognized during the booting sequence. The bus is granted after the completion of loading the current byte. $\overline{\text{BR}}$ during booting may be used to implement booting under the control of a host processor.

RESET

The $\overline{\text{RESET}}$ signal initiates a master reset of the ADSP-2105. The $\overline{\text{RESET}}$ signal must be asserted when the chip is powered up to assure proper initialization. $\overline{\text{RESET}}$ during initial power-up must be held long enough to allow the internal clock to stabilize. If $\overline{\text{RESET}}$ is activated at any time after power-up, the clock continues and does not require this stabilization time.

The power-up sequence is defined as the total time required for the crystal oscillator circuit to stabilize after a valid V_{DD} is applied to the processor and for the internal phase-locked loop (PLL) to lock onto the specific crystal frequency. A minimum of 1000 t_{CK} cycles will ensure that the PLL has locked but does not include the crystal oscillator start-up time. During this power-up sequence the $\overline{\text{RESET}}$ signal should be held low. On any subsequent resets, the $\overline{\text{RESET}}$ signal must meet the minimum pulse width specification, t_{RSP}.

The $\overline{\text{RESET}}$ input contains some hysteresis; however, if you use an RC circuit to generate your $\overline{\text{RESET}}$ signal, the use of an external Schmidt trigger is recommended.

The master reset sets all internal stack pointers to the empty stack condition, masks all interrupts and clears the MSTAT register. When $\overline{\text{RESET}}$ is released, if there is no pending bus request and the chip is configured for booting (MMAP = 0), the boot-loading sequence is performed. Then the first instruction is fetched from internal program memory location 0x0000.

ADSP-2105 REGISTERS

Figure 7 summarizes all the registers in the ADSP-2105. Some registers store values. For example, AX0 stores an ALU operand; I4 stores a DAG2 pointer. Other registers consist of control bits and fields, or status flags. For example, ASTAT contains status flags from arithmetic operations, and fields in DWAIT control the numbers of wait states for different zones of data memory.

The bit and field definitions for control and status registers are given in the rest of this section, except for IMASK, ICNTL and IFC, which are defined earlier in this data sheet. The system control register, DWAIT regis r control registers are all mapped i access these registers by readi a tions rather than register name address is shown with each m

Register bit values shown on th bit values after reset. If no val s terminate at reset. Reserved bit should always be written with zer

A secondary set of registers in all single-cycle context switch.

Data memory locations 0x3FF

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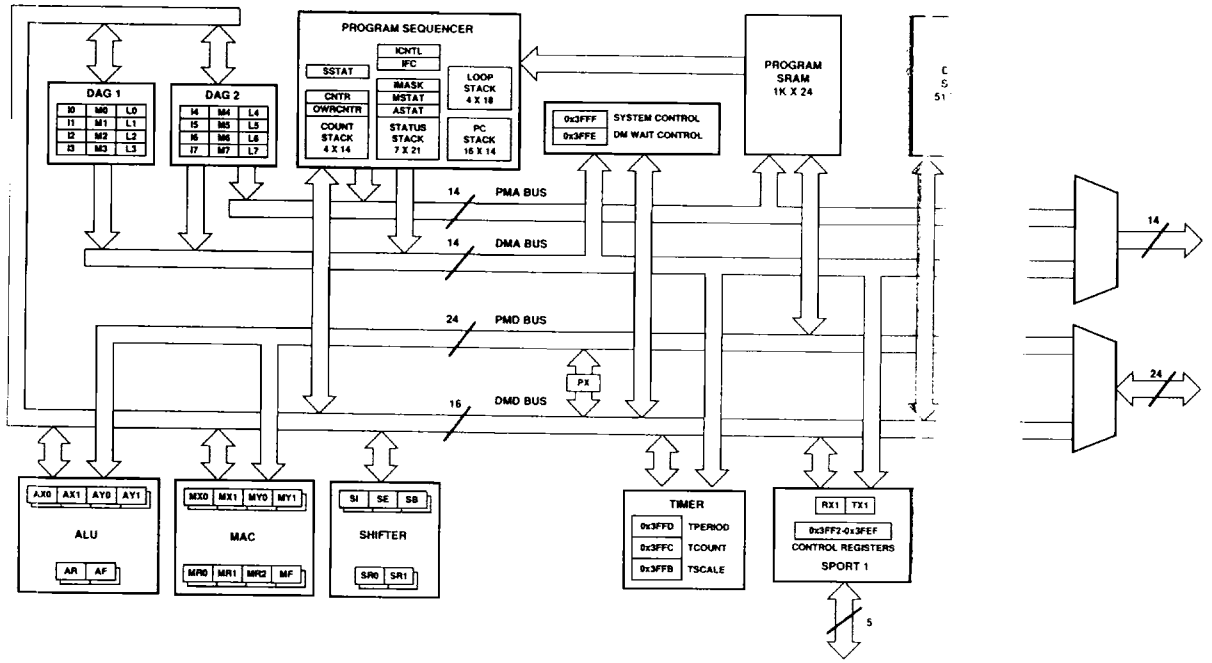
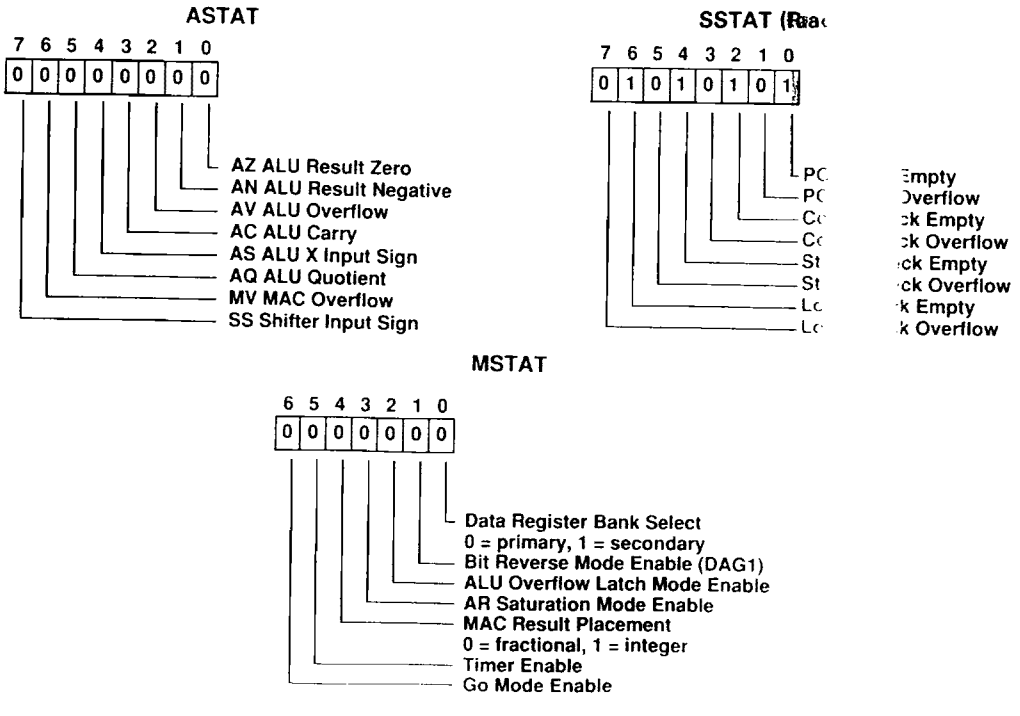


Figure 7. ADSP-2105 Registers



INSTRUCTION SET DESCRIPTION

The ADSP-21xx assembly language uses an algebraic syntax for ease of coding and readability. The sources and destinations of computations and data movements are written explicitly in each assembly statement, eliminating cryptic assembler mnemonics. Every instruction assembles into a single 24-bit word and executes in a single cycle. The instructions encompass a wide variety of instruction types along with a high degree of operational parallelism. There are five basic categories of instructions: data move instructions, computational instructions, multifunction instructions, program flow control instructions and miscellaneous instructions. Each of these instruction types is described briefly. The complete instruction set is summarized at the end of this section. The *ADSP-2100 Family User's Manual* contains a complete reference to the instruction set.

ADSP-2100 Family Compatibility

The ADSP-2105 instruction set is a superset of the ADSP-2100 instruction set. The ADSP-2105 is source and object code compatible with the ADSP-2100 microprocessor and ADSP-2101 and ADSP-2111 microcomputers. An ADSP-2100 program may need to be relocated to utilize internal memory and conform to the ADSP-2105's interrupt vector and reset vector map. An ADSP-2105 program executes on the ADSP-2101 without modification.

Like the ADSP-2101, the ADSP-2105 does not support the ADSP-2100 TRAP instruction since the ADSP-2105 does not have the TRAP/$\overline{\text{HALT}}$ signals. The TRAP instruction executes as a NOP on the ADSP-2105.

Condition Codes

The condition codes are used to determine whether a conditional instruction, such as a jump, trap, call, return, MAC saturation, or arithmetic operation, is performed. The sixteen basic composite status conditions and their derivations are shown in Table III. Since arithmetic status is latched into ASTAT at the end of a processor cycle, the condition logic represents conditions generated on the previous cycle.

Table III. Condition Codes

Code	Status Condition	True If:
EQ	ALU Equal Zero	AZ = 1
NE	ALU Not Equal Zero	AZ = 0
LT	ALU Less Than Zero	AN .XOR. AV = 1
GE	ALU Greater Than or Equal Zero	AN .XOR. AV = 0
LE	ALU Less Than or Equal Zero	(AN .XOR. AV) .OR. AZ = 1
GT	ALU Greater Than Zero	(AN .XOR. AV) .OR. AZ = 0
AC	ALU Carry	AC = 1
NOT AC	Not ALU Carry	AC = 0
AV	ALU Overflow	AV = 1
NOT AV	Not ALU Overflow	AV = 0
MV	MAC Overflow	MV = 1
NOT MV	Not MAC Overflow	MV = 0
NEG	ALU X Input Sign Negative	AS = 1
POS	ALU X Input Sign Positive	AS = 0
NOT CE	Not Counter Expired	CE = 0
FOREVER	Always	Always True

In addition to the basic sixteen conditions, the JUMP and CALL instructions also support the use of the FI (Flag In) pin as a conditional flag. This pin is one of the five dual-function pins used for the serial port. The state of this pin and its complement are available as conditions for JUMP and CALL instructions if the pin is configured as FI rather than DR1.

Table IV. Additional Condition Codes For JUMP and CALL

FLAG_IN	FI pin last sampled 1
NOT FLAG_IN	FI pin last sampled 0

Example Code

The following example is a code fragment that performs the filter tap update for an adaptive (least-mean-squared algorithm) filter. Notice that the computations in the instructions are written like algebraic equations.

```
        MF = MX0*MY1 (RND), MX0 = DM (I2,M1) ; {MF = error*beta}
        MR = MX0*MF (RND), AY0 = PM (I6,M5) ;
        DO adapt UNTIL CE;
          AR = MR1 + AY0, MX0 = DM (I2,M1), AY0 = PM (I6,M7) ;
adapt:    PM(I6,M6) = AR, MR = MX0*MF (RND) ;
        MODIFY (I2, M3) ;                    {Point to oldest data}
        MODIFY (I6, M7) ;                    {Point to start of data}
```

INSTRUCTION SET DESCRIPTION

The ADSP-21xx assembly language uses an algebraic syntax for ease of coding and readability. The sources and destinations of computations and data movements are written explicitly in each assembly statement, eliminating cryptic assembler mnemonics. Every instruction assembles into a single 24-bit word and executes in a single cycle. The instructions encompass a wide variety of instruction types along with a high degree of operational parallelism. There are five basic categories of instructions: data move instructions, computational instructions, multifunction instructions, program flow control instructions and miscellaneous instructions. Each of these instruction types is described briefly. The complete instruction set is summarized at the end of this section. The *ADSP-2100 Family User's Manual* contains a complete reference to the instruction set.

ADSP-2100 Family Compatibility

The ADSP-2105 instruction set is a superset of the ADSP-2100 instruction set. The ADSP-2105 is source and object code compatible with the ADSP-2100 microprocessor and ADSP-2101 and ADSP-2111 microcomputers. An ADSP-2100 program may need to be relocated to utilize internal memory and conform to the ADSP-2105's interrupt vector and reset vector map. An ADSP-2105 program executes on the ADSP-2101 without modification.

Like the ADSP-2101, the ADSP-2105 does not support the ADSP-2100 TRAP instruction since the ADSP-2105 does not have the TRAP/$\overline{\text{HALT}}$ signals. The TRAP instruction executes as a NOP on the ADSP-2105.

Condition Codes

The condition codes are used to determine whether a conditional instruction, such as a jump, trap, call, return, MAC saturation, or arithmetic operation, is performed. The sixteen basic composite status conditions and their derivations are shown in Table III. Since arithmetic status is latched into ASTAT at the end of a processor cycle, the condition logic represents conditions generated on the previous cycle.

Table III. Condition Codes

Code	Status Condition	True If:
EQ	ALU Equal Zero	AZ = 1
NE	ALU Not Equal Zero	AZ = 0
LT	ALU Less Than Zero	AN .XOR. AV = 1
GE	ALU Greater Than or Equal Zero	AN .XOR. AV = 0
LE	ALU Less Than or Equal Zero	(AN .XOR. AV) .OR. AZ = 1
GT	ALU Greater Than Zero	(AN .XOR. AV) .OR. AZ = 0
AC	ALU Carry	AC = 1
NOT AC	Not ALU Carry	AC = 0
AV	ALU Overflow	AV = 1
NOT AV	Not ALU Overflow	AV = 0
MV	MAC Overflow	MV = 1
NOT MV	Not MAC Overflow	MV = 0
NEG	ALU X Input Sign Negative	AS = 1
POS	ALU X Input Sign Positive	AS = 0
NOT CE	Not Counter Expired	CE = 0
FOREVER	Always	Always True

In addition to the basic sixteen conditions, the JUMP and CALL instructions also support the use of the FI (Flag In) pin as a conditional flag. This pin is one of the five dual-function pins used for the serial port. The state of this pin and its complement are available as conditions for JUMP and CALL instructions if the pin is configured as FI rather than DR1.

Table IV. Additional Condition Codes For JUMP and CALL

FLAG_IN	FI pin last sampled 1
NOT FLAG_IN	FI pin last sampled 0

Example Code

The following example is a code fragment that performs the filter tap update for an adaptive (least-mean-squared algorithm) filter. Notice that the computations in the instructions are written like algebraic equations.

```
        MF=MX0*MY1 (RND), MX0=DM (I2,M1) ; {MF=error*beta}
        MR=MX0*MF (RND), AY0=PM (I6,M5) ;
        DO adapt UNTIL CE;
          AR=MR1+AY0, MX0=DM (I2,M1), AY0=PM (I6,M7) ;
adapt:  PM(I6,M6) =AR, MR=MX0*MF (RND) ;
        MODIFY (I2, M3) ;                    {Point to oldest data}
        MODIFY (I6, M7) ;                    {Point to start of data}
```

INSTRUCTION SET SUMMARY

Key

UPPERCASE	Assembler keyword; exact syntax of instruction
[text]	Parts of the instruction in brackets are optional
x | y | z	Choose x, y or z
[,...]	Any of the operations allowed by this instruction can be combined in any order, separated by commas
Ia, Mb or Ic, Md	Index and modify registers for indirect addressing
x	X input; permissible registers depend on instruction
y	Y input; permissible registers depend on instruction
<data>	Immediate data value
<address>	Immediate address value
condition	Condition from Table x
dreg	Computation unit data register
reg	Any register (except memory-mapped registers)
ALU	Any ALU instruction (except division)
MAC	Any multiply/accumulate instruction
SHIFT	Any shifter instruction (except shift immediate)

ALU Instructions

```
[IF condition]   AR | AF  =   x + y   [+C]        ;
                             x + C                 ;
                             x - y   [+C - 1]      ;
                             y - x   [+C - 1]      ;
                             y + 1                 ;
                             y - 1                 ;
                             x AND | OR | XOR y    ;
                             PASS x | y | 0 | 1    ;
                             -x | y                ;
                             NOT x | y             ;
                             ABS x                 ;
DIVS y, x;
DIVQ x;
```

MAC Instructions

```
[IF condition]  MR | MF  =  x * y          (SS | SU | US | UU | RND) ;
                            MR + x * y     (SS | SU | US | UU | RND) ;
                            MR - x * y     (SS | SU | US | UU | RND) ;
                            MR             [(RND)] ;
                            0 ;
IF MV SAT MR;
```

Shifter Instructions

```
[IF condition]   SR = [SR OR] ASHIFT | LSHIFT | NORM x (HI | LO) ;
[IF condition]   SE = EXP x  (HI | LO | HIX) ;
[IF condition]   SB = EXPADJ x ;
SR = [SR OR]  ASHIFT | LSHIFT x  BY <data>  (HI | LO) ;
```

Move Instructions

```
reg                 = reg | <data> | DM (<address>);
DM (<address>)      = reg;
dreg                = DM (Ia, Mb);
DM (Ia, Mb)         = dreg | <data>;
dreg                = PM (Ic, Md);
PM (Ic, Md)         = dreg;
```

Multifunction Instructions

```
ALU | MAC†,                x = DM (Ia, Mb) ,        y = PM (Ic, Md);
x = DM (Ia, Mb),           y = PM (Ic, Md);
ALU | MAC | SHIFT†,        dreg = DM | PM (Ia, Mb);
DM | PM (Ia, Mb) = dreg ,  ALU | MAC | SHIFT†;
ALU | MAC | SHIFT†,        dreg = dreg;
```

†All computation is unconditional; Division and Shift Immediate operations prohibited.

Program Flow Control Instructions

```
[IF condition]          JUMP | CALL          (Ic) | <address> ;
IF [NOT] FLAG_IN        JUMP | CALL          <address> ;
[IF condition]          RTS | RTI ;
DO <address>            [UNTIL termination];
IDLE;
```

Miscellaneous Instructions

```
[IF condition]   SET | RESET | TOGGLE   FLAG_OUT ;
ENA | DIS       BIT_REV     [,...] ;
                 AV_LATCH
                 AR_SAT
                 SEC_REG
                 TIMER
                 G_MODE
                 M_MODE
[PUSH | POP STS] [, POP  CNTR | PC | LOOP]   [,...];
MODIFY (Ia, Mb) ;
NOP;
```

ADSP-2105—SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter		K Grade Min	K Grade Max	B Grade Min	B Grade Max	Unit
V_{DD}	Supply Voltage	4.50	5.50	4.50	5.50	V
T_{AMB}	Ambient Operating Temperature	0	+70	−40	+85	°C

Refer to Environmental Conditions for information on thermal specifications.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	K/B Grades Min	K/B Grades Max	Unit
V_{IH}	Hi-Level Input Voltage[3, 5]	@ V_{DD} = max	2.0		V
V_{IH}	Hi-Level CLKIN Voltage	@ V_{DD} = max	2.2		V
V_{IL}	Lo-Level Input Voltage[1, 3]	@ V_{DD} = min		0.8	V
V_{OH}	Hi-Level Output Voltage[2, 3, 7]	@ V_{DD} = min, I_{OH} = −0.5 mA	2.4		V
		@ V_{DD} = min, I_{OH} = −100 μA[10]	V_{DD}−0.3		V
V_{OL}	Lo-Level Output Voltage[2, 3, 7]	@ V_{DD} = min, I_{OL} = 2 mA		0.4	V
I_{IH}	Hi-Level Input Current[1]	@ V_{DD} = max, V_{IN} = V_{DD} max		10	μA
I_{IL}	Lo-Level Input Current[1]	@ V_{DD} = max, V_{IN} = 0 V		10	μA
I_{OZH}	Tristate Leakage Current[4]	@ V_{DD} = max, V_{IN} = V_{DD} max[6]		10	μA
I_{OZL}	Tristate Leakage Current[4]	@ V_{DD} = max, V_{IN} = 0 V[6]		10	μA
I_{DD}	Supply Current (Idle)[8, 9]	@ V_{DD} = max		14	mA
I_{DD}	Supply Current (Dynamic)[9]	@ V_{DD} = max, t_{CK} = 97.6 ns[11]		55	mA
C_I	Input Pin Capacitance[1, 10]	@ V_{IN} = 2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C		8	pF
C_O	Output Pin Capacitance[4, 10, 12]	@ V_{IN} = 2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C		8	pF

NOTES
[1]Input only pins: CLKIN, $\overline{\text{RESET}}$, $\overline{\text{IRQ2}}$, $\overline{\text{BR}}$, MMAP, DR1.
[2]Output pins: $\overline{\text{BG}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, A0–A13, DT1, CLKOUT.
[3]Bidirectional pins: D0–D23, RFS1, SCLK1, TFS1.
[4]Tristatable pins: A0–A13, D0–D23, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, DT1, SCLK1, TFS1, RFS1.
[5]$\overline{\text{RESET}}$, $\overline{\text{IRQ2}}$, $\overline{\text{BR}}$, MMAP, DR1 input pins.
[6]0 V on $\overline{\text{BR}}$, CLKIN Active (forces tristate condition).
[7]Although specified for TTL outputs, all ADSP-2105 outputs are CMOS-compatible and will drive to V_{DD} and GND assuming no dc load.
[8]Idle refers to ADSP-2105 state of operation during execution of IDLE instruction. Deasserted pins are driven to either V_{DD} or GND.
[9]Current reflects device operating with no output loads.
[10]Guaranteed but not tested.
[11]V_{IN} = 0.4 V and 2.4 V.
[12]Output pin capacitance is the capacitive load for any tristated output pin.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . −0.3 V to +7 V
Input Voltage . . . . . −0.3 V to V_{DD} +0.3 V
Output Voltage Swing . . . . . −0.3 V to V_{DD} +0.3 V
Operating Temperature Range (Ambient) . . . −40°C to +85°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (5 sec) PLCC . . . . . +280°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD SENSITIVITY

The ADSP-2105 features proprietary input protection circuitry to dissipate high-energy discharges (Human Body Model). Per method 3015 of MIL-STD-883C, the ADSP-2105 has been classified as a Class 1 device.

Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges readily accumulate on the human body and test equipment and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed. For further information on ESD precautions, refer to *Analog Devices' ESD Prevention Manual.*

TIMING PARAMETERS

GENERAL NOTES

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add up parameters to derive longer times.

TIMING NOTES

Switching characteristics specify how the processor changes its signals. You have no control over this timing; it is dependent on the internal design. Timing requirements apply to signals that are controlled outside the processor, such as the data input for a read operation.

Timing requirements guarantee that the processor operates correctly with another device. Switching characteristics tell you what the device will do under a given circumstance. Also use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

MEMORY REQUIREMENTS

This chart links common memory device specification names and ADSP-2105 timing parameters for your convenience.

Parameter Name	Function	Common Memory Device Specification Name
t_{ASW}	A0–A13 Setup before $\overline{WR}$ Low	Address Setup to Write Start
t_{AW}	A0–A13 Setup before $\overline{WR}$ Low + $\overline{WR}$ Pulse Width	Address Setup to Write End
t_{WRA}	A0–A13 Hold after $\overline{WR}$ Deasserted	Address Hold Time
t_{DW}	Data Setup before $\overline{WR}$ High	Data Setup Time
t_{DH}	Data Hold after $\overline{WR}$ High	Data Hold Time
t_{RDD}	$\overline{RD}$ Low to Data Valid	$\overline{OE}$ to Data Valid
t_{AA}	A0–A13 to Data Valid	Address Access Time

Parameter		ADSP-2105-40 Min	Max	Unit
Clock Signals				
Timing Requirement:				
t_{CK}[1]	CLKIN Period	97.6	200	ns
t_{CKL}	CLKIN Width Low	20		ns
t_{CKH}	CLKIN Width High	20		ns
Switching Characteristic:				
t_{CPL}	CLKOUT Width Low	$0.5t_{CK}$ – 10		ns
t_{CPH}	CLKOUT Width High	$0.5t_{CK}$ – 10		ns
t_{CKOH}	CLKIN High to CLKOUT High	0	20	ns
Control Signals				
Timing Requirement:				
t_{RSP}	$\overline{\text{RESET}}$ Width Low	$5t_{CK}$[2]		ns

NOTES
[1]t_{CK} values within the range of CLKIN period should be substituted for all relevant timing parameters to obtain specification value. Example: $t_{CPH} = 0.5t_{CK} - 10$ ns = 0.5 (97.6) – 10 ns = 38.8 ns.
[2]Applies after power-up sequence is complete. Internal phase lock loop requires no more than 1000 processor cycles assuming stable CLKIN (not including crystal oscillator start-up time).

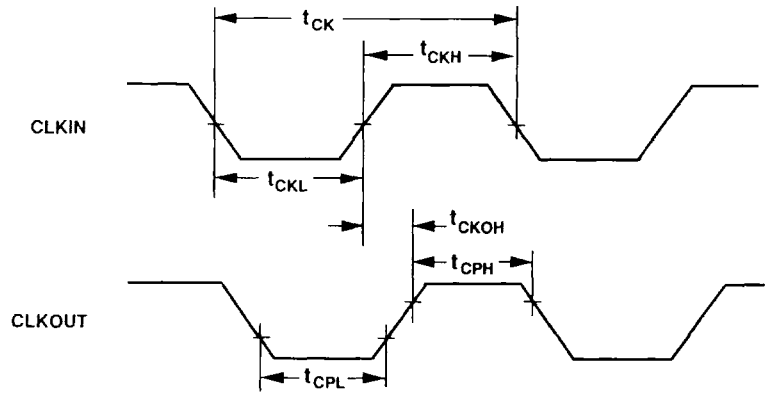


Figure 8. Clock Signals

Parameter		ADSP-2105-40 Min	Max	Unit
Interrupts and Flags				
Timing Requirement:				
t_{IFS}	IRQx or FI Setup before CLKOUT Low[1, 2]	$0.25t_{CK}$ + 15		ns
t_{IFH}	IRQx or FI Hold after CLKOUT High[1, 2]	$0.25t_{CK}$		ns
	IRQx = $\overline{IRQ0}$, $\overline{IRQ1}$, and $\overline{IRQ2}$			
Switching Characteristic:				
t_{FOH}	FO Hold after CLKOUT High	−5		ns
t_{FOD}	FO Delay from CLKOUT High		15	ns

NOTES
[1]If $\overline{IRQx}$ and FI inputs meet t_{IFS} and t_{IFH} setup/hold requirements, they will be recognized during the current clock cycle; otherwise the signals will be recognized on the following cycle. (Refer to "Interrupt Controller Operation" in the Program Control chapter of the User's Manual for further information on interrupt servicing.)
[2]Edge-sensitive interrupts require pulse widths greater than 10 ns; level-sensitive interrupts must be held low until serviced.

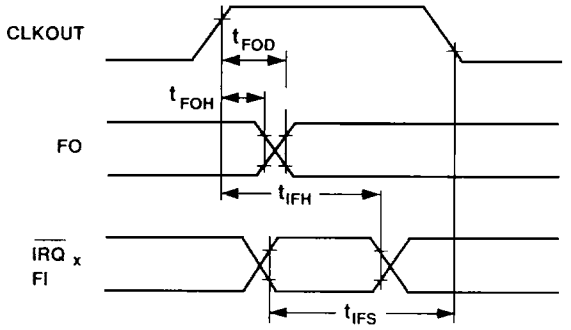


Figure 9. Interrupts and Flags

Parameter		ADSP-2105-40 Min	Max	Unit
Bus Request/Grant				
Timing Requirement:				
t_{BH}	$\overline{BR}$ Hold after CLKOUT High[1]	$0.25t_{CK}$ + 5		ns
t_{BS}	$\overline{BR}$ Setup before CLKOUT Low[1]	$0.25t_{CK}$ + 20		ns
Switching Characteristic:				
t_{SD}	CLKOUT High to $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Disable		$0.25t_{CK}$ + 20	ns
t_{SDB}	$\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BG}$ Low	0		ns
t_{SE}	$\overline{BG}$ High to $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Enable	0		ns
t_{SEC}	$\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Enable to CLKOUT High	$0.25t_{CK}$ – 10		ns

NOTE
[1]$\overline{BR}$ is a synchronous signal which must meet setup/hold time requirements. Refer to the User's Manual for $\overline{BR}/\overline{BG}$ cycle relationships.

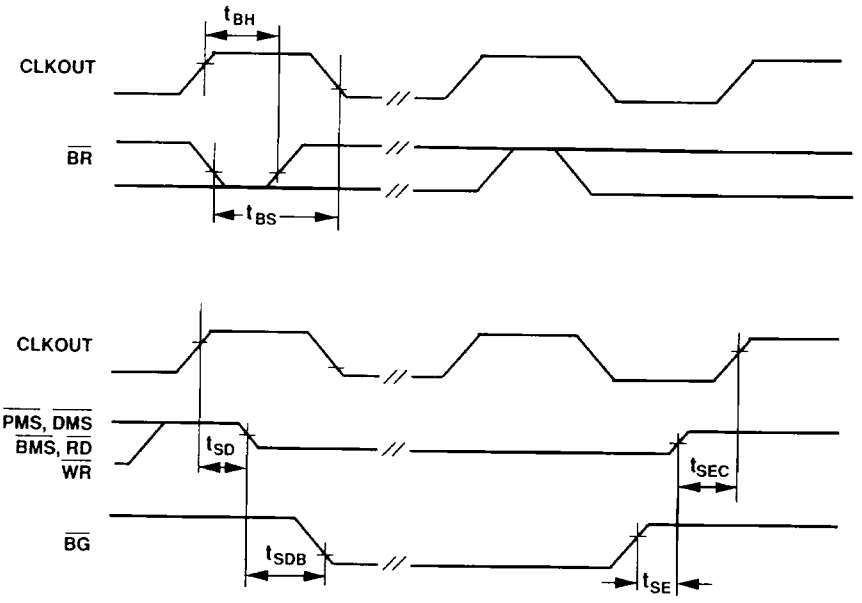


Figure 10. Bus Request–Bus Grant

Parameter		ADSP-2105-40 Min	Max	Unit
Memory Read				
Timing Requirement:				
t_{RDD}	$\overline{RD}$ Low to Data Valid		$0.5t_{CK} - 15+w$	ns
t_{AA}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ to Data Valid		$0.75t_{CK} - 20+w$	ns
t_{RDH}	Data Hold from $\overline{RD}$ High	0		ns
Switching Characteristic:				
t_{RP}	$\overline{RD}$ Pulse Width	$0.5t_{CK} - 5+w$		ns
t_{CRD}	CLKOUT High to $\overline{RD}$ Low	$0.25t_{CK} - 5$	$0.25t_{CK} + 10$	ns
t_{ASR}	A0–A13, $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$ Setup before $\overline{RD}$ Low	$0.25t_{CK} - 12$		ns
t_{RDA}	A0–A13, $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$ Hold after $\overline{RD}$ Deasserted	$0.25t_{CK} - 10$		ns
t_{RWR}	$\overline{RD}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 5$		ns
		w = wait states × (t_{CK})		

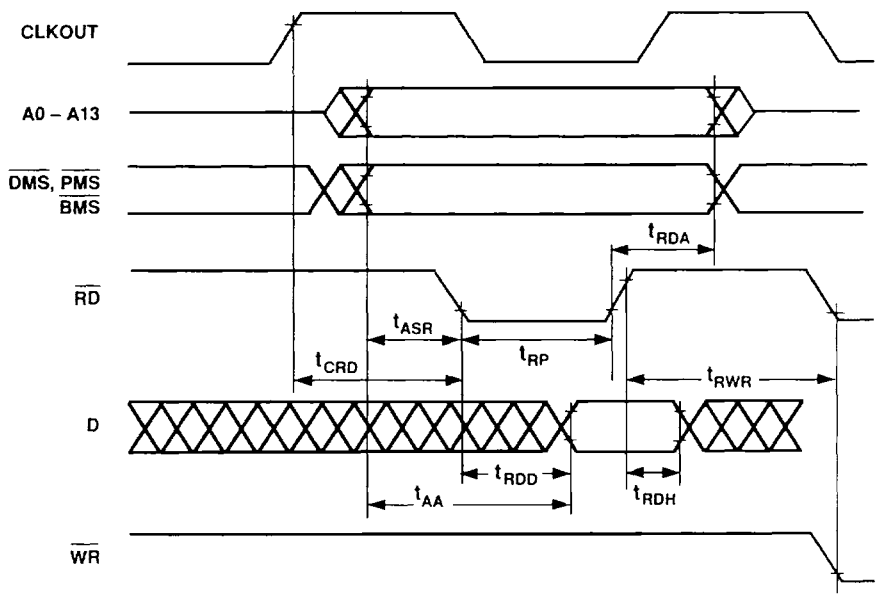


Figure 11. Memory Read

Parameter		ADSP-2105-40 Min	Max	Unit
Memory Write				
Switching Characteristic:				
t_{DW}	Data Setup before $\overline{WR}$ High	$0.5t_{CK} - 10+w$		ns
t_{DH}	Data Hold after $\overline{WR}$ High	$0.25t_{CK} - 10$		ns
t_{WP}	$\overline{WR}$ Pulse Width	$0.5t_{CK} - 5+w$		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	0		ns
t_{ASW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Setup before $\overline{WR}$ Low	$0.25t_{CK} - 12$		ns
t_{DDR}	Data Disable before $\overline{WR}$ or $\overline{RD}$ Low	$0.25t_{CK} - 10$		ns
t_{CWR}	CLKOUT High to $\overline{WR}$ Low	$0.25t_{CK} - 5$	$0.25t_{CK} + 10$	ns
t_{AW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Setup before $\overline{WR}$ Deasserted	$0.75t_{CK} - 15+w$		ns
t_{WRA}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Hold after $\overline{WR}$ Deasserted	$0.25t_{CK} - 10$		ns
t_{WWR}	$\overline{WR}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 5$		ns
		w = wait states × (t_{CK})		

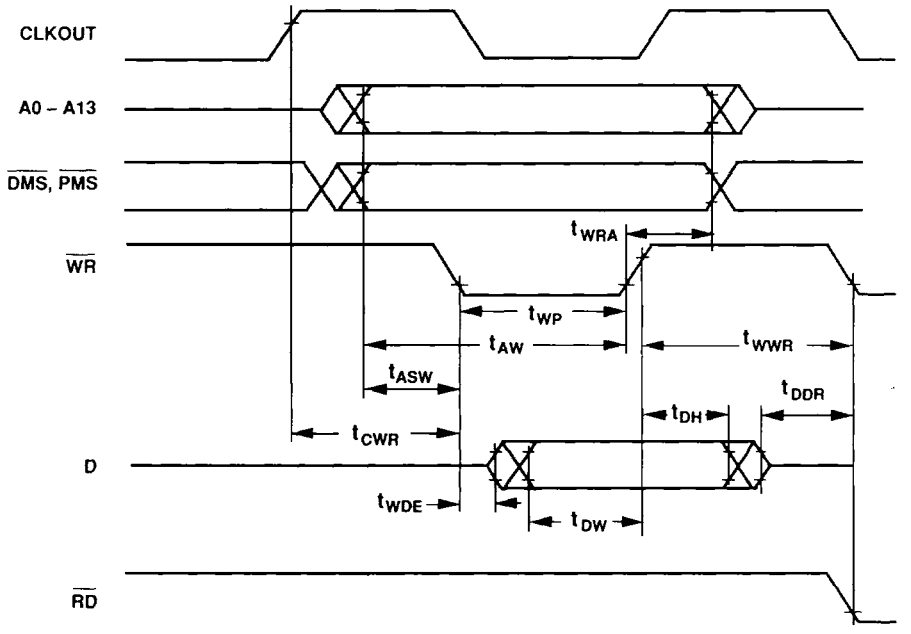


Figure 12. Memory Write

Parameter		ADSP-2105-40 Min	Max	Unit
Serial Port				
Timing Requirement:				
t_{SCK}	SCLK Period	97.6		ns
t_{SCS}	DR/TFS/RFS Setup before SCLK Low	10		ns
t_{SCH}	DR/TFS/RFS Hold after SCLK Low	10		ns
t_{SCP}	$SCLK_{in}$ Width	38		ns
Switching Characteristic:				
t_{CC}	CLKOUT High to $SCLK_{out}$	$0.25t_{CK}$	$0.25t_{CK}$ + 15	ns
t_{SCDE}	SCLK High to DT Enable	0		ns
t_{SCDV}	SCLK High to DT Valid		25	ns
t_{RH}	TFS/RFS_{out} Hold after SCLK High	0		ns
t_{RD}	TFS/RFS_{out} Delay from SCLK High		25	ns
t_{SCDH}	DT Hold after SCLK High	0		ns
t_{TDE}	TFS_{in} (alt) to DT Enable	0		ns
t_{TDV}	TFS_{in} (alt) to DT Valid		20	ns
t_{SCDD}	SCLK High to DT Disable		30	ns

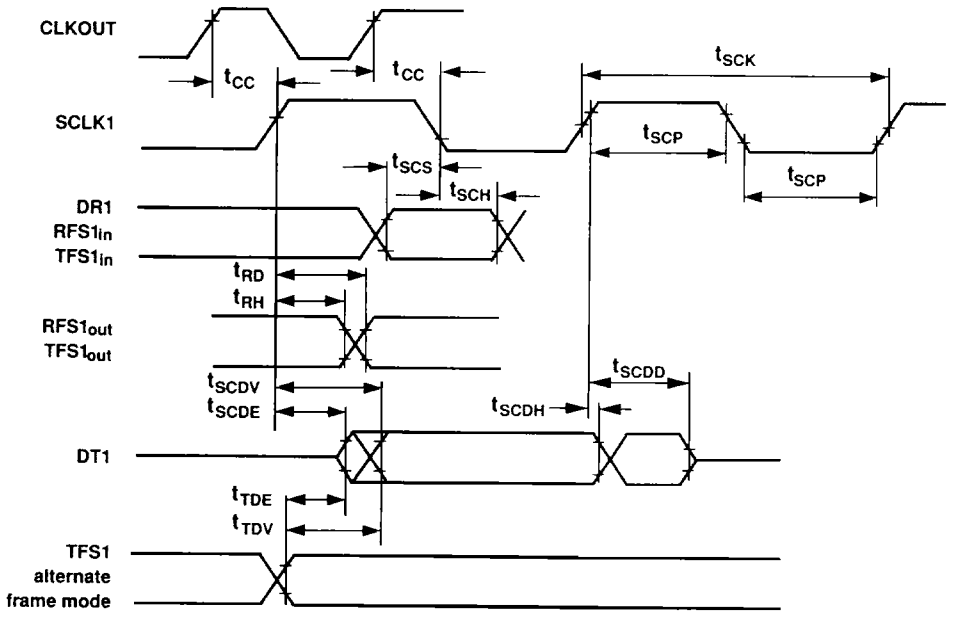


Figure 13. Serial Port

ENVIRONMENTAL CONDITIONS

Ambient Temperature Rating:

$T_{amb} = T_{case} - (PD \times \theta_{CA})$

T_{case} = Case temp in °C
PD = Power dissipation in W
θ_{CA} = Thermal resistance (case-to-ambient)
θ_{JA} = Thermal resistance (junction-to-ambient)
θ_{JC} = Thermal resistance (junction-to-case)

Package	θ_{JA}	θ_{JC}	θ_{CA}
PLCC	27°C/W	16°C/W	11°C/W

Power Dissipation

To determine total power dissipation in a specific application, the following equation should be applied for each output:

$$C \times V_{DD}^2 \times f$$

C = load capacitance, f = output switching frequency.

Example:

In an application where external data memory is used and no other outputs are active, power dissipation is calculated as follows.

Assumptions:

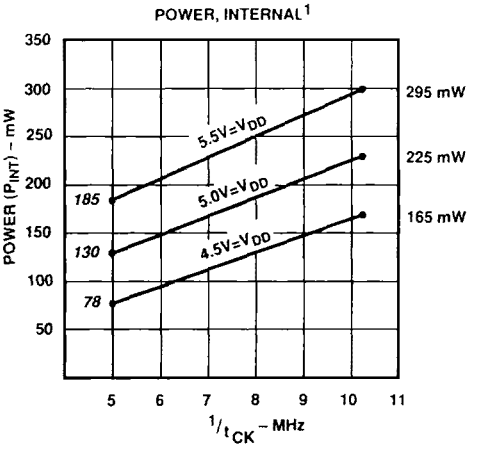
- External data memory is accessed every cycle with 50% of address pins switching.
- External data memory writes occur every other cycle with 50% of address pins switching.
- Each address and data pin has a 10 pF total load at the pin.
- The application operates at V_{DD} = 5.0 V and t_{CK} = 100 ns.

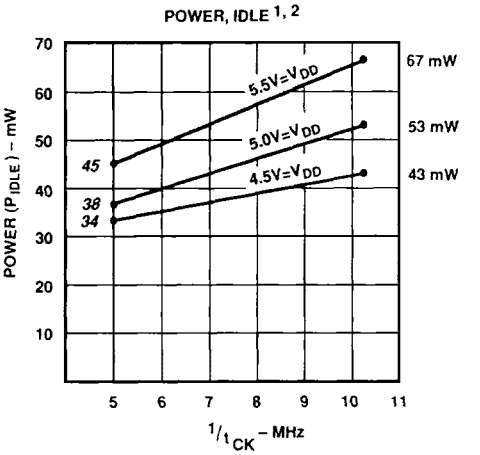
Total Power Dissipation = $P_{INT} + (C \times V_{DD}^2 \times f)$

P_{INT} = internal power dissipation, from Figure 14.
$C \times V_{DD}^2 \times f$ is calculated for each output:

	# of Pins	× C	$\times V_{DD}^2$	× f
Address, $\overline{DMS}$	8	× 10 pF	× 5^2 V	× 10 MHz= 20.00 mW
Data Output, $\overline{WR}$	9	× 10 pF	× 5^2 V	× 5 MHz = 11.25 mW
$\overline{RD}$	1	× 10 pF	× 5^2 V	× 5 MHz = 1.25 mW
CLKOUT	1	× 10 pF	× 5^2 V	× 10 MHz= 2.50 mW
				35.00 mW

Total power dissipation in the example is P_{INT}+35.00 mW.





Valid for all temperature grades.

[1] Power reflects device operating with no output loads.

[2] IDLE refers to ADSP-2105 state of operation during execution of IDLE instruction. Deasserted pins are driven to either V_{DD} or GND.

Figure 14. Power vs. Frequency

CAPACITIVE LOADING

Figures 15 and 16 show capacitive loading characteristics for the ADSP-2105.

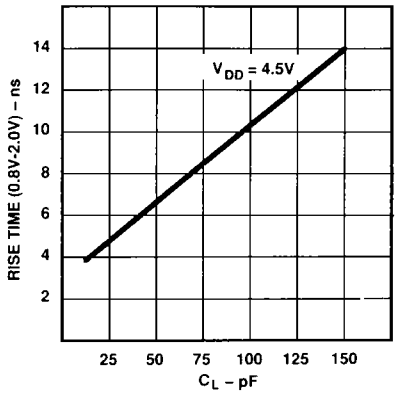


Figure 15. Typical Output Rise Time vs. Load Capacitance, C_L, (at Maximum Ambient Operating Temperature)

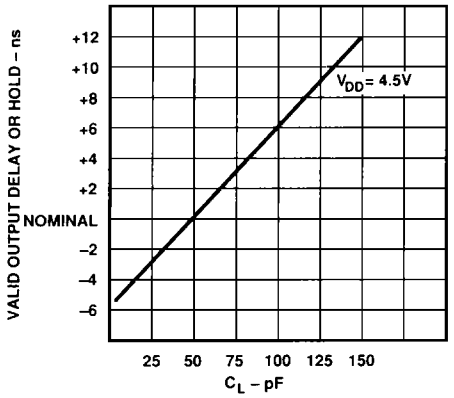


Figure 16. Typical Output Valid Delay or Hold vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

TEST CONDITIONS

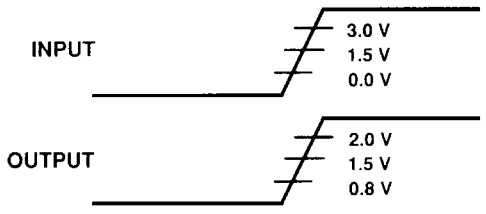


Figure 17. Voltage Reference Levels for AC Measurement (Except Output Enable/Disable)

Output Disable Time

Output pins are considered to be disabled when they have stopped driving and started a transition from the measured output high or low voltage to a high-impedance state. The output disable time (t_{DIS}) is the difference of $t_{MEASURED}$ and t_{DECAY}, as shown in the Output Enable/Disable diagram below. The time, $t_{MEASURED}$, is the interval from when a reference signal reaches a high or low voltage level to when the output voltages have changed by 0.5 V from the measured output high or low voltage. The decay time, t_{DECAY}, is dependent on the capacitive load, C_L, and the current load, i_L, on the output pin. It can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \cdot 0.5\ V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. If multiple pins (such as the data bus) are disabled, the measurement value is that of the last pin to stop driving.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high-impedance state to when they start driving. The output enable time (t_{ENA}) is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in the Output Enable/Disable diagram. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

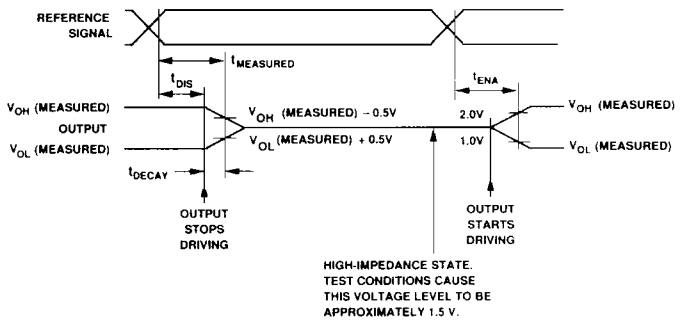


Figure 18. Output Enable/Disable

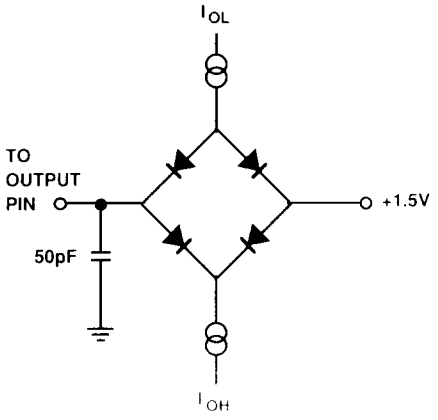


Figure 19. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

DIFFERENCES BETWEEN THE ADSP-2101 AND ADSP-2105

Internal Memory

The ADSP-2105 has less on-chip memory than the ADSP-2101. Internal program memory is 1K words instead of 2K words. Internal data memory is 0.5K (512) words instead of 1K words. The internal memory locations on the ADSP-2101 that are not on the ADSP-2105 are reserved on the ADSP-2105. External memory spaces are the same for both devices.

Serial Port

The ADSP-2105 has one serial port, SPORT1, whereas the ADSP-2101 has two. The ADSP-2105 SPORT1 is identical to SPORT1 on the ADSP-2101. The SPORT0 pins on the ADSP-2101 are no-connects on the ADSP-2105. Note that SPORT1 does not have the multichannel capability of the ADSP-2101's SPORT0.

Interrupts

The ADSP-2105 has two fewer interrupts than the ADSP-2101. It does not have the SPORT0 transmit and receive interrupts. The IMASK and IFC bits that control these interrupts are reserved on the ADSP-2105 and must be zeros.

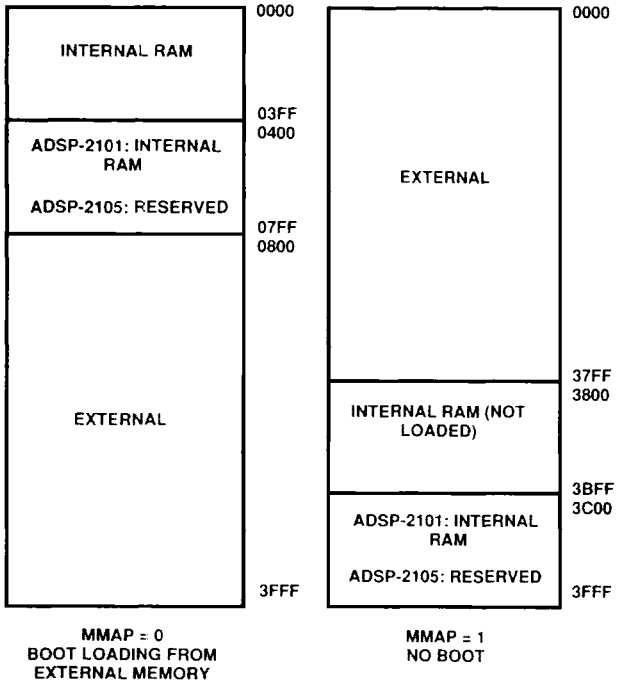


Figure 20. Program Memory Map

Boot Memory

On both the ADSP-2101 the ADSP-2105, D23, D22 and A13 supply the boot page number. For the 8K-byte pages of the ADSP-2101, A12 is the address MSB. For the 4K-byte boot pages of the ADSP-2105, address line A12 is not needed and is always zero; A11 is the address MSB.

If your system has more than 1K of boot code, you will be able to upgrade from the ADSP-2105 to the ADSP-2101 without hardware modifications if you design your system with 8K-byte (2K-word) boot pages. Initially, the ADSP-2105 will boot in only the lower half (1K words) of each page, so the upper half of each page must be empty. When you upgrade to the ADSP-2101, you can use all 2K words in each boot page.

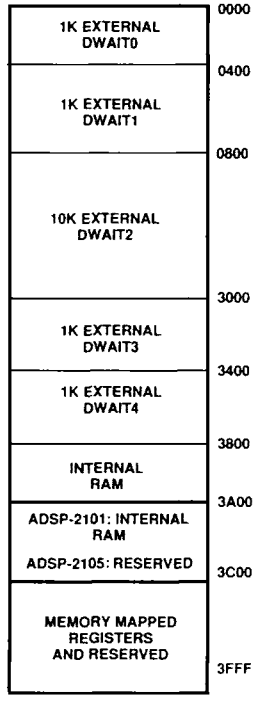


Figure 21. Data Memory Map

EMULATOR MECHANICAL SPECIFICATIONS

If you plan to use the ADSP-2101 emulator to debug your system, you should take into consideration the physical dimensions of the emulator probe (the part of the emulator that fits in the ADSP-2105 socket in your system). There must be enough clearance around the ADSP-2105 socket to connect the probe.

The emulator probe consists of a target processor board (which holds the emulating ADSP-2101) and two optional boards, an overlay RAM board and interface board. Figures 22 and 23 specify maximum (unless otherwise noted) dimensions for the probe. Figure 22 is the top view of the target processor board; Figure 23 is the side view of the probe including overlay RAM board and interface board. Also shown are the probe fan and PGA-PLCC adaptor. The PGA-PLCC adaptor is available from: Emulation Technology, 2344 Walsh Ave., Bldg. F, Santa Clara, CA 95051, (408) 982-0660, (P/N AP4-68-PGA); and EDI Corp., P.O. Box 366, Patterson, CA 95363, (209) 892-3270, (P/N 68-PGA/PLCC).

For more information, see the ADDS-21XX-ICE data sheet.

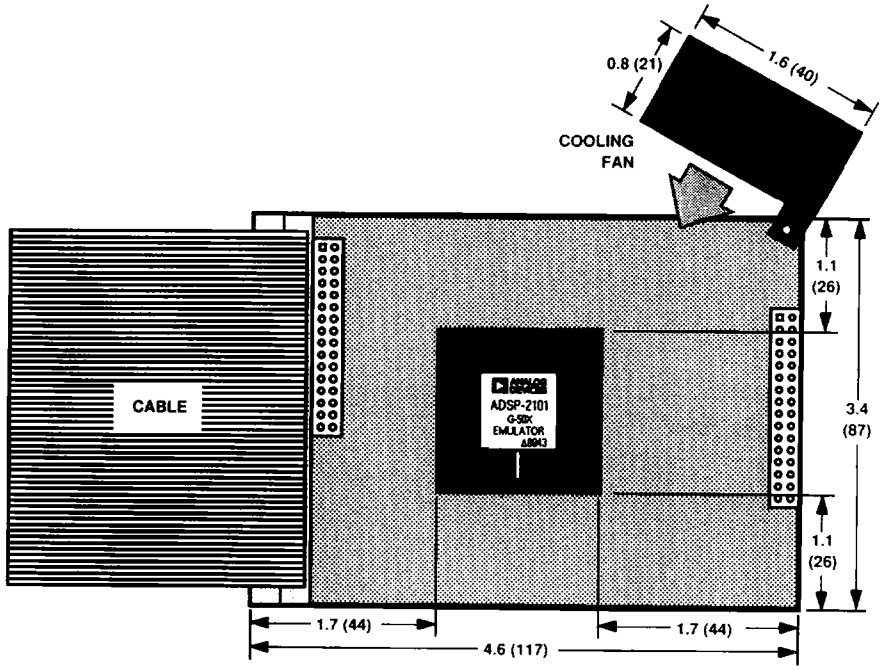


Figure 22. Probe (Top View) Dimensions in Inches (mm)

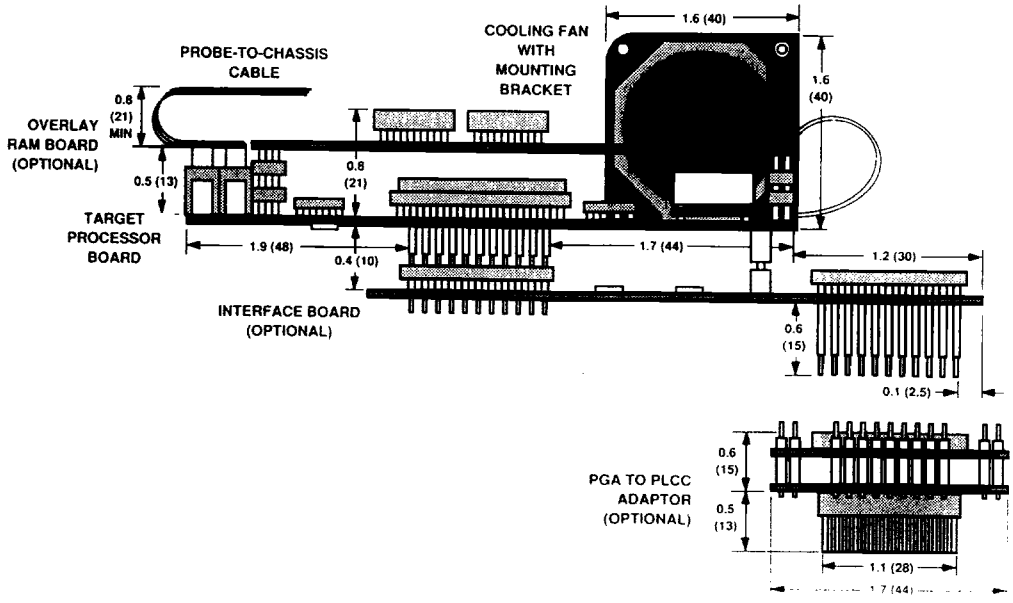
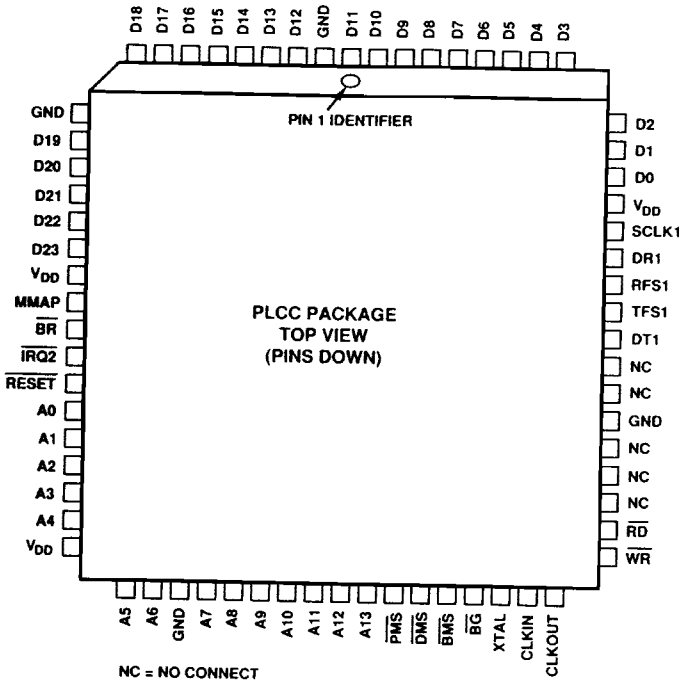


Figure 23. Probe (Side View) Dimensions in Inches (mm)

ADSP-2105

PIN CONFIGURATION



PIN CONFIGURATION

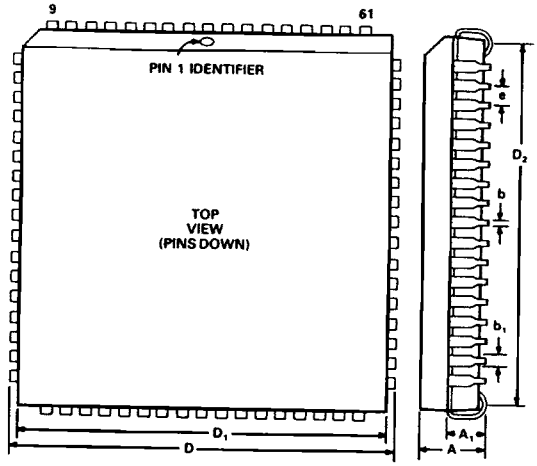
PLCC NUMBER	PIN NAME	PLCC NUMBER	PIN NAME
1	D11	35	A12
2	GND	36	A13
3	D12	37	$\overline{PMS}$
4	D13	38	$\overline{DMS}$
5	D14	39	$\overline{BMS}$
6	D15	40	$\overline{BG}$
7	D16	41	XTAL
8	D17	42	CLKIN
9	D18	43	CLKOUT
10	GND	44	$\overline{WR}$
11	D19	45	$\overline{RD}$
12	D20	46	NC
13	D21	47	NC
14	D22	48	NC
15	D23	49	GND
16	V_{DD}	50	NC
17	MMAP	51	NC
18	$\overline{BR}$	52	DT1
19	$\overline{IRQ2}$	53	TFSI
20	$\overline{RESET}$	54	RFSI
21	A0	55	DR1
22	A1	56	SCLK1
23	A2	57	V_{DD}
24	A3	58	D0
25	A4	59	D1
26	V_{DD}	60	D2
27	A5	61	D3
28	A6	62	D4
29	GND	63	D5
30	A7	64	D6
31	A8	65	D7
32	A9	66	D8
33	A10	67	D9
34	A11	68	D10

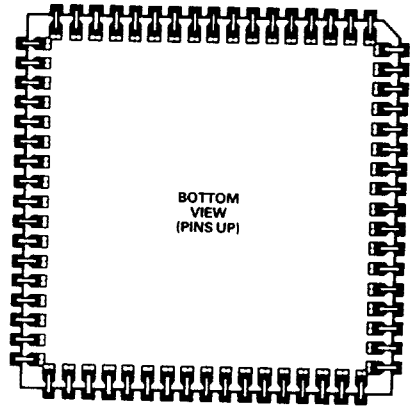
NC = NO CONNECT.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

68-Lead Plastic Leaded Chip Carrier (PLCC)





SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.169	0.175	4.29	4.45
A_1	0.014 TYP		2.64 TYP	
b	0.017	0.019	0.43	0.48
b_1	0.027	0.029	0.69	0.74
D	0.885	0.995	22.48	25.27
D_1	0.950	0.954	24.13	24.23
D_2	0.895	0.925	22.73	23.50
e	0.050 TYP		1.27 TYP	

ORDERING GUIDE

Part Number	Ambient Temperature Range	Instruction Rate (MHz)	Package
ADSP-2105KP-40	0°C to +70°C	10.24	68-Lead PLCC
ADSP-2105BP-40	-40°C to +85°C	10.24	68-Lead PLCC