NEC

MOS INTEGRATED CIRCUIT

μPD29F032203AL-Y

32M-BIT CMOS LOW-VOLTAGE DUAL OPERATION FLASH MEMORY 4M-WORD BY 8-BIT (BYTE MODE) / 2M-WORD BY 16-BIT (WORD MODE)

Description

The μPD29F032203AL-Y is a flash memory organized of 33,554,432 bits and 71 sectors. Sectors of this memory can be erased at a low voltage (2.7 to 3.3 V, 3.0 to 3.6 V) supplied from a single power source, or the contents of the entire chip can be erased. Two modes of memory organization, BYTE mode (4,194,304 words × 8 bits) and WORD mode (2,097,152 words × 16 bits), are selectable so that the memory can be programmed in byte or word units.

The μPD29F032203AL-Y can be read while its contents are being erased or programmed. The memory cell is divided into two banks. While sectors in one bank are being erased or programmed, data can be read from the other bank thanks to the simultaneous execution architecture. The banks are 8M bits and 24M bits.

This flash memory comes in two types. The T type has a boot sector located at the highest address (sector) and the B type has a boot sector at the lowest address (sector).

Because the μPD29F032203AL-Y enables the boot sector to be erased, it is ideal for storing a boot program. In addition, program code that controls the flash memory can be also stored, and the program code can be programmed or erased without the need to load it into RAM. Eight small sectors for storing parameters are provided, each of which can be erased in 8K bytes units.

Once a program or erase command sequence has been executed, an automatic program or automatic erase function internally executes program or erase and verification automatically.

Because the μPD29F032203AL-Y can be electrically erased or programmed by writing an instruction, data can be reprogrammed on-board after the flash memory has been installed in a system, making it suitable for a wide range of applications.

This flash memory is packed in a 48-pin PLASTIC TSOP(I) and 63-pin TAPE FBGA.

Features

- Two bank organization enabling simultaneous execution of program / erase and read
- Bank organization: 2 banks (8M bits + 24M bits)
- Memory organization : 4,194,304 words × 8 bits (BYTE mode)
  2,097,152 words × 16 bits (WORD mode)
- Sector organization : 71 sectors (8K bytes / 4K words × 8 sectors, 64K bytes / 32K words × 63 sectors)
- 2 types of sector organization
  - T type : Boot sector allocated to the highest address (sector)
  - B type : Boot sector allocated to the lowest address (sector)
- 3-state output
- Automatic program
  - Program suspend / resume

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The mark ★ shows major revised points.

- Unlock bypass program
- Automatic erase
  - Chip erase
  - Sector erase (sectors can be combined freely)
- Erase suspend / resume
- Program / Erase completion detection
  - Detection through data polling and toggle bits
  - Detection through RY (/BY) pin
- Sector group protection
  - Any sector group can be protected
  - Any protected sector group can be temporary unprotected
- Sectors can be used for boot application
- Hardware reset and standby using /RESET pin
- Automatic sleep mode
- Boot block sector protect by /WP (ACC) pin
- Conforms to common flash memory interface (CFI)
- Extra One Time Protect Sector provided

μPD29F032203AL	Access time ns (MAX.)	Operating supply voltage V	Power supply current (Active mode) mA (MAX.)		Standby current μA (MAX.)
			Read	Program / Erase	
-A85TY, -A85BY	85	3.0 to 3.6	16	30	5
-B85TY, -B85BY		2.7 to 3.3			

- Operating ambient temperature: –40 to +85°C
- Program / erase time
  - Program: 9.0 μs / byte (TYP.)
    11.0 μs / word (TYP.)
  - Sector erase :
    Program / erase cycle : 100,000 cycles
    0.3 s (TYP.) (4K words sector), 0.5 s (TYP.) (32K words sector)
    Program / erase cycle : 300,000 cycles
    0.5 s (TYP.) (4K words sector), 0.7 s (TYP.) (32K words sector)
- Program / erase cycle : 300,000 cycles (MIN.)

Ordering Information

Part number	Access time ns (MAX.)	Operating supply voltage V	Boot sector	Package
μPD29F032203ALGZ-A85TY-MJH	85	3.0 to 3.6	Top address (sector) (T type)	48-pin PLASTIC TSOP (I) (12 × 20) (Normal bent)
μPD29F032203ALGZ-A85BY-MJH			Bottom address (sector) (B type)	
μPD29F032203ALF9-A85TY-BS2			Top address (sector) (T type)	63-pin TAPE FBGA (11 × 7)
μPD29F032203ALF9-A85BY-BS2			Bottom address (sector) (B type)	
μPD29F032203ALGZ-B85TY-MJH		2.7 to 3.3	Top address (sector) (T type)	48-pin PLASTIC TSOP (I) (12 × 20) (Normal bent)
μPD29F032203ALGZ-B85BY-MJH			Bottom address (sector) (B type)	
μPD29F032203ALF9-B85TY-BS2			Top address (sector) (T type)	63-pin TAPE FBGA (11 × 7)
μPD29F032203ALF9-B85BY-BS2			Bottom address (sector) (B type)	

Remark For address organization of sectors, see section **Sector Organization / Sector Address Table**.

Pin Configurations

/xxx indicates active low signal.

48-pin PLASTIC TSOP (I) (12 × 20) (Normal bent)

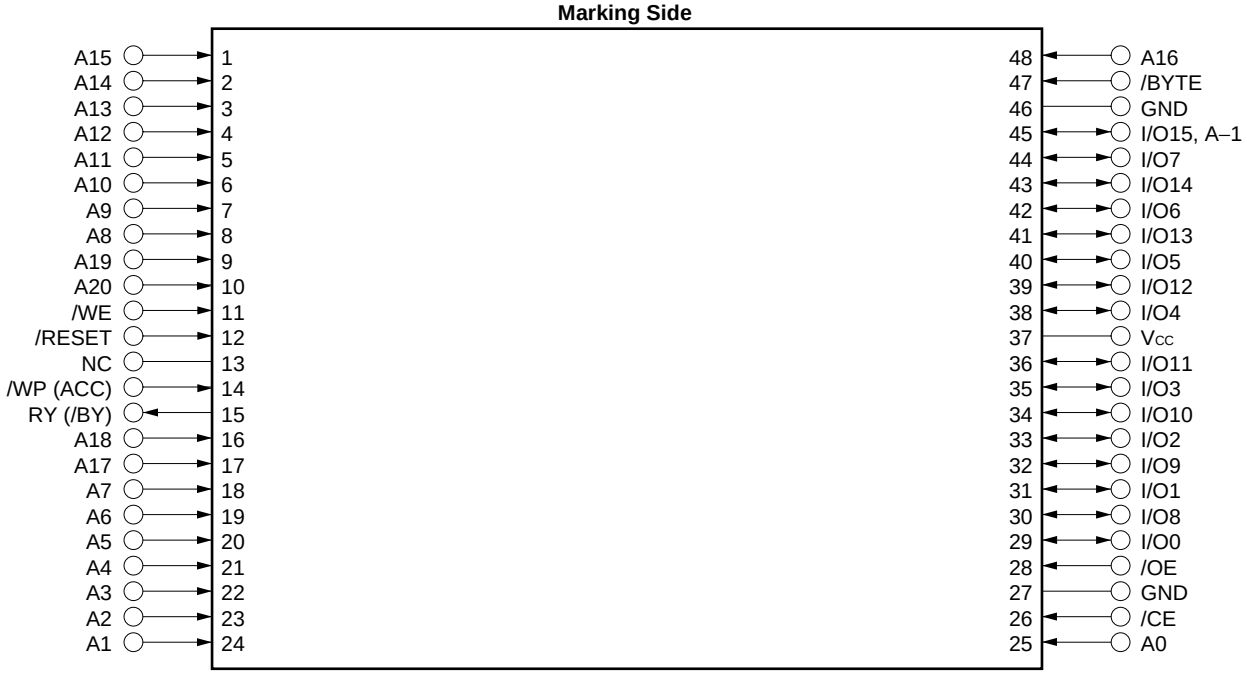
[μPD29F032203ALGZ-A85TY-MJH]

[μPD29F032203ALGZ-A85BY-MJH]

[μPD29F032203ALGZ-B85TY-MJH]

[μPD29F032203ALGZ-B85BY-MJH]

Marking Side



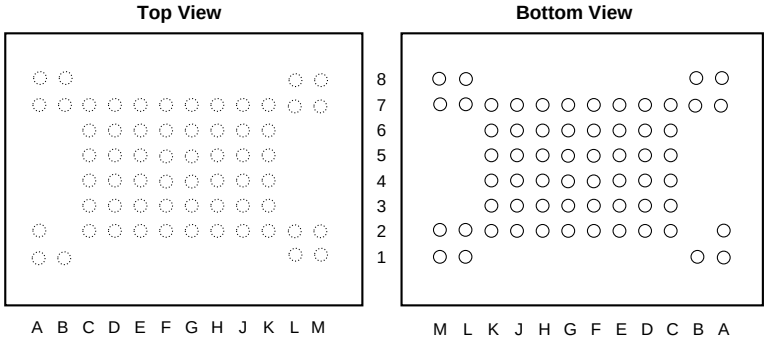
A0 to A20	:	Address inputs
I/O0 to I/O14	:	Data Inputs / Outputs
I/O15, A–1	:	Data 15 Input / output (WORD mode) LSB address input (BYTE mode)
/CE	:	Chip Enable
/WE	:	Write Enable
/OE	:	Output Enable
/BYTE	:	Mode select
/RESET	:	Hardware reset input
RY (/BY)	:	Ready (Busy) output
/WP (ACC)	:	Write Protect (Accelerated) input
V_{CC}	:	Supply Voltage
GND	:	Ground
NC [Note]	:	No Connection

Note Some signals can be applied because this pin is not connected to the inside of the chip.

Remark Refer to **Package Drawings** for the 1-pin index mark.

63-pin TAPE FBGA (11 × 7)

[μPD29F032203ALF9-A85TY-BS2]
[μPD29F032203ALF9-A85BY-BS2]
[μPD29F032203ALF9-B85TY-BS2]
[μPD29F032203ALF9-B85BY-BS2]



Top View

	A	B	C	D	E	F	G	H	J	K	L	M
8	NC	NC									NC	NC
7	NC	NC	A13	A12	A14	A15	A16	/BYTE	I/O15,A–1	GND	NC	NC
6			A9	A8	A10	A11	I/O7	I/O14	I/O13	I/O6		
5			/WE	/RESET	NC	A19	I/O5	I/O12	V_{CC}	I/O4		
4			RY(/BY)	/WP(ACC)	A18	A20	I/O2	I/O10	I/O11	I/O3		
3			A7	A17	A6	A5	I/O0	I/O8	I/O9	I/O1		
2	NC		A3	A4	A2	A1	A0	/CE	/OE	GND	NC	NC
1	NC	NC									NC	NC

A0 to A20	: Address inputs
I/O0 to I/O14	: Data Inputs / Outputs
I/O15, A–1	: Data 15 Input / output (WORD mode) LSB address input (BYTE mode)
/CE	: Chip Enable
/WE	: Write Enable
/OE	: Output Enable
/BYTE	: Mode select
/RESET	: Hardware reset input
RY (/BY)	: Ready (Busy) output
/WP (ACC)	: Write Protect (Accelerated) input
V_{CC}	: Supply Voltage
GND	: Ground
NC [Note]	: No Connection

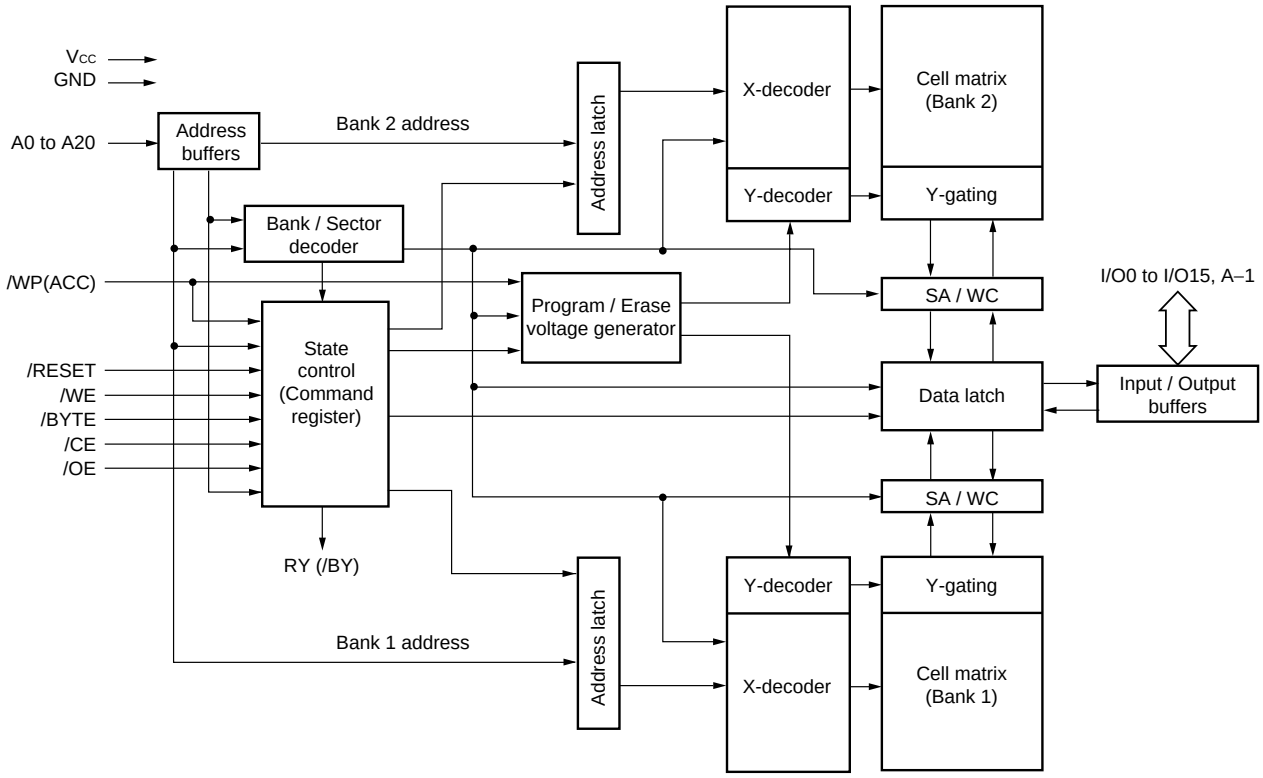
Note Some signals can be applied because this pin is not connected to the inside of the chip.

Remark Refer to **Package Drawings** for the index mark.

INPUT / OUTPUT PIN FUNCTION

Refer to **DUAL OPERATION FLASH MEMORY 32M BITS A SERIES Information (M14914E)**.

Block Diagram



Sector Organization / Sector Address Table

[-A85TY, -B85TY] **(1/2)**

Bank	Sector Organization K bytes / K words	Address BYTE mode	Address WORD mode	Sectors Address	Sector Address Table Bank Address Table A20	A19	A18	A17	A16	A15	A14	A13	A12
Bank 1	8/4	3FFFFFH 3FE000H	1FFFFFH 1FF000H	FSA70	1	1	1	1	1	1	1	1	1
	8/4	3FDFFFH 3FC000H	1FEFFFH 1FE000H	FSA69	1	1	1	1	1	1	1	1	0
	8/4	3FBFFFH 3FA000H	1FDFFFH 1FD000H	FSA68	1	1	1	1	1	1	1	0	1
	8/4	3F9FFFH 3F8000H	1FCFFFH 1FC000H	FSA67	1	1	1	1	1	1	1	0	0
	8/4	3F7FFFH 3F6000H	1FBFFFH 1FB000H	FSA66	1	1	1	1	1	1	0	1	1
	8/4	3F5FFFH 3F4000H	1FAFFFH 1FA000H	FSA65	1	1	1	1	1	1	0	1	0
	8/4	3F3FFFH 3F2000H	1F9FFFH 1F9000H	FSA64	1	1	1	1	1	1	0	0	1
	8/4	3F1FFFH 3F0000H	1F8FFFH 1F8000H	FSA63	1	1	1	1	1	1	0	0	0
	64/32	3EFFFFH 3E0000H	1F7FFFH 1F0000H	FSA62	1	1	1	1	1	0	x	x	x
	64/32	3DFFFFH 3D0000H	1EFFFFH 1E8000H	FSA61	1	1	1	1	0	1	x	x	x
	64/32	3CFFFFH 3C0000H	1E7FFFH 1E0000H	FSA60	1	1	1	1	0	0	x	x	x
	64/32	3BFFFFH 3B0000H	1DFFFFH 1D8000H	FSA59	1	1	1	0	1	1	x	x	x
	64/32	3AFFFFH 3A0000H	1D7FFFH 1D0000H	FSA58	1	1	1	0	1	0	x	x	x
	64/32	39FFFFH 390000H	1CFFFFH 1C8000H	FSA57	1	1	1	0	0	1	x	x	x
	64/32	38FFFFH 380000H	1C7FFFH 1C0000H	FSA56	1	1	1	0	0	0	x	x	x
	64/32	37FFFFH 370000H	1BFFFFH 1B8000H	FSA55	1	1	0	1	1	1	x	x	x
	64/32	36FFFFH 360000H	1B7FFFH 1B0000H	FSA54	1	1	0	1	1	0	x	x	x
	64/32	35FFFFH 350000H	1AFFFFH 1A8000H	FSA53	1	1	0	1	0	1	x	x	x
	64/32	34FFFFH 340000H	1A7FFFH 1A0000H	FSA52	1	1	0	1	0	0	x	x	x
	64/32	33FFFFH 330000H	19FFFFH 198000H	FSA51	1	1	0	0	1	1	x	x	x
	64/32	32FFFFH 320000H	197FFFH 190000H	FSA50	1	1	0	0	1	0	x	x	x
	64/32	31FFFFH 310000H	18FFFFH 188000H	FSA49	1	1	0	0	0	1	x	x	x
	64/32	30FFFFH 300000H	187FFFH 180000H	FSA48	1	1	0	0	0	0	x	x	x
Bank 2	64/32	2FFFFFH 2F0000H	17FFFFH 178000H	FSA47	1	0	1	1	1	1	x	x	x
	64/32	2EFFFFH 2E0000H	177FFFH 170000H	FSA46	1	0	1	1	1	0	x	x	x
	64/32	2DFFFFH 2D0000H	16FFFFH 168000H	FSA45	1	0	1	1	0	1	x	x	x
	64/32	2CFFFFH 2C0000H	167FFFH 160000H	FSA44	1	0	1	1	0	0	x	x	x
	64/32	2BFFFFH 2B0000H	15FFFFH 158000H	FSA43	1	0	1	0	1	1	x	x	x
	64/32	2AFFFFH 2A0000H	157FFFH 150000H	FSA42	1	0	1	0	1	0	x	x	x
	64/32	29FFFFH 290000H	14FFFFH 148000H	FSA41	1	0	1	0	0	1	x	x	x
	64/32	28FFFFH 280000H	147FFFH 140000H	FSA40	1	0	1	0	0	0	x	x	x
	64/32	27FFFFH 270000H	13FFFFH 138000H	FSA39	1	0	0	1	1	1	x	x	x
	64/32	26FFFFH 260000H	137FFFH 130000H	FSA38	1	0	0	1	1	0	x	x	x
	64/32	25FFFFH 250000H	12FFFFH 128000H	FSA37	1	0	0	1	0	1	x	x	x
	64/32	24FFFFH 240000H	127FFFH 120000H	FSA36	1	0	0	1	0	0	x	x	x
	64/32	23FFFFH 230000H	11FFFFH 118000H	FSA35	1	0	0	0	1	1	x	x	x

[-A85TY, -B85TY] **(2/2)**

Bank	Sector Organization	Address		Sectors Address	Sector Address Table								
					Bank Address Table								
	K bytes / K words	BYTE mode	WORD mode		A20	A19	A18	A17	A16	A15	A14	A13	A12
Bank 2	64/32	22FFFFH 220000H	117FFFH 110000H	FSA34	1	0	0	0	1	0	x	x	x
	64/32	21FFFFH 210000H	10FFFFH 108000H	FSA33	1	0	0	0	0	1	x	x	x
	64/32	20FFFFH 200000H	107FFFH 100000H	FSA32	1	0	0	0	0	0	x	x	x
	64/32	1FFFFFH 1F0000H	0FFFFFH 0F8000H	FSA31	0	1	1	1	1	1	x	x	x
	64/32	1EFFFFH 1E0000H	0F7FFFH 0F0000H	FSA30	0	1	1	1	1	0	x	x	x
	64/32	1DFFFFH 1D0000H	0EFFFFH 0E8000H	FSA29	0	1	1	1	0	1	x	x	x
	64/32	1CFFFFH 1C0000H	0E7FFFH 0E0000H	FSA28	0	1	1	1	0	0	x	x	x
	64/32	1BFFFFH 1B0000H	0DFFFFH 0D8000H	FSA27	0	1	1	0	1	1	x	x	x
	64/32	1AFFFFH 1A0000H	0D7FFFH 0D0000H	FSA26	0	1	1	0	1	0	x	x	x
	64/32	19FFFFH 190000H	0CFFFFH 0C8000H	FSA25	0	1	1	0	0	1	x	x	x
	64/32	18FFFFH 180000H	0C7FFFH 0C0000H	FSA24	0	1	1	0	0	0	x	x	x
	64/32	17FFFFH 170000H	0BFFFFH 0B8000H	FSA23	0	1	0	1	1	1	x	x	x
	64/32	16FFFFH 160000H	0B7FFFH 0B0000H	FSA22	0	1	0	1	1	0	x	x	x
	64/32	15FFFFH 150000H	0AFFFFH 0A8000H	FSA21	0	1	0	1	0	1	x	x	x
	64/32	14FFFFH 140000H	0A7FFFH 0A0000H	FSA20	0	1	0	1	0	0	x	x	x
	64/32	13FFFFH 130000H	09FFFFH 098000H	FSA19	0	1	0	0	1	1	x	x	x
	64/32	12FFFFH 120000H	097FFFH 090000H	FSA18	0	1	0	0	1	0	x	x	x
	64/32	11FFFFH 110000H	08FFFFH 088000H	FSA17	0	1	0	0	0	1	x	x	x
	64/32	10FFFFH 100000H	087FFFH 080000H	FSA16	0	1	0	0	0	0	x	x	x
	64/32	0FFFFFH 0F0000H	07FFFFH 078000H	FSA15	0	0	1	1	1	1	x	x	x
	64/32	0EFFFFH 0E0000H	077FFFH 070000H	FSA14	0	0	1	1	1	0	x	x	x
	64/32	0DFFFFH 0D0000H	06FFFFH 068000H	FSA13	0	0	1	1	0	1	x	x	x
	64/32	0CFFFFH 0C0000H	067FFFH 060000H	FSA12	0	0	1	1	0	0	x	x	x
	64/32	0BFFFFH 0B0000H	05FFFFH 058000H	FSA11	0	0	1	0	1	1	x	x	x
	64/32	0AFFFFH 0A0000H	057FFFH 050000H	FSA10	0	0	1	0	1	0	x	x	x
	64/32	09FFFFH 090000H	04FFFFH 048000H	FSA9	0	0	1	0	0	1	x	x	x
	64/32	08FFFFH 080000H	047FFFH 040000H	FSA8	0	0	1	0	0	0	x	x	x
	64/32	07FFFFH 070000H	03FFFFH 038000H	FSA7	0	0	0	1	1	1	x	x	x
	64/32	06FFFFH 060000H	037FFFH 030000H	FSA6	0	0	0	1	1	0	x	x	x
	64/32	05FFFFH 050000H	02FFFFH 028000H	FSA5	0	0	0	1	0	1	x	x	x
	64/32	04FFFFH 040000H	027FFFH 020000H	FSA4	0	0	0	1	0	0	x	x	x
	64/32	03FFFFH 030000H	01FFFFH 018000H	FSA3	0	0	0	0	1	1	x	x	x
	64/32	02FFFFH 020000H	017FFFH 010000H	FSA2	0	0	0	0	1	0	x	x	x
	64/32	01FFFFH 010000H	00FFFFH 008000H	FSA1	0	0	0	0	0	1	x	x	x
	64/32	00FFFFH 000000H	007FFFH 000000H	FSA0	0	0	0	0	0	0	x	x	x

[-A85BY, -B85BY] **(1/2)**

Bank	Sector Organization	Address		Sectors Address	Sector Address Table								
					Bank Address Table								
	K bytes / K words	BYTE mode	WORD mode		A20	A19	A18	A17	A16	A15	A14	A13	A12
Bank 2	64/32	3FFFFFH 3F0000H	1FFFFFH 1F8000H	FSA70	1	1	1	1	1	1	x	x	x
	64/32	3EFFFFH 3E0000H	1F7FFFH 1F0000H	FSA69	1	1	1	1	1	0	x	x	x
	64/32	3DFFFFH 3D0000H	1EFFFFH 1E8000H	FSA68	1	1	1	1	0	1	x	x	x
	64/32	3CFFFFH 3C0000H	1E7FFFH 1E0000H	FSA67	1	1	1	1	0	0	x	x	x
	64/32	3BFFFFH 3B0000H	1DFFFFH 1D8000H	FSA66	1	1	1	0	1	1	x	x	x
	64/32	3AFFFFH 3A0000H	1D7FFFH 1D0000H	FSA65	1	1	1	0	1	0	x	x	x
	64/32	39FFFFH 390000H	1CFFFFH 1C8000H	FSA64	1	1	1	0	0	1	x	x	x
	64/32	38FFFFH 380000H	1C7FFFH 1C0000H	FSA63	1	1	1	0	0	0	x	x	x
	64/32	37FFFFH 370000H	1BFFFFH 1B8000H	FSA62	1	1	0	1	1	1	x	x	x
	64/32	36FFFFH 360000H	1B7FFFH 1B0000H	FSA61	1	1	0	1	1	0	x	x	x
	64/32	35FFFFH 350000H	1AFFFFH 1A8000H	FSA60	1	1	0	1	0	1	x	x	x
	64/32	34FFFFH 340000H	1A7FFFH 1A0000H	FSA59	1	1	0	1	0	0	x	x	x
	64/32	33FFFFH 330000H	19FFFFH 198000H	FSA58	1	1	0	0	1	1	x	x	x
	64/32	32FFFFH 320000H	197FFFH 190000H	FSA57	1	1	0	0	1	0	x	x	x
	64/32	31FFFFH 310000H	18FFFFH 188000H	FSA56	1	1	0	0	0	1	x	x	x
	64/32	30FFFFH 300000H	187FFFH 180000H	FSA55	1	1	0	0	0	0	x	x	x
	64/32	2FFFFFH 2F0000H	17FFFFH 178000H	FSA54	1	0	1	1	1	1	x	x	x
	64/32	2EFFFFH 2E0000H	177FFFH 170000H	FSA53	1	0	1	1	1	0	x	x	x
	64/32	2DFFFFH 2D0000H	16FFFFH 168000H	FSA52	1	0	1	1	0	1	x	x	x
	64/32	2CFFFFH 2C0000H	167FFFH 160000H	FSA51	1	0	1	1	0	0	x	x	x
	64/32	2BFFFFH 2B0000H	15FFFFH 158000H	FSA50	1	0	1	0	1	1	x	x	x
	64/32	2AFFFFH 2A0000H	157FFFH 150000H	FSA49	1	0	1	0	1	0	x	x	x
	64/32	29FFFFH 290000H	14FFFFH 148000H	FSA48	1	0	1	0	0	1	x	x	x
	64/32	28FFFFH 280000H	147FFFH 140000H	FSA47	1	0	1	0	0	0	x	x	x
	64/32	27FFFFH 270000H	13FFFFH 138000H	FSA46	1	0	0	1	1	1	x	x	x
	64/32	26FFFFH 260000H	137FFFH 130000H	FSA45	1	0	0	1	1	0	x	x	x
	64/32	25FFFFH 250000H	12FFFFH 128000H	FSA44	1	0	0	1	0	1	x	x	x
	64/32	24FFFFH 240000H	127FFFH 120000H	FSA43	1	0	0	1	0	0	x	x	x
	64/32	23FFFFH 230000H	11FFFFH 118000H	FSA42	1	0	0	0	1	1	x	x	x
	64/32	22FFFFH 220000H	117FFFH 110000H	FSA41	1	0	0	0	1	0	x	x	x
	64/32	21FFFFH 210000H	10FFFFH 108000H	FSA40	1	0	0	0	0	1	x	x	x
	64/32	20FFFFH 200000H	107FFFH 100000H	FSA39	1	0	0	0	0	0	x	x	x
	64/32	1FFFFFH 1F0000H	0FFFFFH 0F8000H	FSA38	0	1	1	1	1	1	x	x	x
	64/32	1EFFFFH 1E0000H	0F7FFFH 0F0000H	FSA37	0	1	1	1	1	0	x	x	x
	64/32	1DFFFFH 1D0000H	0EFFFFH 0E8000H	FSA36	0	1	1	1	0	1	x	x	x
	64/32	1CFFFFH 1C0000H	0E7FFFH 0E0000H	FSA35	0	1	1	1	0	0	x	x	x

[-A85BY, -B85BY] **(2/2)**

Bank	Sector Organization	Address		Sectors Address	Sector Address Table								
					Bank Address Table								
	K bytes / K words	BYTE mode	WORD mode		A20	A19	A18	A17	A16	A15	A14	A13	A12
Bank 2	64/32	1BFFFFH 1B0000H	0DFFFFH 0D8000H	FSA34	0	1	1	0	1	1	x	x	x
	64/32	1AFFFFH 1A0000H	0D7FFFH 0D0000H	FSA33	0	1	1	0	1	0	x	x	x
	64/32	19FFFFH 190000H	0CFFFFH 0C8000H	FSA32	0	1	1	0	0	1	x	x	x
	64/32	18FFFFH 180000H	0C7FFFH 0C0000H	FSA31	0	1	1	0	0	0	x	x	x
	64/32	17FFFFH 170000H	0BFFFFH 0B8000H	FSA30	0	1	0	1	1	1	x	x	x
	64/32	16FFFFH 160000H	0B7FFFH 0B0000H	FSA29	0	1	0	1	1	0	x	x	x
	64/32	15FFFFH 150000H	0AFFFFH 0A8000H	FSA28	0	1	0	1	0	1	x	x	x
	64/32	14FFFFH 140000H	0A7FFFH 0A0000H	FSA27	0	1	0	1	0	0	x	x	x
	64/32	13FFFFH 130000H	09FFFFH 098000H	FSA26	0	1	0	0	1	1	x	x	x
	64/32	12FFFFH 120000H	097FFFH 090000H	FSA25	0	1	0	0	1	0	x	x	x
	64/32	11FFFFH 110000H	08FFFFH 088000H	FSA24	0	1	0	0	0	1	x	x	x
	64/32	10FFFFH 100000H	087FFFH 080000H	FSA23	0	1	0	0	0	0	x	x	x
Bank 1	64/32	0FFFFFH 0F0000H	07FFFFH 078000H	FSA22	0	0	1	1	1	1	x	x	x
	64/32	0EFFFFH 0E0000H	077FFFH 070000H	FSA21	0	0	1	1	1	0	x	x	x
	64/32	0DFFFFH 0D0000H	06FFFFH 068000H	FSA20	0	0	1	1	0	1	x	x	x
	64/32	0CFFFFH 0C0000H	067FFFH 060000H	FSA19	0	0	1	1	0	0	x	x	x
	64/32	0BFFFFH 0B0000H	05FFFFH 058000H	FSA18	0	0	1	0	1	1	x	x	x
	64/32	0AFFFFH 0A0000H	057FFFH 050000H	FSA17	0	0	1	0	1	0	x	x	x
	64/32	09FFFFH 090000H	04FFFFH 048000H	FSA16	0	0	1	0	0	1	x	x	x
	64/32	08FFFFH 080000H	047FFFH 040000H	FSA15	0	0	1	0	0	0	x	x	x
	64/32	07FFFFH 070000H	03FFFFH 038000H	FSA14	0	0	0	1	1	1	x	x	x
	64/32	06FFFFH 060000H	037FFFH 030000H	FSA13	0	0	0	1	1	0	x	x	x
	64/32	05FFFFH 050000H	02FFFFH 028000H	FSA12	0	0	0	1	0	1	x	x	x
	64/32	04FFFFH 040000H	027FFFH 020000H	FSA11	0	0	0	1	0	0	x	x	x
	64/32	03FFFFH 030000H	01FFFFH 018000H	FSA10	0	0	0	0	1	1	x	x	x
	64/32	02FFFFH 020000H	017FFFH 010000H	FSA9	0	0	0	0	1	0	x	x	x
	64/32	01FFFFH 010000H	00FFFFH 008000H	FSA8	0	0	0	0	0	1	x	x	x
	8/4	00FFFFH 00E000H	007FFFH 007000H	FSA7	0	0	0	0	0	0	1	1	1
	8/4	00DFFFH 00C000H	006FFFH 006000H	FSA6	0	0	0	0	0	0	1	1	0
	8/4	00BFFFH 00A000H	005FFFH 005000H	FSA5	0	0	0	0	0	0	1	0	1
	8/4	009FFFH 008000H	004FFFH 004000H	FSA4	0	0	0	0	0	0	1	0	0
	8/4	007FFFH 006000H	003FFFH 003000H	FSA3	0	0	0	0	0	0	0	1	1
	8/4	005FFFH 004000H	002FFFH 002000H	FSA2	0	0	0	0	0	0	0	1	0
	8/4	003FFFH 002000H	001FFFH 001000H	FSA1	0	0	0	0	0	0	0	0	1
	8/4	001FFFH 000000H	000FFFH 000000H	FSA0	0	0	0	0	0	0	0	0	0

Sector Group Address Table

[-A85TY, -B85TY]

Sector group	A20	A19	A18	A17	A16	A15	A14	A13	A12	Size	Sector
SGA0	0	0	0	0	0	0	×	×	×	64K Bytes (1 Sector)	FSA0
SGA1	0	0	0	0	0	1	×	×	×	192K Bytes (3 Sectors)	FSA1 to FSA3
					1	0					
					1	1					
SGA2	0	0	0	1	×	×	×	×	×	256K Bytes (4 Sectors)	FSA4 to FSA7
SGA3	0	0	1	0	×	×	×	×	×	256K Bytes (4 Sectors)	FSA8 to FSA11
SGA4	0	0	1	1	×	×	×	×	×	256K Bytes (4 Sectors)	FSA12 to FSA15
SGA5	0	1	0	0	×	×	×	×	×	256K Bytes (4 Sectors)	FSA16 to FSA19
SGA6	0	1	0	1	×	×	×	×	×	256K Bytes (4 Sectors)	FSA20 to FSA23
SGA7	0	1	1	0	×	×	×	×	×	256K Bytes (4 Sectors)	FSA24 to FSA27
SGA8	0	1	1	1	×	×	×	×	×	256K Bytes (4 Sectors)	FSA28 to FSA31
SGA9	1	0	0	0	×	×	×	×	×	256K Bytes (4 Sectors)	FSA32 to FSA35
SGA10	1	0	0	1	×	×	×	×	×	256K Bytes (4 Sectors)	FSA36 to FSA39
SGA11	1	0	1	0	×	×	×	×	×	256K Bytes (4 Sectors)	FSA40 to FSA43
SGA12	1	0	1	1	×	×	×	×	×	256K Bytes (4 Sectors)	FSA44 to FSA47
SGA13	1	1	0	0	×	×	×	×	×	256K Bytes (4 Sectors)	FSA48 to FSA51
SGA14	1	1	0	1	×	×	×	×	×	256K Bytes (4 Sectors)	FSA52 to FSA55
SGA15	1	1	1	0	×	×	×	×	×	256K Bytes (4 Sectors)	FSA56 to FSA59
SGA16	1	1	1	1	0	0	×	×	×	192K Bytes (3 Sectors)	FSA60 to FSA62
					0	1					
					1	0					
SGA17	1	1	1	1	1	1	0	0	0	8K Bytes (1 Sector)	FSA63
SGA18	1	1	1	1	1	1	0	0	1	8K Bytes (1 Sector)	FSA64
SGA19	1	1	1	1	1	1	0	1	0	8K Bytes (1 Sector)	FSA65
SGA20	1	1	1	1	1	1	0	1	1	8K Bytes (1 Sector)	FSA66
SGA21	1	1	1	1	1	1	1	0	0	8K Bytes (1 Sector)	FSA67
SGA22	1	1	1	1	1	1	1	0	1	8K Bytes (1 Sector)	FSA68
SGA23	1	1	1	1	1	1	1	1	0	8K Bytes (1 Sector)	FSA69
SGA24	1	1	1	1	1	1	1	1	1	8K Bytes (1 Sector)	FSA70

Remark × : V_{IH} or V_{IL}

[-A85BY, -B85BY]

Sector group	A20	A19	A18	A17	A16	A15	A14	A13	A12	Size	Sector
SGA0	0	0	0	0	0	0	0	0	0	8K Bytes (1 Sector)	FSA0
SGA1	0	0	0	0	0	0	0	0	1	8K Bytes (1 Sector)	FSA1
SGA2	0	0	0	0	0	0	0	1	0	8K Bytes (1 Sector)	FSA2
SGA3	0	0	0	0	0	0	0	1	1	8K Bytes (1 Sector)	FSA3
SGA4	0	0	0	0	0	0	1	0	0	8K Bytes (1 Sector)	FSA4
SGA5	0	0	0	0	0	0	1	0	1	8K Bytes (1 Sector)	FSA5
SGA6	0	0	0	0	0	0	1	1	0	8K Bytes (1 Sector)	FSA6
SGA7	0	0	0	0	0	0	1	1	1	8K Bytes (1 Sector)	FSA7
SGA8	0	0	0	0	0	1	×	×	×	192K Bytes (3 Sectors)	FSA8 to FSA10
					1	0					
					1	1					
SGA9	0	0	0	1	×	×	×	×	×	256K Bytes (4 Sectors)	FSA11 to FSA14
SGA10	0	0	1	0	×	×	×	×	×	256K Bytes (4 Sectors)	FSA15 to FSA18
SGA11	0	0	1	1	×	×	×	×	×	256K Bytes (4 Sectors)	FSA19 to FSA22
SGA12	0	1	0	0	×	×	×	×	×	256K Bytes (4 Sectors)	FSA23 to FSA26
SGA13	0	1	0	1	×	×	×	×	×	256K Bytes (4 Sectors)	FSA27 to FSA30
SGA14	0	1	1	0	×	×	×	×	×	256K Bytes (4 Sectors)	FSA31 to FSA34
SGA15	0	1	1	1	×	×	×	×	×	256K Bytes (4 Sectors)	FSA35 to FSA38
SGA16	1	0	0	0	×	×	×	×	×	256K Bytes (4 Sectors)	FSA39 to FSA42
SGA17	1	0	0	1	×	×	×	×	×	256K Bytes (4 Sectors)	FSA43 to FSA46
SGA18	1	0	1	0	×	×	×	×	×	256K Bytes (4 Sectors)	FSA47 to FSA50
SGA19	1	0	1	1	×	×	×	×	×	256K Bytes (4 Sectors)	FSA51 to FSA54
SGA20	1	1	0	0	×	×	×	×	×	256K Bytes (4 Sectors)	FSA55 to FSA58
SGA21	1	1	0	1	×	×	×	×	×	256K Bytes (4 Sectors)	FSA59 to FSA62
SGA22	1	1	1	0	×	×	×	×	×	256K Bytes (4 Sectors)	FSA63 to FSA66
SGA23	1	1	1	1	0	0	×	×	×	192K Bytes (3 Sectors)	FSA67 to FSA69
					0	1					
					1	0					
SGA24	1	1	1	1	1	1	×	×	×	64K Bytes (1 Sector)	FSA70

Remark × : V_{IH} or V_{IL}

Product ID Code (Manufacturer Code / Device Code)

Product ID Code			Input					Output																
			A20 to A12	A6	A1	A0	A–1 Note1	I/O15	I/O14	I/O13	I/O12	I/O11	I/O10	I/O9	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	HEX
Manufacturer Code			×	V_{IL}	V_{IL}	V_{IL}	V_{IL}	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0010H
★ Device code	BYTE mode	-A85TY -B85TY	×	V_{IL}	V_{IL}	V_{IH}	V_{IL}	A–1	High-Z							0	1	0	1	0	0	0	0	50H
		-A85BY -B85BY						A–1	High-Z							0	1	0	1	0	0	1	1	53H
	WORD mode	-A85TY -B85TY	×	V_{IL}	V_{IL}	V_{IH}	×	0	0	1	0	0	0	1	0	0	1	0	1	0	0	0	0	2250H
		-A85BY -B85BY						0	0	1	0	0	0	1	0	0	1	0	1	0	0	1	1	2253H
Sector group protection			SGA	V_{IL}	V_{IH}	V_{IL}	V_{IL}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0001H Note2

Notes 1. A–1 is valid only in the BYTE mode. I/O8 to I/O14 go into a high impedance state in the BYTE mode, and I/O15 is A–1 of the lowest address.

2. If 0001H is output, the sector group is protected. If 0000H is output, the sector group is unprotected.

Remark × : V_{IH} or V_{IL}, SGA : Sector group address

Command Sequence

Command sequence		Bus	1st bus Cycle		2nd bus Cycle		3rd bus Cycle		4th bus Cycle		5th bus Cycle		6th bus Cycle	
		Cycle	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data
Read / Reset [Note1]		1	×××H	F0H	RA	RD	–	–	–	–	–	–	–	–
Read / Reset [Note1]	BYTE mode	3	AAAH	AAH	555H	55H	AAAH	F0H	RA	RD	–	–	–	–
	WORD mode		555H		2AAH		555H							
Program	BYTE mode	4	AAAH	AAH	555H	55H	AAAH	A0H	PA	PD	–	–	–	–
	WORD mode		555H		2AAH		555H							
Program Suspend [Note 2]		1	BA	B0H	–	–	–	–	–	–	–	–	–	–
Program Resume [Note 3]		1	BA	30H	–	–	–	–	–	–	–	–	–	–
Chip Erase	BYTE mode	6	AAAH	AAH	555H	55H	AAAH	80H	AAAH	AAH	555H	55H	AAAH	10H
	WORD mode		555H		2AAH		555H		555H		2AAH		555H	
Sector Erase	BYTE mode	6	AAAH	AAH	555H	55H	AAAH	80H	AAAH	AAH	555H	55H	FSA	30H
	WORD mode		555H		2AAH		555H		555H		2AAH			
Sector Erase Suspend [Note 4]		1	BA	B0H	–	–	–	–	–	–	–	–	–	–
Sector Erase Resume [Note 5]		1	BA	30H	–	–	–	–	–	–	–	–	–	–
Unlock Bypass Set	BYTE mode	3	AAAH	AAH	555H	55H	AAAH	20H	–	–	–	–	–	–
	WORD mode		555H		2AAH		555H							
Unlock Bypass Program [Note 6]		2	×××H	A0H	PA	PD	–	–	–	–	–	–	–	–
Unlock Bypass Reset [Note 6]		2	BA	90H	×××H	00H[Note11]	–	–	–	–	–	–	–	–
Product ID	BYTE mode	3	AAAH	AAH	555H	55H	(BA) AAAH	90H	IA	ID	–	–	–	–
	WORD mode		555H		2AAH		(BA) 555H							
Sector Group Protection [Note 7]		4	×××H	60H	SPA	60H	SPA	40H	SPA	SD	–	–	–	–
Sector Group Unprotect [Note 8]		4	×××H	60H	SUA	60H	SUA	40H	SUA	SD	–	–	–	–
Query [Note 9]	BYTE mode	1	AAH	98H	–	–	–	–	–	–	–	–	–	–
	WORD mode		55H											
Extra One Time Protect	BYTE mode	3	AAAH	AAH	555H	55H	AAAH	88H	–	–	–	–	–	–
Sector Entry	WORD mode		555H		2AAH		555H							
Extra One Time Protect	BYTE mode	4	AAAH	AAH	555H	55H	AAAH	A0H	PA	PD	–	–	–	–
Sector Program [Note 10]	WORD mode		555H		2AAH		555H							
Extra One Time Protect	BYTE mode	6	AAAH	AAH	555H	55H	AAAH	80H	AAAH	AAH	555H	55H	EOTPSA	30H
Sector Erase [Note 10]	WORD mode		555H		2AAH		555H		555H		2AAH			
Extra One Time Protect	BYTE mode	4	AAAH	AAH	555H	55H	AAAH	90H	xxxH	00H	–	–	–	–
Sector Reset [Note 10]	WORD mode		555H		2AAH		555H							
Extra One Time Protect Sector Protection [Note 10]		4	×××H	60H	EOTPSA	60H	EOTPSA	40H	EOTPSA	SD	–	–	–	–

Notes 1. Both these read / reset commands reset the device to the read mode.

2. Programming is suspended if B0H is input to the bank address being programmed to in a program operation.

3. Programming is resumed if 30H is input to the bank address being suspended to in a program-suspend operation.

4. Erasure is suspended if B0H is input to the bank address being erased in a sector erase operation.

5. Erasure is resumed if 30H is input to the bank address being suspended in a sector-erase-suspend operation.

6. Valid only in the Unlock Bypass mode.

7. Valid only in /RESET = V_{ID} (except in the Extra One Time Protect Sector mode).

8. The command sequence that protects a sector group is excluded.

9. Only A0 to A6 are valid as an address.

10. Valid only in the Extra One Time Protect Sector mode.

11. This command can be used even if this data is F0H.

Remarks 1. The system should generate the following address pattern :

WORD mode : 555H or 2AAH (A10 to A0)

BYTE mode : AAAH or 555H (A10 to A0, and A–1)

2. RA : Read address

RD : Read data

IA : Address input as follows

××00H (to read the manufacturer code)

××02H (to read the device code in the BYTE mode)

××01H (to read the device code in the WORD mode)

ID : Code output. For the manufacture code, device code and sector group protection information, refer to the **Product ID code**.

PA : Program address

PD : Program data

FSA : Erase sector address. The sector to be erased is selected by the combination of A20 to A12. Refer to the **Sector Organization / Sector Address Table**.

BA : Bank address. Refer to the **Sector Organization / Sector Address Table**.

★ SPA : Sector group address to be protected or protection-verified. Set the sector group address (SGA) and (A6, A1, A0) = (V_{IL}, V_{IH}, V_{IL}).
Sector group protection can be set for each sector group address. For details, refer **DUAL OPRATION FLASH MEMORY 32M BITS A SERIES Information (M14914E)**.
For the sector group address, refer to the **Sector Group Address Table**.

★ SUA : Sector group address to be unprotected or unprotection-verified. Set the sector group address (SGA) and (A6, A1, A0) = (V_{IH}, V_{IH}, V_{IL}).
Sector group unprotect is performed for all sector group using a single command, however, unprotect verification must be performed for each sector group address. For details, refer to **DUAL OPRATION FLASH MEMORY 32M BITS A SERIES Information (M14914E)**.
For the sector group address, refer to the **Sector Group Address Table**.

EOTPSA : Extra One Time Protect Sector area addresses. These addresses are 3F0000H to 3FFFFFH (BYTE mode) / 1F8000H to 1FFFFFH (WORD mode) for top boot, and 000000H to 00FFFFH (BYTE mode) / 000000H to 007FFFH (WORD mode) for bottom boot.

SD : Data for verifying whether sector groups read from the address specified by SPA, SUA, EOTPSA are protected or unprotected.

3. The sector group address is don't care except when a program / erase address or read address are selected.

4. For the operation of bus, refer **DUAL OPRATION FLASH MEMORY 32M BITS A SERIES Information (M14914E)**.

5. × of address bit indicates V_{IH} or V_{IL}.

BUS OPERATIONS, COMMANDS, HARDWARE SEQUENCE FLAGS, HARDWARE DATA PROTECTION

Refer to **DUAL OPERATION FLASH MEMORY 32M BITS A SERIES Information (M14914E).**

Electrical Characteristics

Before turning on power, input GND ± 0.2 V to the /RESET pin until $V_{CC} \geq V_{CC}$ (MIN.).

Absolute Maximum Ratings

Parameter	Symbol	Condition		Rating	Unit
Supply voltage	V_{CC}	with respect to GND		–0.5 to +4.0	V
Input / Output voltage	V_T	with respect to GND	/WP(ACC), /RESET	–0.5 Note 1 to +13.0	V
			except /WP(ACC), /RESET	–0.5 Note 1 to V_{CC} + 0.4 (4.0 V MAX.) Note 2	
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–55 to +125	°C

Notes 1. –2.0 V (MIN.) (pulse width ≤ 20 ns)

2. V_{CC} + 2.0 V (MAX.) (pulse width ≤ 20 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Test condition	-A85TY, -A85BY			-B85TY, -B85BY			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply voltage	V_{CC}		3.0		3.6	2.7		3.3	V
Operating ambient temperature	T_A		–40		+85	–40		+85	°C

Capacitance (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V			TBD	pF
Input / Output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			TBD	pF

Remarks 1. V_{IN} : Input voltage, $V_{I/O}$: Input / Output voltage

2. These parameters are not 100% tested.

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

Parameter			Symbol	Test condition		MIN.	TYP.	MAX.	Unit
High level input voltage			V_{IH}			2.4		V_{CC}+0.3	V
Low level input voltage			V_{IL}			– 0.3		+0.5	V
High level output voltage			V_{OH}	I_{OH} = –500 μA, V_{CC} = V_{CC} (MIN.)		2.4			V
Low level output voltage			V_{OL}	I_{OL} = +1.0 mA, V_{CC} = V_{CC} (MIN.)				0.4	V
Input leakage current			I_{LI}			–1.0		+1.0	μA
I/O leakage current			I_{LO}			–1.0		+1.0	μA
Power supply current	Read	BYTE mode	I_{CC1}	V_{CC} = V_{CC} (MAX.), /CE = V_{IL}, /OE = V_{IH}	t_{CYCLE} = 5 MHz		10	16	mA
					t_{CYCLE} = 1 MHz		2	4	
		WORD mode			t_{CYCLE} = 5 MHz		10	16	
					t_{CYCLE} = 1 MHz		2	4	
	Program, Erase		I_{CC2}	V_{CC} = V_{CC} (MAX.), /CE = V_{IL}, /OE = V_{IH}			15	30	mA
	Standby		I_{CC3}	V_{CC} = V_{CC}(MAX.), /CE = /RESET = /WP(ACC) = V_{CC} ± 0.3 V, /OE = V_{IL}			0.2	5	μA
	Standby / Reset		I_{CC4}	V_{CC} = V_{CC} (MAX.), /RESET = GND ± 0.2 V			0.2	5	μA
	Automatic sleep mode		I_{CC5}	V_{IH} = V_{CC} ± 0.2 V, V_{IL} = GND ± 0.2 V			0.2	5	μA
	Read during programming		I_{CC6}	V_{IH} = V_{CC} ± 0.2 V, V_{IL} = GND ± 0.2 V			21	45	mA
	Read during erasing		I_{CC7}	V_{IH} = V_{CC} ± 0.2 V, V_{IL} = GND ± 0.2 V			21	45	mA
	Programming during suspend		I_{CC8}	/CE = V_{IL}, /OE = V_{IH}, Automatic programming during suspend			17	35	mA
	Accelerated programming		I_{ACC}	/WP (ACC) pin			5	10	mA
				V_{CC}			15	30	
/RESET high level input voltage			V_{ID}	High Voltage is applied		11.5		12.5	V
Accelerated programming voltage			V_{ACC}	High Voltage is applied		8.5		9.5	V
Low V_{CC} lock-out voltage[Note]			V_{LKO}					1.7	V

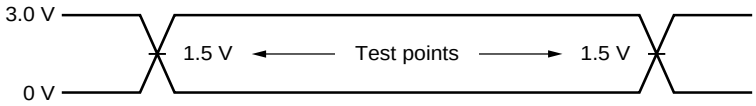
Note When V_{CC} is equal to or lower than V_{LKO}, the device ignores all write cycles. Refer to **DUAL OPERATION FLASH MEMORY 32M BITS A SERIES Information (M14914E).**

Remark These DC characteristics are in common regardless of product classification.

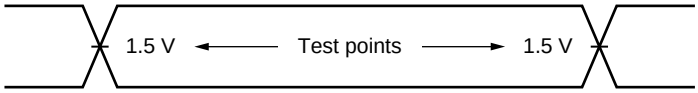
AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

AC Test Conditions

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform



Output Load

1 TTL + 30 pF

Read Cycle

	Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit	Note
	Read cycle time	t_{RC}		85			ns	
	Address access time	t_{ACC}	/CE = /OE = V_{IL}			85	ns	
	/CE access time	t_{CE}	/OE = V_{IL}			85	ns	
	/OE access time	t_{OE}	/CE = V_{IL}			40	ns	
	Output disable time	t_{DF}	/OE = V_{IL} or /CE = V_{IL}			30	ns	
	Output hold time	t_{OH}		0			ns	
	/RESET pulse width	t_{RP}		500			ns	
	/RESET hold time before read	t_{RH}		50			ns	
	/RESET low to read mode	t_{READY}				20	μs	
	/CE low to /BYTE low, high	t_{ELFL}/t_{ELFH}				5	ns	
	/BYTE low output disable time	t_{FLQZ}				30	ns	
	/BYTE high access time	t_{FHQV}		85			ns	
★	/OE low level time from /WE high level	t_{OEH}		20			ns	

Remark t_{DF} is the time from inactivation of /CE or /OE to high impedance state output.

Write Cycle (Program / Erase) **(1/2)**

Parameter		Symbol	MIN.	TYP.	MAX.	Unit	Note
Write cycle time		t_{WC}	85			ns	
Address setup time (/WE to address)		t_{AS}	0			ns	
Address setup time (/CE to address)		t_{AS}	0			ns	
Address hold time (/WE to address)		t_{AH}	45			ns	
Address hold time (/CE to address)		t_{AH}	45			ns	
Input data setup time		t_{DS}	35			ns	
Input data hold time		t_{DH}	0			ns	
/OE hold time	Read	t_{OEH}	0			ns	
	Toggle bit, Data polling		10				
Read recovery time before write (/OE to /CE)		t_{GHEL}	0			ns	
Read recovery time before write (/OE to /WE)		t_{GHWL}	0			ns	
/WE setup time (/CE to /WE)		t_{WS}	0			ns	
/CE setup time (/WE to /CE)		t_{CS}	0			ns	
/WE hold time (/CE to /WE)		t_{WH}	0			ns	
/CE hold time (/WE to /CE)		t_{CH}	0			ns	
Write pulse width		t_{WP}	35			ns	
/CE pulse width		t_{CP}	35			ns	
Write pulse width high		t_{WPH}	30			ns	
/CE pulse width high		t_{CPH}	30			ns	
Byte programming operation time		t_{BPG}		9	200	μs	
Word programming operation time		t_{WPG}		11	200	μs	
Sector erase operation time	4K words sector	t_{SER}		0.3	1.0	s	1,2
	32K words sector			0.5	1.5		
	4K words sector			0.5	3.0		1,3
	32K words sector			0.7	5.0		
Chip erase operation time		t_{CER}		33.9	102.5	s	1,2
				48.1	339		1,3
Accelerated programming time		t_{ACCPG}		7	150	μs	
Program / erase cycle			300,000			cycle	
V_{CC} setup time		t_{VCS}	50			μs	
RY (/BY) recovery time		t_{RB}	0			ns	
/RESET pulse width		t_{RP}	500			ns	
/RESET high-voltage (V_{ID}) hold time from high of RY(/BY) when sector group is temporarily unprotect		t_{RRB}	20			μs	
/RESET hold time		t_{RH}	50			ns	

Notes 1. The preprogramming time prior to the erase operation is not included.

2. Program / erase cycle : 100,000 cycles

3. Program / erase cycle : 300,000 cycles

Write Cycle (Program / Erase) **(2/2)**

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Note
From completion of automatic program / erase to data output time	t_{EOE}			85	ns	
RY (/BY) delay time from valid program or erase operation	t_{BUSY}			90	ns	
Address setup time to /OE low in toggle bit	t_{ASO}	15			ns	
Address hold time to /CE or /OE high in toggle bit	t_{AHT}	0			ns	
/CE pulse width high for toggle bit	t_{CEPH}	20			ns	
/OE pulse width high for toggle bit	t_{OEPH}	20			ns	
Voltage transition time	t_{VLHT}	4			μs	1
Rise time to V_{ID} (/RESET)	t_{VIDR}	500			ns	2
Rise time to V_{ACC} (/WP(ACC))	t_{VACCR}	500			ns	1
Erase timeout time	t_{TOW}	50			μs	3
Erase suspend transition time	t_{SPD}			20	μs	3

Notes 1. Sector group protection and accelerated mode only.

2. Sector group protection only.

3. Table only.

Write operation (Erase / Program) Performance

Parameter	Description		MIN.	TYP.	MAX.	Unit	Note
Sector erase time	The preprogramming time prior to the erase operation is not included	4K words sector		0.3	1.0	s	1
		32K words sector		0.5	1.5		
		4K words sector		0.5	3.0	s	2
		32K words sector		0.7	5.0		
Chip erase time	The preprogramming time prior to the erase operation is not included			33.9	102.5	s	1
				48.1	339		2
Byte programming time	Excludes system-level overhead			9	200	μs	
Word programming time	Excludes system-level overhead			11	200	μs	
Chip programming time	Excludes system-level overhead	BYTE mode		40		s	
		WORD mode		25			
Accelerated programming time	Excludes system-level overhead			7	150	μs	
Program / erase cycle			300,000			cycle	

Notes 1. Program / erase cycle : 100,000 cycles

2. Program / erase cycle : 300,000 cycles

TIMING CHARTS, FLOW CHARTS

Refer to **DUAL OPERATION FLASH MEMORY 32M BITS A SERIES Information (M14914E).**

CFI Code List **(1/2)**

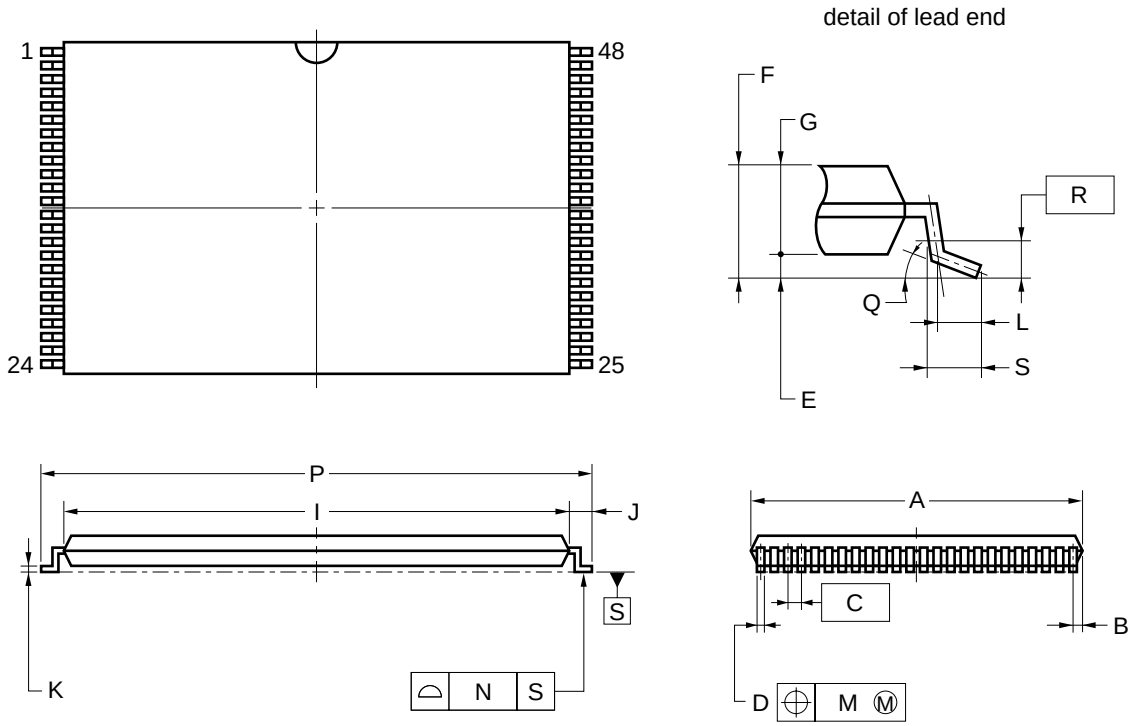
Address A6 to A0	Data I/O15 to I/O0	Description
10H	0051H	"QRY" (ASCII code)
11H	0052H	
12H	0059H	
13H	0002H	Main command set
14H	0000H	2 : AMD/FJ standard type
15H	0040H	Start address of PRIMARY table
16H	0000H	
17H	0000H	Auxiliary command set
18H	0000H	00H : Not supported
19H	0000H	Start address of auxiliary algorithm table
1AH	0000H	
1BH	0027H	Minimum V_{CC} voltage (program / erase) I/O7 to I/O4 : 1 V/bit I/O3 to I/O0 : 100 mV/bit
1CH	0036H	Maximum V_{CC} voltage (program / erase) I/O7 to I/O4 : 1 V/bit I/O3 to I/O0 : 100 mV/bit
1DH	0000H	Minimum V_{PP} voltage
1EH	0000H	Maximum V_{PP} voltage
1FH	0004H	Typical word program time (2^N μs)
20H	0000H	Typical buffer program time (2^N μs)
21H	000AH	Typical sector erase time (2^N ms)
22H	0000H	Typical chip erase time (2^N ms)
23H	0005H	Maximum word program time (typical time × 2^N)
24H	0000H	Maximum buffer program time (typical time × 2^N)
25H	0004H	Maximum sector erasing time (typical time × 2^N)
26H	0000H	Maximum chip erasing time (typical time × 2^N)
27H	0016H	Capacity (2^N Bytes)
28H	0002H	I/O information
29H	0000H	2 : ×8/×16-bit organization
2AH	0000H	Maximum number of bytes when two banks are programmed (2^N)
2BH	0000H	
2CH	0002H	Type of erase block
2DH	0007H	Information about erase block 1
2EH	0000H	bit0 to bit15 : y = number of sectors
2FH	0020H	bit16 to bit31 : z = size
30H	0000H	(Z × 256 Bytes)

CFI Code List **(2/2)**

Address A6 to A0	Data I/O15 to I/O0	Description
31H	003EH	Information about erase block 2
32H	0000H	bit0 to bit15 : y = number of sectors
33H	0000H	bit16 to bit31 : z = size
34H	0001H	(z × 256 Bytes)
40H	0050H	"PRI" (ASCII code)
41H	0052H	
42H	0049H	
43H	0031H	Main version (ASCII code)
44H	0032H	Minor version (ASCII code)
45H	0000H	Address during command input 00H : Necessary 01H : Unnecessary
46H	0002H	Temporary erase suspend function 00H : Not supported 01H : Read only 02H : Read / Program
47H	0001H	Sector group protection 00H : Not supported 01H : Supported
48H	0001H	Temporary sector group protection 00H : Not supported 01H : Supported
49H	0004H	Sector group protection algorithm
4AH	00xxH	Number of sectors of bank 2 00H : Not supported 30H : μPD29F032203AL-Y
4BH	0000H	Burst mode 00H : Not supported
4CH	0000H	Page mode 00H : Not supported
4DH	0085H	Minimum V_{ACC} voltage I/O7 to I/O4 : 1 V/bit I/O3 to I/O0 : 100 mV/bit
4EH	0095H	Maximum V_{ACC} voltage I/O7 to I/O4 : 1 V/bit I/O3 to I/O0 : 100 mV/bit
4FH	00xxH	Boot organization 02H : Bottom boot (-A85BY, -B85BY) 03H : Top boot (-A85TY, -B85TY)
50H	0001H	Temporary program suspend function 00H : Not supported 01H : Supported

Package Drawings

48-PIN PLASTIC TSOP (I) (12x20)



NOTES

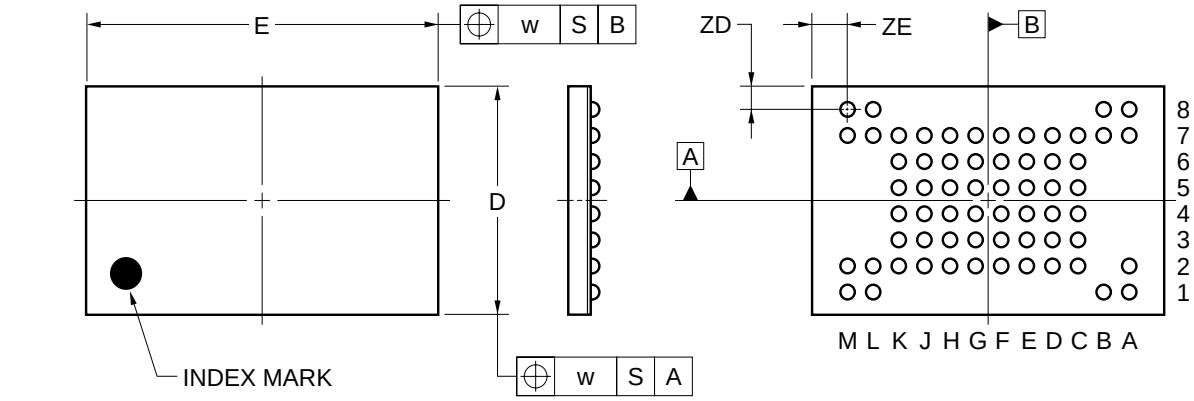
1) Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

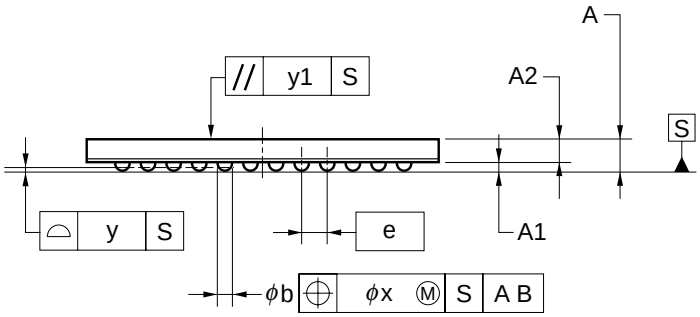
2) "A" excludes mold flash. (Includes mold flash : 12.4 mm MAX.)

ITEM	MILLIMETERS
A	12.0±0.1
B	0.45 MAX.
C	0.5 (T.P.)
D	0.22±0.05
E	0.1±0.05
F	1.2 MAX.
G	1.0±0.05
I	18.4±0.1
J	0.8±0.2
K	0.145±0.05
L	0.5
M	0.10
N	0.10
P	20.0±0.2
Q	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
R	0.25
S	0.60±0.15

S48GZ-50-MJH-1

63-PIN TAPE FBGA (11x7)





ITEM	MILLIMETERS
D	7.00±0.10
E	11.00±0.10
w	0.20
A	0.97±0.10
A1	0.27±0.05
A2	0.70
e	0.80
b	0.45±0.05
x	0.08
y	0.10
y1	0.20
ZD	0.70
ZE	1.10

P63F9-80-BS2

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD29F032203AL-Y.

Types of Surface Mount Device

μPD29F032203ALGZ-MJH : 48-pin PLASTIC TSOP(I) (12 × 20) (Normal bent)
μPD29F032203ALF9-BS2 : 63-pin TAPE FBGA (11 × 7)

Revision History

Edition/ Date	Page		Type of revision	Location	Description (Previous edition -> This edition)
	This edition	Previous edition			
5th edition/ Sep.2002	p.13	p.13	Modification	Product ID Code	Device code(Byte mode):I/O15 = Hi-Z→A–1
	p.16	p.15	Modification	Command Sequence	Remark 2 : SPA, SUA
	p.20	p.19	Addition	Read Cycle	t_{OEH}

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Related Documents

Document Name	Document Number
DUAL OPERATION FLASH MEMORY 32M BITS A SERIES Information	M14914E

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