ANALOG DEVICES

Multiport Register File

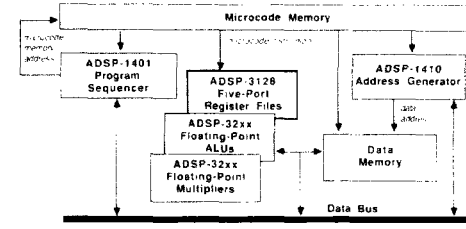
ADSP-3128

FEATURES

128 × 16 or 64 × 32 Register File Organization
Five Ports
  Two Input
  Two Output
  One Bidirectional
Cascadable Horizontally and Vertically
50ns Cycle Time from Single 1× Clock
22ns Clock-to-Valid-Output (Registered)
35ns Address-to-Valid-Output (Transparent)
Flexible Latching Modes at Address and Data Ports:
  Transparent, Latched, Registered
Prioritized Write Ports
Write Flow-Through Control at Each Write Port
Write Inhibit Control on Each Write Port
Correctly Pipelined Bank Select and Port Select
Register-to-Register Transfers
Three-State Outputs
Fully Static Operation
1.75W Power Dissipation in Low-Power TTL-Compatible CMOS
144-Pin Grid Array

APPLICATIONS

High-Speed Temporary Data Storage in
  Digital Signal Processing
  Numeric Processing
  Graphics
Floating-Point and Fixed-Point



Word-Slice™ Floating-Point Microcoded System using ADSP-3128 Multiport Register Files

GENERAL DESCRIPTION

The ADSP-3128 Multiport Register File is a versatile data storage component that can greatly expand the computational bandwidth of a fast-arithmetic processor. (See Figure 1 for the ADSP-3128's Functional Block Diagram.) The ADSP-3128 also simplifies processor design by permitting flexible data routing through its five 16-bit data ports: two input ports, two output ports, and a bidirectional port. This Register File complements the floating-point and fixed-point multipliers and ALUs available from Analog Devices. Because of its flexibility, however, it has application in a broad range of processor designs.

The ADSP-3128 is configurable via a control pin as either a 128 × 16 Register File or a 64 × 32 Register File. In the Single-Precision 128 × 16 configuration, the ADSP-3128 is best suited for fixed-point and single-precision (32-bit) floating-point data storage. For single-precision floating-point, two Register Files should be used "horizontally" yielding 128 words of 32-bit storage. The 64 × 32 Double-Precision configuration is intended for double-precision (64-bit) floating-point, again with two Register Files in a horizontal architecture. In this Double-Precision mode, the Register Files will each transfer 16-bits in each phase of the clock, 32-bits of data per port in a one-cycle write or read operation. Microcode need only be applied to the Register File at its single clock's 1× cycle rate.

To accommodate critical system timing requirements, the ADSP-3128 offers a variety of latching modes on both data and address ports. The prioritized write data ports have control lines that define the input data latching mode for Single-Precision as (a) latched on clock HI, (b) transparent, or (c) registered on the clock's falling edge. However loaded, data can also be held at the input latches for subsequent cycles.

In *Single-Precision mode*, the Multiport Register File's five ports allow six 16-bit data transfer operations per cycle. The input and output latches transfer data to and from the RAM using effectively 16-bit internal buses. The bidirectional Edata-Port can be directly controlled to either (a) write, (b) read, (c) both write and read in a single cycle, or (d) perform two reads in a single cycle. Normal operation allows up to three 16-bit writes in clock HI and three 16-bit reads in clock LO per cycle. However, additional reads can be made in clock HI in lieu of writes, allowing up to six 16-bit reads per cycle. Register-to-register transfers are made via the bidirectional Edata-Port (which can be accomplished in two sequential clock phases).

In *Double-Precision mode*, the Multiport Register File's five ports allow five 32-bit data transfer operations per cycle for a total bandwidth of 160 bits per cycle. The input and output latches transfer data to and from the RAM via 32-bit internal buses. The input data latching modes allow either an Early

Input or a Late Input mode. With Early Input, the Least Significant Word (LSW) is presented to the input data latches in clock HI and the Most Significant Word (MSW) in clock LO. With Late Input, the LSW is presented to the input latches in clock LO and the MSW in clock HI of the next cycle. For data transfers with a slower system bus, the Edata-Port allows both input and output values to be transferred more slowly than the ADSP-3128's clock rate (Edata Slow Input and Edata Slow Read). Register-to-register transfers are made via the bidirectional Edata-Port.

Each *write data* port of the ADSP-3128 provides an independent Write-Flow-Through control that allows data to pass through the Register File without a pipeline delay. Data is written to RAM and read out in the same (extended) clock LO phase. Each input port also has an independent Write-Inhibit control that disables the write operation that normally occurs during clock HI. Write-Inhibit allows cancelling a write based on a condition not known until early in the cycle of an attempted write.

The *read data* ports have control lines that define the output data latching mode for Single-Precision as (a) registered on the clock's rising edge or (b) transparent. In Double-Precision mode, the output data latching modes allow either an Early Read or a Late Read. With Early Read, the LSW can be output in clock LO and the MSW in clock HI of the next cycle. With Late Read, the LSW can be output in clock HI and the MSW in clock LO of the same cycle. Each read data port has an independent tristate control that allows putting that output port into a high-impedance state.

The 7-bit *write address* latches corresponding to the write ports can be defined to latch addresses in one of two ways. Either (a) the write address is latched to an address latch on clock HI, or (b) the address latch is transparent. The 7-bit *read address* latches can be defined to latch addresses in one of two different ways. Either (a) the read address is registered to an address latch on the clock's rising edge, or (b) the address latch is transparent. In Double-Precision mode, there are half as many words that are twice as wide. For Double-Precision addressing, the (unneeded) highest-order address bits function as Port Select lines. Port Select enables or disables individual ports consistent with their pipelines.

Bank Select enables or disables an entire ADSP-3128 consistent with all read and write pipelines. Bank Select and Port Select allow the user to expand register file storage "vertically" for more than 128 single-precision or 64 double-precision data words.

The ADSP-3128 is fabricated in double-metal 1.5μm CMOS. Each chip consumes 1.75W maximum, significantly less than comparable bipolar solutions. The differential between the chip-set's junction temperature and the ambient temperature stays small because of this low power dissipation. Thus, the ADSP-3128 can be safely specified for operation at environmental temperatures over its extended temperature range (−55°C to +125°C ambient).

The ADSP-3128 is available for both commercial and extended temperature ranges. Extended temperature range parts are available with optional high-reliability processing ("PLUS" parts, see Figure 26) or processed fully to MIL-STD-883, Class B. The ADSP-3128 is packaged in a ceramic 144-lead pin grid array.

ADSP-3128 MULTIPORT REGISTER FILE PIN LIST
(Positive True Logic Convention)

Pin Name	Description
DATA PORTS	
$Adata_{15-0}$	Write Adata-Port Input Data
$Bdata_{15-0}$	Write Bdata-Port Input Data
$Cdata_{15-0}$	Read Cdata-Port Output Data
$Ddata_{15-0}$	Read Ddata-Port Output Data
$Edata_{15-0}$	Bidirectional Edata-Port Input and Output Data
ADDRESS PORTS	
$Aadr_{6-0}$	Address Port for Adata-Port Writes (and Cdata-Port for Single-Precision Extra Read)
$Badr_{6-0}$	Address Port for Bdata-Port Writes (and Ddata-Port for Single-Precision Extra Read)
$Cadr_{6-0}$	Address Port for Cdata-Port Reads
$Dadr_{6-0}$	Address Port for Ddata-Port Reads
$Eadr_{6-0}$	Address Port for Edata-Port Writes and Reads and for Register-to-Register Transfers
GENERAL CONTROLS	
BS	Bank Select (Registered or Asynchronous, Depending on Address Port Latches)
DP	Double-Precision Mode (Registered)
ADDRESS LATCH CONTROLS	
Wadctn	Write Address Latch Transparent (Registered)
Radtrn	Read Address Latch Transparent (Registered)
DATA INPUT AND WRITE CONTROLS	
ABlt, ABht	Input Latch Controls for Both Adata-Port and Bdata-Port (Registered)
Elt, Eht	Input Latch Controls for Edata-Port (Registered)
Awinh	Inhibit Write to RAM from Adata-Port Input Latches (Asynchronous)
Bwinh	Inhibit Write to RAM from Bdata-Port Input Latches (Asynchronous)
Ewinh	Inhibit Write to RAM from Edata-Port Input Latches (Asynchronous)
Awft	Write Flow-Through from Adata-Port (Asynchronous)
Bwft	Write Flow-Through from Bdata-Port (Asynchronous)
Ewft	Write Flow-Through from Edata-Port (Asynchronous)
DATA READ AND OUTPUT CONTROLS	
CDtran	Output Latch Controls (Make Transparent) for Both Cdata-Port and Ddata-Port (Registered)
Etran	Output Latch Controls (Make Transparent) for Edata-Port (Registered)
Rfltran	Read Port (Cdata-Port, Ddata-Port, and Edata-Port) Fully Transparent Control for Extra Reads in Single-Precision Mode (Registered)
Eio	Edata-Port Input and Output (In the Same Cycle) in Single-Precision Mode; Edata-Port Slow Read Control in Double-Precision Mode (Registered)
Ctri	Cdata-Port Three-State Control (Asynchronous)
Dtri	Ddata-Port Three-State Control (Asynchronous)
Etri	Edata-Port Three-State Control (Asynchronous)
MISCELLANEOUS	
CLK	Clock
GND	Ground (Four Lines)
V_{DD}	+5V Power Supply (Three Lines)

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FUNCTIONAL DESCRIPTION

The ADSP-3128 Multiport Register File consists of a high-speed static RAM (configurable as either 128 × 16 or 64 × 32) surrounded by the latches and control logic needed for simple system interfacing (see Figure 1). Six internal data paths, all 32 bits wide, connect this RAM with multiplexers (muxes) and latches. Three are read data paths; three are write data paths. Three 7-bit internal address paths connect this RAM with muxes and address latches. These three address paths are time-multiplexed to allow the presentation of six addresses to the RAM per cycle. Hence, up to a total of six reads from and writes to the RAM are possible per cycle. Because of the abundance of data paths, many of which can transfer data twice per cycle, many combinations of six reads and writes are possible.

Three addresses are presented to RAM in clock HI from the Aadr, Badr, and Eadr address latches. Normally in clock HI, these are RAM write addresses. They are prioritized in case of conflict. Three addresses are presented to RAM in clock LO from the Cadr, Dadr, and Eadr address latches. Normally in clock LO, these are RAM read addresses. Three simultaneous reads from the same RAM location are possible for normal, clock LO reads. The EadrPort feeds both a write (clock HI) address latch and a read (clock LO) address latch, which can be independently set to latched or transparent modes.

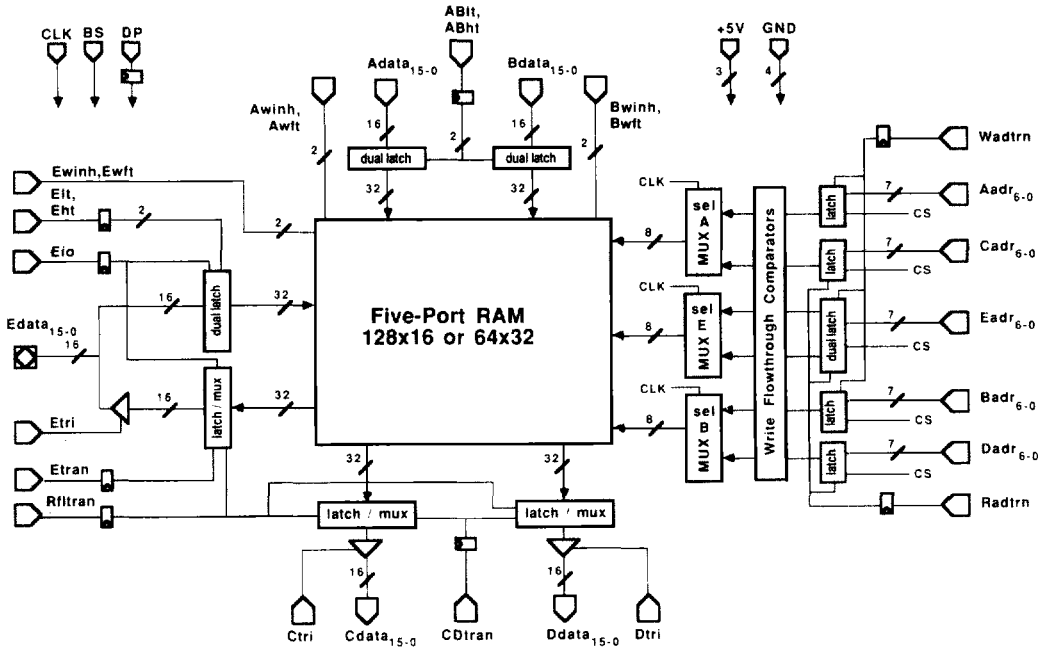


Figure 1. ADSP-3128 Multiport Register File Functional Block Diagram

Physically, the RAM is *always* reading from all three presented address locations to the data latches. For this reason, clock HI addresses can also be used for "extra" reads in clock HI from the RAM to the output latches. In Single-Precision mode, this feature can be enabled by making the output latches transparent for the entire clock cycle (Rfltran HI) to read two 16-bit words per cycle through the Cdata-, Ddata-, and/or Edata-port. The Aadr specifies the word to be read through the Cdata-Port in clock HI, and the Badr, for the Ddata-Port. The Eadr clock HI address latch is selected for any clock HI read to the Edata-Port output latch. (Some restrictions apply to the addresses used in extra reads. See "SP Normal and Extra Reads" below.) If a write to RAM occurs in the clock HI of an extra read, the data written will also be the data read. Thus, in Single-Precision mode, data can be passed through the register file (with write) in the same (extended) clock HI.

Writes to the RAM normally occur in clock HI when Awinh and/or Bwinh and/or Ewinh are LO. Note that data writen in clock HI is available to be read in the same clock cycle. Write data, however, may not be available in a user's system until late in the clock cycle. The Write-Flow-Through controls – Awft, Bwft, and Ewft – allow a write to RAM and a read from the same RAM location to occur in the same clock LO for low-latency data pass-through. Write Flow-Through Comparators monitor the addresses and detect legal Write-Flow-Through operations. Because of these Comparators, the ADSP-3128 can use both a clock HI write address and a clock LO read address to accomplish a Write Flow-Through in a particular (extended) clock LO phase, in spite of the address muxes.

The DP control determines whether the Register File is in Double-Precision mode (HI) or Single-Precision mode (LO). In Single-Precision mode, all data paths between RAM and data latches behave as if they were 16 bits. The data latches also behave like 16-bit latches. The register file is 128 × 16 in Single-Precision mode, and each location is addressed with seven bits. DP can be changed dynamically, consistent with the constraints imposed in the timing diagrams (Figures 4 through 22).

In Double-Precision mode, the Register File is 64 × 32, and each location is addressed with six bits. In Double-Precision mode, all data paths between RAM and data latches are 32 bits, as are the data latches. Writes (32-bit) to the RAM occur in clock HI and reads (32-bit) from the RAM occur in clock LO; the only exception is Write Flow-Through which allows a clock LO 32-bit write to RAM (and read from RAM). Multiplexers between the latches and the 16-bit data ports alternately select Least Significant (LSW) and Most Significant (MSW) 16-bit words. Note that when ADSP-3128 Register Files are configured in horizontal pairs for Double-Precision operation, the LSWs from the pair will make up half the external 64-bit double-precision word and the MSWs the other half.

In Single-Precision mode, the input latches can be configured to latch input data at clock HI, to register input data on the falling clock edge, to be made transparent, or to hold the most recent data. The output latches can be configured to register data from the RAM on the rising clock edge, to be transparent clock LO and latched clock HI, or to be fully transparent through both phases (for extra reads). The bidirectional Edata-Port can be configured to do either one read, one write, two reads, or both a read and a write each cycle. Each read port has an independent three-state enable control.

In Double-Precision mode, the input latches can be configured for an Early Input, a Late Input, a Slow Input on the Edata-Port (for transfers from slow devices), or a hold of the most recent data. Early and Late Inputs are distinguished by a one clock phase difference between when the LSW and MSW are written to the input latches. The output latches can be configured for an Early Read, a Late Read, or a Slow Read on the Edata-Port (for transfers to slow devices). Early and Late Reads are distinguished by a one clock phase difference between when the LSW and MSW are read from the output latches. To accomplish Late Inputs and Early Reads, the latches are transparent for 16 bits of the data transfer, allowing either a direct write of the MSW to RAM or a direct read of the LSW from RAM, respectively.

The write address latches can be made transparent or latched at clock HI. The read address latches can be made transparent or registered at clock HI. In Double-Precision mode, the unused high-order address bit is interpreted as Port Select. Port Select and Bank Select (BS) are treated as part of the address field so that their write-disable and three-state effects properly track the selected pipeline delays.

The output drivers at the Cdata-, Ddata-, and Edata-ports are dual NMOS in structure rather than true CMOS. Their steady-state HI voltage level will be between three and four volts, rather than the V_{DD} characteristic of CMOS drivers. These drivers are faster HI to LO because of shorter voltage swings; the HI to LO transition time is the same as the LO to HI transition. Shorter voltage swings into a given capacitance reduce the peak current drain. Because their peak current drain is reduced, the ADSP-3128 exhibits improved noise immunity to ground spikes and reduced power consumption.

CONTROLS

The ADSP-3128 Register File has 21 control lines. Their functional consequences are summarized in mode Tables I through III.

Most control lines are registered, as indicated in the "Pin List" and in Figure 1. All registered controls meet the timing requirements of Figure 2. The timing requirements for the three asynchronous three-state controls, Ctri, Dtri, and Etri, are shown in Figure 3. The timing for the remaining asynchronous controls are illustrated in the relevant timing diagrams.

CYCLE RATE

The maximum cycle rate for the ADSP-3128 is t_{CLK}, which presumes that all read data is registered. For Double-Precision reads, only Late Reads meet this requirement. The cycle rate for the Register File will have to be extended if any reads are transparent, for Write Flow-Through, for Single-Precision Write-Plus-Extra-Read, or for most Register-to-Register Transfers.

The cycle rate to encompass Write Flow-Through when all read data is registered is t_{CLKFT}. Clock LO will also have to be a minimum of t_{LOWR}.

If all addresses are latched or registered, all write data is latched, and *any* reads are transparent (DP Early Reads), then the maximum cycle rate for the ADSP-3128 will be t_{CLKS} to accommodate the output delays from transparent reads. (In Single-Precision mode, the clock *can* be run faster, with output data allowed to slide into the next clock phase. The user, however, would have to clock the output data externally by the next falling clock edge.) The cycle rate to encompass Write Flow-Through or SP Write-Plus-Extra-Read when all addresses are latched or registered, all write data is latched, and *any* reads are transparent is t_{CLKSFT}. Clock LO will also have to be a minimum of t_{LOWR} for Write Flow-Through and clock HI will have to be a minimum of t_{HIER} for Write-Plus-Extra-Read.

BS	DP	AB & Elt	AB & Eht	A & B & Einh	A & B & Ewft	Description
0	X	X	X	X	X	Disable chip (consistent with pipelines) but advance pipelines with clock cycle
1	0	0	0	X	X	Register write data at A & B or Edata input latches on falling edge
1	0	0	1	X	X	Hold most recent data at A & B or Edata input latches for the next cycle
1	0	1	0	X	X	Latch write data at A & B or Edata input latches at clock HI
1	0	1	1	X	X	Make transparent A & B or Edata input latches
1	X	X	X	0	X	Allow write to RAM from the A, B, and Edata input latches
1	X	X	X	1	X	Inhibit write to RAM from the A, B, and Edata input latches
1	0	X	X	0	0	Normal write to RAM from the A or B or Edata input latches during clock HI
1	0	X	X	X	1	Flow-through write (transparent) to RAM from the A or B or Edata input latches during clock LO when write/read addresses are equal
1	1	0	0	X	X	Early Input to A & B or Edata input latches: register LSW on falling edge to input latches and latch MSW to input latches in clock HI
1	1	0	1	X	0	Late Input to A & B or Edata input latches: latch LSW to input latches in clock HI and make input latches transparent for MSW in clock HI
1	1	0	0	X	1	Undefined
1	1	1	X	X	X	Hold most recent data at A & B or Edata input latches for the next cycle
1	1	1	1→0	X	X	Edata Slow Input: register LSW to Edata input latch on next falling edge (Eht only)
1	1	1	0→1	X	X	Edata Slow Input: register MSW to Edata input latch on next falling edge (Eht only)

Table I. ADSP-3128 Summary of Data Input and Write Control Modes

BS	DP	CD & Etran	Rfltran	C & D & Etri	Eio	Description
0	X	X	X	X	X	Disable chip (consistent with pipelines) but advance pipelines with clock cycle
1	X	X	X	0	X	Drive data from output latches through C or D or Edata-Port
1	X	X	X	1	X	Three-state (high impedance) output C or D or Edata-Port
1	0	0	X	X	X	Register data from RAM to C & D or Edata output latches on rising edge
1	0	1	0	X	X	C & D or Edata output latches are transparent clock LO latched clock HI
1	0	1	1	X	0	C & D or Edata RAM output latches are fully transparent for both phases. If Awinh/Bwinh/Ewinh = 1, an additional read(s) can be performed at C/D/Edata, respectively
1	0	X	X	X	0	Edata-Port is configured for one read, one write, or two reads per cycle
1	0	X	X	X	1	Edata-Port is configured for both a read and a write every cycle; read Eadr is registered on falling edge and write Eadr is registered on rising edge
1	1	0	0	X	0	Configured for Late Read at C&D or Edata-Port: register LSW & MSW from RAM to output latches on rising edge; output LSW in clock HI, output MSW on next clock LO
1	1	1	0	X	0	Configured for Early Read at C&D or Edata-Port: output LSW from RAM through transparent output latches in clock LO; latch MSW to output latches and output in clock HI
1	1	0	0	X	1	Configured for Edata Slow Read: hold RAM read data at Edata output latch; output LSW at clock HI
1	1	1	0	X	1	Configured for Edata Slow Read: hold RAM read data at Edata output latch; output MSW at clock HI
1	1	X	1	X	X	Undefined

Table II. ADSP-3128 Summary of Data Read and Output Control Modes

BS	DP	Wadtrn	Radtrn	A/B/C/D/Eadr$_6$ (Port Select)	Description
0	X	X	X	X	Disable chip (consistent with pipelines) but advance pipelines with clock cycle
1	X	0	X	X	Latch A or B or Eadr write addresses at clock HI*
1	X	1	X	X	A or B or Eadr write address latches are transparent*
1	X	X	0	X	Register C or D or Eadr read address latches on the rising edge*
1	X	X	1	X	C or D or Eadr read address latches are transparent*
X	1	X	X	0	Disable A/B/C/D/Edata-Port
1	1	X	X	1	Enable A/B/C/D/Edata-Port

*Note: Eio = 1 overrides Wadtrn and Radtrn at the Eadr-Port (only). That is, when Eio = 1, Eadr write addresses are registered on rising edges and read addresses are registered on falling edges, regardless of the state of Wadrn and Radtrn. The other four address ports are unaffected by Eio and always behave as described in this table.

Table III. ADSP-3128 Summary of Address Control Modes

If at least one address *or* one data write is transparent *and* at least one data read is transparent (DP Early Read), then the ADSP-3128's cycle time will have to be extended to t_{CLKA} to accommodate transparent setup times and output delays. If any Write Flow-Throughs or SP Write-Plus-Extra-Reads are attempted, the cycle time will be t_{CLKAFT} when at least one address *or* one data write is transparent *and* at least one data read is transparent. Clock LO will also have to be a minimum of t_{LOWR} for Write Flow-Through and clock HI will have to be a minimum of t_{HIER} for Write-Plus-Extra-Read.

	All reads clocked	All addresses latched or registered, all writes latched, and at least one read transparent	At least one address or write transparent, and at least one read transparent
No Write Flow-Throughs or SP Write Plus Extra Reads	t_{CLK}	t_{CLKS}	t_{CLKA}
Some Write Flow Throughs or SP Write-Plus Extra Reads	t_{CLKFT}	t_{CLKSFT}	t_{CLKAFT}

Table IV. ADSP-3128 Cycle Times

Register-to-register transfers are accomplished by driving the source through the Edata-Port and reading that data back through the Edata-Port's input latch. Therefore the ADSP-3128's cycle rate must allow for both data output delay and input setup time.

Single-Precision register-to-register transfers in Single I/O Per Cycle Mode (Eio = 0) can be accomplished at the fastest specified clock rate, t_{CLK}, under the following conditions: clocked read address, transparent read, and transparent write. This works because ($t_{ODRT} + t_{DST}$)<t_{CLK}. In general, for Single-Precision *transparent inputs* (when Eio = 0), the maximum clock cycle time must be equal to or greater than the sum of the chosen data output delay, $t_{OD?T}$, and t_{DST}, the setup time for transparent writes. (See Figure 10.)

If Single-Precision inputs in Single I/O Per Cycle Mode (Eio = 0) are *latched*, similar requirements apply to clock LO, since both data output delay and input setup must be completed in that clock phase. That is, for latched inputs (when Eio = 0), clock LO must be equal to or greater than the sum of the chosen (transparent) data output delay, $t_{OD?T}$, and t_{DSR}, the setup time for the Edata-Port's input latch. (See Figure 9.)

If Single-Precision inputs in Double I/O Per Cycle Mode (Eio = 1) are *latched*, clock LO must be long enough so that clock LO $\geq(t_{ODRT} + t_{DSR})$. (See Figure 11.) If Single-Precision inputs in Double I/O Per Cycle Mode (Eio = 1) are *transparent*, clock HI must be long enough so that clock HI $\geq(t_{ODC} + t_{DST})$. (See Figure 12.)

The minimum cycle rate to accommodate Double-Precision register-to-register transfers depends on the chosen timing mode. For Early Read/Late Write, there are two requirements: clock LO $\geq$(transparent output delay $+ t_{DSR}$) and clock HI $\geq(t_{ODC} + t_{DST})$. (See Figure 19.) For Late Read/Early Write the requirements are the same for both clock LO and clock HI: clock LO $\geq(t_{ODC} + t_{DSR})$ and clock HI $\geq(t_{ODC} + t_{DSR})$. (See Figure 20.) That in turn implies a minimum clock rate $\geq 2*(t_{ODC} + t_{DSR})$.

ADDRESS LATCHES FOR BOTH SINGLE- AND DOUBLE-PRECISION MODES

The three read (clock HI) address latches hold the seven bits required for Register File addressing and Port Select, and also Bank Select. Radtrn controls whether these three latches are transparent or latched. When Radtrn is HI, addresses presented at the read address ports are transferred directly to the RAM with no pipeline delay. When Radtrn is LO, addresses presented at the read address ports are registered on the rising edge of the clock, to be used during the next clock LO.

The three write (clock LO) address latches hold the seven bits required for Register File addressing and Port Select, and also Bank Select. Wadtrn controls whether these three latches are transparent or latched. When Wadtrn is HI, addresses presented at the read address ports are transferred directly to the RAM with no pipeline delay. When Wadtrn is LO, addresses presented at the read address ports are latched on the rising edge of the clock, to be used immediately during the next clock HI.

Both Radtrn and Wadtrn latch controls are registered and affect the configuration of the address latches on the rising clock edge in which they are registered. They remain in effect until the next rising edge.

Transparent addresses must be valid at least t_{AST} before the end of the phase in which they are used. (See Figures 3-7, 9-17, 19, and 20.) The setup time for latched or registered addresses is t_{ASR}. All addresses must be held valid t_{AH} after the end of the phase in which they are asserted.

Output delays for transparent data reads from transparent addresses are referenced from address valid. To a limited degree, transparent read addresses can be setup in the phase *before* the actual RAM read while maintaining the specified relationship between address valid and data valid (t_{ODTT}). The maximum usable setup for transparent addresses is $-t_{ASTE}$ prior to the RAM read phase (note that t_{ASTE} is negative). Setting up the read address any earlier than that will not get the read data out any sooner; the earliest possible data out will be (t_{ODTT} plus t_{ASTE}) after the clock edge beginning the RAM read phase. The transparent read address must still be held valid throughout the RAM read phase.

SINGLE-PRECISION OPERATION

Single-Precision mode is determined by the registered DP control being LO. Single-Precision mode must be asserted as shown in the timing diagrams to insure that the high-order single-precision address bits are *not* misinterpreted as Double-Precision Port Select bits and that latch controls are given their proper Single-Precision interpretation. A general discussion of dynamic switching between Single- and Double-Precision modes can be found below in "DP/SP Changeover." In Single-Precision mode, the Register File is configured as 128 words that are 16 bits in width. The 128 words are addressed by 7-bit addresses from the five address ports. All data paths and data latches behave as if they were 16 bits wide.

	min clock LO	min clock HI	min clock period
SP Single I/O Per Cycle – Transparent Inputs			$t_{OD??} + t_{DST}$
SP Single I/O Per Cycle – Latched Inputs	$t_{OD?T} + t_{DSR}$		
SP Double I/O Per Cycle – Transparent Inputs		$t_{ODC} + t_{DST}$	
SP Double I/O Per Cycle – Latched Inputs	$t_{ODRT} + t_{DSR}$		
DP Early Read Late Write	$t_{OD?T} + t_{DSR}$	$t_{ODC} + t_{DST}$	
DP Late Read Early Write	$t_{ODC} + t_{DSR}$	$t_{ODC} + t_{DSR}$	

Table V. ADSP-3128 Register-to-Register Cycle Time Requirements

Up to six 16-bit data transfers per cycle are possible in Single-Precision mode. These six transfers can be comprised of three writes and three reads, two writes and four reads, one write and five reads, or six reads.

SP NORMAL AND EXTRA READS

The operations of transferring data from RAM to a latch and from a latch to the output pins are logically distinct with the ADSP-3128. Transfers from RAM to latch are called "reads" in this data sheet; transfers from latch to output port are called "outputs."

Read addresses can be transparent or registered (Figure 4). In all timing diagrams, the phase in which an address causes a *RAM read or write* is indicated by a Greek letter. For Figure 4's normal reads, all addresses shown cause a read in phase α. Not all controls are shown on this or other timing diagrams as explicit waveforms. In Figure 4, for example, the expression "Radtrn = 1" at a rising edge implies that Radtrn was asserted HI before that edge and met the standard setup and hold time requirements of Figure 2 for controls.

The output latches can be set transparent via registered controls CDtran HI and/or Etran HI. Note that one control, CDtran, affects both Cdata-Port and Ddata-Port output latches. From a transparent read address (Radtrn HI), read data will be valid t_{ODTT} after a valid read address when the output latches are transparent. As described above, the transparent address can be setup $-t_{ASTE}$ before the RAM read phase and still maintain the t_{ODTT} output delay. From a transparent read address, read data will be valid t_{ODC} after the rising clock edge when the output *latches are in registered mode.*

When the read addresses are registered (Radtrn LO), the data output timing is very similar except that the output delay for a transparent read is now referenced from a clock edge rather than address valid. The transparent read data will be valid t_{ODRT} after the falling clock edge. See "Cycle Rate" above for clock rate implications of various read modes.

Note that in all four cases the read from RAM took place in phase α. Specifying registered output latches simply introduces an additional clock phase of pipelining. Note also that for all four Single-Precision normal reads, the data out is held valid throughout the phase *after* the data became valid. In the case of transparent data reads, the latch is actually holding the data valid for this phase. Data will be held valid t_{ODH} after the clock edge for all reads (in all modes).

Each read port has its own asynchronous three-state control: Ctri, Dtri, and Etri. See Figure 3 for enable and disable timing.

Extra reads through the Cdata-Port, Ddata-Port, and/or Edata-Port can be accomplished by making the output latches fully transparent with registered control Rfltran HI. The latches must already be transparent (CDtran/Etran HI); Rfltran HI prevents the transparent latches from holding data in the second phase after output as described for normal reads. The latches remain transparent throughout the clock cycle, allowing two 16-bit reads in the same cycle. If CDtran or Etran is LO, Rfltrn will have no effect on the relevant ports.

Extra reads are unusual in that they occur in clock HI (phase β in Figure 4), normally a write phase. Single-Precision extra reads are the only exception to the "read in clock LO" general rule. Extra reads require extra addresses. They must be supplied at the write address ports. The Aadr "write" address will determine the data read out of the Cdata-Port as an extra read. Badr will determine the Ddata-Port extra read. Aadr and Badr can be either transparent or latched. For Edata-Port extra reads, the Eadr must be transparent to enable two addresses to reach the RAM in a single cycle. Note that the timing parameters for extra reads are the same as for normal reads. The key difference is that data is only held valid until t_{ODH} after the next clock edge, not throughout the entire next phase.

Concurrent extra reads through any two or three of the three output ports are allowed. However, only one extra read from a given set of RAM locations, $(n, n \pm 64)$, is possible during a given clock HI. If more than one, simultaneous extra read is attempted from (n, $n \pm 64$), only the result at the highest priority port will be valid. Results at all other ports are undefined. The ports for extra reads are prioritized: Edata-Port (Eadr) first, Cdata-Port (Aadr) second, and Ddata-Port (Badr) third.

Each write data port has an independent Write Inhibit Control (Awinh, Bwinh, and Ewinh). If the write data ports are not inhibited (as shown in Figure 5), the data at the write data latches will be written to the RAM in phase β. An extra read performed in the same phase will read out the very same data written to RAM (*Write-Plus-Extra-Read*). So single-precision data can be passed through the Register File in clock HI without a pipeline delay, subject to the constraint that Adata goes to the Cdata-Port and Bdata goes to the Ddata-Port. A Write-Plus-Extra-Read will cause a cycle time penalty. Clock HI will have to be extended to t_{HIER} or results will be indeterminate. See "Cycle Rate" above for clock rate implications of SP Write-Plus-Extra-Reads.

Attempting a write-plus-extra-read with the Edata-Port will cause a contention, since the ADSP-3128 and the external device would both be driving. So Ewinh must be HI for an Edata-Port extra read. See "SP Write Flow-Through"and "DP Write Flow-Through" sections below for a more general way of passing data through the ADSP-3128 in the same clock phase, clock LO.

SP NORMAL WRITES

Single-Precision mode must be asserted as shown in Figure 5 to insure that the high-order single-precision address bits are *not* misinterpreted as Double-Precision Port Select bits and that latch controls are given their proper Single-Precision interpretation. The operations of transferring data from a port to a latch and from a latch to the RAM are logically distinct with the ADSP-3128. Transfers from port to latch are called "inputs" in this data sheet; transfers from latch to RAM are called "writes."

Write addresses can be transparent (Wadtrn HI) or registered (Wadtrn LO), exactly as with read addresses (Figure 5).

The Adata-Port and Bdata-Port input latches can be set to transparent, latched, or clock-on-falling mode via the ABlt and ABht controls (Table I and Figure 5). The Edata-Port input latch can be set to transparent, latched, or clock-on-falling mode via the Elt and Eht controls. When the "lt" and "ht" controls are both asserted HI, the latches are transparent ("t"). When only "lt" is asserted, the latches are in latched mode ("l"). When only "ht" is asserted the latches are in hold mode ("h"). When both controls are LO, the latches are in clock-on-falling mode.

Note that one set of controls, ABlt and ABht, affects both Adata-Port and Bdata-Port input latches. (These controls also permit holding the most recent write data at the input latches. See "SP Write to Input Latches and Hold" below.) These controls are always registered on the rising edge and become effective as of the next falling edge. When the input latches are transparent, write data must be valid t_{DST} before the end of the write phase. When the input latches are in latched mode, write data must be valid t_{DSR} before the beginning of the write phase. When the input latches are in clock-on-falling mode, write data must be valid t_{DSN} before the falling clock edge prior to the write phase. In all cases, the write data presented at write data ports must be held t_{DH} after the next clock edge.

The operations of inputting data to an input latch and writing data from the input latch to RAM are distinct. To write input data to the RAM, the asynchronous Write Inhibit Controls (Awinh, Bwinh, and/or Ewinh) must be LO as shown in Figure 5. Writes should not be enabled until at least t_{ARBE} after the rising clock edge and no later than t_{WEN} before the falling edge. (The design target for t_{ARBE} is zero; see "Specifications" below.) If a transparent write address is used, there is the additional requirement that the address be valid t_{ATBE} before A/B/Ewinh goes LO; otherwise a write might be attempted at the wrong address, i.e., a wrong write.

Note that a write can be enabled later than a write can be inhibited. If you might want to inhibit a write to the Register File as late as the very phase in which a write is attempted, you can keep the A/Binh controls normally HI, i.e., write inhibited, and bring them LO every time you actually want to write. Alternatively, for simplicity, the A/Binh controls can be wired LO (write enable) and dummy writes be performed to an unused RAM location in every clock HI (if t_{ARBE} is zero; see "Specifications" below). Write addresses must always be stable, however, whenever the Write Inhibit controls are LO. (Do not hardwire Ewinh.)

The write ports are prioritized with the Edata-Port of highest priority, followed by the Adata-Port, followed by the Bdata-Port. If writes to the same RAM location are attempted in a given clock HI phase, the data presented at the higher priority enabled write data port will be the data written to RAM.

SP WRITE FLOW-THROUGH

Write Flow-Through allows a low-latency write to RAM and read from the same RAM location in clock LO (Figure 6). With Write Flow-Through, the designer can pass data through the RAM late in the clock cycle without suffering a pipeline delay. (If write data is available early in the clock cycle, a normal write followed by a normal read can pass data through the ADSP-3128 in one cycle.) Write Flow-Through is the only exception to the "write in clock HI" general rule. In Figure 6, both the write to RAM and the read from RAM occur in phase γ, a clock LO.

Write Flow-Through is enabled at the respective write data ports by asynchronous controls Awft, Bwft, and Ewft. The Write Flow-Through controls override the Write Inhibit controls and always force a write whenever write and read addresses match, independent of the levels on the Write Inhibit controls. (If no read address matches the Write-Flow-Through write address, the write will not take place.) The Write Flow-Through Controls must be asserted HI t_{WFT} before the clock's rising edge. By the next clock LO they must be LO.

Only transparent write addresses can be used in Write Flow-Through mode. (Write addresses latched at the previous rising edge would no longer be valid by clock LO.) Read addresses can be either transparent or registered. Transparent addresses are also required to be valid t_{AWFT} before Write Flow-Through for the data port in question is asserted as shown in Figure 6.

The data setup and hold requirements are the same whether the input data latches are configured for transparent or latched write data (since their behavior in clock LO is the same either way). Write data must be setup t_{DSTFT} before the rising edge if the read is transparent and t_{DSCFT} if the read is registered. The output delay for a transparent read will be t_{ODTFT} from the write data valid or t_{ODWFT} from the Write Flow-Through control's rising edge, whichever is greater. The output delay for a registered read will be t_{ODCFT} from the rising edge.

For clock-on-falling write data, the data setup time is t_{DSN}, the same as shown in Figure 5. The output delay for a transparent read will be t_{ODTFT} *from the falling clock edge* or t_{ODWFT} from the Write Flow-Through control's rising edge, whichever is greater. The output delay for a registered read will be t_{ODCFT} from the rising edge.

Two independent Write Flow-Through operations can occur in the same phase LO. (There aren't enough ports for three.) There are no restrictions on the relationships between addresses, even when attempting two concurrent Write Flow-Throughs.

The write ports are prioritized for Write Flow-Through in exactly the same way as for normal writes with the Edata-Port of highest priority, followed by the Adata-Port, followed by the Bdata-Port. If writes to the same RAM location are attempted in a given clock LO phase, the data presented at the higher priority enabled write data port will be the data written to RAM.

Using Write Flow-Through will cause a cycle time penalty. Clock LO will have to be extended to t_{LOFT} for any phase in which a Write Flow-Through is attempted. See "Cycle Rate" above for clock rate implications of Write Flow-Through.

SP BIDIRECTIONAL EDATA-PORT

The Edata-Port will behave like any write port if treated as such. Alternatively, it will also behave like any read port if treated as such, including supporting extra reads. The Edata-Port can be used as a write port in one cycle, a read port in the next, and a write port in the third cycle, as long as the Edata-Port is disabled to high-impedance before setting up write data. In Single-Precision mode, the Edata-Port can also function as a bidirectional port both reading and writing in every clock cycle (Figure 7).

The control that configures the Edata-Port for bidirectional operation is the registered Eio control. It must be asserted in conjunction with the DP control as shown in Figure 7 for proper interpretation. (Eio has a different meaning in Double-Precision mode.) It takes effect in the cycle immediately after it is asserted.

When in Bidirectional mode, all Eadr-Port latches go to registered mode, *regardless of the state of Radtrn and Wadtrn* (Table III). All other address ports are unaffected by Eio. Address setup and hold times are the usual t_{ASR} and t_{AH} for registered and latched addresses.

Three combinations of Edata-Port input and output latch settings are possible: transparent write and transparent read, clock-on-falling write and transparent read, and latched write and registered read. Note carefully in Figure 7 that because of the pipelining differences, only in the first case do data and addresses track in the same order. All reads from the RAM are in phase γ and all writes to the RAM are in phase δ which follows. But in the

latter two cases the phase δ write data is presented before the phase γ read data is output.

Setup times and output delays are standard. Note that minimum output delays are specified for both t_{ODRT} and t_{ODC}, indicating when the device writing to the Edata-Port must be no longer driving to avoid contention. The Edata-Port will be in a high-impedance state t_{EDIS} after the clock edge after the read data became valid. That is, when the Edata-Port is configured for bidirectional operation (Eio HI), it will automatically go into a high-impedance state to allow writes without forcing the user to manipulate Etri. This disable time, t_{EDIS}, is measured as shown for t_{ENA} in Figure 3.

SP INPUT TO INPUT LATCHES AND HOLD

Data input to the input latches can be held at those latches with the ABlt and ABht and Elt and Eht controls (Table I). These controls are always registered on the rising edge and become effective as of the next falling edge. Figure 8 shows how data written to the latches in any of the three input modes can be held at a latch as long as desired. As of the falling edge after hold is asserted, data at the write data port is ignored and will be ignored until the next falling edge after one of the three input modes is asserted. The hold feature allows the input latches to be used for temporary data storage. Examples of using this feature include delaying a write to the RAM to avoid overwriting some data currently in the RAM and writing the same data to multiple RAM locations.

SP REGISTER-TO-REGISTER TRANSFERS

Register-to-register transfers are accomplished with the Multiport Register File by reading data from the Edata-Port output latch and writing that very data to the Edata-Port input latch. The input Edata-Port latch can hold the data in question as just described, allowing a large number of possible ways to accomplish a register-to-register transfer. Figures 9, 10, 11 and 12 illustrate those register-to-register transfers that *don't* involve data holds. A read in clock LO is followed by a write in the next clock HI. Figures 9 and 10 represent two methods with Eio LO; Figures 11 and 12, one method with Eio HI. All three make RAM reads in phase γ and RAM writes in phase δ.

To get the data from Edata-Port output latch to the input latch, the data must be driven through the Edata-Port. That is, Etri must be LO as shown in Figures 9 through 12. What actually shows up at the Edata-Port is described at the bottom of Figures 9 through 12 and follows standard timing. Note that the read data will only be held valid through a full phase if both DP and Eio are LO.

With Eio LO (Edata-Port not bidirectional), there are several ways to accomplish the transfer. The Edata input latch can be either transparent or in latched mode. With a registered read address (Eadr), the write address (Eadr) can be either latched or transparent. If the read address (Eadr) is transparent, however, the write address (Eadr) must be transparent also. The combination of a transparent E read address and latched E write address is impossible, since both would have to be valid in the same phase γ.

With Eio HI (Edata-Port bidirectional), the read and write Eadrs will be registered, since Eio HI forces that addressing mode.

Since the data driven off-chip must be re-input to the ADSP-3128 in a register-to-register transfer, the clock period, clock LO, and/or clock HI, as relevant, must be long enough to allow for data output delays and input setup times. This requirement imposes some restrictions on the maximum speed at which the Register File can be operated. See "Clock Rate" above for a detailed description of timing issues related to register-to-register transfers. These timing requirements are summarized in Table V.

SP BANK SELECT

Bank Select is treated in exactly the same way in both Single-Precision and Double-Precision modes (Figure 21). The BS control is not registered in general but rather follows the addresses through the address latches (Figure 1). Hence, its setup requirement is t_{AST} and t_{ASR}, the setup requirement for read and write addresses for transparent and latched/registered modes respectively. All applicable requirements must be met. Flowing with addresses allows Bank Select to track all read and write pipelines as shown in Figure 21. When LO, writes will be disabled and output ports put in high-impedance.

With Bank Select, the user's register file space can be extended "vertically" beyond 128 single-precision words to whatever register file space is desired. The user would typically use more than seven bits for addressing, decoding the high-order bits to select a horizontal row of ADSP-3128s that produce a single "word" and applying the low-order seven bits to the address ports in all rows. In other words, the register file space can be expanded in exactly the way a designer normally builds up a random access memory.

The only restriction on this method of extending the register file address space using Bank Select is that all reads and writes in a given cycle must be from the same horizontal row of ADSP-3128s. (Port Select removes this restriction for Double-Precision mode). In Single-Precision mode, the user can select/deselect individual *ports* using the asynchronous Write Inhibit and Three-State controls. The user would have to apply these with timing based on the latch modes currently selected to properly track the pipelines.

Note that the timing requirements for Bank Select are simple if write addresses are latched but are more complicated for transparent write addresses because of the way BS flows with the write address. For a Bank Deselect, the BS control must be LO in the clock HI write phase β (Figure 21). If writes are currently enabled, BS must be set up in phase α; if they're inhibited, BS is not needed LO until phase β to disable writes. Since the Write Inhibit controls for the three write data ports are independent, if any is enabled in phase α, BS will have to be LO in phase α to disable all writes. Also, if there is any possibility of a Write Flow-Through in phase γ, BS will have to be LO throughout phase γ.

DOUBLE-PRECISION OPERATION

Double-Precision mode is determined by the registered DP control being HI. A general discussion of dynamic switching between Single- and Double-Precision modes can be found below in "DP/SP Changeover." In Double-Precision mode, the Register File is configured as 64 words that are 32 bits in width. The 64 words are addressed by 6-bit addresses from the five

address ports. The seventh, high-order bit used in Single-Precision addressing is redefined as the Port Select bit. All data paths between RAM and data latches are true 32-bit paths. That is, all 32-bit reads from the RAM to the latches and 32-bit writes to the RAM from the latches take place in a single read or write clock phase. The ports, however, are 16-bits wide. Data transfers through the ports are time-multiplexed.

The ADSP-3128 automatically controls the multiplexing through the data ports once the DP control is HI. The user only supplies one address to reference the two 16-bit halves of the data word transferred through the data ports. In Slow Input and Slow Read modes, however, the user does have direct control over these multiplexers to allow communication with slower devices.

Up to five 32-bit data transfers per cycle are possible in Double-Precision mode. These five transfers can be comprised of three writes and two reads or two writes and three reads, depending on whether the Edata-Port is used as a read port or a write port.

Double-Precision mode is intended for interfacing to processors that use time-multiplexed 64-bit data, like Analog Devices' ADSP-32XX Floating-Point Multipliers and ADSP-32XX Floating-Point ALUs. Normally, two ADSP-3128 Multiport Register Files would be used "horizontally" to communicate with 32-bit buses.

In the descriptions that follow, one 16-bit half of a given ADSP-3128's 32-bit word is referenced as an "LSW," the other half as an "MSW". Note that normally a user would put together the LSWs from two ADSP-3128s to create the 32-bit Least Significant Word of a 64-bit double-precision floating-point number. Similarly, the floating-point number's Most Significant Word would be constituted from the MSWs of two ADSP-3128s.

What is called an "LSW" in this data sheet is simply the 16-bit half of a 32-bit field that is written to the Register File first and read from the Register File first. For interfacing with Analog Devices' ADSP-3210 Floating-Point Multiplier, this is the more meaningful name for the first datum transferred. But it is nothing more than a semantic convention; what is called here an "LSW" can be the more significant data in a user's system. The key point is that whichever half is written first will be the half read first.

DP NORMAL READS

Double-Precision mode must be asserted as shown in Figure 13 to insure that the Port Select bits are *not* misinterpreted as Single-Precision address bits and that latch controls are given their proper Double-Precision interpretation. Addresses can be transparent or registered (Figure 13), just as in Single-Precision mode.

The two normal read options in Double-Precision mode are Early Read and Late Read. They are controlled via registered controls CDtran and/or Etran, which can make the output latches transparent or latched. The effect in Double-Precision mode is to create two pipelining options. Note that one control, CDtran, affects both Cdata-Port and Ddata-Port output latches.

Early Reads are generated when CDtran and/or Etran are HI. The LSW is read transparently from the RAM in phase γ through the output data port with delays, t_{ODRT} and t_{ODTT}, corresponding to registered and transparent read addresses respectively. The MSW is also read from the RAM in phase γ but is held at the 32-bit output latch to be multiplexed out the output data port in the next phase with output delay t_{ODC}. Data hold times for Early Reads as for all other kinds is t_{ODH}. As described in "Address Latches," the transparent address can be setup $-t_{ASTE}$ before the RAM read phase and still maintain the t_{ODTT} output delay for the LSW, as in Single-Precision mode.

Late Reads are generated when CDtran and/or Etran are LO. As with Early Reads, both the LSW and MSW are read from the RAM to the 32-bit output latches in phase γ. In the case of Late Read, the LSW is held at the output latch until the next phase, when it is driven off chip with delay t_{ODC}. The MSW follows in the phase after that with the same delay characteristic of registered reads. See "Cycle Rate" above for clock rate implications of various read modes.

Each read port has its own asynchronous three-state control: Ctri, Dtri, and Etri. See Figure 3 for enable and disable timing.

DP NORMAL WRITES

Double-Precision mode must be asserted as shown in Figure 14 to insure that the Port Select bits are *not* misinterpreted as Single-Precision address bits and that latch controls are given their proper Double-Precision interpretation. Addresses can be transparent or registered (Figure 14), just as with Double-Precision reads.

The two normal write options in Double-Precision mode are Early Write and Late Write. They are exactly analogous to Early Read and Late Read in that they offer two pipelining options. They are controlled via registered controls ABlt, ABht, Elt, and Eht as shown in Figure 14 and Table II. Note that one set of controls, ABlt and ABht, affects both Adata-Port and Bdata-Port input latches. These controls become effective as of the falling edge after they are registered.

In Early Write, both LSW and MSW are written to the 32-bit input latches before they are both written to RAM in phase δ. Both LSW and MSW have the setup time requirement, t_{DSR}, characteristic of latched-mode data inputs. Data hold requirements for Early Write and all other writes is t_{DH}.

With Late Write, the user can input the LSW and MSW into the Register File one-half cycle later for a phase δ write to RAM. The LSW is latched with setup time t_{DSR}. The MSW, however, is transparently written to RAM in phase δ. Note that the setup requirement on the MSW is therefore t_{DST}.

The actual write to RAM occurs in the single phase δ. Hence the Write Inhibit controls in Double-Precision work exactly as they do in Single-Precision. To write input data to the RAM, the asynchronous Write Inhibit Controls (Awinh, Bwinh, and/or Ewinh) must be LO as shown in Figure 14. Writes should not be enabled until at least t_{ARBE} after the rising clock edge and no later than t_{WEN} before the falling edge. (The design target for t_{ARBE} is zero; see "Specifications" below.) If a transparent write address is used, there is the additional requirement that the address be valid t_{ATBE} before A/B/Ewinh goes LO; otherwise a write might be attempted to the wrong address.

Note that a write can be enabled later than a write can be inhibited. If you might want to inhibit a write to the Register File as late as the very phase in which a write is attempted, you can keep the A/B/Ewinh controls normally HI, i.e., write inhibited, and bring them LO every time you actually want to write. Alternatively, for simplicity, the A/B/Ewinh controls can be wired LO (write enable) and dummy writes be performed to an unused RAM location in every clock HI (if t_{ARBE} is zero; see "Specifications" below). Write addresses must always be stable, however, whenever the Write Inhibit controls are LO.

The write ports are prioritized with the Edata-Port of highest priority, followed by the Adata-Port, followed by the Bdata-Port. If writes to the same RAM location are attempted in a given clock HI phase, the data presented at the higher priority enabled write data port will be the data written to RAM.

DP WRITE FLOW-THROUGH

Write Flow-Through is an available option in Double-Precision. It allows the user to pass double-precision data through the Register File with minimal latency (three clock phases). See Figure 15. Write Flow-Through allows both a 32-bit write from latch to RAM and a 32-bit read from RAM to latch in the same clock LO. (If write data is available one phase earlier than shown in Figure 15, a normal Late Write followed by a normal Early Read can pass data through the ADSP-3128 in four clock phases.) Write Flow-Through is the only exception to the "write in clock HI" general rule. In Figure 15, both the write to RAM and the read from RAM occur in phase γ.

Only Early Writes can be used for Write Flow-Through. Since the write actually occurs in clock LO, Late Write is too late.

Write Flow-Through is enabled at the respective write data ports by asynchronous controls Awft, Bwft, and Ewft. The Write Flow-Through controls override the Write Inhibit controls and always force a write whenever write and read addresses match, independent of the levels on the Write Inhibit controls. (If no read address matches the Write-Flow-Through write address, the write will not take place.) The Write Flow-Through Controls must be asserted HI t_{WFT} before the clock's rising edge. By the next clock LO they must be LO.

Only transparent write addresses can be used in Write Flow-Through mode. (Write addresses latched at the previous rising edge would no longer be valid by clock LO.) Read addresses can be either transparent or registered. Transparent addresses are also required to be valid t_{AWFT} before Write Flow-Through for the data port in question is asserted as shown in Figure 15.

The LSW must be setup t_{DSR} before the falling edge, as for a normal Early Write. For the MSW, however, the timing characteristic of Write Flow-Through becomes effective. The MSW must be setup t_{DSTFT} before the rising edge if the read is Early and t_{DSCFT} if the read is Late. The output delay for the LSW for an Early Read will be t_{ODWFT} from the Write Flow-Through control's rising edge. The output delay for the LSW for a Late Read will be t_{ODCFT} from the rising edge. MSWs read out are registered with delay t_{ODC} for both Early and Late Reads.

Two independent Write Flow-Through operations can occur in the same phase LO. There are no restrictions on address locations for two concurrent Write Flow-Throughs in Double-Precision.

The write ports are prioritized for Write Flow-Through in exactly the same way as for normal writes with the Edata-Port of highest priority, followed by the Adata-Port, followed by the Bdata-Port. If writes to the same RAM location are attempted in a given clock LO phase, the data presented at the higher priority enabled write data port will be the data written to RAM.

Using Write Flow-Through will cause a cycle time penalty. Clock LO will have to be extended to t_{LOFT} for any phase in which a Write Flow-Through is attempted. See "Cycle Rate" above for clock rate implications of Write Flow-Through.

DP EDATA-PORT SLOW INPUT AND SLOW READ

The bidirectional Edata-Port is intended to be the port interfaced to a system bus, which may run more slowly than local buses. To simplify the interface for Double-Precision, the ADSP-3128 provides a mode for loading the LSW and MSW into the input latches over multiple ADSP-3128 clock cycles (Figure 16). Also a mode is provided for multiplexing LSW and MSW read data from the output latches over multiple clock cycles (Figure 17).

For a Slow Input (Figure 16), the input latches are updated when there is a *transition* in Eht from one clock rising edge to the next clock rising edge. Elt must be concurrently HI (Hold mode). Data is setup to the input latches with setup time t_{DSR}. When Eht is LO in the cycle after it was HI, the data will be written to the LSW position in the Edata input latch at the next falling edge and held there. When Eht is HI in the cycle after it was LO, the data will be written to the MSW position in the Edata input latch at the next falling edge and held there. A write to RAM can be enabled (with Ewinh LO) at the next clock HI from either latched or transparent Eadr. Because it is the *transition* in Eht that determines whether data is loaded to the LSW or MSW position in the input latch, the user needs to program Eht for setup in both phase α and phase γ.

For a Slow Read, registered control Eio, when asserted HI in conjunction with Double-Precision (DP HI), configures the Edata-Port for a Slow Read. When Eio goes HI, data at the output latch is held. In Figure 15, this is the 32-bit data read at phase γ. For a Slow Read, output delays will be t_{ODC}. Data will be held t_{ODH} after the clock edges shown in Figure 17. When configured for Slow Read, the ADSP-3128's registered Etran control becomes a direct controller of the Edata-Port's Double-Precision output multiplexer. When Etran is LO, the LSW read from RAM in phase γ will be driven through the Edata-Port (if enabled with Etri). When Etran is HI, the MSW read from RAM in phase γ will be driven through the Edata-Port (if enabled with Etri). The outputs will be driven as long as Eio is HI and Etran doesn't change.

DP INPUT TO INPUT LATCHES AND HOLD

Data input to the input latches can be held at those latches with the ABlt, ABht, Elt, and Eht controls (Table I). These controls are always registered on the rising edge and become effective as of the next falling edge. Figure 18 shows how data written to the latches in either Early Write or Late Write modes can be held at a latch as long as desired. As of the falling edge after hold is asserted with ABlt/Elt HI, data at the write data port is ignored and will be ignored until the next falling edge after either ABlt/Elt goes LO or Eht makes a transition. (If Eht makes a transition, the ADSP-3128 will make a Slow Input.) The hold feature allows the input latches to be used for temporary data storage.

DP REGISTER-TO-REGISTER TRANSFERS

Register-to-register transfers are accomplished with the Multiport Register File by reading data from the Edata-Port output latch and writing that very data to the Edata-Port input latch. The input Edata-Port latch can hold the data in question as just described, allowing a large number of possible ways to accomplish a register-to-register transfer. Figures 19 and 20 illustrate those register-to-register transfers that *don't* involve data holds.

Only two combinations of Double-Precision reads and writes can be used for Register-to-Register transfers: Early Read with Late Write (Figure 19) and Late Read with Early Write (Figure 20). Early Read with Late Write offers the lower latency.

To get the data from Edata-Port output latch to the input latch, the data must be driven through the Edata-Port. That is, Etri must be LO as shown in Figures 19 and 20. What actually shows up at the Edata-Port is described at the bottom of Figures 19 and 20 and follows standard timing.

Since the data driven off-chip must be re-input to the ADSP-3128 in a register-to-register transfer, clock LO, and clock HI must each be long enough to allow for data output delays and input setup times. This requirement imposes some restrictions on the maximum speed at which the Register File can be operated. See "Clock Rate" above for a detailed description of timing issues related to register-to-register transfers. These timing requirements are summarized in Table V.

DP BANK SELECT AND PORT SELECT

Bank Select is treated in exactly the same way in both Single-Precision and Double Precision modes (Figure 21). The BS control is not registered in general but rather follows the addresses through the address latches (Figure 1). In Double-Precision, the seventh address bit (not needed for Double-Precision addressing) is redefined to function as Port Select for the ports being addressed. DP must be asserted HI as shown in Figure 22 to insure that these bits are interpreted as Double-Precision Port Selects and not Single-Precision address bits (and that latch controls are given their proper Double-Precision interpretation).

Behaving as addresses, both BS and A/B/C/D/Eadr$_6$ have setup requirements of t_{AST} and t_{ASR}, the setup requirement for read and write addresses for transparent and latched/registered modes respectively. All applicable requirements must be met. Flowing with addresses allows Bank Select and Port Select to track all read and write pipelines as shown in Figures 21 and 22. When LO, writes will be disabled and output ports put in high-impedance.

With either Bank Select or Port Select, the user's register file space can be extended "vertically" beyond 128 single-precision words to whatever register file space is desired. The user would typically use more than six bits for addressing, decoding the high-order bits to select a horizontal row of ADSP-3128s with Bank Select or individual ports with Port Select that produce a single "word" and applying the low-order six bits to the address ports of all ADSP-3128s. In other words, the register file space can be expanded in exactly the way a designer normally builds up a random access memory.

The only restriction on this method of extending the register file address space using Bank Select is that all reads and writes in a given cycle must be from the same horizontal row of ADSP-3128s.

Port Select removes this restriction for Double-Precision mode (only). Like Bank Select, the Port Select controls track the ADSP-3128's internal pipelines. But since every port can be independently selected or deselected, reads can be made from and writes made to any combination of locations in the user's register file space. They need not be all made from the same horizontal row.

Note that the timing requirements for Bank Select and Port Select are simple if write addresses are latched but are more complicated for transparent write addresses because of the way BS and A/B/Eadr$_6$ flow with the write address. For a Bank or Port Deselect, the BS or A/B/Eadr$_6$ control must be LO in the clock HI write phase β (Figures 21 and 22). If writes are currently enabled, BS or A/B/Eadr$_6$ must be set up in phase α; if they're inhibited, BS or A/B/Eadr$_6$ is not needed LO until phase β to disable writes. Since the Write Inhibit controls for the three write data ports are independent, if any is enabled in phase α, BS or A/B/Eadr$_6$ will have to be LO in phase α to disable all writes. Also, if there is any possibility of a Write Flow-Through in phase γ, BS or A/B/Eadr$_6$ will have to be LO throughout phase γ.

DP/SP CHANGEOVER

Many controls are interpreted and internal states affected by the DP control. The timing diagrams show when DP must be HI and when it must be LO to accomplish the operation described in each timing diagram. For times when the state of DP is not explicitly shown, it can be changed. That is, the user can dynamically reconfigure the ADSP-3128 from Single-Precision to Double-Precision and conversely as long as these restrictions are observed.

It may be useful to know that a 32-bit word in Double-Precision mode consists of two 16-bit words that can be addressed in Single-Precision mode with seven bit addresses by the six bit address used in double precision mode (n) and that address plus 64 ($n \pm 64$). The LSW of the double-precision word will be in n; the MSW in $n \pm 64$. By switching from Double- to Single-Precision, the user can independently access the LSW and the MSW.

DESIGN CONSIDERATIONS

Power Up

At power up, any or all of the three output ports, Edata-Port, Cdata-Port, or Ddata-Port, may be driving off chip. Because of pipelining, Bank Select should not be used to serve a reset or "chip select" function unless no other devices on the buses driven by these ports could themselves possibly be driving. Bank Select will tristate these ports, but they cannot be guaranteed to be in a high-impedance state until t_{DIS} into the second cycle after the rising edge at which BS is LO (Figure 21).

Any ADSP-3128 output port that shares a buses should be forced into a high-impedance state at power up using the Etri/Ctri/Dtri controls. The bits driving these pins from microcode can be gated with the user's general system reset control.

Power Supply Decoupling

The ADSP-3128 register file is designed with high-speed drivers on all output pins. This means that large peak currents may pass through the driver ground and V_{DD} pins, particularly when all output port lines are simultaneously charging their load capacitance in transition, whether from LO to HI or vice versa. These peak currents can cause a large disturbance in the ground and supply lines. To help isolate the effects of this disturbance, the ADSP-3128 provides separate pins for driver GND and V_{DD}s and logic GND and V_{DD}s. For printed circuit boards, the ADSP-3128's GND and V_{DD} pins must be tied directly to solid ground and V_{DD} planes, respectively, with 0.1μF ceramic and 20μF tantalum bypass capacitors as close as possible to the tie points. Lead lengths and trace lengths should be as short as possible. The ground plane should tie to driver GND in particular with a very low inductance path.

For breadboarding with wirewrap construction, the driver V_{DD} should be bypassed to the driver GND with 0.1μF ceramic and 20μF tantalum capacitors. The logic GND and V_{DD} need a

separate 0.1μF bypass. Both sets of capacitors should then be common at a point with a low impedance path to the power supply. Lead lengths should be as short as possible. This will reduce coupling of output driver current spikes into the logic supply.

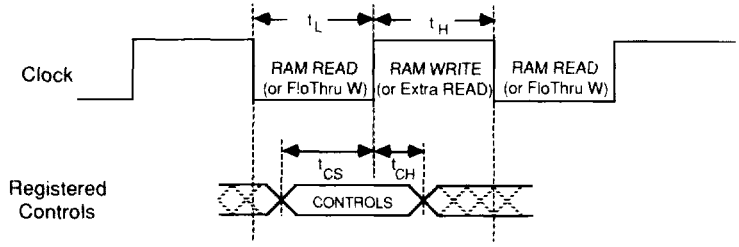
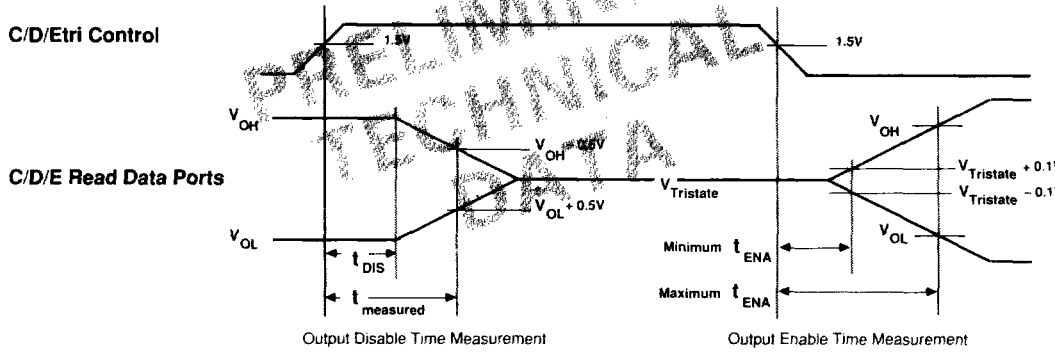


Figure 2. Register Controls Timing



Output disable time, t_{DIS}, is measured from the time OEN reaches 1.5V to the time when all outputs have ceased driving. This is calculated by measuring the time, $t_{measured}$, from the same starting point to when the output voltages have changed by 0.5V toward +1.5V. From the tester capacitive loading, C_L, and the measured current, i_L, the decay time, t_{DECAY}, can be approximated to first order by:

$$t_{DECAY} = \frac{C_L \cdot 0.5V}{i_L}$$

from which

$$t_{DIS} = t_{measured} - t_{DECAY}$$

is calculated. Disable times are longest at the highest specified temperature.

The minimum output enable time, minimum t_{ENA}, is the earliest that outputs begin to drive. It is measured from the control signal OEN reaching 1.5V to the point at which the fastest outputs have changed by 0.1V from $V_{Tristate}$ toward their final output voltages. Minimum enable times are shortest at the lowest specified temperature.

The maximum output enable time, maximum t_{ENA}, is also measured from OEN at 1.5V to the time when all outputs have reached TTL input levels (V_{OH} or V_{OL}). This could also be considered as "data valid." Maximum enable times are longest at the highest specified temperature.

Figure 3. Three-State Disable and Enable Timing

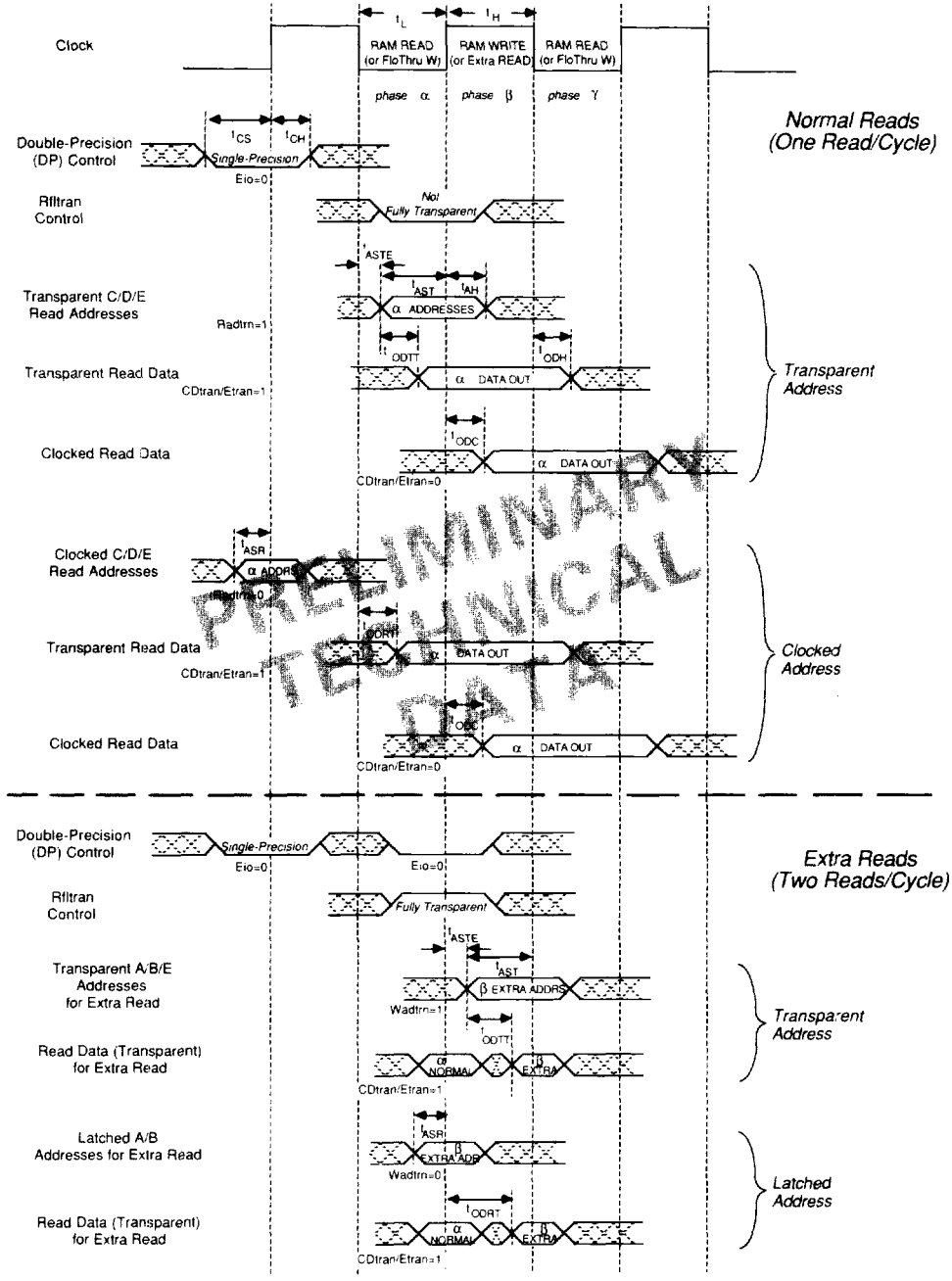


Figure 4. Single-Precision Read Output Timing

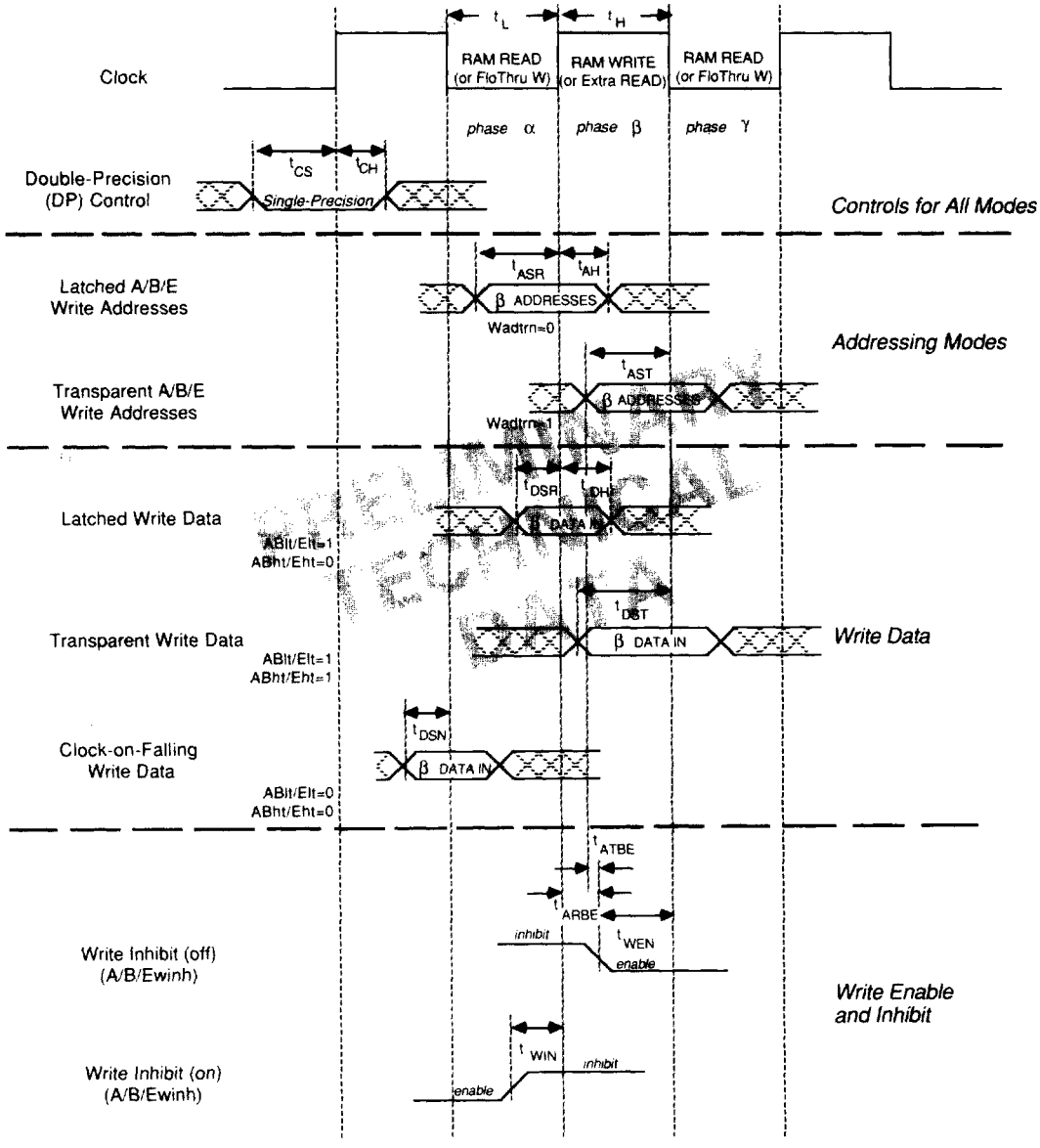
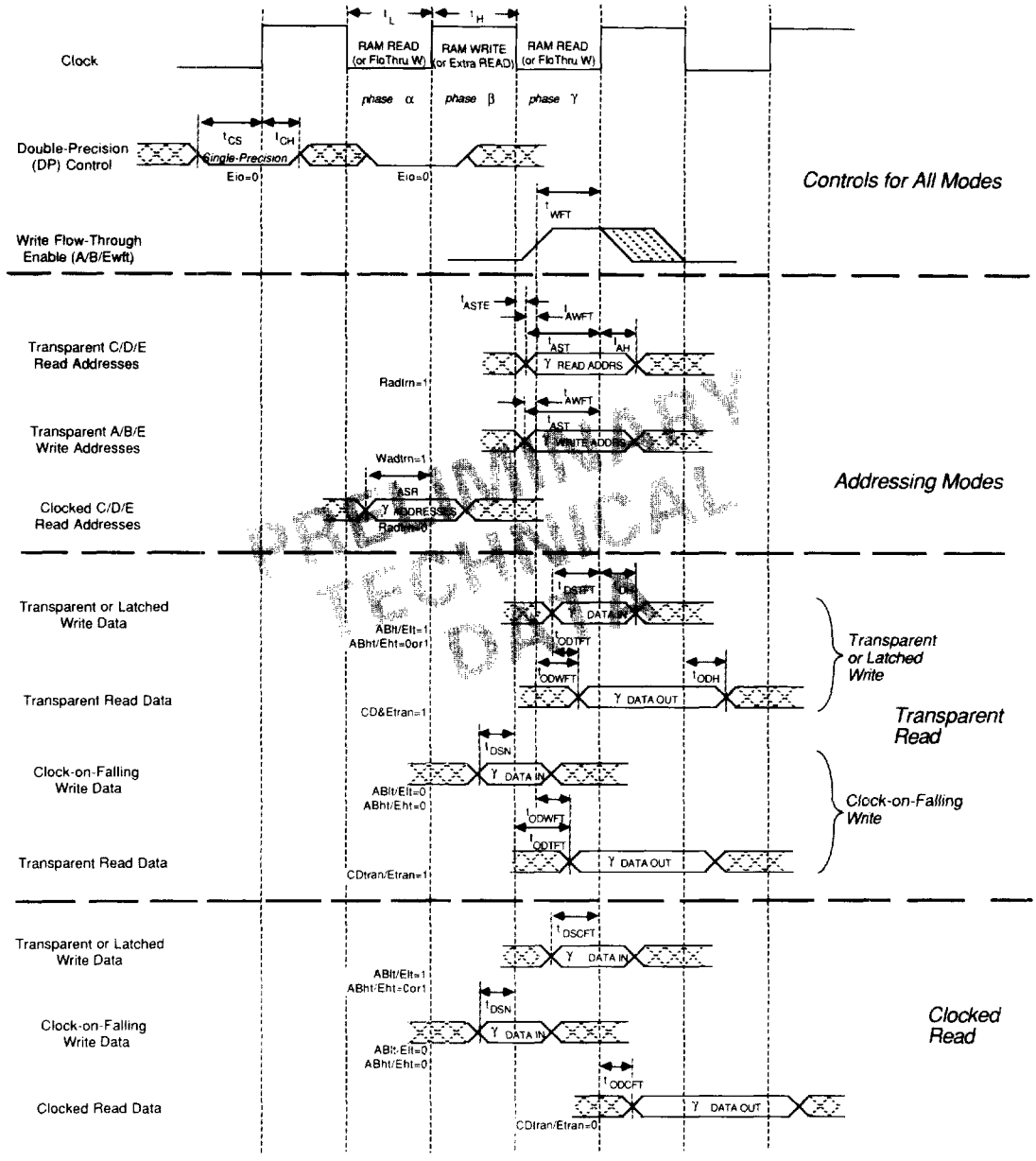
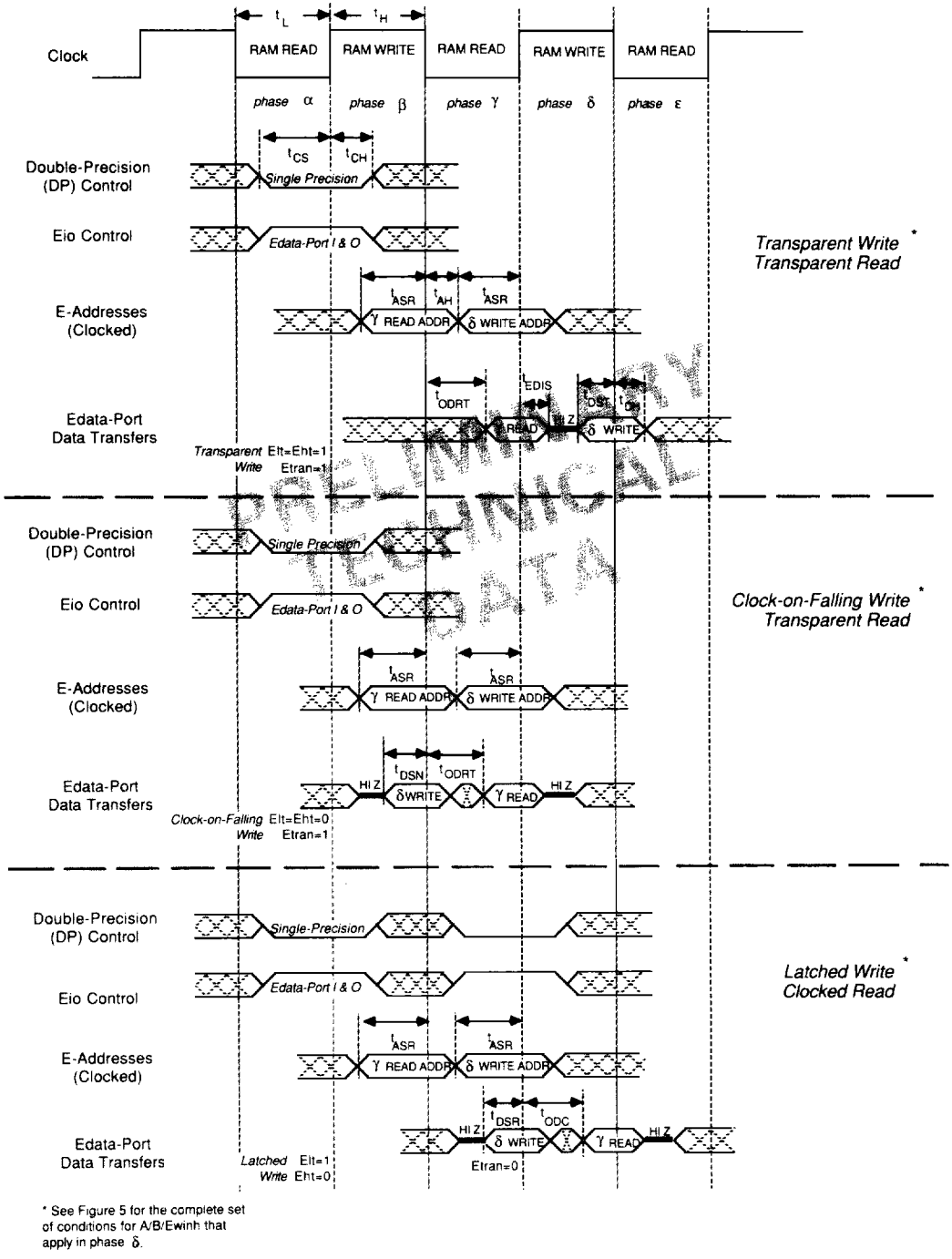


Figure 5. Single-Precision Normal Write Input Timing



* If Eio=1, data outputs from the EdataPort will cross only a single clock edge, as shown in Figure 7.

Figure 6. Single-Precision Write Flowthrough Timing



* See Figure 5 for the complete set of conditions for A/B/Ewinh that apply in phase δ.

Figure 7. Single-Precision Timing for Bidirectional Edata-Port

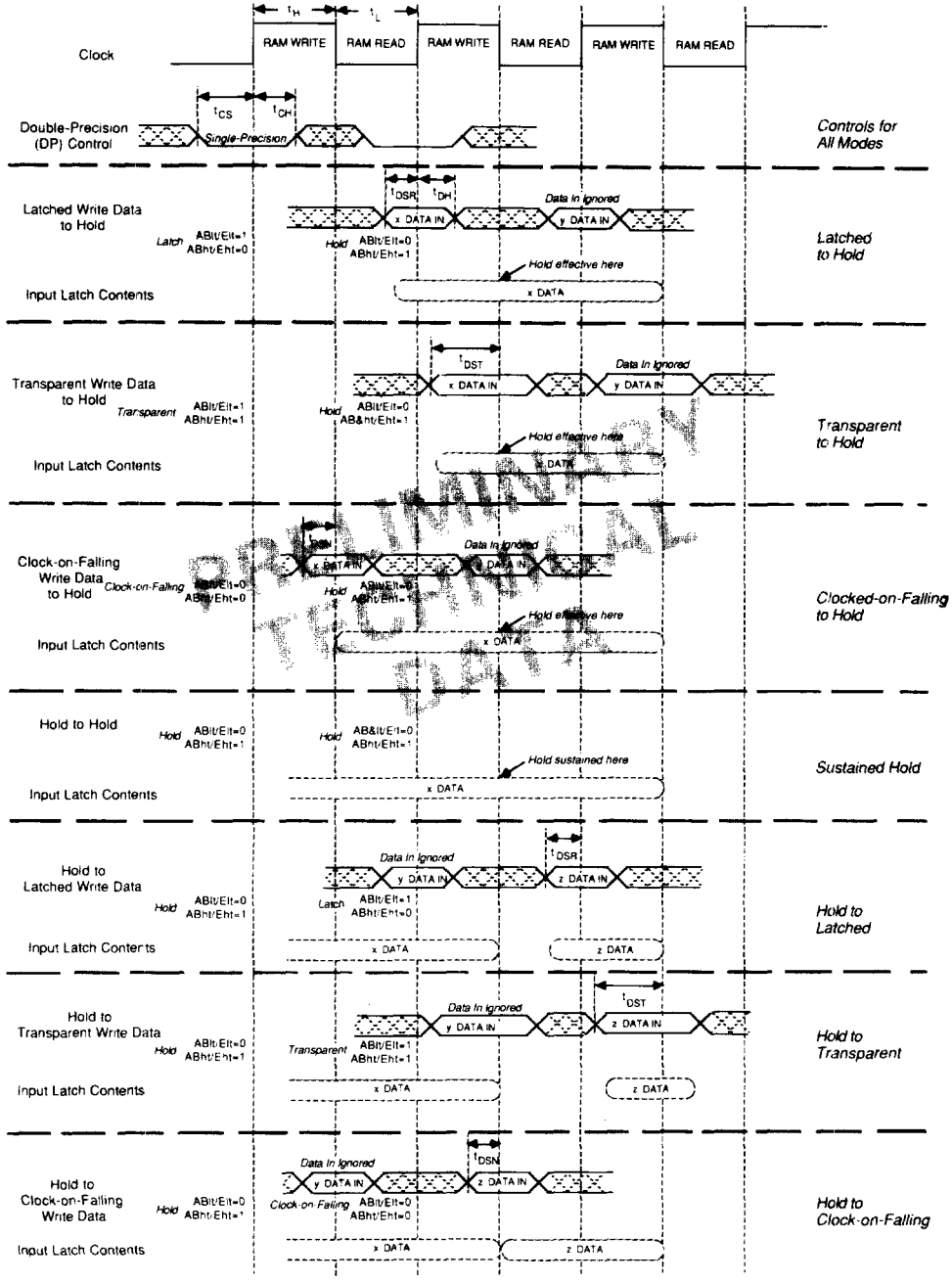
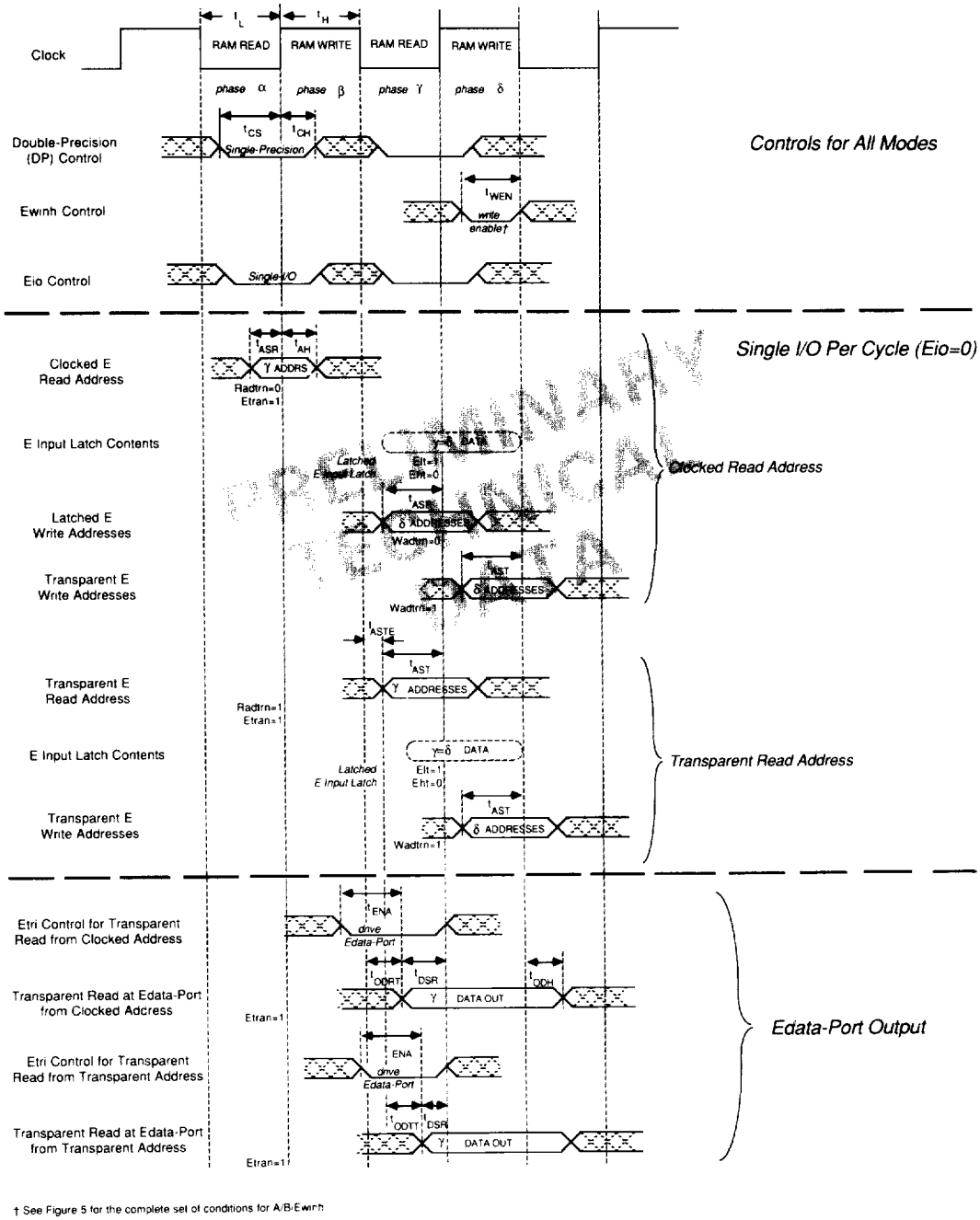
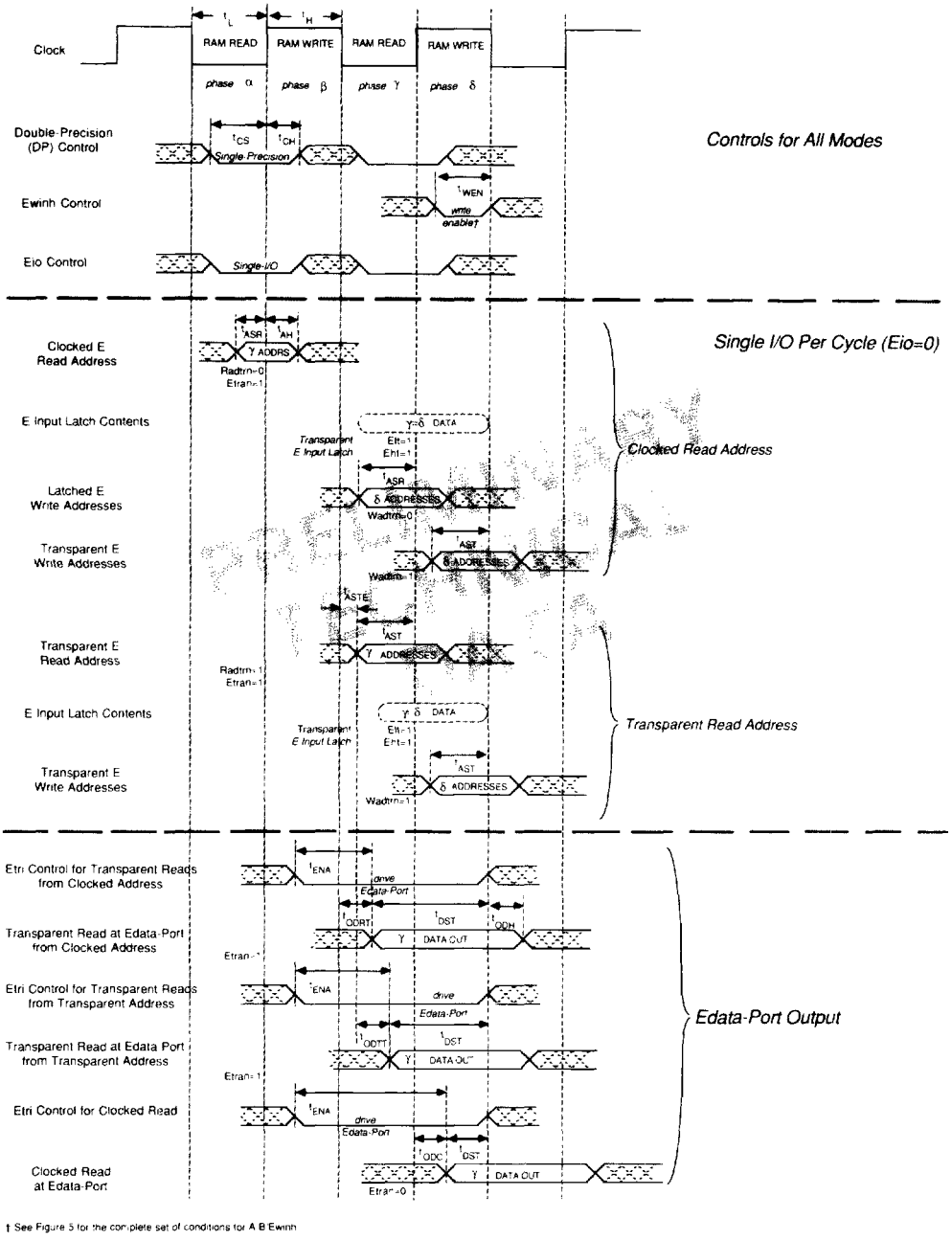


Figure 8. Single-Precision Write to Input Latches and Hold Timing



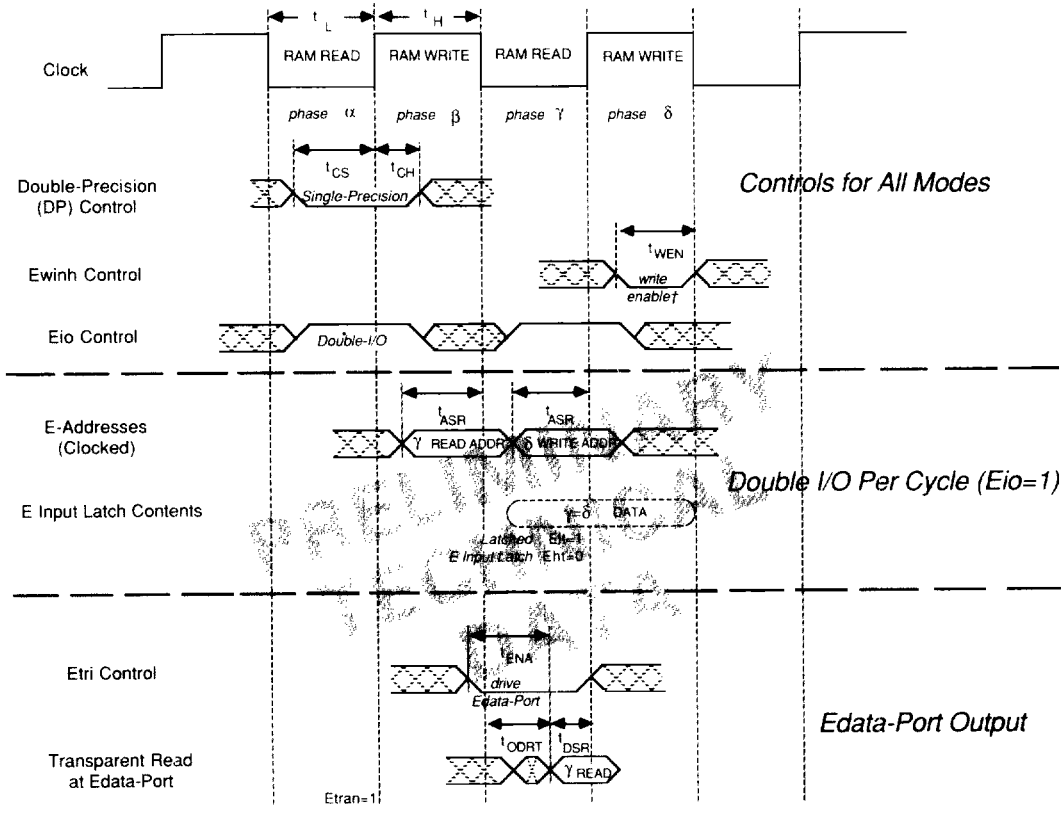
† See Figure 5 for the complete set of conditions for A/B-Ewinh

Figure 9. Single-Precision Timing for Register-to-Register Transfer via Edata-Port – Edata-Port in Single I/O per Cycle Mode (Eio = 0) and Latched Inputs



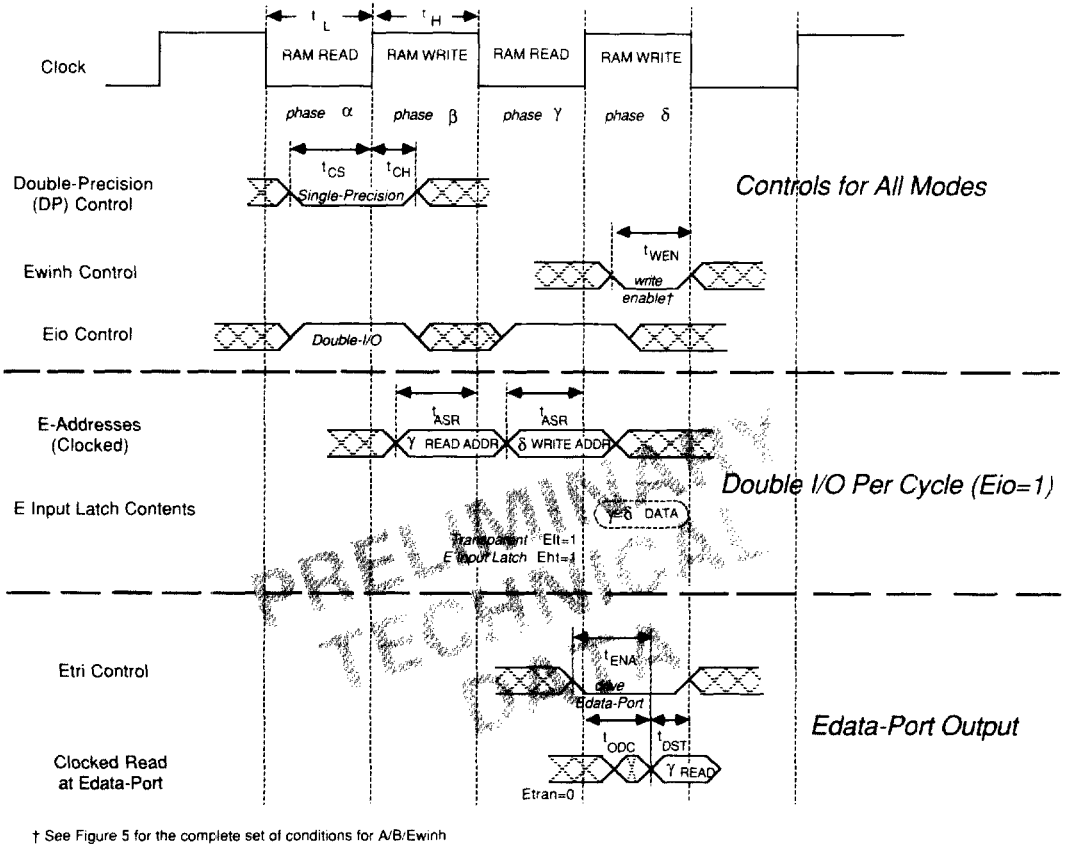
† See Figure 5 for the complete set of conditions for A B Ewinh

Figure 10. Single-Precision Timing for Register-to-Register Transfer via Edata-Port – Edata-Port in Single I/O per Cycle Mode (Eio = 0) and Transparent Inputs



† See Figure 5 for the complete set of conditions for A/B/Ewinh

Figure 11. Single-Precision Timing for Register-to-Register Transfer via Edata-Port – Edata-Port in Double I/O per Cycle Mode (Eio = 1) and Latched Inputs



† See Figure 5 for the complete set of conditions for A/B/Ewinh

Figure 12. Single-Precision Timing for Register-to-Register Transfer via Edata-Port – Edata-Port in Double I/O per Cycle Mode (Eio = 1) and Transparent Inputs

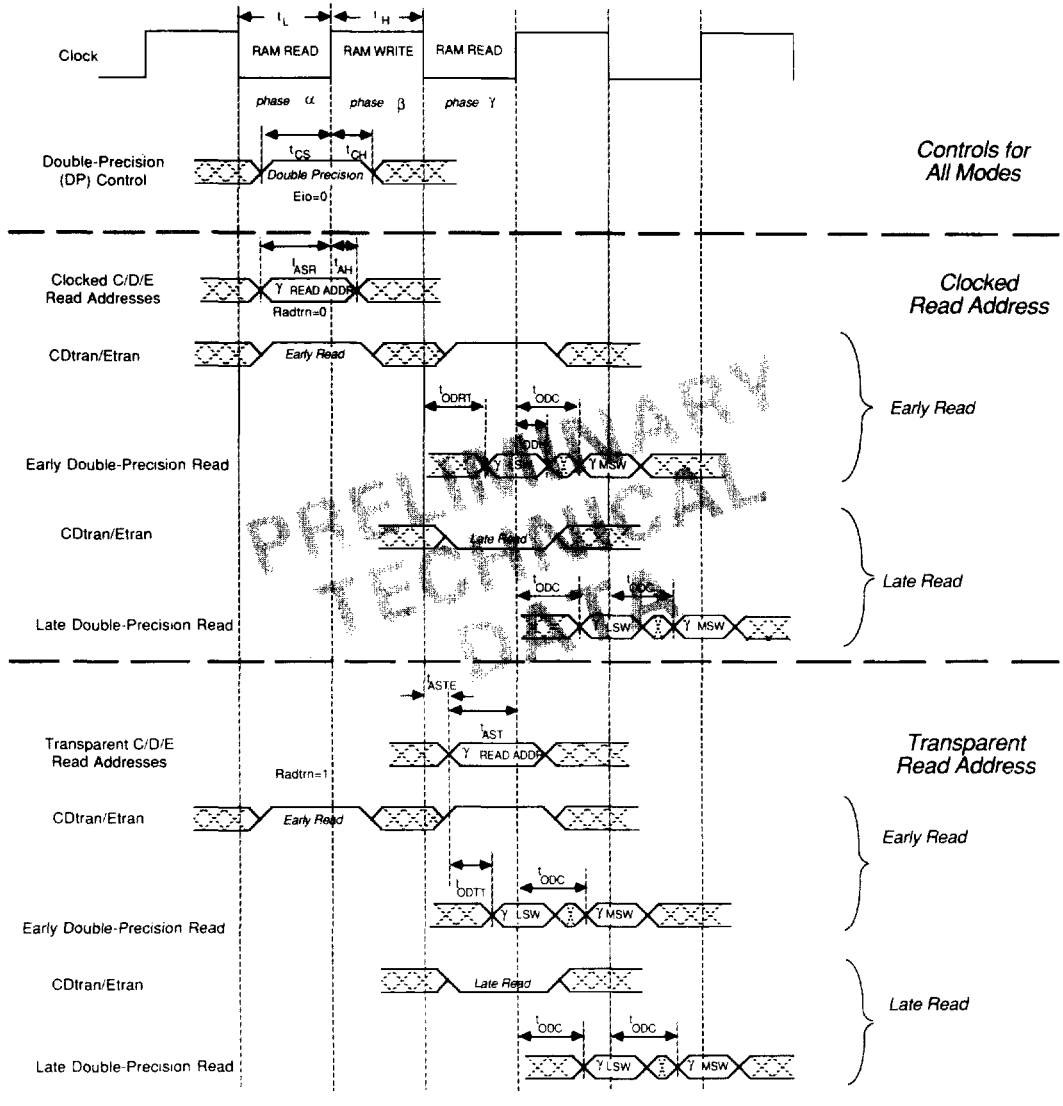


Figure 13. Double-Precision Read Output Timing.

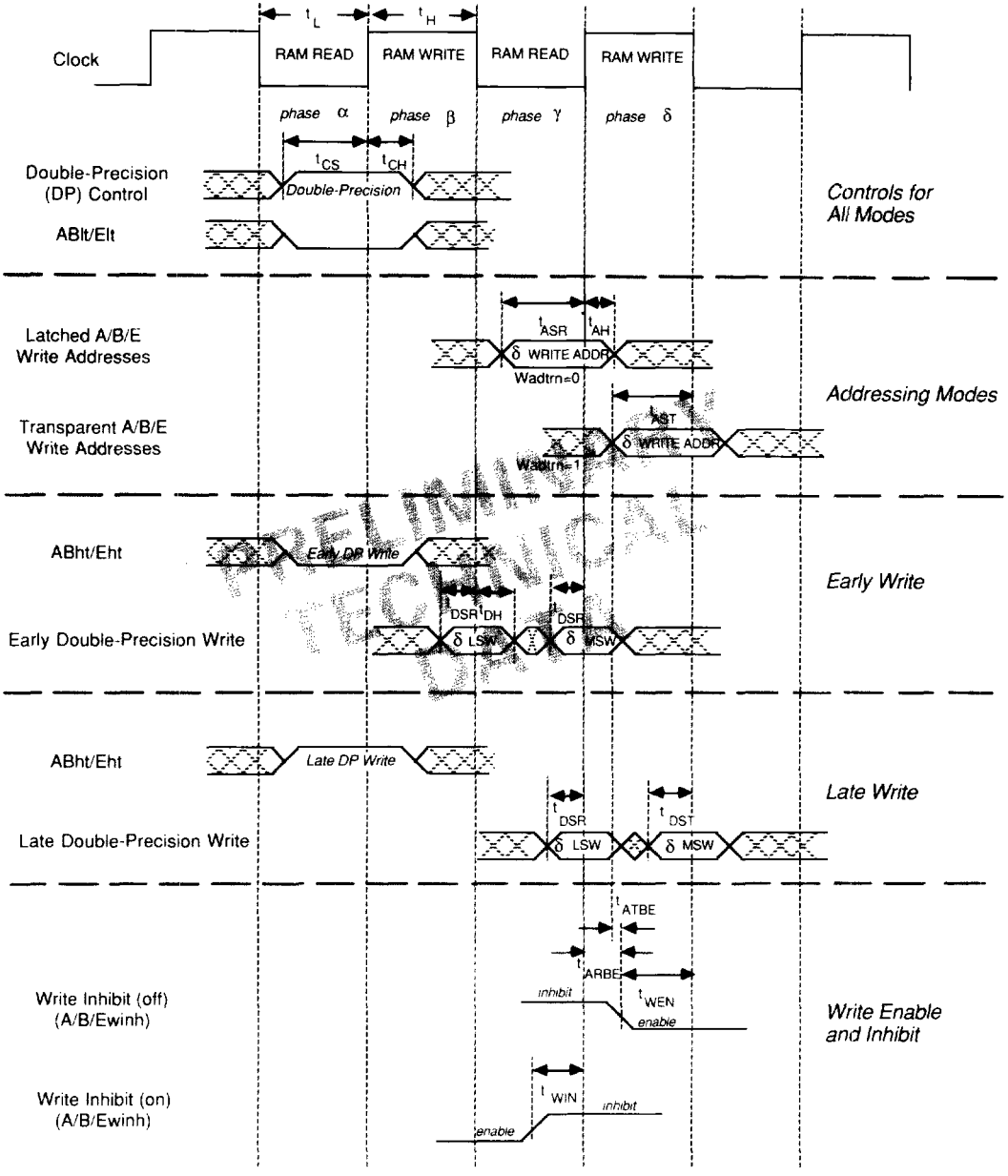


Figure 14. Double-Precision Normal Write Input Timing

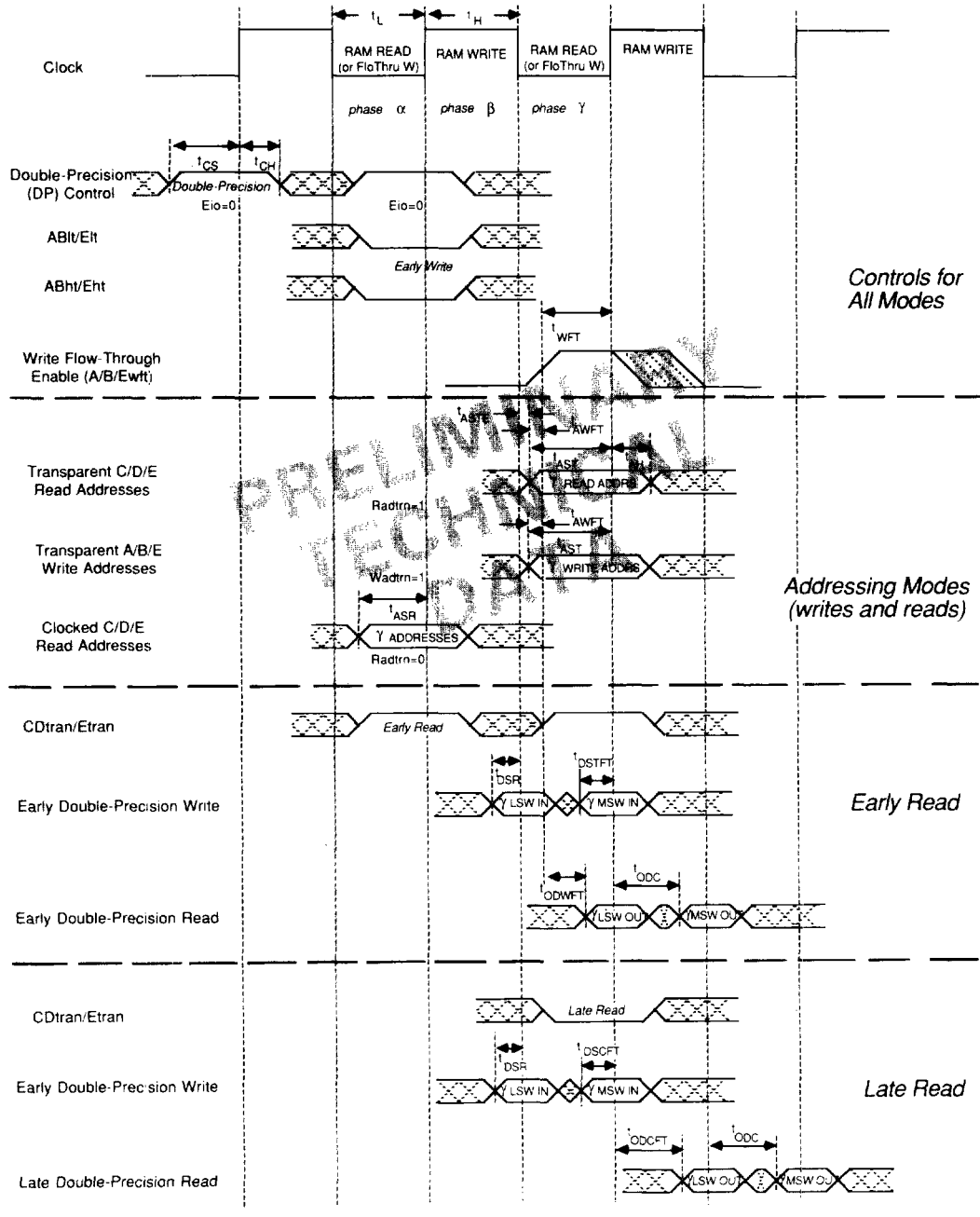


Figure 15. Double-Precision Write Flow-Through Time (Early DP Write Only)

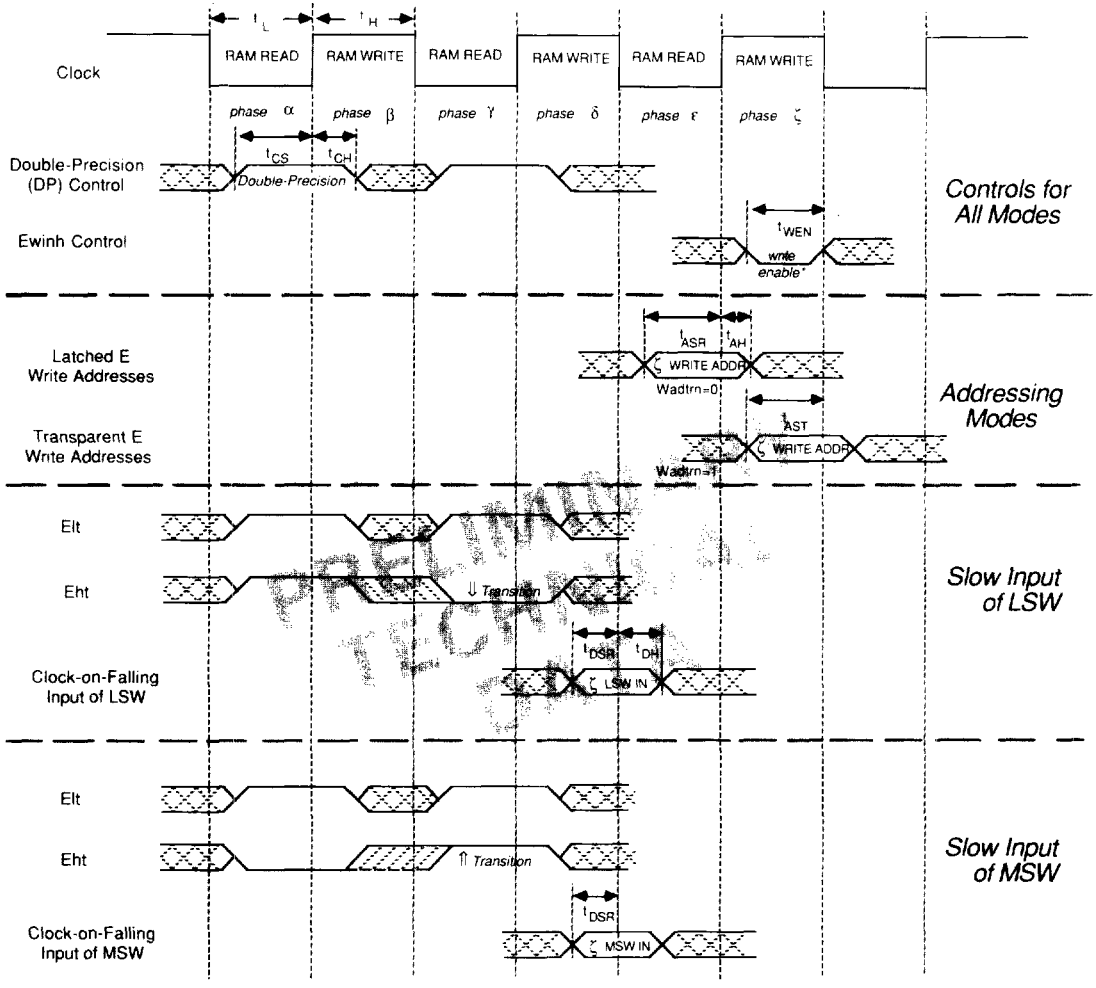


Figure 16. Double-Precision Slow Input Timing

*See Figure 14 for the complete set of conditions for A/B/Ewinh.

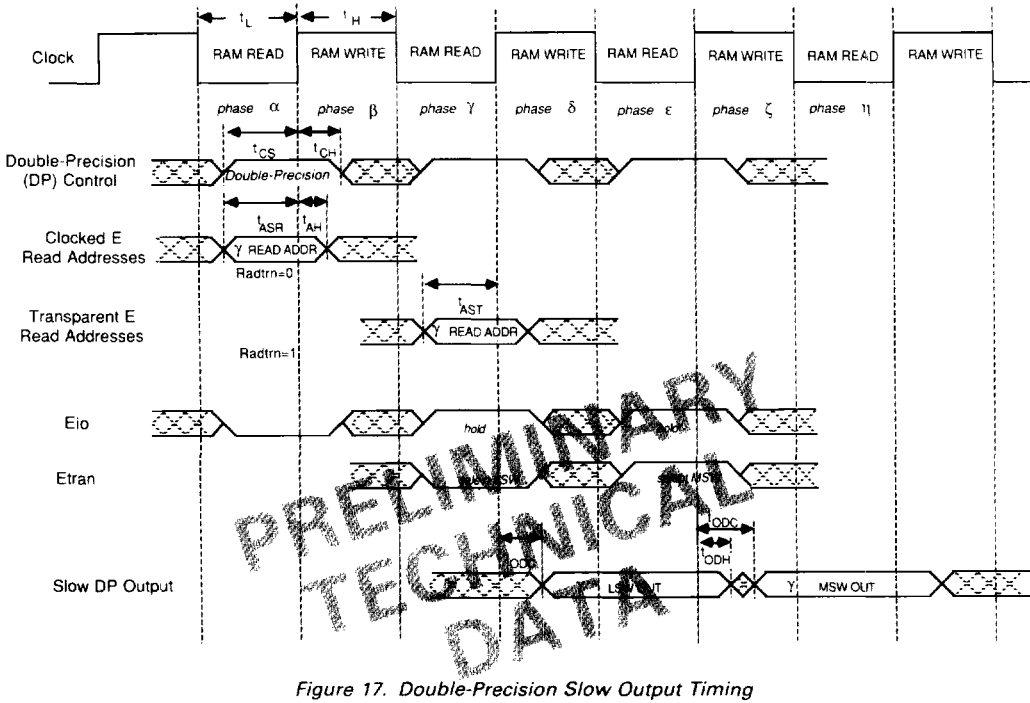


Figure 17. Double-Precision Slow Output Timing

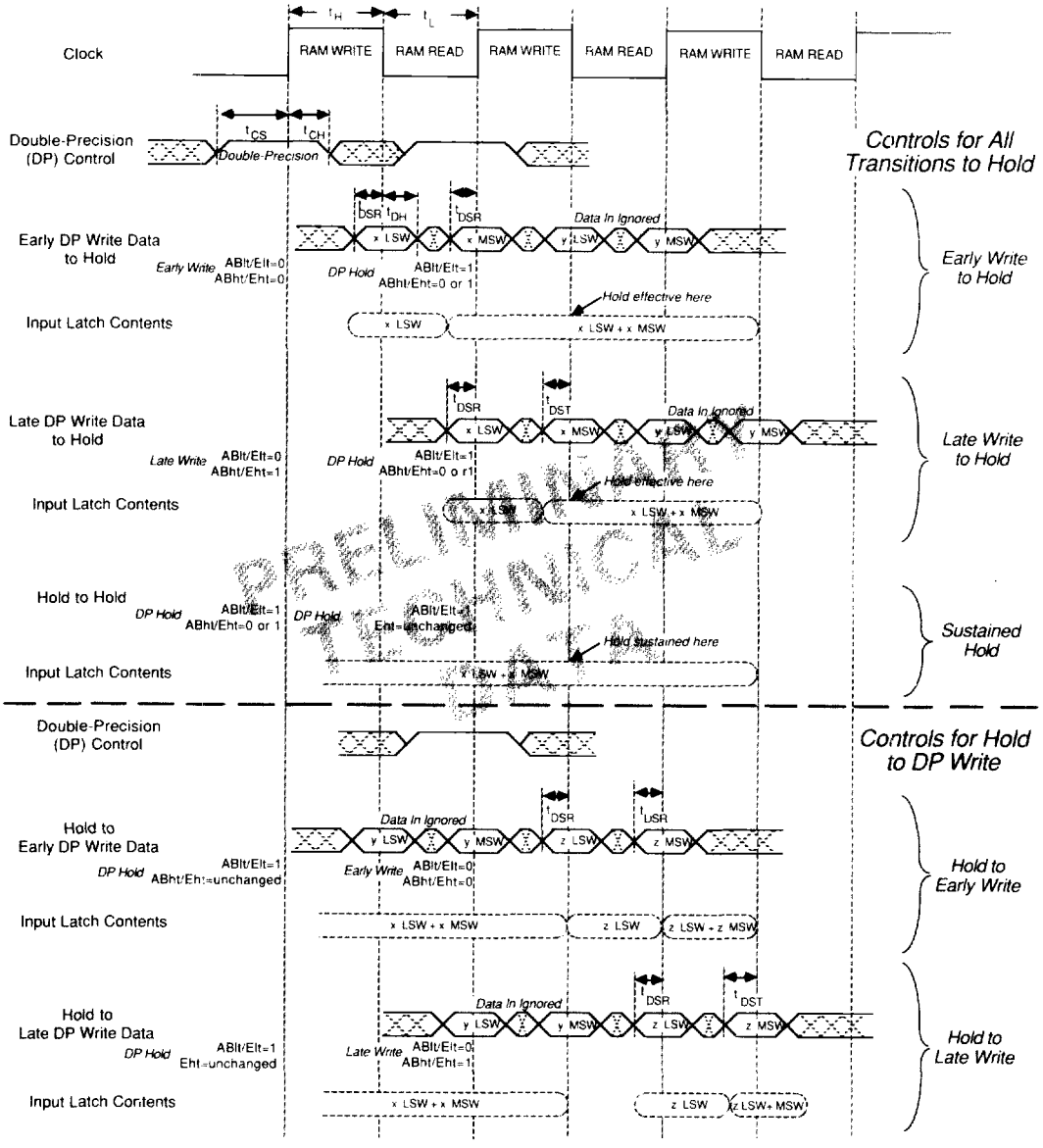


Figure 18. Double-Precision Write to Input Latches and Hold Timing

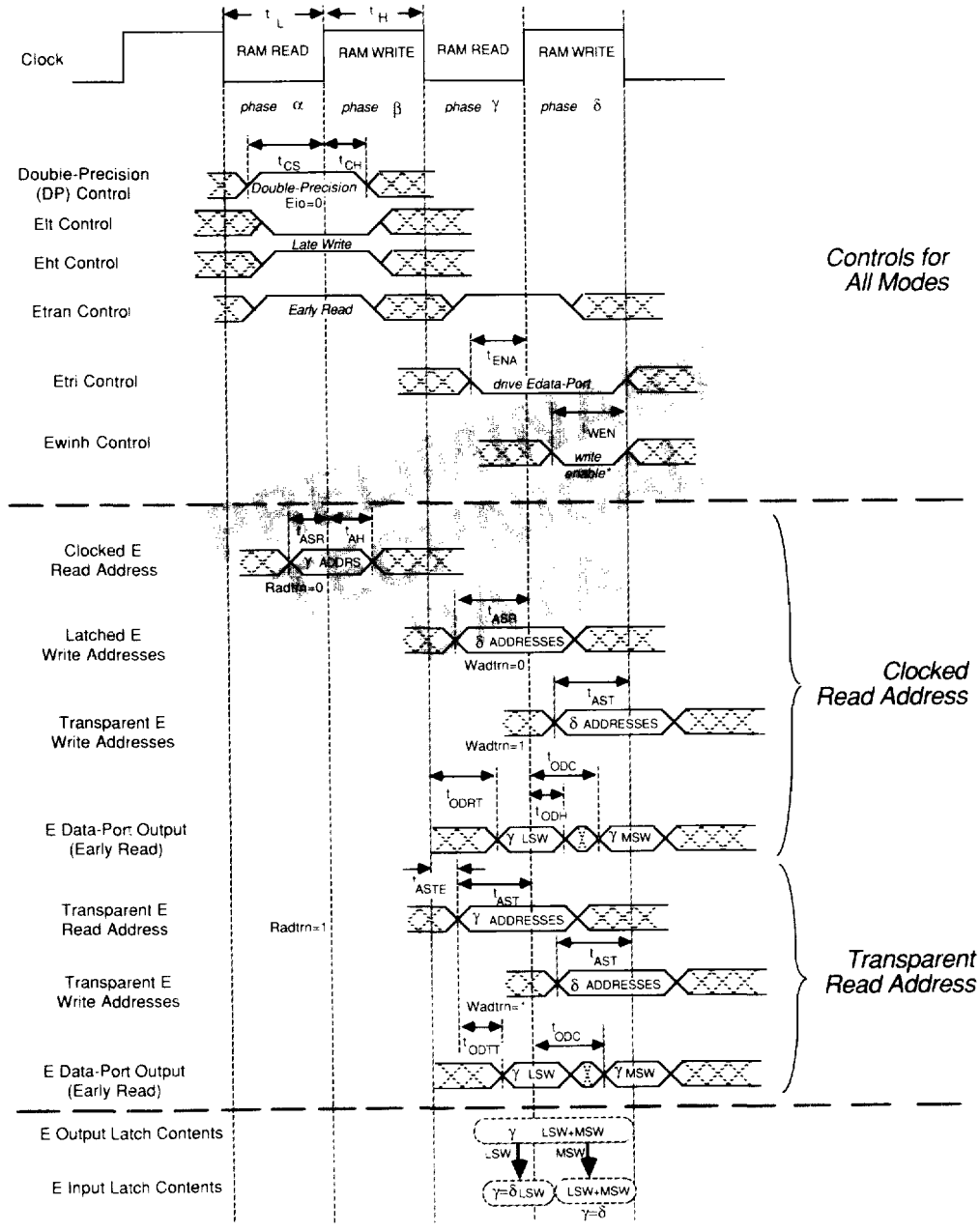


Figure 19. Double-Precision Timing for Register-to-Register Transfer via Edata-Port, Early Read Late Write Mode

*See Figure 14 for the complete set of conditions for A/B/Ewinh.

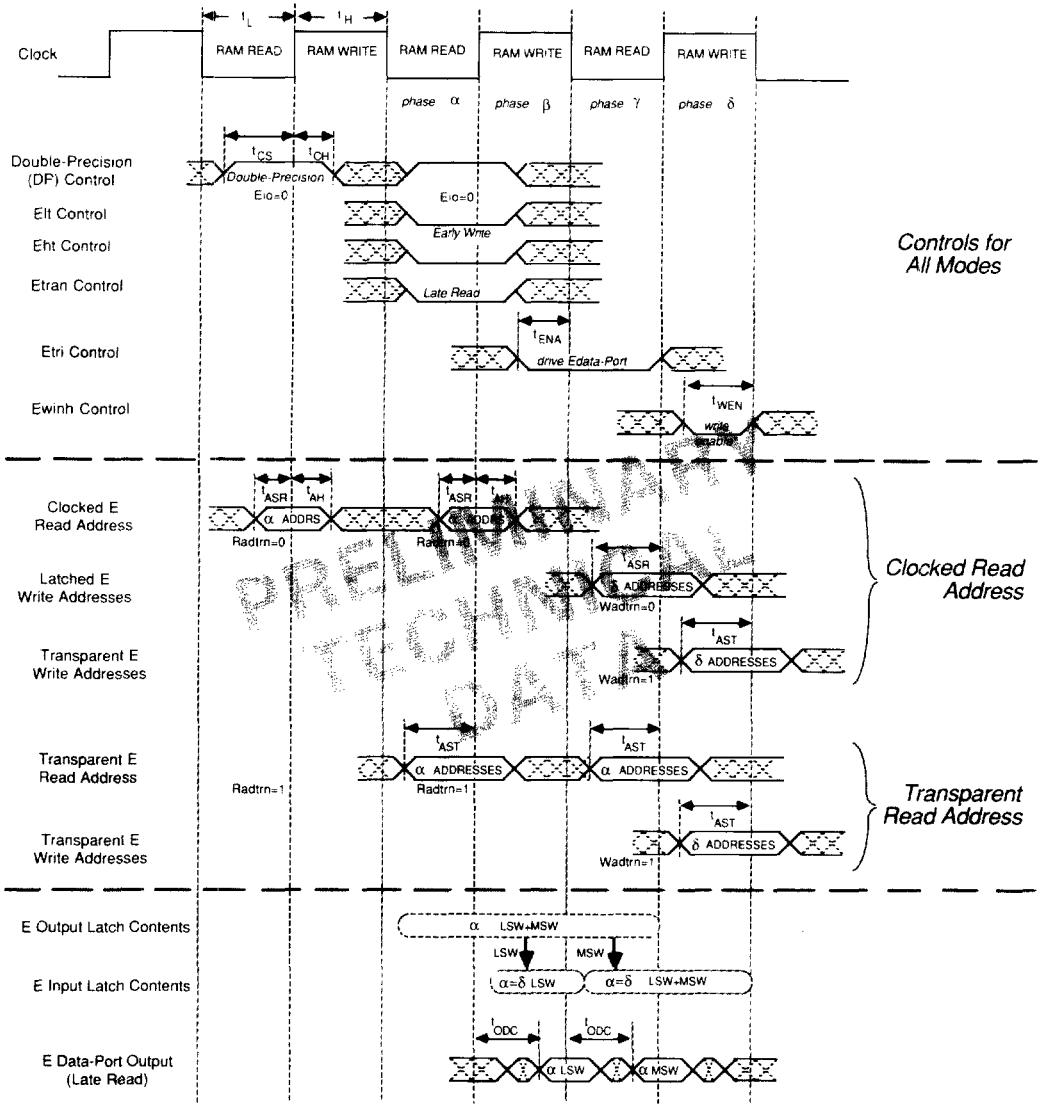


Figure 20. Double-Precision Timing for Register-to-Register Transfer via Edata-Port, Late Read Early Write Mode

*See Figure 14 for the complete set of conditions for A/B/Ewinh.

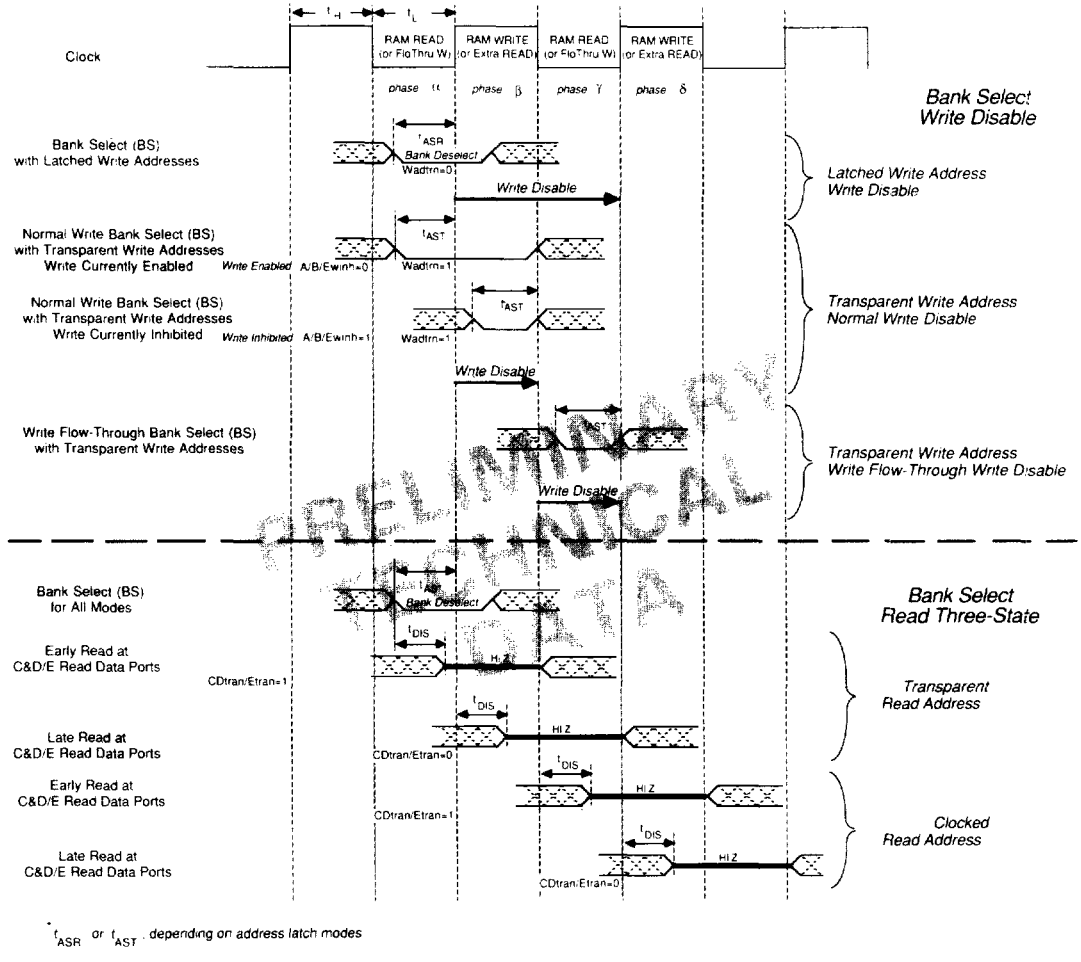


Figure 21. Chip Select Timing

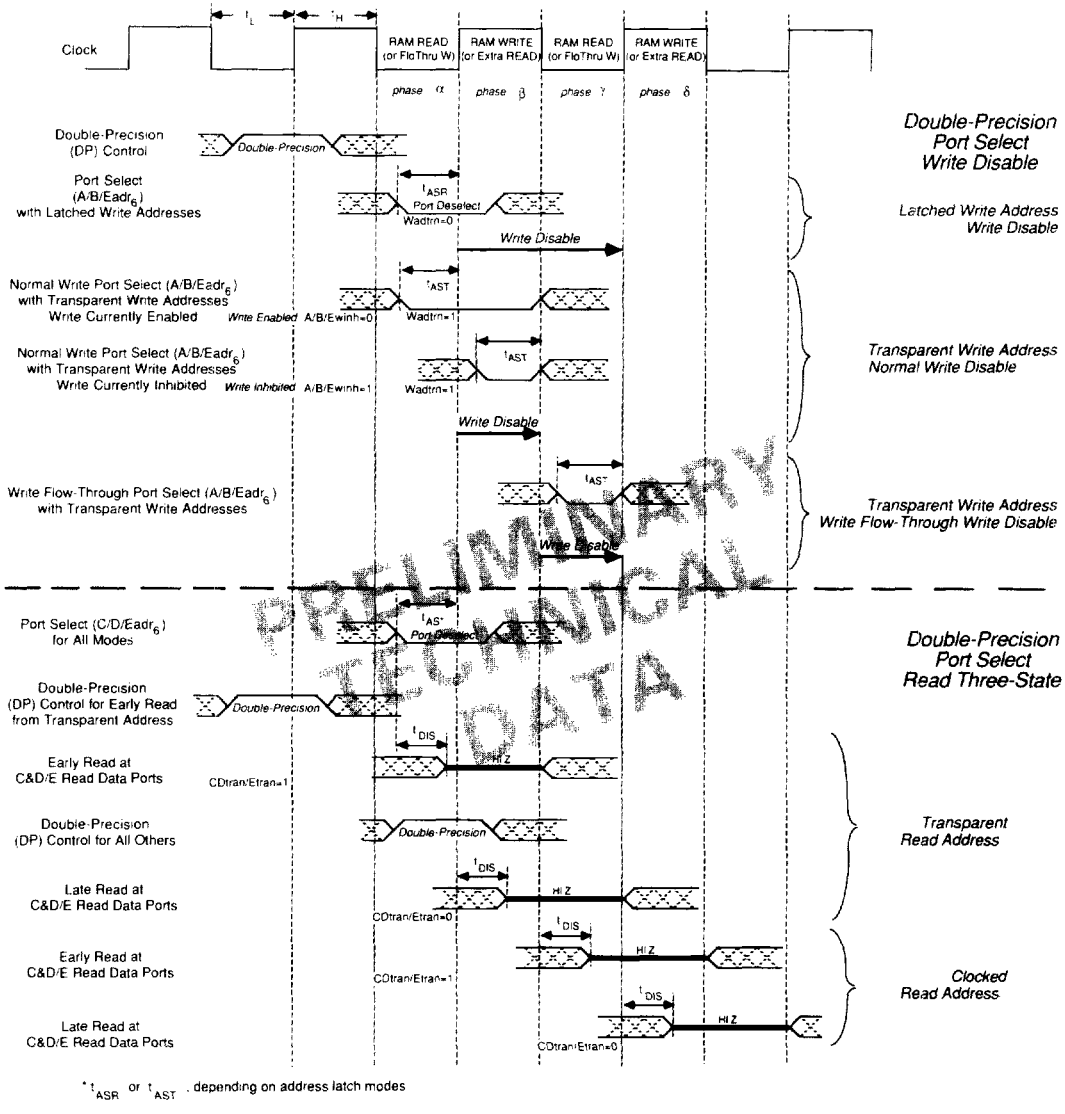
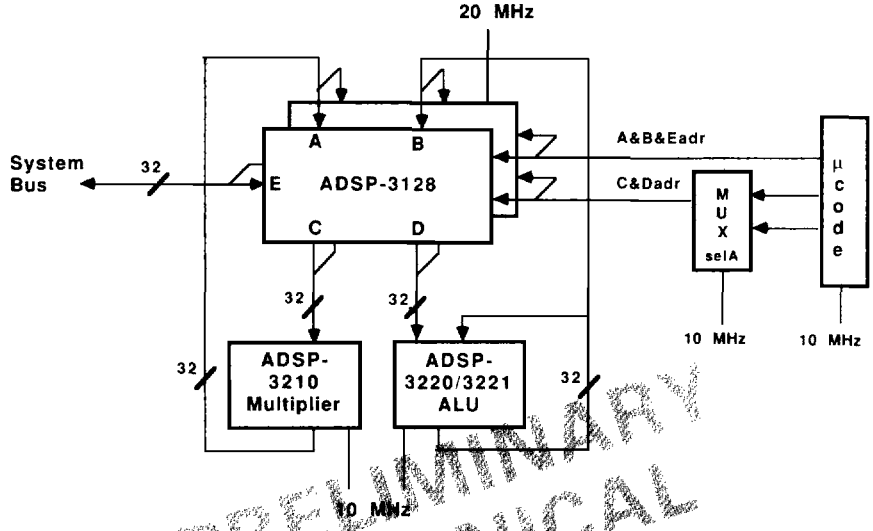
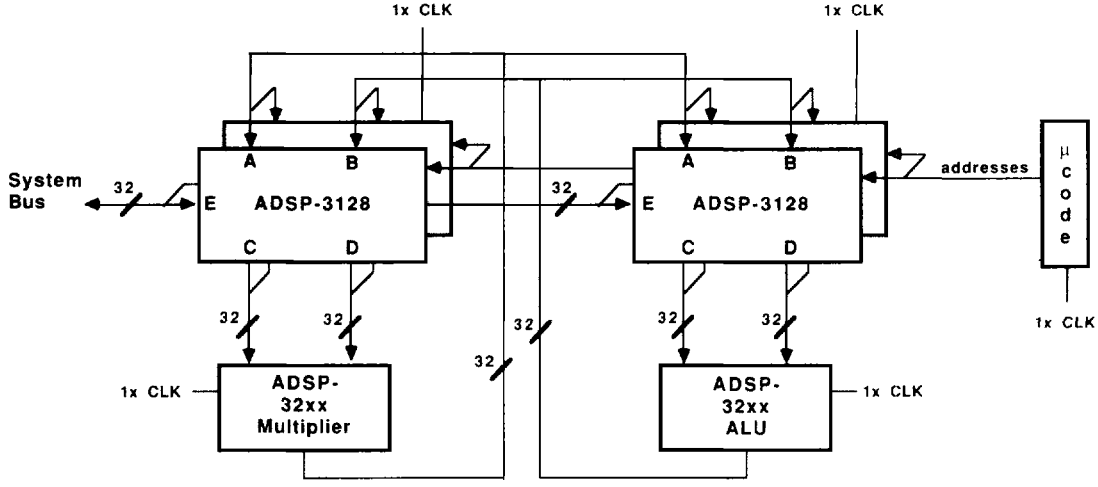


Figure 22. Port Select Timing



Muxing the read addresses allows two reads (per 10 MHz) for loading the input ports of both the ADSP-3210 and ADSP-3220/3221 with two 32-bit words per 3210/3220/3221 cycle (10MHz) while still using 10 MHz μcode rates. In this application, write data is latched on clock HI and read data is registered on the rising edge. Write addresses are latched; read addresses are transparent.

Figure 23. ADSP-3128 Single-Precision Applications with ADSP-3210/ADSP-3220/ADSP-3221. Microcode Operates at 10MHz



Double-Precision mode allows transfers of both MSW and LSW in a single cycle while still using μcode at the same cycle rate. Pairing pairs of ADSP-3128s creates a seven-port register file for unconstrained data transfers. The same data is always written to both the right and left pairs (therefore, the same A, B, and Eadrs go to both pairs). In this application, Early Writes are used at the input ports for the simplest interface to the floating-point chipset's output. The data read from the two sides is generally distinct, so the C and Dadrs for each pair are distinct. Late Reads match the input loading requirements of these chips and are therefore used on the rightmost pair of ADSP-3128s.

Figure 24. ADSP-3128 Seven-Port Double-Precision Application with ADSP-3211 and ADSP-3220/ADSP-3221. Microcode Operates at 10MHz

SPECIFICATIONS[1]

RECOMMENDED OPERATING CONDITIONS

Parameter		ADSP-3128 J and K Grades Min	Max	ADSP-3128 S and T Grades[2] Min	Max	Unit
V_{DD}	Supply Voltage	4.75	5.25	4.5	5.5	V
T_{AMB}	Operating Temperature (Ambient)	0	+70	−55	+125	°C

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	ADSP-3128 J and K Grades Min	Max	ADSP-3128 S and T Grades[2] Min	Max	Unit
V_{IH}	High-Level Input Voltage	@ V_{DD} = max	2.0		2.0		V
V_{IHA}	High-Level Input Voltage, CLK and All Asynchronous Inputs	@ V_{DD} = max	2.4		2.6		V
V_{IL}	Low-Level Input Voltage	@ V_{DD} = min		0.8		0.8	V
V_{OH}	High-Level Output Voltage	@ V_{DD} = min & I_{OH} = −1.0mA	2.4		2.4		V
V_{OL}	Low-Level Output Voltage	@ V_{DD} = min & I_{OL} = 4.0mA		0.4		0.6	V
I_{IH}	High-Level Input Current, All Inputs	@ V_{DD} = max & V_{IN} = 5.0V		10		10	µA
I_{IL}	Low-Level Input Current, All Inputs	@ V_{DD} = max & V_{IN} = 0V		10		10	µA
I_{OZ}	Three-State Leakage Current	@ V_{DD} = max, High Z, V_{IN} = 0V or max					µA
I_{DD}	Supply Current	@ max clock rate; TTL inputs					mA
I_{DD}	Supply Current-Quiescent	All V_{IN} = 0V; High Z Output					µA
I_{DD}	Supply Current-Quiescent	All V_{IN} = 2.4V					mA

ORDERING INFORMATION

Part Number	Temperature Range	Package	Package Outline
ADSP-3128JG	0 to +70°C	144-Pin Grid Array	G-144A
ADSP-3128KG	0 to +70°C	144-Pin Grid Array	G-144A
ADSP-3128SG	−55°C to +125°C	144-Pin Grid Array	G-144A
ADSP-3128TG	−55°C to +125°C	144-Pin Grid Array	G-144A
ADSP-3128SG/+	−55°C to +125°C	144-Pin Grid Array	G-144A
ADSP-3128TG/+	−55°C to +125°C	144-Pin Grid Array	G-144A
ADSP-3128SG/883B	−55°C to +125°C	144-Pin Grid Array	G-144A
ADSP-3128TG/883B	−55°C to +125°C	144-Pin Grid Array	G-144A

Contact DSP Marketing in Norwood concerning the availability of other package types.

SWITCHING CHARACTERISTICS

		ADSP-3128								
		J Grades 0 to 70°C		K Grades 0 to 70°C		S Grades[2] −55°C to +125°C		T Grades[2] −55°C to +125°C		
		Min	Max	Min	Max	Min	Max	Min	Max	Unit
t_{CLK}	Clock Period – Clocked Reads									ns
t_{CLKFT}	WFT Clock Period – Clked Reads									ns
t_{CLKS}	Clock Period – Trans Reads									ns
t_{CLKSFT}	WFT Clock Period – Transparent Reads									ns
t_{CLKA}	Clock Period – Transparent I/O									ns
t_{CLKAFT}	WFT Clock Period – Transparent I/O									ns
t_L	Clock LO Period									ns
t_H	Clock HI Period									ns
t_{HIER}	Clock HI Period – Write plus Extra Read									ns
t_{LOWR}	Clock LO Period – Write Flow-Through									ns
t_{CS}	Control Setup									ns
t_{CH}	Control Hold									ns
t_{AST}	Transparent Address Setup									ns
t_{ASTE}	Trans Address Max Usable Setup									ns
t_{ASR}	Registered Address Setup									ns
t_{AH}	Address Hold									ns
t_{ENA}	Three-State Enable Delay									ns
t_{DIS}	Three-State Disable Delay									ns
t_{EDIS}	Three-State Eport Auto Disable									ns
t_{ODTT}	Trans Adr-to-Trans Output Delay									ns
t_{ODC}	Clk-to-Data Output Delay									ns
t_{ODRT}	Clkd Adr-to-Trans Output Delay									ns
t_{ODH}	Output Data Hold									ns
t_{DSR}	Latched Data Setup									ns
t_{DST}	Transparent Data Setup									ns
t_{DSN}	Clock-on-Falling Data Setup									ns
t_{DH}	Input Data Hold									ns
t_{WEN}	Write Inhibit-to-Enable Setup									ns
t_{WIN}	Write Enable-to-Inhibit Setup									ns
t_{ATBE}	Trans Adr to Write Enable									ns
t_{ARBE}	Clock to Write Enable									ns
t_{WFT}	Write Flow-Through Setup									ns
t_{AWFT}	Trans Adr to WFT									ns
t_{DSTFT}	WFT Data Setup – Trans Read									ns
t_{DSCFT}	WFT Data Setup – Clkd Read									ns
t_{ODCFT}	WFT Clk-to-Data Output Delay									ns
t_{ODTFT}	WFT Address to Trans Data									ns
t_{ODWFT}	WFT to Trans Data									ns

NOTES

[1]All min and max specifications are over power-supply and temperature range indicated. Input levels are GND and 3.0V. Rise times are 5ns. Input timing reference levels and output reference levels are 1.5V, except for t_{ENA} and t_{DIS} which are as indicated in Figure 3 and t_{EDIS} in Figure 7. Input timing reference levels and output reference levels are 1.5V, except for 1) t_{ENA} and t_{DIS} which are as indicated in Figure 3 and t_{EDIS} in Figure 7 and 2) t_{DS} and t_{DH} which are measured from clock V_{IHA} to data input V_{IH} or V_{IL} crossing points.

[2]S and T grade parts are available processed in accordance with MIL-STD-883, Class B. The processing and test methods used for S/883B and T/883B versions of the ADSP-3128 can be found in Analog Devices Military Databook. S and T grade parts are also available with optional high-reliability "PLUS" processing as shown in Figure 26. Regular S and T grade parts are tested at +125°C.

Specifications subject to change without notice.

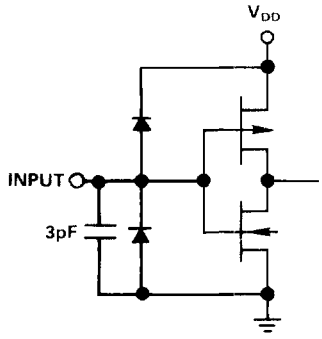


Figure 25. Equivalent Input Circuits

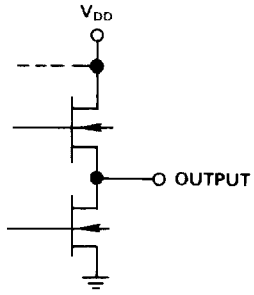


Figure 26. Equivalent Output Circuits

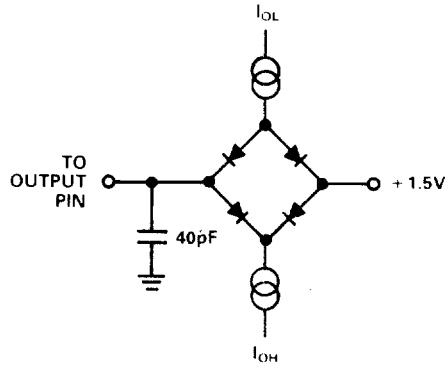


Figure 27. Normal Load for ac Measurements

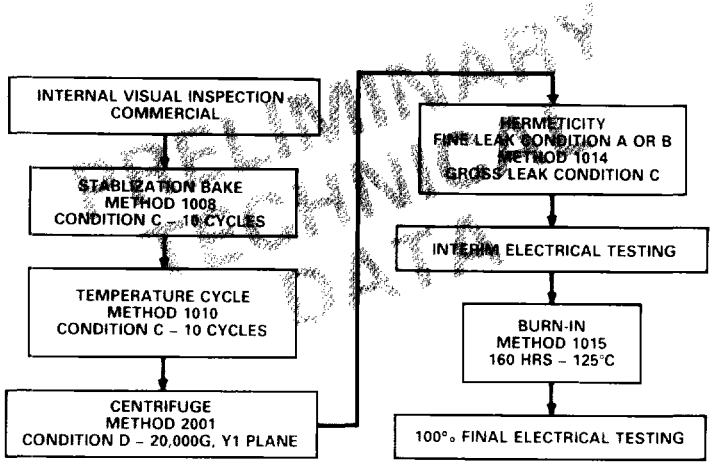


Figure 28. PLUS Processing Flow

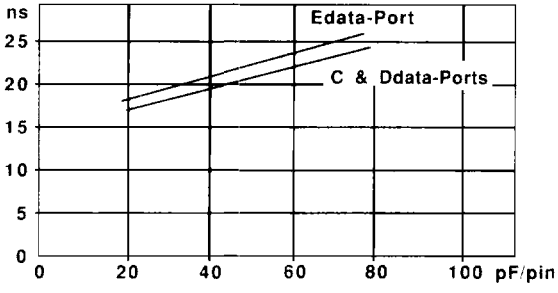


Figure 29. Clocked Output Delay as a Function of Load Capacitance

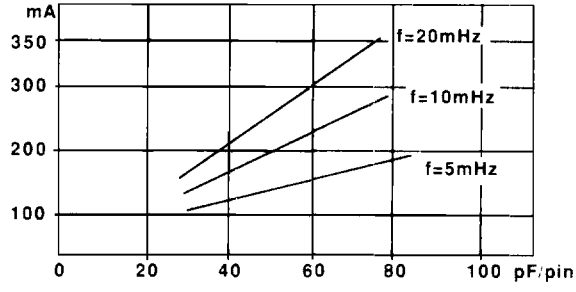
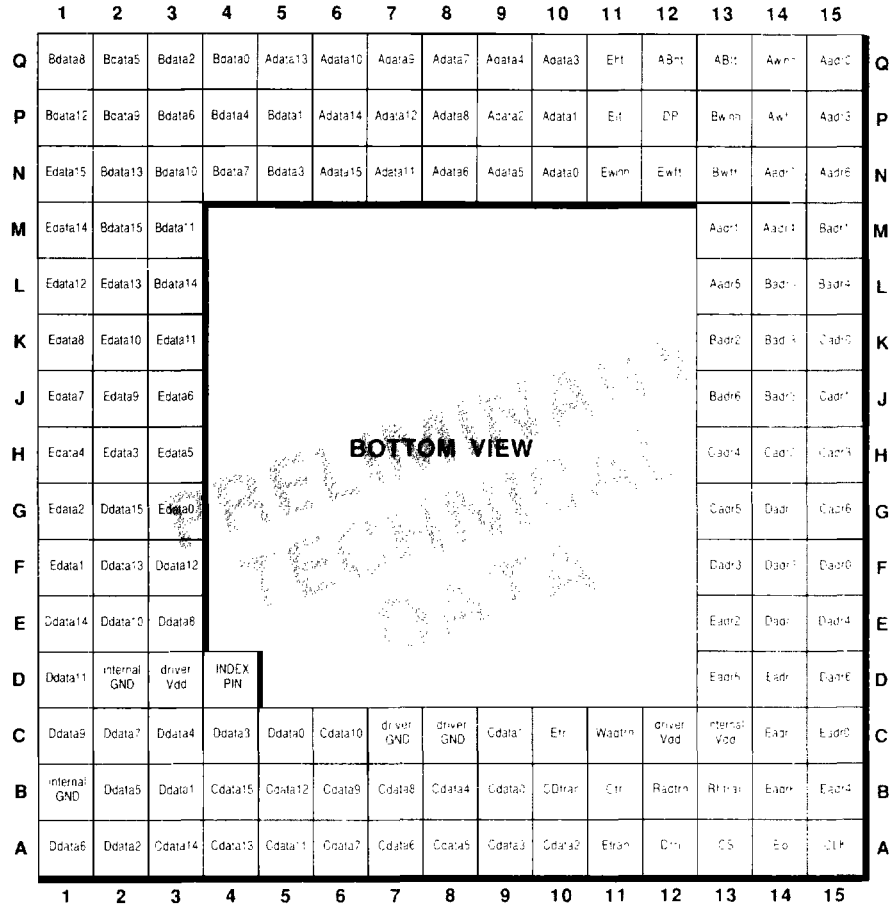


Figure 30. Typical Current Consumption as a Function of Load Capacitance, All Outputs Switching



ADSP-3128 Pin Configuration