256 Megabit CMOS DDR SDRAM
DPDD16MX16TSBY5

ADVANCED INFORMATION

DESCRIPTION:

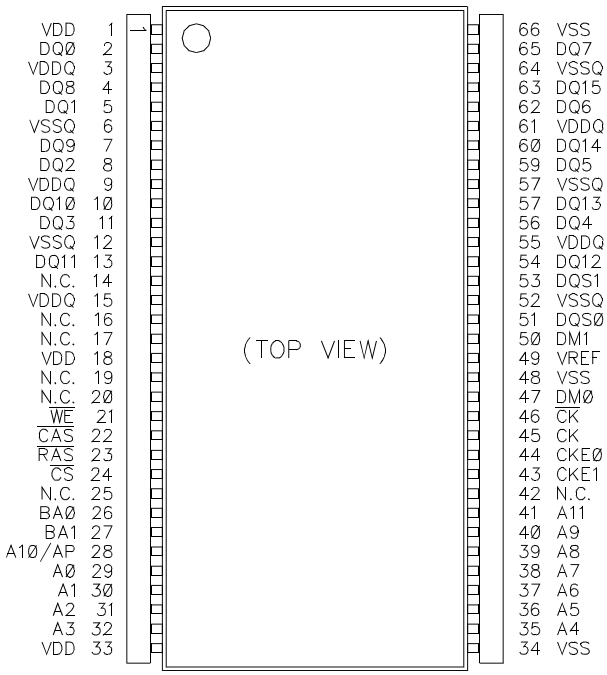
The *LP-Stack*™ series is a family of interchangeable memory devices. The 256 Megabit Double Data Rate Synchronous DRAM is a member of this family which utilizes the new and innovative space saving TSOP stacking technology. The devices are constructed with two 16 Meg x 8 DDR SDRAM's.

The 256 Megabit *LP-Stack*™ modules DPDD16MX16TSBY5, based on 128 Megabit devices, has been designed to fit in the same footprint as the 16 Meg x 8 DDR SDRAM TSOP monolithic. This allows for system upgrade without electrical or mechanical redesign. Providing an immediate and low cost memory solution.

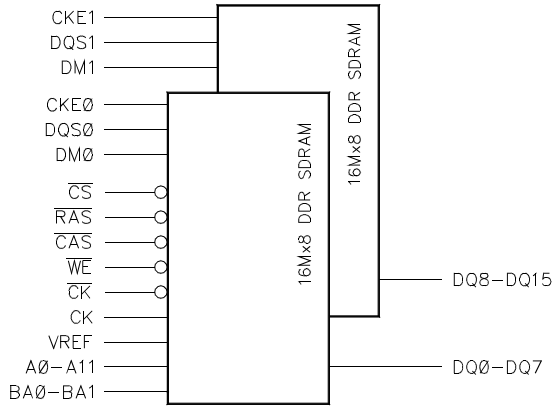
FEATURES:

- Configurations Available:
  16 Meg x 16 (2 Banks of 4 Meg x 8 bits x 4)
- Clock Frequencies:
  100, 125, 133, 143 MHz
- 2.5 Volt DQ Supply
- JEDEC Standard SSTL_2 Interface for all Inputs/Outputs
- Four Bank Operation
- Programmable Burst Type:
  Burst Length and Read Latency
- Refresh:
  4096 Cycles/64ms
- Refresh Types:
  Auto and Self
- JEDEC Approved Footprint and Pinout
- Package:
  66-Pin Leadless TSOP Stack

PIN-OUT DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



PIN NAMES	
A0 - A11	Row Address: A0 - A11 Column Address: A0 - A9
BA0,BA1	Bank Select Address
A10 / AP	Auto Precharge
DQ0 - DQ15	Data In / Data Out
$\overline{CAS}$	Column Address Strobe
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Data Write Enable
CK, $\overline{CK}$	Differential Clock Inputs
CKE0, CKE1	Clock Enables
DQS0, DQS1	Data Strobes
DM0, DM1	Data Masks
V_{DD}	Power Supply (+2.5V)
V_{SS}	Ground
V_{DDQ}	DQ Power Supply (+2.5V)
V_{SSQ}	DQ Ground
V_{REF}	Reference Voltage for Inputs
N.C.	No Connect
NU	Not Used

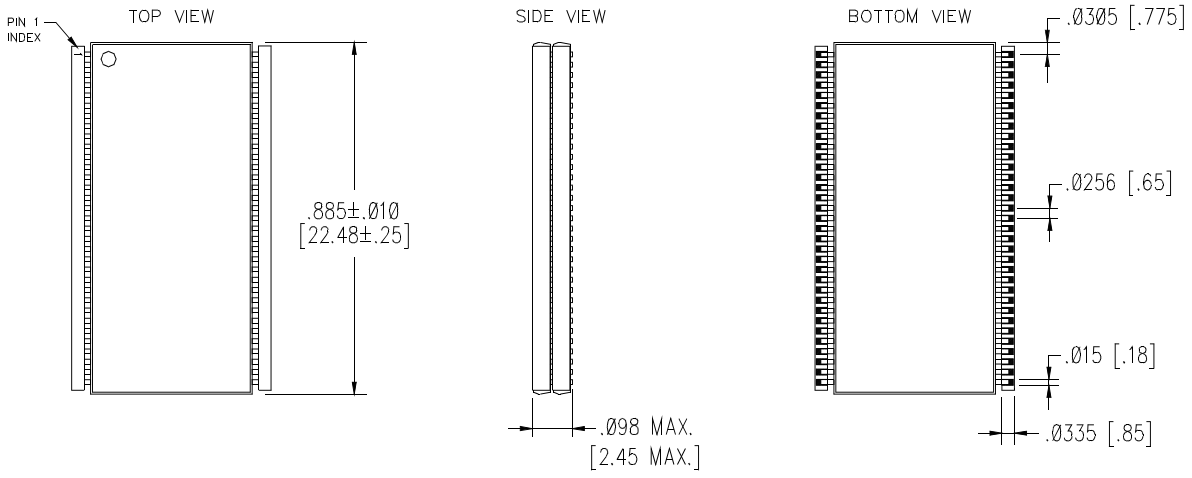
ADVANCED INFORMATION

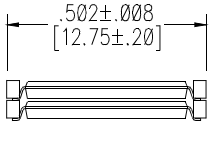
ORDERING INFORMATION

DP	DD	16M	X	16	T	S	B	Y5	–	DP	–	XX	XX	XX
PREFIX	TYPE	MEMORY DEPTH	DESIG	MEMORY WIDTH	DESIG	I/O TYPE	DEVICE WIDTH	PACKAGE		SUPPLIER		MFR ID	CYCLE TIME	CAS LATENCY

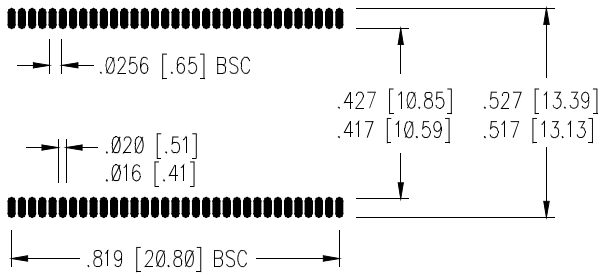
- CAS LATENCY: 15 = CAS LATENCY 1.5; 20 = CAS LATENCY 2.0; 25 = CAS LATENCY 2.5
- CYCLE TIME: 07 = 7ns (143MHz); 75 = 7.5ns (133MHz); 08 = 8ns (125MHz); 10 = 10ns (100MHz)
- MFR ID: MANUFACTURER CODE*
- SUPPLIER: SUPPLIER CODE*
- PACKAGE: STACKABLE TSOP
- DEVICE WIDTH: x8 MEMORY BASED
- I/O TYPE: SSTL INPUTS/OUTPUTS
- MEMORY DEPTH: 128 MEGABIT BASED
- DESIG: MEMORY MODULE WITHOUT SUPPORT LOGIC
- TYPE: DOUBLE DATA RATE SYNCHRONOUS DRAM

MECHANICAL DRAWING





Standard TSOP pad layout is acceptable, however, when possible, the following pad layout is recommended for optimal manufacture and inspection. See Application Note 53A001–00 for further information.



dense-pac microsystems, inc.

7321 lincoln way, garden grove, california 92841-1431 • (714) 898-0007 • (800) 642-4477 • fax: (714) 897-1772 • http://www.dense-pac.com