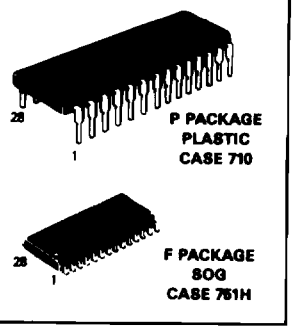
MCM60L256A-C

Advance Information

32K × 8 Bit CMOS Static Random Access Memory

Extended Temperature Range: – 40 to 85°C



4

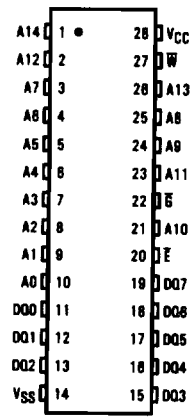
The MCM60L256A-C is a 262,144 bit low-power static random access memory organized as 32,768 words of 8 bits, fabricated using silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides greater reliability. The operating current is 5 mA/MHz (typ) and the cycle time is 100 ns. For long cycle times (>100 ns), the automatic power down (APD) circuitry will temporarily shut down various power consuming circuits, thereby reducing the active power consumption.

Chip enable ($\overline{E}$) controls the power-down feature. It is not a clock but rather a chip control that affects power consumption. When $\overline{E}$ is a logic high, the part is placed in low power standby mode. The maximum standby current is 2 μA (T_A = 25°C). Chip enable also controls the data retention mode. Another control feature, output enable ($\overline{G}$) allows access to the memory contents as fast as 50 ns. Thus the MCM60L256A-C is suitable for use in various microprocessor application systems where high speed, low power, and battery backup are required.

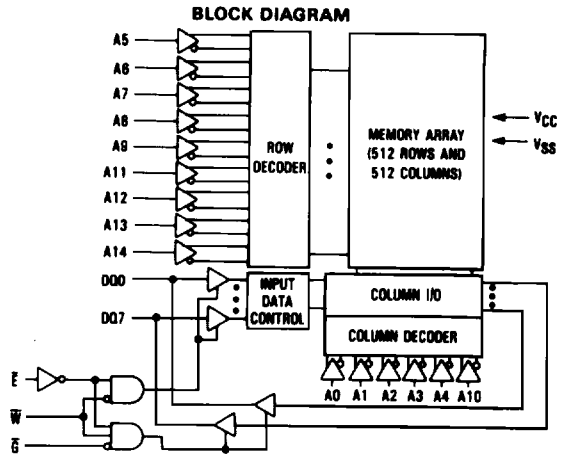
The MCM60L256A-C is offered in a 28 pin, 600 mil plastic dual-in-line package and a 330 mil gull-wing SO package.

- Single 5 V Supply, ± 10%
- 32K × 8 Organization
- Fully Static — No Clock or Timing Strobes Necessary
- Low Power Dissipation—27.5 mW/MHz (Typical Active)
- Output Enable and Chip Enable Inputs for More System Design Flexibility and Low Power Standby Mode
- Battery Backup Capability (Maximum Standby Current = 2 μA @ 25°C)
- Data Retention Supply Voltage = 2.0 V to 5.5 V
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Time: MCM60L256A-C10 = 100 ns (Max)

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES	
A0-A14	Address
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

This document contains information on a new product. Specifications and information herein are subject to change without notice.

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	Supply Current	I/O Pin
H	X	X	Not Selected	I_{SB}	High Z
L	H	H	Output Disabled	I_{CC}	High Z
L	L	H	Read	I_{CC}	D_{out}
L	X	L	Write	I_{CC}	D_{in}

X = don't care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC}	−0.3 to +7.0	V
Voltage to Any Pin with Respect to V_{SS}		V_{in}, V_{out}	−0.5 to V_{CC} +0.5	V
Power Dissipation (T_A = 25°C)	PDIP SOG	P_D	1.0 0.6	W
Operating Temperature		T_A	−40 to +85	°C
Storage Temperature		T_{stg}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = −40 to 85°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	−0.3*	—	0.8	V

*V_{IL} (min) = −0.3 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤50 ns)

DC CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	—	<0.01	±1.0	μA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH} or $\overline{W}$ = V_{IL}, V_{out} = 0 to V_{CC})		$I_{lkg(O)}$	—	<0.01	±1.0	μA
Operating Current (Read Cycle) ($\overline{E}$ = V_{IL}, $\overline{W}$ = V_{IH}, Other Input = V_{IH}/V_{IL}, I_{out} = 0 mA)	t_{AVQV} = 1 μs t_{AVQV} = 100 ns	I_{CCA1}	— —	10 —	15 70	mA
($\overline{E}$ = 0.2 V, $\overline{W}$ = V_{CC} − 0.2 V, Other Input = V_{CC} − 0.2 V/0.2 V, I_{out} = 0 mA)	t_{AVQV} = 1 μs t_{AVQV} = 100 ns	I_{CCA2}	— —	5 —	8 60	
Standby Current ($\overline{E}$ = V_{IH})		I_{SB1}	—	—	3.0	mA
Standby Current ($\overline{E}$ ≥ V_{CC} − 0.2 V, V_{CC} = 2.0 to 5.5 V) (T_A = 25°C)		I_{SB2}	— —	2 —	100 2	μA
Output Low Voltage (I_{OL} = 4.0 mA)		V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = −1.0 mA)		V_{OH}	2.4	—	—	V

Typical values are referenced to T_A = 25°C and V_{CC} = 5.0 V

CAPACITANCE (f = 1 MHz, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Min	Max	Unit
Input Capacitance (V_{in} = 0 V)	All Inputs Except DQ	C_{in}	—	10	pF
I/O Capacitance ($V_{I/O}$ = 0 V)	DQ	$C_{I/O}$	—	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = −40 to 85°C, Unless Otherwise Noted)

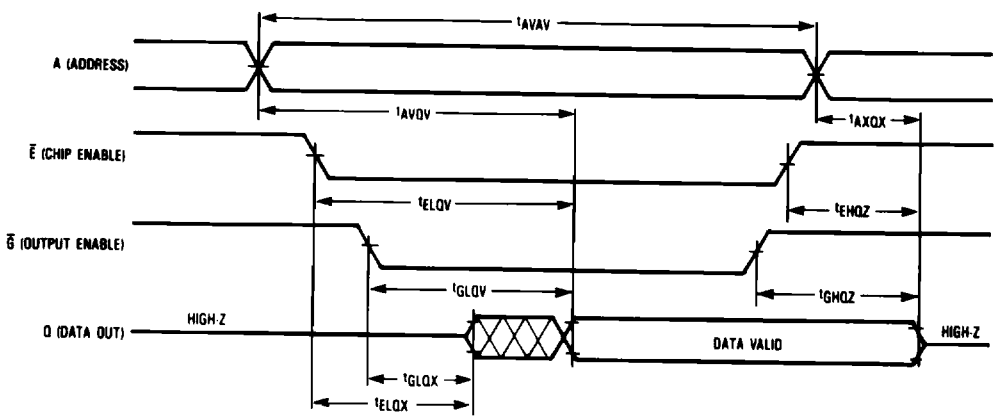
Input Pulse Levels . . . . . 0.6 V, 2.4 V
Input Rise/Fall Time . . . . . 5 ns
Input Timing Measurement Reference Levels . . . . . 1.5 V
Output Timing Measurement Reference Levels . . . . . 0.8 and 2.2 V
Output Load . . . . . See Figure 1

READ CYCLE (See Note 1)

Parameter	Symbol	Alt Symbol	Min	Max	Unit	Notes
Read Cycle Time	t_{AVAV}	t_{RC}	100	–	ns	–
Address Access Time	t_{AVQV}	t_{AA}	–	100	ns	–
$\overline{E}$ Access Time	t_{ELQV}	t_{AC}	–	100	ns	–
$\overline{G}$ Access Time	t_{GLQV}	t_{OE}	–	50	ns	–
Output Hold from Address Change	t_{AXQX}	t_{OH}	10	–	ns	–
Chip Enable to Output Low-Z	t_{ELQX}	t_{CLZ}	10	–	ns	2, 3
Output Enable to Output Low-Z	t_{GLQX}	t_{OLZ}	5	–	ns	2, 3
Chip Enable to Output High-Z	t_{EHQZ}	t_{CHZ}	0	35	ns	2, 3
Output Enable to Output High-Z	t_{GHQZ}	t_{OHZ}	0	35	ns	2, 3

NOTES:
1. $\overline{W}$ is high at all times for read cycles.
2. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 100 mV transition from the previous steady state voltage.
3. These parameters are periodically sampled and not 100% tested.

READ CYCLE



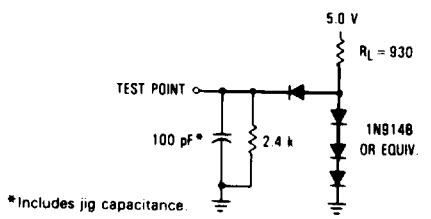


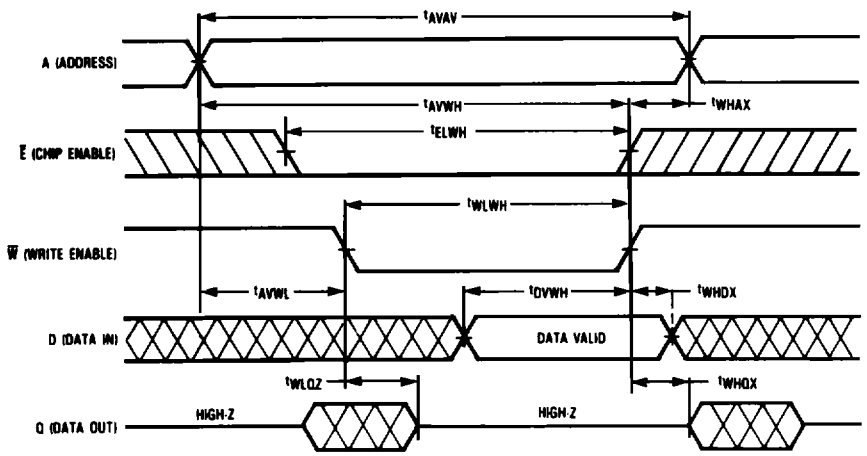
Figure 1. AC Test Load

WRITE CYCLE 1 AND 2 (See Note 1)

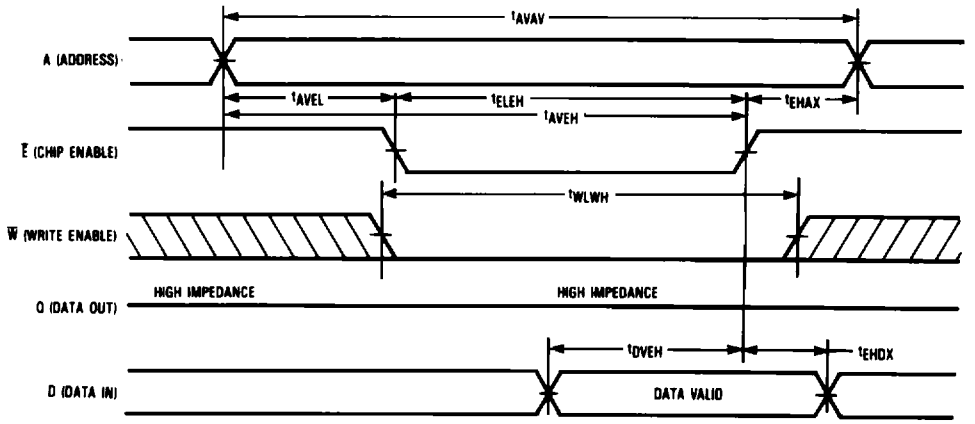
Parameter	Symbol	Alt Symbol	Min	Max	Unit	Notes
Write Cycle Time	t_{AVAV}	t_{WC}	100	–	ns	–
Address Setup Time	t_{AVWL}/t_{AVEL}	t_{AS}	0	–	ns	–
Address Valid to End of Write	t_{AVWH}/t_{AVEH}	t_{AW}	80	–	ns	–
Write Pulse Width	t_{WLWH}	t_{WP}	80	–	ns	2
Data Valid to End of Write	t_{DVWH}/t_{DVEH}	t_{DW}	35	–	ns	–
Data Hold Time	t_{WHDX}/t_{EHDX}	t_{DH}	0	–	ns	–
Write Low to Output in High-Z	t_{WLQZ}	t_{WHZ}	0	25	ns	3, 4
Write High to Output Low-Z	t_{WHQX}	t_{WLZ}	10	–	ns	3, 4
Write Recovery Time	t_{WHAX}/t_{EHAX}	t_{WR}	0	–	ns	5
Chip Enable to End of Write	t_{ELWH}/t_{ELEH}	t_{CW}	80	–	ns	–

NOTES:
1. Outputs are in high impedance state if $\overline{G}$ is high during Write Cycle.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{E}$ and a low $\overline{W}$. If $\overline{W}$ goes low prior to $\overline{E}$ low then outputs will remain in a high impedance state.
3. All high-Z and low-Z parameters are considered in a high or low impedance state when the outputs have made a 100 mV transition from the previous steady state voltage.
4. These parameters are periodically sampled and not 100% tested.
5. t_{WR} is measured from the earlier of $\overline{E}$ or $\overline{W}$ going high to the end of write cycle.

WRITE CYCLE 1 ($\overline{W}$ CONTROLLED)



WRITE CYCLE 2 ($\overline{E}$ Controlled)

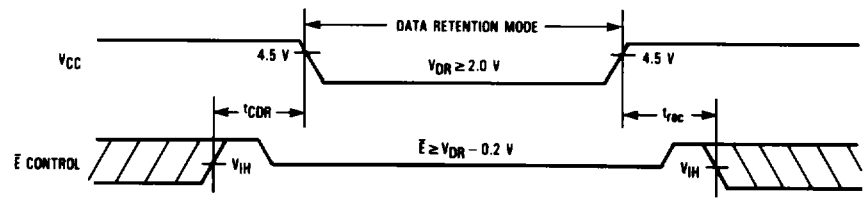


DATA RETENTION CHARACTERISTICS (T_A = −40 to 85°C)

Parameter		Symbol	Min	Typ	Max	Unit
V_{CC} for Data Retention ($\overline{E} \geq V_{CC} - 0.2$ V)		V_{DR}	2.0	–	5.5	V
Data Retention Current ($\overline{E} \geq V_{CC} - 0.2$ V)	V_{CC} = 3.0 V	I_{CCDR}	–	–	50	µA
	V_{CC} = 5.5 V		–	–	100	
Chip Disable to Data Retention Time		t_{CDR}	0	–	–	ns
Operation Recovery Time		t_{rec}	t_{AVAV}*	–	–	ns

*t_{AVAV} = Read Cycle Time

DATA RETENTION MODE



NOTE: If the V_{IH} of $\overline{E}$ is 2.4 V in operation, I_{SB1} current flows during the period that the V_{CC} voltage is decreasing from 4.5 V to 2.4 V.

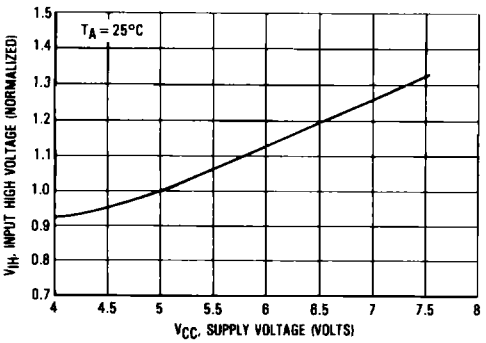


Figure 1. Input High Voltage versus Supply Voltage

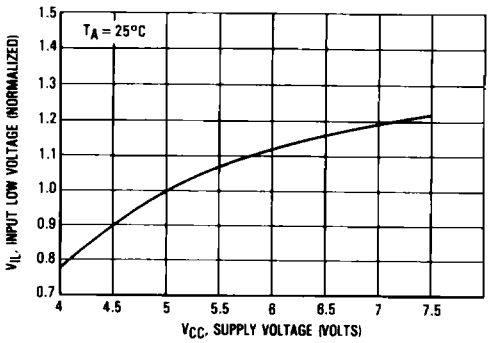


Figure 2. Input Low Voltage versus Supply Voltage

4

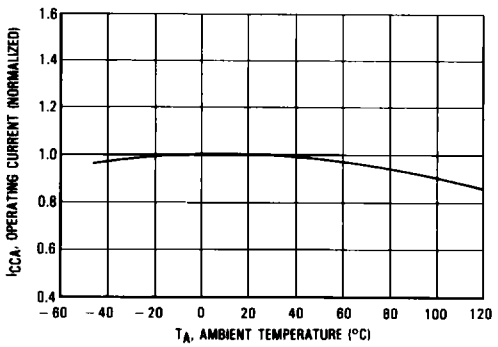


Figure 3. Operating Current versus Ambient Temperature

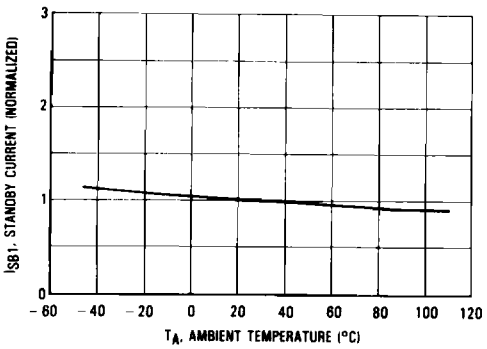


Figure 4. I_{SB1} Standby Current versus Ambient Temperature

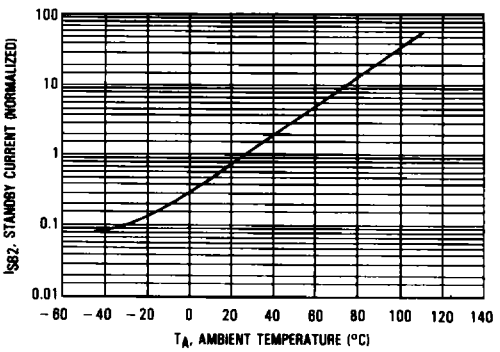


Figure 5. I_{SB2} Standby Current versus Ambient Temperature

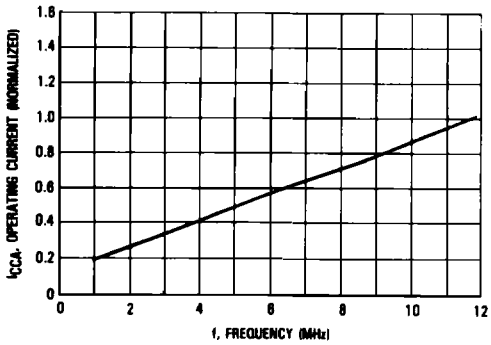


Figure 6. Low Power Operating Current versus Frequency (Read)

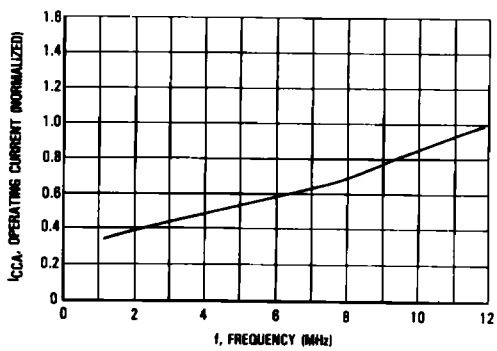


Figure 7. Operating Current versus Frequency (Write)

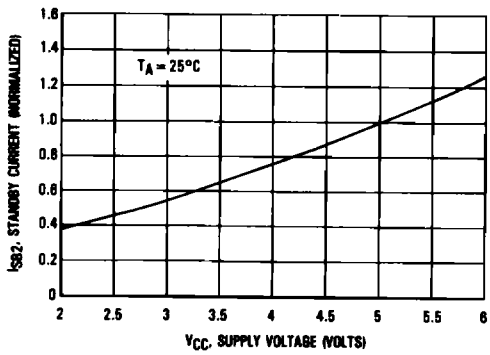


Figure 8. Low Power I_{SB2} Standby Current versus Supply Voltage

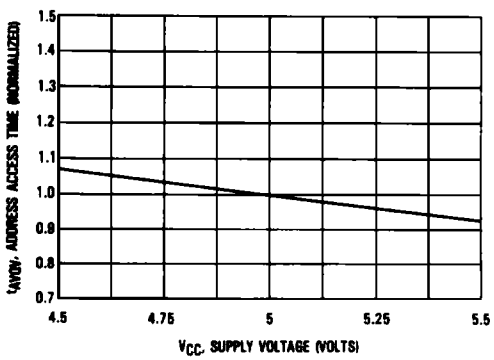


Figure 9. Access Time versus Supply Voltage

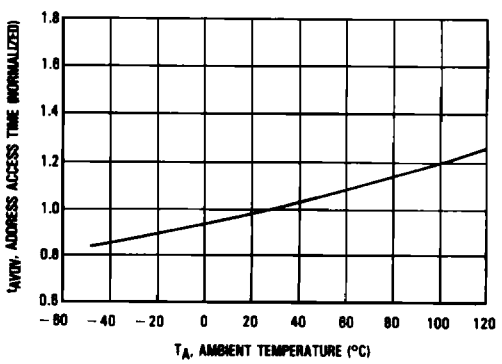
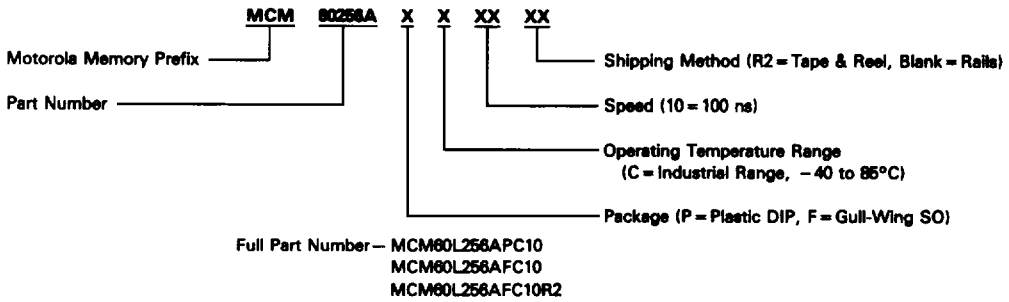


Figure 10. Access Time versus Ambient Temperature

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Number — MCM60L256APC10
MCM60L256AFC10
MCM60L256AFC10R2

4