QuickLogic® PolarPro® Device Data Sheet — 86-Pin TFBGA QL1P100

QuickLogic

• • • • • • **Combining Low Power, Performance, Density, and Embedded RAM**

Device Highlights

Low Power Programmable Logic

- As low as 2.2 µA
- 0.18 µm, six layer metal CMOS process
- 1.8 V core voltage, 1.8/2.5/3.3 V drive capable I/Os
- 36 kilobits of SRAM
- 48 I/Os available
- 100,000 system gates
- Nonvolatile, instant-on
- IEEE 1149.1 boundary scan testing compliant

Embedded Dual-Port SRAM

- Eight dual-port 4-kilobit high performance SRAM blocks
- True dual-port capability
- Embedded synchronous/asynchronous FIFO controller
- Configurable and cascadable aspect ratio

Programmable I/O

- Bank programmable drive strength
- Bank programmable slew rate control
- Independent I/O banks capable of supporting multiple I/O standards in one device
- Bank programmable I/O standards: LVTTL, LVCMOS, LVCMOS18, PCI, SSTL2, SSTL3 and SSDL18

Advanced Clock Network

- Multiple low skew clock networks
  ‣ 1 dedicated global clock network
  ‣ 4 programmable global clock networks

- Quadrant-based segmentable clock networks
  ‣ 16 quad clock networks per device
  ‣ 4 quad clock networks per quadrant
- One user Configurable Clock Manager (CCM)

Very Low Power (VLP) Mode

- QuickLogic PolarPro has a special VLP pin which can enable a low power sleep mode that significantly reduces the overall power consumption of the device by placing the device in standby
- Enter VLP mode from normal operation in less than 250 µs (typical)
- Exit from VLP mode to normal operation in less than 250 µs (typical)

Security Links

There are several security links to disable JTAG access to the device. Programming these optional links completely disables access to the device from the outside world and provides an extra level of design security not possible in SRAM-based FPGAs.

Figure 1: QuickLogic PolarPro Block Diagram
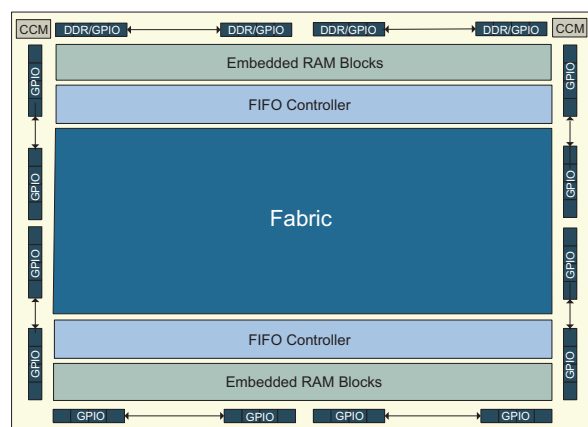
Ultra-Low Power FPGA Combining Performance, Density, and Embedded RAM

Table 1: PolarPro 86-Pin TFBGA Product Information

Features		QL1P100
Max Gates		100,000
Logic Cells		640
Max I/O		48
Distributed Clocks		5
RAM Modules		8
FIFO Controllers		8
RAM bits		36,864
CCM		1
Package	TFBGA (0.5 mm) (6 mm x 6 mm)	86

Process Data

The QuickLogic PolarPro is fabricated on a 0.18μ, six layer metal CMOS process. The core voltage is 1.8 V. The I/O voltage input tolerance and output drive can be set as 1.8 V, 2.5 V, and 3.3 V.

Programmable Logic Architectural Overview

The QuickLogic PolarPro logic cell structure presented in **Figure 2** is a single register, multiplexer-based logic cell. It is designed for wide fan-in and multiple, simultaneous output functions. The cell has a high fan-in, fits a wide range of functions with up to 24 simultaneous inputs (including register control lines), and four outputs (three combinatorial and one registered). The high logic capacity and fan-in of the logic cell accommodates many user functions with a single level of logic delay.

The QuickLogic PolarPro logic cell can implement:

- Two independent 3-input functions
- Any 4-input function
- 8 to 1 mux function
- Independent 2 to 1 mux function
- Single dedicated register with clock enable, active high set and reset signals
- Direct input selection to the register, which allows combinatorial and register logic to be used separately
- Combinatorial logic that can also be configured as an edge-triggered master-slave D flip-flop

Figure 2: PolarPro Logic Cell
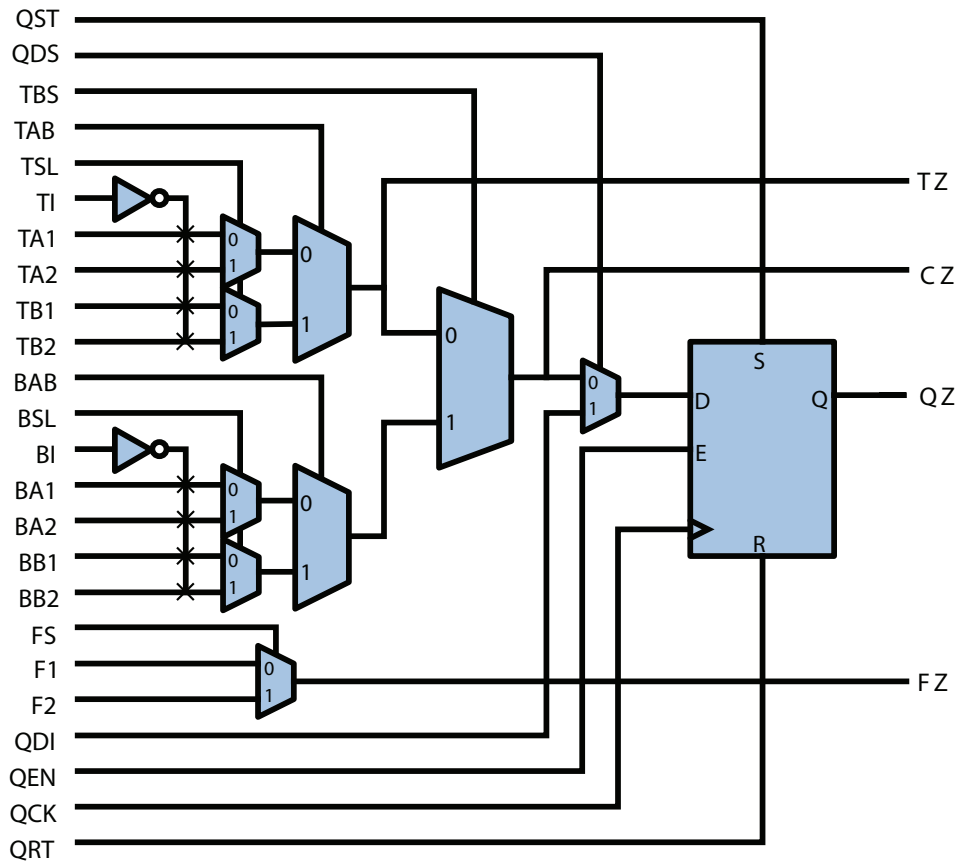
RAM Modules

The PolarPro family of devices includes up to eight 4 kilobits of dual-port RAM modules for implementing RAM and FIFO functions.

The RAM features include:

- Independently configurable read and write data bus widths

- Independent read and write clocks

- Horizontal and vertical concatenation

- Write byte enables

- Selectable pipelined or non-pipelined read data
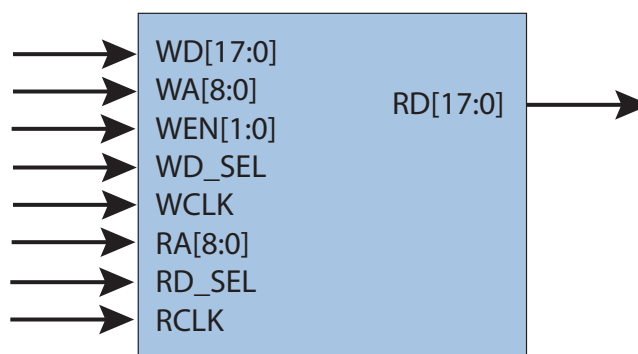
Figure 3: 4-Kilobit Dual-Port RAM Block

WD[17:0]
WA[8:0]
WEN[1:0]
WD_SEL   RD[17:0]
WCLK
RA[8:0]
RD_SEL
RCLK

Table 2: RAM Interface Signals

Signal Name	Function
Inputs	
WD [17:0]	Write Data
WA [8:0]	Write Address
WEN [1:0]	Write Enable (two 9-bit enables)
WD_SEL	Write Chip Select
WCLK	Write Clock
RA [8:0]	Read Address
RD_SEL	Read Chip Select
RCLK	Read Clock
Output	
RD [17:0]	Read Data

The read and write data buses of a RAM block can be arranged to variable bus widths. The bus widths can be configured using the RAM Wizard available in QuickWorks, QuickLogic's development software. The selection of the RAM depth and width determines how the data is addressed.

The RAM blocks also support data concatenation. Designers can cascade multiple RAM modules to increase the depth or width by connecting corresponding address lines together and dividing the words between modules. Generally, this requires the use of additional programmable logic resources. However, when concatenating only two 4-kilobit RAM blocks, they can be concatenated horizontally or vertically without using any additional programmable fabric resources.

For example, two internal 4-kilobit dual-port RAM blocks can be concatenated vertically to create a 512x18 RAM block or horizontally to create a 256x36 RAM block. A block diagram of horizontal and vertical concatenation is displayed in **Figure 4**.
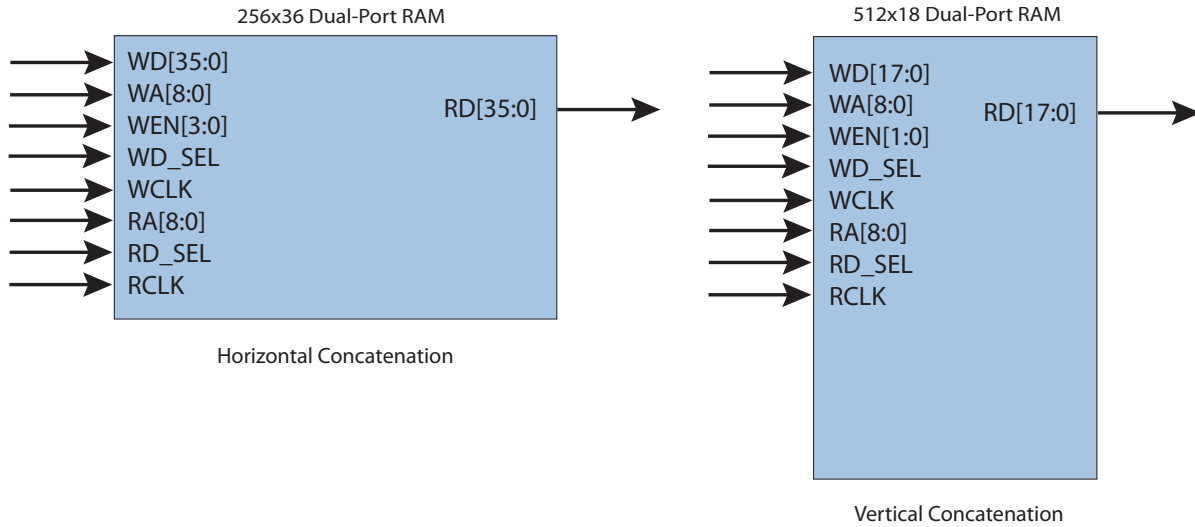
Figure 4: Horizontal and Vertical Concatenation Examples

256x36 Dual-Port RAM

WD[35:0]
WA[8:0]
WEN[3:0]   RD[35:0]
WD_SEL
WCLK
RA[8:0]
RD_SEL
RCLK

Horizontal Concatenation

512x18 Dual-Port RAM

WD[17:0]
WA[8:0]
WEN[1:0]   RD[17:0]
WD_SEL
WCLK
RA[8:0]
RD_SEL
RCLK

Vertical Concatenation

Table 3 shows the various RAM configurations supported by the PolarPro RAM modules.

Table 3: Available Dual-Port RAM Configurations

Device	Number of RAM Blocks	Depth	Width
	1	256	1-18
	1	512	1-9
QL1P100	2	256	1-36
	2	512	1-18
	2	1024	1-9

True Dual-Port RAM

PolarPro dual-port RAM modules can also be concatenated to generate true dual-port RAMs. The true dual-port RAM module's Port1 and Port2 have completely independent read and write ports, and separate read and write clocks. This allows Port1 and Port2 to have different data widths and clock domains. It is important to note that there is no circuitry preventing a write and read operation to the same address space at the same time. Therefore, it is up to the designer to ensure that the same address is not read from and written to simultaneously, otherwise the data is considered invalid. Likewise, the same address must not be written to from both ports at the same time. However, it is possible to read from the same address. **Figure 5** shows an example of a 512x18 true dual-port RAM.

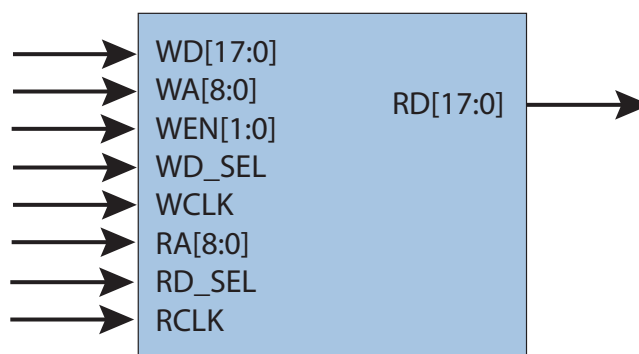Figure 5: 512x18 4-Kilobit True Dual-Port RAM Block

WD[17:0]
WA[8:0]
WEN[1:0]
WD_SEL
WCLK
RA[8:0]
RD_SEL
RCLK

RD[17:0]

Table 5: True Dual-Port RAM Interface Signals

Port	Signal Name	Function
Port1	**Inputs**	
	Port1_WD[17:0]	Write Data
	Port1_A[8:0]	Write Address
	Port1_WEN[1:0]	Write Enable
	Port1_CS	Chip Select
	Port1_CLK	Clock
	Output	
	Port1_RD[17:0]	Read Data
Port2	**Inputs**	
	Port2_WD[17:0]	Write Data
	Port2_A[8:0]	Write Address
	Port2_WEN[1:0]	Write Enable
	Port2_CS	Chip Select
	Port2_CLK	Clock
	Output	
	Port2_RD[17:0]	Read Data

Table 6: Available True Dual-Port RAM Configurations

| Device	Depth	Width
QL1P100	512	1-18
	1024	1-9

Embedded FIFO Controllers

Every 4-kilobit RAM block can be implemented as a synchronous or asynchronous FIFO. There are built-in FIFO controllers that allow for varying depths and widths without requiring programmable fabric resources.

The PolarPro FIFO controller features include:

- x9, x18 and x36 data bus widths
- Independent PUSH and POP clocks
- Independent programmable data width on PUSH and POP sides
- Configurable synchronous or asynchronous FIFO operation
- 4-bit PUSH and POP level indicators to provide FIFO status outputs for each port
- Pipelined read data to improve timing

Figure 6: FIFO Module
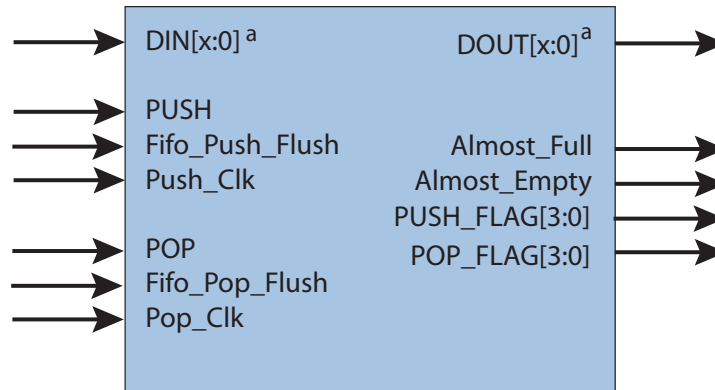
a. x = {1,2,3,....35}.

Table 7: Available FIFO Configurations

Device	Number of RAM Blocks	Depth	Supported Widths
QL1P100	1	256	1-18 bits
	1	512	1-9 bits
	2	256	1-36 bits
	2	512	1-18 bits
	2	1024	1-9 bits

Table 8 lists the FIFO controller interface signals.

Table 8: FIFO Interface Signals

Signal Name	Width (bits)	Direction	Function
PUSH Signals			
DIN	1 to 36	I	Data bus input
PUSH	1	I	Initiates a data push
Fifo_Push_Flush	1	I	Empties the FIFO
Push_Clk	1	I	Push data clock
POP Signals			
DOUT	1 to 36	O	Data bus output
POP	1	I	Initiates a data pop
Fifo_Pop_Flush	1	I	Empties the FIFO
Pop_Clk	1	I	Pop data clock
Status Flags			
Almost_Full	1	O	Asserted when FIFO has one location available
Almost_Empty	1	O	Asserted when FIFO has one location used
PUSH_FLAG[3:0]	4	O	FIFO PUSH level indicator
POP_FLAG[3:0]	4	O	FIFO POP level indicator

Table 9 and **Table 10** highlight the corresponding FIFO level indicator for each 4-bit value of the PUSH_FLAG and POP_FLAG outputs.

Table 9: FIFO PUSH Level Indicator Values

Value	Status
0000	Full
0001	Empty
0010	Room for more than one-half
0011	Room for more than one-forth
1000	Room for 8 or more
1001	Room for 7
1010	Room for 6
1011	Room for 5
1100	Room for 4
1101	Room for 3
1110	Room for 2
1111	Room for 1
Others	Reserved

Table 10: FIFO POP Level Interface Signals

Value	Status
0000	Empty
0001	1 entry in FIFO
0010	2 entries in FIFO
0011	3 entries in FIFO
0100	4 entries in FIFO
0101	5 entries in FIFO
0110	6 entries in FIFO
0111	7 entries in FIFO
1000	8 or more entries in FIFO
1101	One-forth or more full
1110	One-half or more full
1111	Full
Others	Reserved

FIFO Flush Procedure

When a flush is triggered from one side of the FIFO, the signal propagates and re-synchronizes internally to the other clock domain. During a flush operation, the values of the FIFO flags are invalid for a specific number of cycles (see **Figure 7** and **Figure 8**).

As shown in **Figure 7**, when the **Fifo_Push_Flush** asserts, the **Almost_Full** and **PUSH_FLAG** signals become invalid until the FIFO can flush the data with regards to the Push clock domain as well as the Pop clock domain. After the **Fifo_Push_Flush** is asserted, the next rising edge of the Pop clock starts the Pop flush routine.

Figure 7 illustrates a FIFO Flush operation. After the **Fifo_Push_Flush** is asserted at 2 (**PUSH_Clk**), four POP clock cycles (12 through 15) are required to update the **POP_FLAG**, and **PUSH_FLAG** signals. The **Almost_Empty** signal is asserted to indicate that the push flush operation has been completed. On the following rising edge of the **PUSH_Clk** (8), the **PUSH_FLAG** is accordingly updated to reflect the successful flush operation.
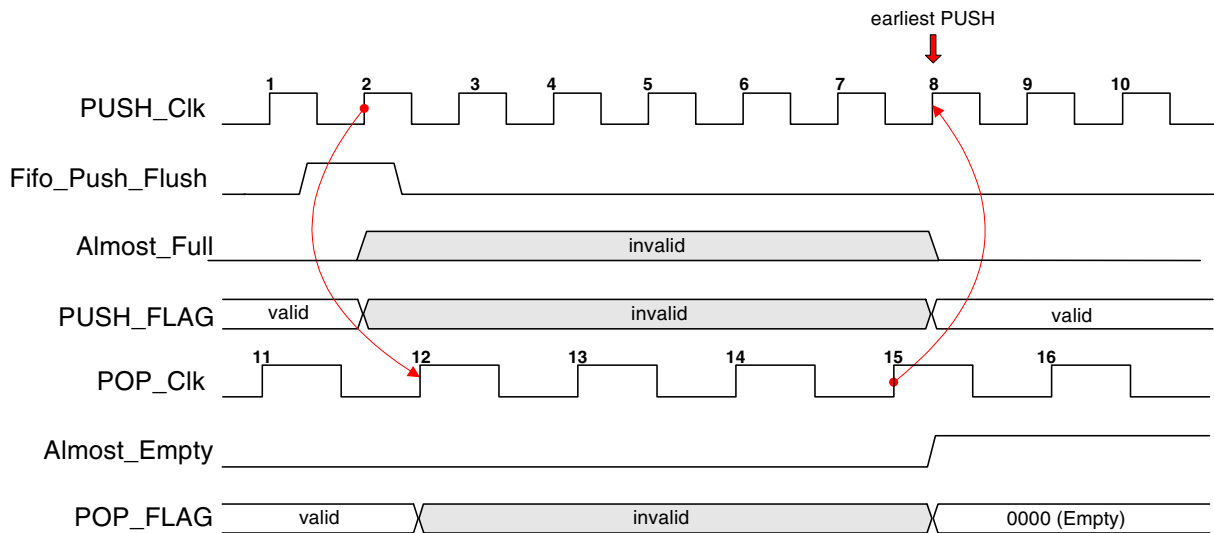
Figure 7: FIFO Flush from PUSH Side

Figure 8 illustrates a POP flush operation. After the **Fifo_Pop_Flush** is asserted at 2 (**POP_Clk**), four PUSH clock cycles (12 through 15) are required to update the **POP_FLAG**, and **PUSH_FLAG** signals. The **Almost_Empty** signal is asserted to indicate that the pop flush operation has been completed. On the following rising edge of the **POP_Clk** (8), the **POP_FLAG** is updated accordingly to reflect the successful flush operation.
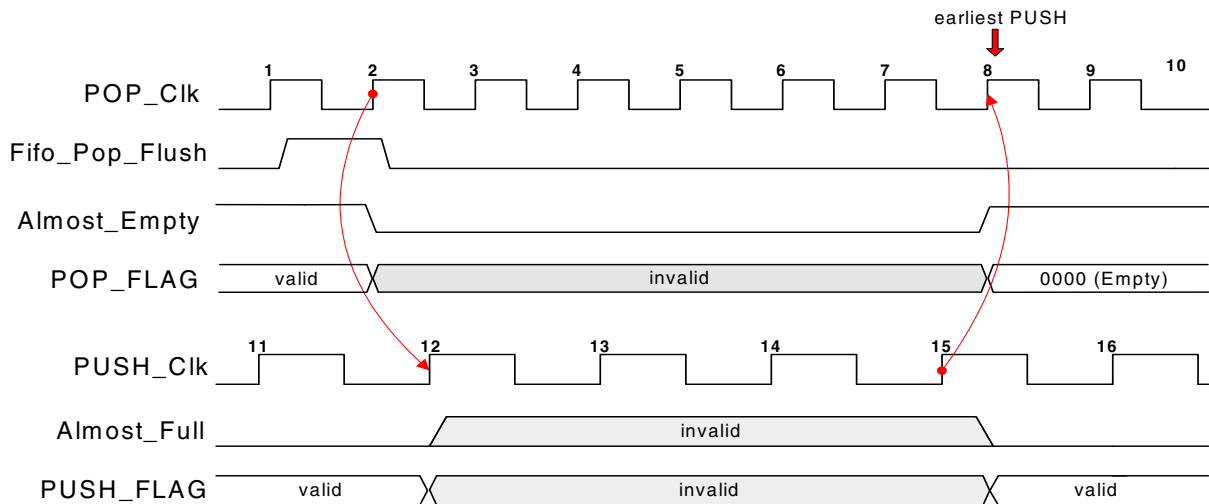
Figure 8: FIFO Flush from POP Side

Figure 7 and **Figure 8** are only true for this particular PUSH-POP clock frequency combination. The clock frequency and phase difference between POP_Clk and PUSH_Clk can cause an additional flush delay of one clock cycle in either domain because of the asynchronous relationship between the two clocks.

86-Pin TFBGA QL1P100 Clock Network Architecture

Clock Network Architecture

The PolarPro clock network architecture consists of a 2-level H-tree network as shown in Figure 9. The first level of each clock tree (high-lighted in red) spans from the clock input pad to the global clock network and to the center of each quadrant of the chip. The second level (high-lighted in blue) spans from the quadrant clock network to every logic cell inside that quadrant. There are five global clocks in the global clock network, and five quadrant clocks in each quadrant clock network. All global clocks drive the quadrant clock network inputs. The quadrant clocks output to clock inversion muxes, which pass either the original input clock or an inverted version of the input clock to the logic cells in that quadrant. The global clocks can drive RAM block clock inputs and reset, set, enable, and clock inputs to I/O registers. Furthermore, the quadrant clock outputs can be routed to all logic cell inputs.

Figure 9: PolarPro Clock Architecture
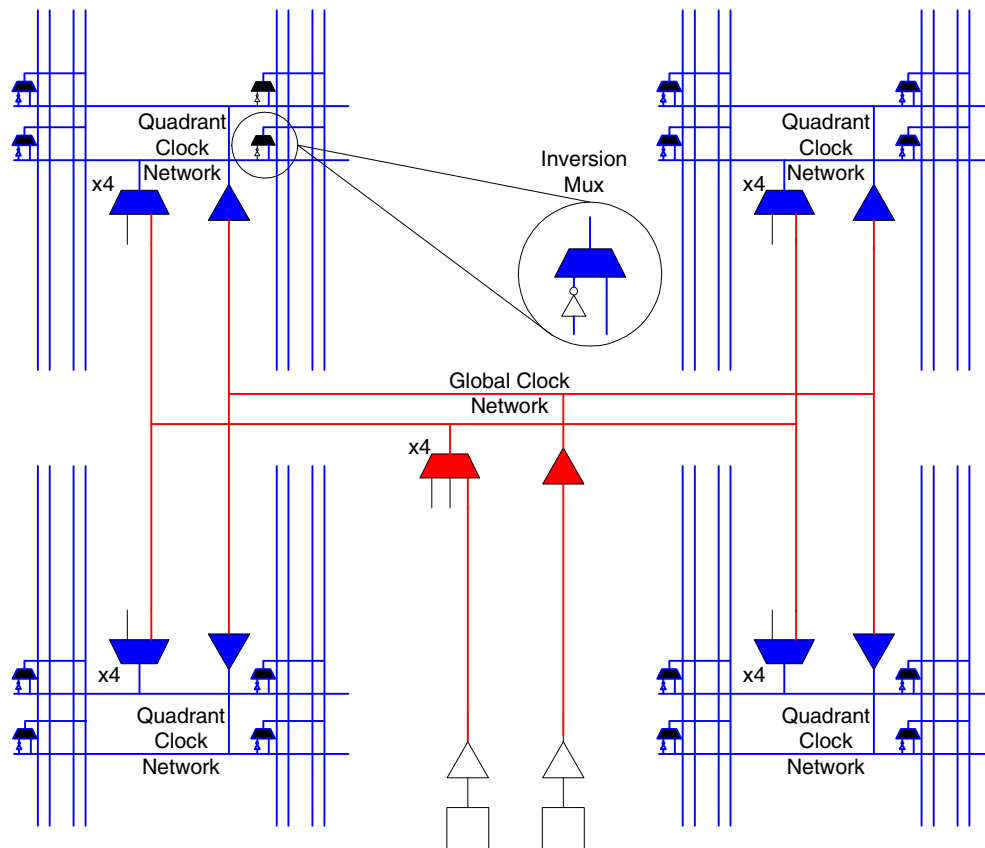
Of the five global clock networks, four can be either driven directly by clock pads, Configurable Clock Manager (CCM) outputs, or internally generated signals. These four global clocks go through 3-input global clock muxes located in the middle of the die. See **Figure 10** for a diagram of a 3-input global clock mux. The fifth is a dedicated global clock network that goes directly to the quadrant clock network and is used as a dedicated fast clock.
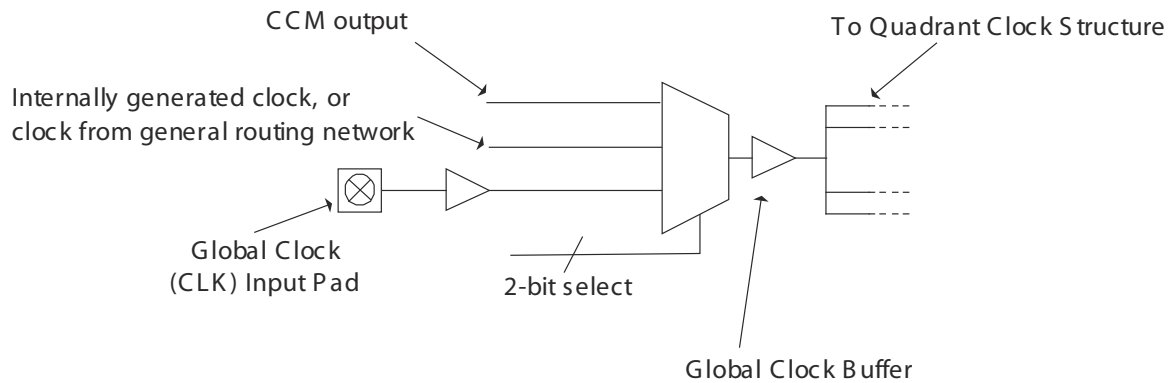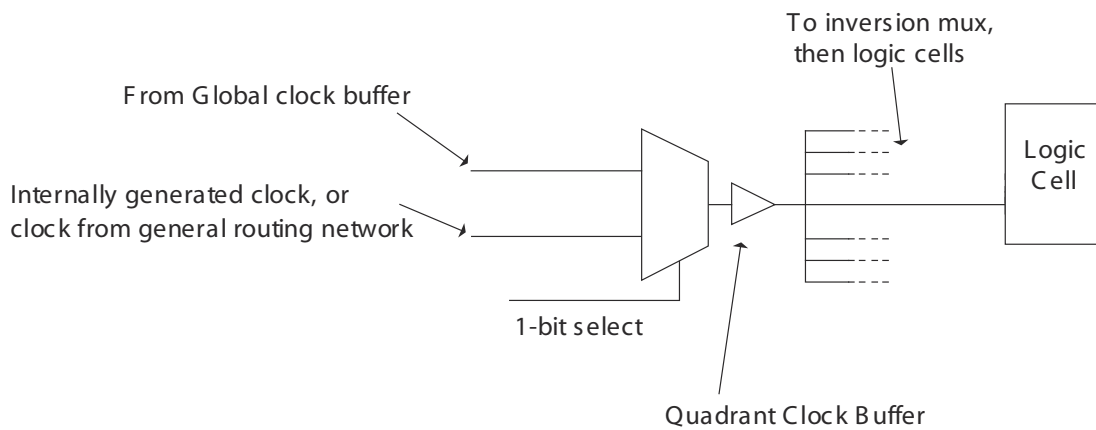
Figure 10: Global Clock Structure

Figure 11 illustrates the quadrant clock 2-input mux.

Figure 11: Quadrant Clock Structure

It is important to note that the select lines for the global clock and quadrant clock muxes are static signals and cannot be changed dynamically during device operation. For more information about global and quadrant clock networks and how to use them, refer to *Application Note 85 Clock Networks in PolarPro Devices*.

Configurable Clock Manager (CCM)

The CCM features include:

- Input frequency range from 10 MHz to 200 MHz

- Output frequency range from 25 MHz to 200 MHz

- Output jitter is less than 200 ps peak-to-peak

- Two outputs: pllout0 (with 0° phase shift), and pllout1 (with an option of 0°, 90°, 180°, or 270° phase shift plus a programmable delay).

- Programmable delay allows delays up to 2.5 ns at 250 ps intervals

- Fixed feedback path

- Output frequency lock time in less than 10 µs

Figure 12: Configurable Clock Manager
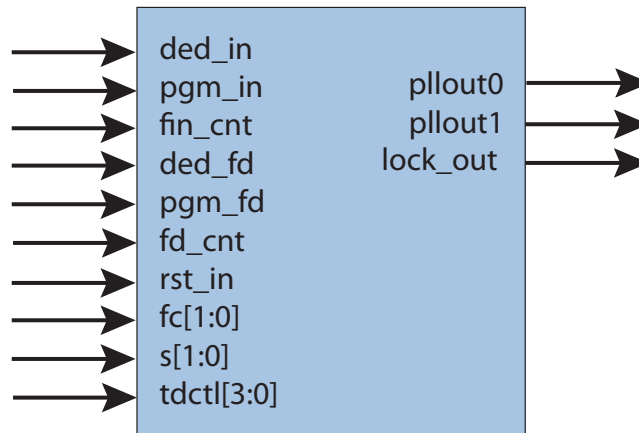
The reset signal can be routed from a clock pad or generated using internal logic. The lock_out signal can be routed to internal logic and/or an output pad. CCM clock outputs can drive the global clock networks, as well as any general purpose I/O pin. Once the CCM has synchronized the output clock to the incoming clock, the lock_out signal will be asserted to indicate that the output clock is valid. Lock detection requires at least 10 µs after reset to assert lock_out. The PolarPro CCMs have three modes of operation, based on the input frequency and desired output frequency. **Table 11** indicates the features of each mode.

Table 11: CCM PLL Mode Frequencies

Output Frequency	Input Frequency Range	Output Frequency Range	PLL Mode
x1	25 MHz to 200 MHz	25 MHz to 200 MHz	PLL_MULT1
x2	15 MHz to 100 MHz	30 MHz to 200 MHz	PLL_MULT2
x4	10 MHz to 50 MHz	40 MHz to 200 MHz	PLL_MULT4

CCM Signals

Table 12 provides the name, direction, function and description of the CCM ports.

Table 12: CCM Signals

Signal Name	Direction	Function	Description
Routable Ports			
ded_in	I	Dedicated Input	Clock pad CCM input source.
ded_fd	I	Dedicated Feedback	Automatically calculated and routed by the software tools.
rst_in	I	Reset	Active high reset: If rst_in is asserted, pllout0 and pllout1 are reset to 0. This signal must be asserted and then released for lock_out to assert.
pllout0	O	0° Phase Clock	0° phase clock output.
pllout1	O	Configurable Phase Clock	0°, 90°,180°, or 270° phase clock output with programmable delay.
lock_out	O	Lock Detect	Active high lock detection signal. Active when the pllout signals correctly output the configured functionality.
Static Ports			
fc[1:0]	I	Phase Shift Control	Determines whether pllout1 is 0°, 90°, 180°, or 270° degrees out of phase with pllout0[a].
s[1:0]	I	Set Mode	Determines pllout1 and pllout0 frequency multiplier (x1, x2, or x4).
tdctl[3:0]	I	Time Delay Control	Pllout1 programmable delay, configurable in 250 ps increments up to a maximum of 2.5 ns. NOTE: 250 ps can vary depending on process variation.

a. The pllout1 output can vary up to -5% with respect to the pllout0 output. Therefore, QuickLogic recommends thorough post-layout simulation in order to verify satisfactory operation of the CCMs.

Table 13, **Table 14** and **Table 15** give the values used to configure the Set Mode, Phase Shift Control and Time Delay Control bits.

Table 13: Set Mode Values

s[1:0]	Multiplier
00	x1
01	x2
10	x4
11	Reserved

Table 14: Phase Shift Control Values

fc[1:0]	Phase Shift (Deg.)
00	0
01	90
10	180
11	270

Table 15: Time Delay Control Values

tdctl[3:0]	Time Delay (ps)
0000	0
0001	250
0010	500
0011	750
0100	1000
0101	1250
0110	1500
0111	1750
1000	2000
1001	2250
1010	2500
1011	Reserved
1100	Reserved
1101	Reserved
1110	Reserved
1111	Reserved

CCM Configurations

The main purpose of the CCM is to align the clock arrival times of two separate clock destinations, whether it is within the FPGA or external to the chip. The difference between the two clock destinations is referred to as clock skew. To correct for clock skew the CCMs can be configured to shift the phase and/or delay of the pllout1 clock output.

In most cases the desired phase or added delay can be accomplished by configuring both the clock source input and feedback input as dedicated. In the case of a dedicated clock source and dedicated feedback, the QuickLogic development software calculates and generates all of the required routing delays to produce the requested configuration.

Table 16: Available Configurations

| Clock	Feedback	Example Usage	Comments
Dedicated clock pad	Dedicated feedback	Standard PLL application. Reduce set-up or clock-to-out time.	If the clock pad and destination are in phase.

For more information on CCMs and how to use them in QuickWorks, refer to *Application Note 87 Configurable Clock Managers*.

General Purpose Input Output (GPIO) Cell Structure

The GPIO features include:

- Direct or registered input with input path select
- Direct or registered output with output path select
- Direct or registered output enable with OE path select
- Input buffer enable to reduce power
- Programmable weak keeper, programmable pull-up/pull-down control
- Programmable drive strength
- Configurable slew rate
- Support for JTAG boundary scan

Figure 13: PolarPro GPIO Cell
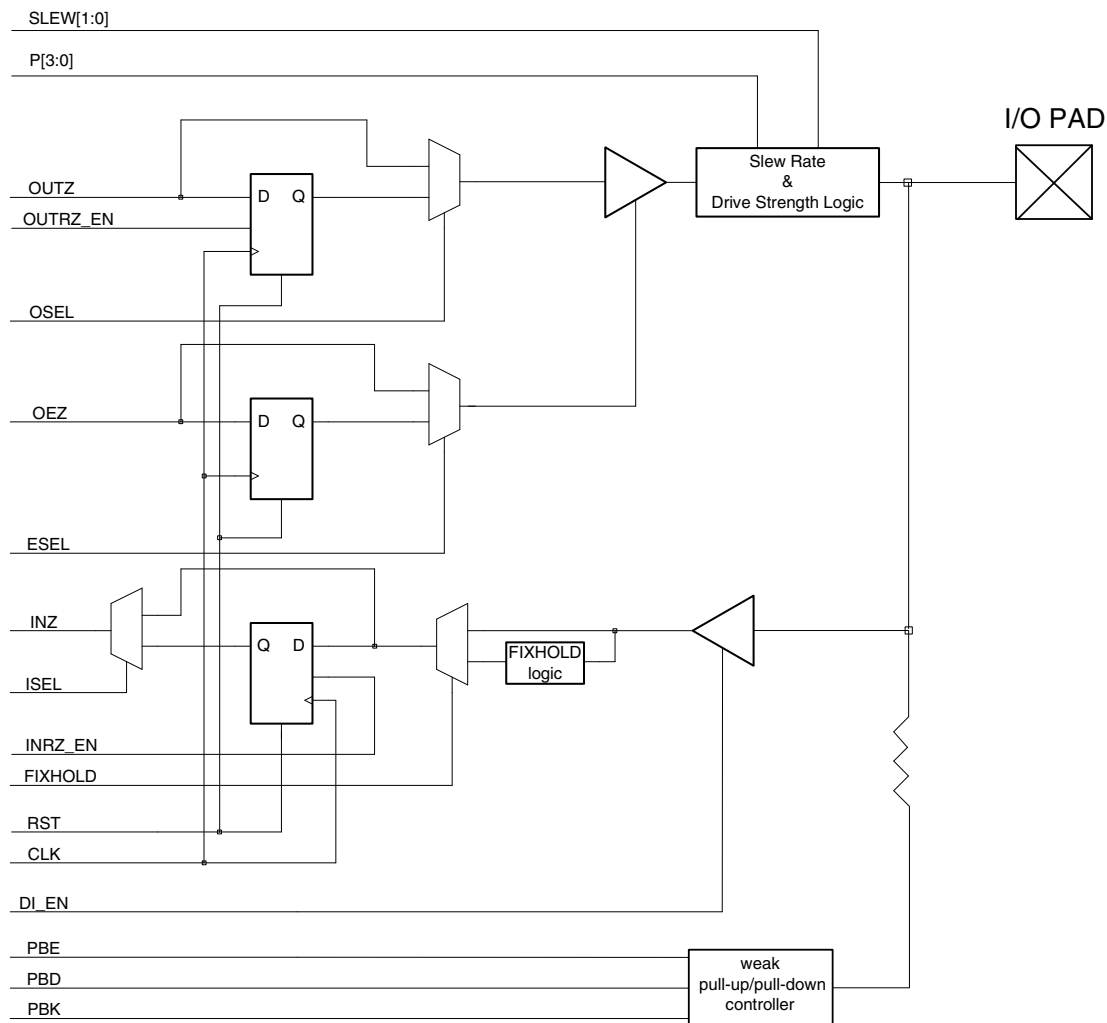
With bi-directional I/O pins and global clock input pins, the PolarPro device maximizes I/O performance, functionality, and flexibility. All input and I/O pins are 1.8 V, 2.5 V, and 3.3 V tolerant and comply with the specific I/O standard selected. For single-ended I/O standards, the corresponding VCCIO bank input specifies the input tolerance and the output drive voltage. Drive strength and slew rate are configured for an entire bank. Weak keeper, pull-up, and pull-down functions can be configured for individual I/O. The default configuration for QuickLogic QuickWorks software has the drive strength set to 4 and the slew rate set to wow.

Table 17: GPIO Interface Signals

Signal Name	Direction	Function
Routable Signals		
OUTZ	I	Data out from internal logic
OUTRZ_EN	I	Enable for registered OUTZ
OEZ	I	Tristate enable for the output signal
INZ	O	Input signal to the internal logic
INRZ_EN	I	Enable for registered INZ
RST	I	Reset for optional registers
CLK	I	Clock signal for optional registers
DI_EN	I	Enable for I/O input signal. Drives a 1 to internal logic when disabled.
Static Signals		
SLEW[1:0]	I	2-bit slew rate control
P[3:0]	I	Programmable drive strength
OSEL	I	Select signal for registered or flow through OUTZ
ESEL	I	Select signal for registered or flow-through OEZ
ISEL	I	Select signal for registered or flow-through INZ
FIXHOLD	I	Enable control for I/O input delay for hold fixing
PBE	I	Input signals for the weak keeper, pull-up/pull-down controller, see **Table 18** for functional behavior
PBD	I	
PBK	I	

Programmable Weak Keeper, Pull-Up, and Pull-Down

A programmable Weak Keeper, Pull-Up or Pull-Down controller is also available on each General Purpose I/O bank. When implementing the Weak Keeper, Pull-Up, and Pull-Down functions, each I/O can be configured separately. The I/O Weak Pull-Up and Pull-Down eliminates the need for external resistors. When PBK=1 the keeper block is placed into keeper mode. In the keeper mode, the pad pin (if the driver is tristated), will be kept at whichever level it was last forced, either by the driver itself, or by an external driver.

Table 18: Weak Pull-Up, and Pull-Down Controller

PBK	PBD	PBE	Function
0	0	0	Tristate (floating)
0	0	1	Weak Pull-Down
0	1	1	Weak Pull-Up
1	X	X	Weak Keeper (retains state)
0	1	0	Reserved

Programmable Drive Strength

Every GPIO has independent drive strength control. Twelve different drive strength levels are available for designers to choose from. For additional information about corresponding drive strength see **DC Characteristics** on page 20.

Programmable Slew Rate

Each I/O has programmable slew rate capability. The PolarPro GPIOs allow up to four different slew rate speeds (slow, fast, vfast, and wow). Slower slew rates can be used to reduce noise caused by I/O switching.

I/O interface standards are programmable on a per bank basis. **Table 19** illustrates the I/O bank configurations available. Each I/O bank is independent of other I/O banks and each I/O bank has its own VCCIO supply inputs. A mixture of different I/O standards can be used on a PolarPro device. However, there is a limitation as to which I/O standards can be supported within a given bank. Only standards that share a common VCCIO can be shared within the same bank (e.g., PCI and LVTTL).

Table 19: I/O Standards and Applications

I/O Standard	VCCIO Voltage	Application
LVTTL	3.3 V	General Purpose
LVCMOS25	2.5 V	General Purpose
LVCMOS18	1.8 V	General Purpose
PCI	3.3 V	PCI Bus Applications

Very Low Power (VLP) Mode

The QuickLogic PolarPro devices have a unique feature, referred to as VLP mode, which reduces power consumption by placing the device in standby. Specifically, VLP mode can bring the total standby current down to less than 10 µA at room temperature when no incoming signals are toggled. VLP mode is controlled by the VLP pin. The VLP pin is active low, so VLP mode is activated by pulling the VLP pin to ground. Conversely, the VLP pin must be pulled to 3.3 V for normal operation.

When a PolarPro device goes into VLP mode, the following occurs:

- All logic cell registers and GPIO registers values are held
- All RAM cell data is retained
- The outputs from all GPIO to the internal logic are tied to a weak '1'
- GPIO outputs drive the previous values
- GPIO output enables retain the previous values
- DDRIO outputs are pulled down through a weak pull down circuit
- Clock pad inputs are gated
- CCMs are held in the reset state

The entire operation from normal mode to VLP mode requires 250 µs (300 µs maximum). As mentioned in the VLP behavioral description above, the output of the GPIO to the internal logic is a weak '1'. Therefore, to preserve data retention GPIO should not be used for a set, reset, or clock signal. During the transition from VLP mode to normal operation, the VLP pin can draw up to 1.5 mA. Consequently, if using a pull-up resistor, use a pull-up resistor with a value that is less than 2 KΩ.

As the device exits out of VLP mode, the data from the registers, RAM, and GPIO will be used to recover the functionality of the device. Furthermore, since the CCMs were in a reset state during VLP mode, they will have to re-acquire the correct output signals before asserting lock_out. The time required to go from VLP mode to normal operation is 250 µs (300 µs maximum). **Figure 14** displays the delays associated with entering and exiting VLP mode.

Figure 14: Typical VLP Mode Timing
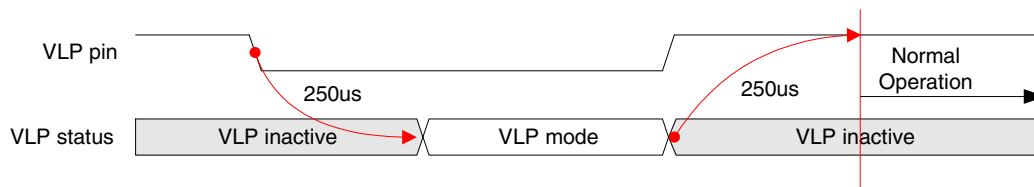
Electrical Specifications

DC Characteristics

The DC Specifications are provided in **Table 20** through **Table 23**.

Table 20: Absolute Maximum Ratings

Parameter	Value	Parameter	Value
VCC Voltage	-0.5 V to 2.2 V	Latch-up Immunity	±100 mA
VCCIO Voltage	-0.5 V to 4.0 V	ESD Pad Protection	2 kV
VREF Voltage	-0.5 V to 2.0 V	Leaded Package Storage Temperature	-65° C to + 150° C
Input Voltage	-0.5 V to 4.0 V	Laminate Package (BGA) Storage Temperature	-55° C to + 125° C

Table 21: Recommended Operating Range

Symbol	Parameter	Military		Industrial		Commercial		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
VCC	Supply Voltage	1.71	1.89	1.71	1.89	1.71	1.89	V
VCCIO	I/O Input Tolerance Voltage	1.71	3.60	1.71	3.60	1.71	3.60	V
TJ	Junction Temperature	-55	125	-40	100	0	85	°C

Table 22: DC Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_I	I or I/O Input Leakage Current	VI = VCCIO or GND	-	-	1	µA
I_{OZ}	3-State Output Leakage Current	VI = VCCIO or GND	-	-	1	µA
C_I	I/O Input Capacitance	VCCIO = 3.6 V	-	-	10	pF
C_{CLOCK}	Clock Input Capacitance	VCCIO = 3.6 V	-	-	10	pF
I_{REF}	Quiescent Current on INREF	-	-	-	5	µA
I_{PD}	Current on programmable pull-down	VCCIO = 3.6 V	-200	-	-50	µA
		VCCIO = 2.75 V	-150	-	-25	µA
		VCCIO = 1.89 V	-100	-	-10	µA
I_{PU}	Current on programmable pull-up	VCCIO = 3.6 V	50	-	200	µA
		VCCIO = 2.75 V	25	-	150	µA
		VCCIO = 1.89 V	10	-	100	µA
I_{VLP}	Quiescent Current on VLP pin	VLP=3.3	-	1	10	µA
I_{CCM}	Quiescent Current on each CCMVCC	VCC=1.89 V	-	1	10	µA
I_{VCC}	Quiescent Current [a]	VLP=GND	-	2.2	40	µA
		VLP=3.3V	-	40	100	µA
I_{VCCIO}	Quiescent Current on VCCIO	VCCIO = 3.6 V	-	2	10	µA
		VCCIO = 2.75 V	-	2	10	µA
		VCCIO = 1.89 V	-	2	10	µA

a. Quiescent current values correspond to the QL1P100.

Table 23: DC Input and Output Levels[a]

Symbol	INREF		V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V_{MIN}	V_{MAX}	V_{MIN}	V_{MAX}	V_{MIN}	V_{MAX}	V_{MAX}	V_{MIN}	mA	mA
LVTTL	n/a	n/a	-0.3	0.8	2.2	VCCIO + 0.3	0.4	2.4	2.0	-2.0
LVCMOS2	n/a	n/a	-0.3	0.7	1.7	VCCIO + 0.3	0.7	1.7	2.0	-2.0
LVCMOS18	n/a	n/a	-0.3	0.63	1.2	VCCIO + 0.3	0.7	1.7	2.0	-2.0
GTL+	0.88	1.12	-0.3	INREF - 0.2	INREF + 0.2	VCCIO + 0.3	0.6	n/a	40	n/a
PCI	n/a	n/a	-0.3	0.3 x VCCIO	0.6 x V_{CCIO}	VCCIO + 0.5	0.1 x VCCIO	0.9 x VCCIO	1.5	-0.5
SSTL2	1.15	1.35	-0.3	INREF - 0.18	INREF + 0.18	VCCIO + 0.3	0.74	1.76	7.6	-7.6
SSTL3	1.3	1.7	-0.3	INREF - 0.2	INREF + 0.2	VCCIO + 0.3	1.10	1.90	8	-8

a. The data provided in **Table 23** represents the JEDEC and PCI specification. QuickLogic devices either meet or exceed these requirements.

Table 24 lists the worst case process (T_J=125°C) output currents (in mA) across the output driver at three levels of I/O voltages. All drive strength data was measured at I/O voltages of 0.4 V and VCCIO - 0.4 V.

Table 24: GPIO Programmable Drive Strength

Drive Strength	IOH (mA)			IOL (mA)		
	1.8V	2.5V	3.3V	1.8V	2.5V	3.3V
1	2.2	2.8	3.2	1.7	2.3	2.7
2	4.1	5.2	5.9	3.4	4.4	5
3	6.2	7.8	8.8	5.1	6.7	7.6
4	8	10	11.2	6.6	8.6	9.7
5	10	12.4	13.9	8.3	10.7	12.1
6	11.8	14.6	16.3	9.8	12.7	14.2
7	13.7	16.9	18.9	11.5	14.7	16.6
8	15.3	18.9	21	12.9	16.5	18.5
9	17.1	21.1	23.4	14.5	18.5	20.7
10	18.8	23	25.5	15.9	20.2	22.6
11	20	25	27.6	17.4	22	24.6
12	21.7	26.4	29.1	18.6	23.5	26.1
N/A	Reserved					

Figure 15 and **Figure 16** illustrate quiescent current for QL1P100 with VLP = 0 V and 3.3 V.

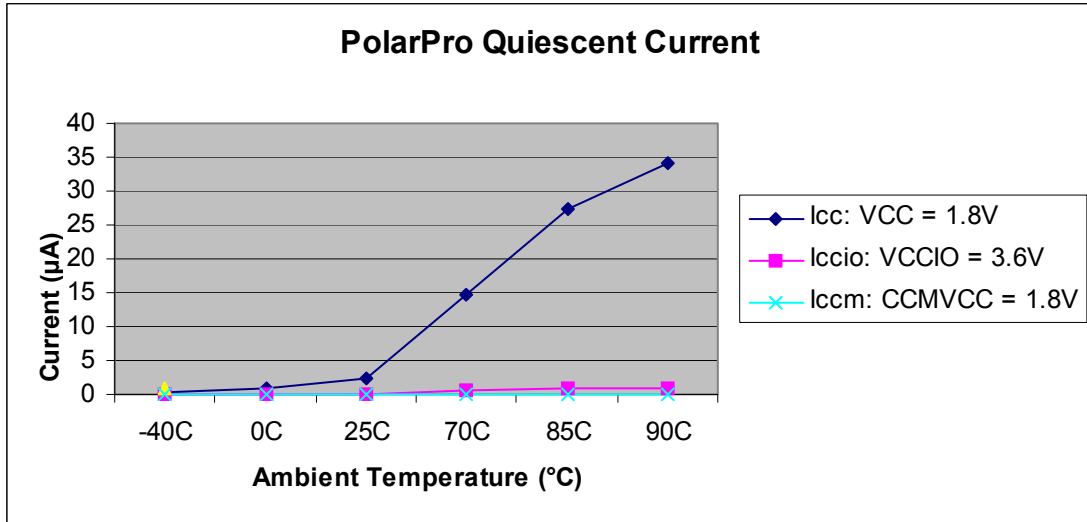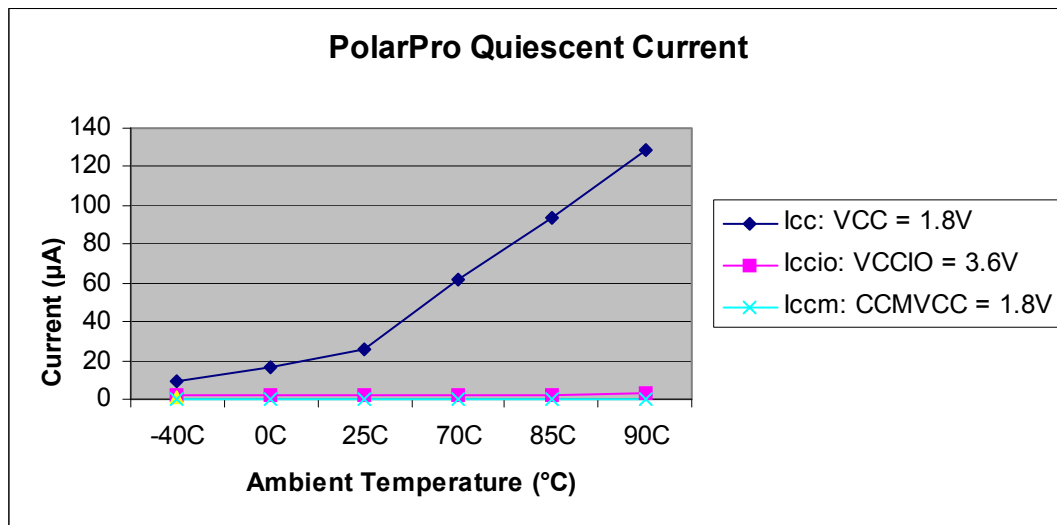Figure 15: Quiescent Current for QL1P100 with VLP = 0 V

PolarPro Quiescent Current

Figure 16: Quiescent Current for QL1P100 with VLP = 3.3 V

PolarPro Quiescent Current

AC Characteristics

AC specifications are provided in **Table 25** through **Table 37**. Logic cell diagrams and waveforms are provided in **Figure 17** through **Figure 30**. All of the following AC timing numbers are for worst case Commercial (T = 85°C Junction, V= 1.71V), and worst case Industrial (T = 100°C Junction, V=1.71V) conditions.

Figure 17: PolarPro Logic Cell
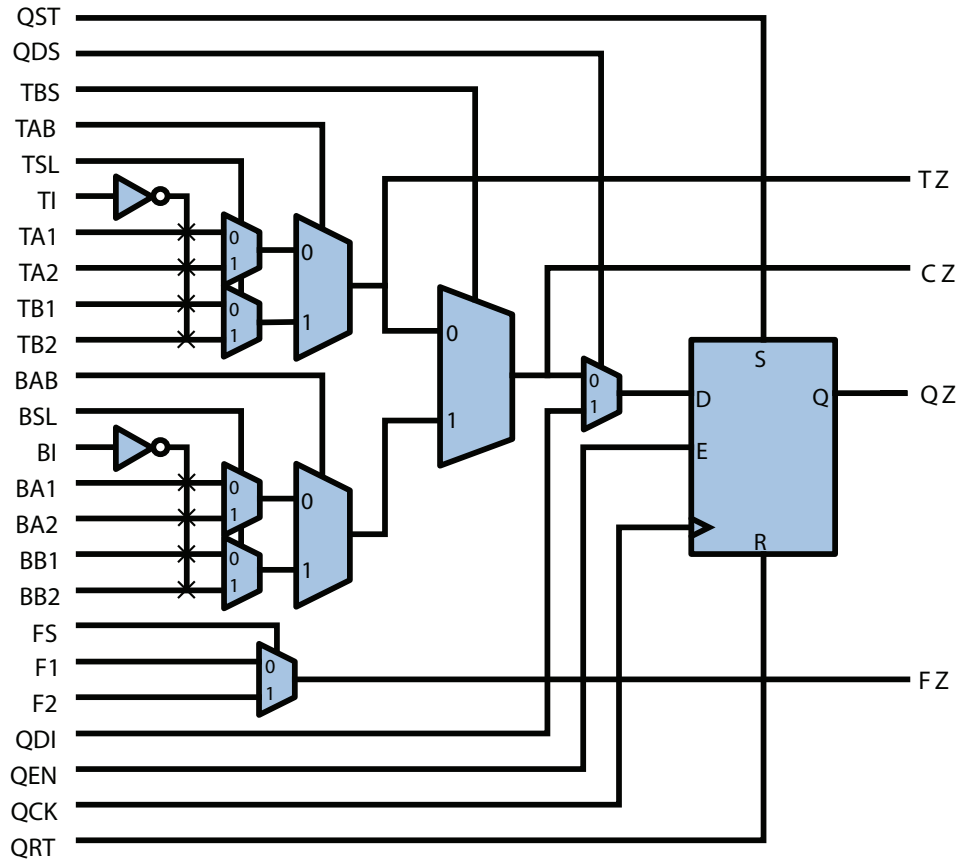
Table 25: Logic Cell Delays

Symbol	Parameter	Commercial		Industrial	
		Min.	Max.	Min.	Max.
t_{PD}	Combinatorial delay of the longest path: time taken by the combinatorial circuit to output	0.32 ns	0.59 ns	0.34 ns	0.62 ns
t_{SU}	Setup time: time the synchronous input of the flip-flop must be stable before the active clock edge	0.23 ns	0.56 ns	0.24 ns	0.58 ns
t_{HL}	Hold time: time the synchronous input of the flip-flop must be stable after the active clock edge	0 ns	N/A	0 ns	N/A
t_{ESU}	Enable setup time: time the enable input of the flip-flop must be stable before the active clock edge	0.23 ns	0.85 ns	0.89 ns	0.24 ns
t_{EHL}	Enable hold time: time the enable input of the flip-flop must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{CO}	Clock-to-out delay: the amount of time taken by the flip-flop to output after the active clock edge.	0.48 ns	0.52 ns	0.50 ns	0.55 ns
t_{CWHI}	Clock high time: required minimum time the clock stays high	0.46 ns	0.46 ns	0.46 ns	0.46 ns
t_{CWLO}	Clock low time: required minimum time that the clock stays low	0.46 ns	0.46 ns	0.46 ns	0.46 ns
t_{SET}	Set delay: time between when the flip-flop is "set" (high) and when the output is consequently "set" (high)	0.60 ns	0.60 ns	0.61 ns	0.61 ns
t_{RESET}	Reset delay: time between when the flip-flop is "reset" (low) and when the output is consequently "reset" (low)	0.68 ns	0.68 ns	0.71 ns	0.71 ns
t_{SW}	Set width: time that the SET signal must remain high/low	0.30 ns	0.30 ns	0.30 ns	0.30 ns
t_{RW}	Reset width: time that the RESET signal must remain high/low	0.30 ns	0.30 ns	0.30 ns	0.30 ns

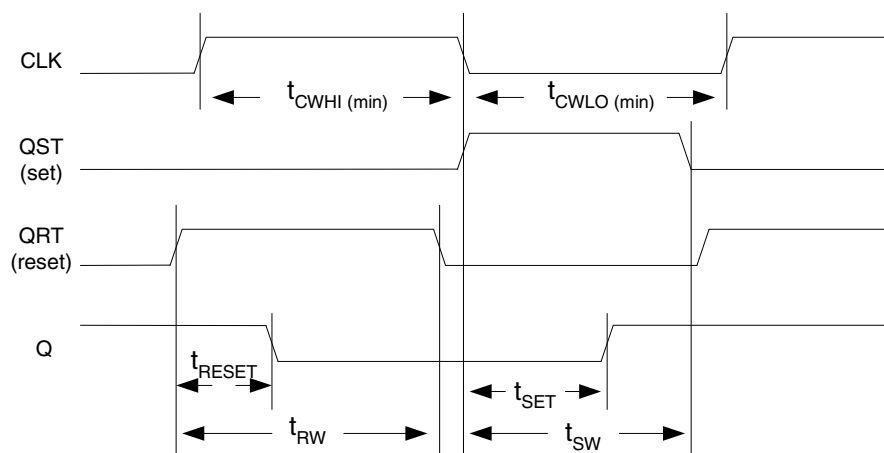Figure 18: Logic Cell Flip-Flop Timings—First Waveform

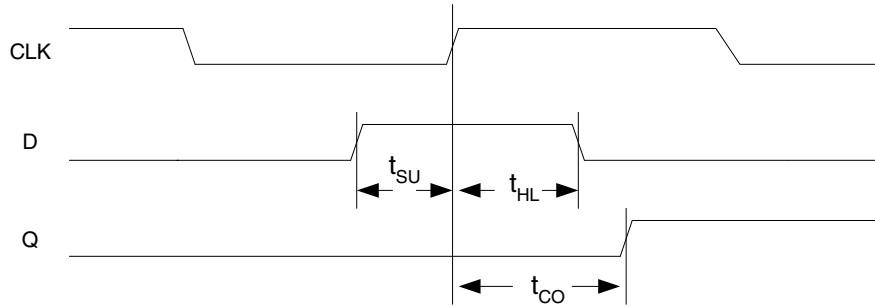Figure 19: Logic Cell Flip-Flop Timings—Second Waveform
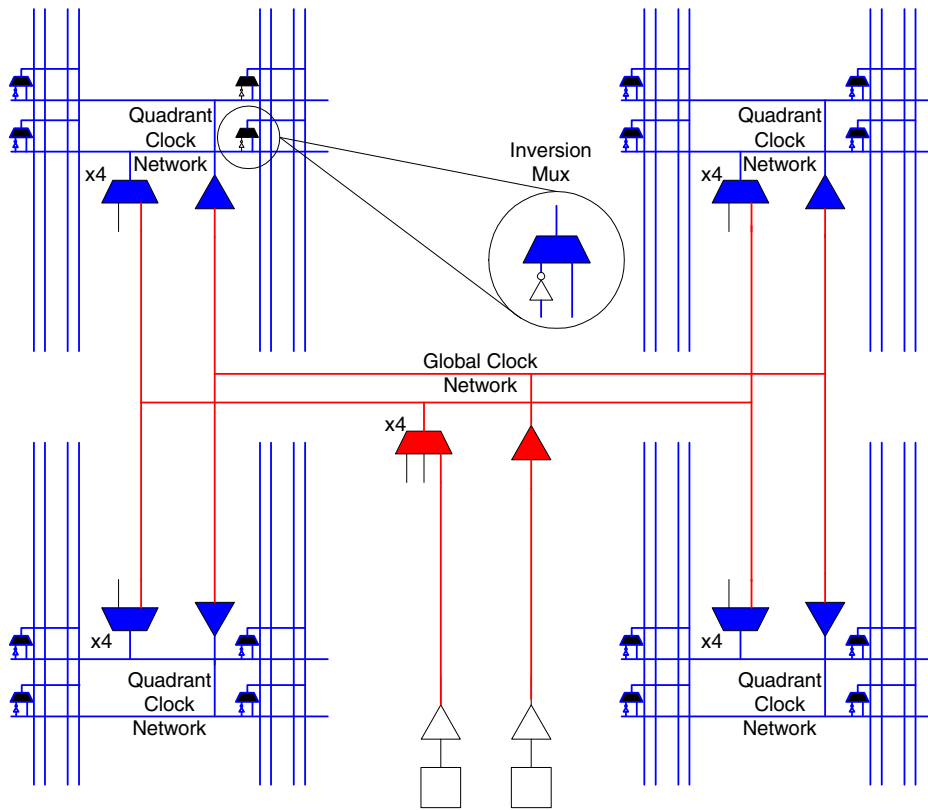

Figure 20: PolarPro Clock Network

Table 26: PolarPro Tree Clock Delay

Clock Segment	Parameter	Commercial		Industrial	
		Min.	Max.	Min.	Max.
t_{PGCK}	Delay from global clock pad input to quadrant network	1.54 ns	1.86 ns	1.56 ns	1.88 ns
t_{PDCK}	Delay from dedicated clock pad input to quadrant network	1.4 ns	1.66 ns	1.42 ns	1.68 ns
t_{BGCK}	Global clock tree delay (quad net to flip-flop)	20 ps	200 ps	30 ps	220 ps
t_{GSKEW}	Global delay clock skew	30 ps	190 ps	40 ps	200 ps
t_{DSKEW}	Dedicated clock skew	30 ps	190 ps	40 ps	200 ps

RAM Timing

Figure 21: RAM Module
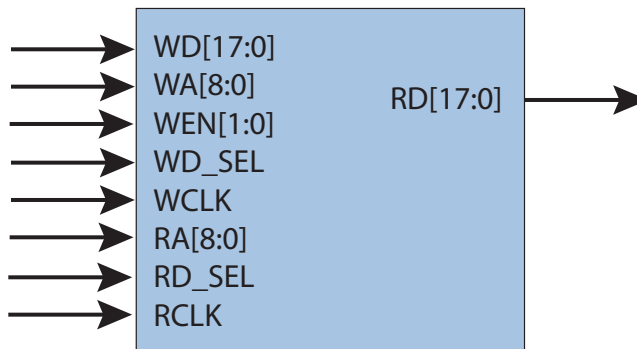
Table 27: RAM Cell Synchronous Write Timing

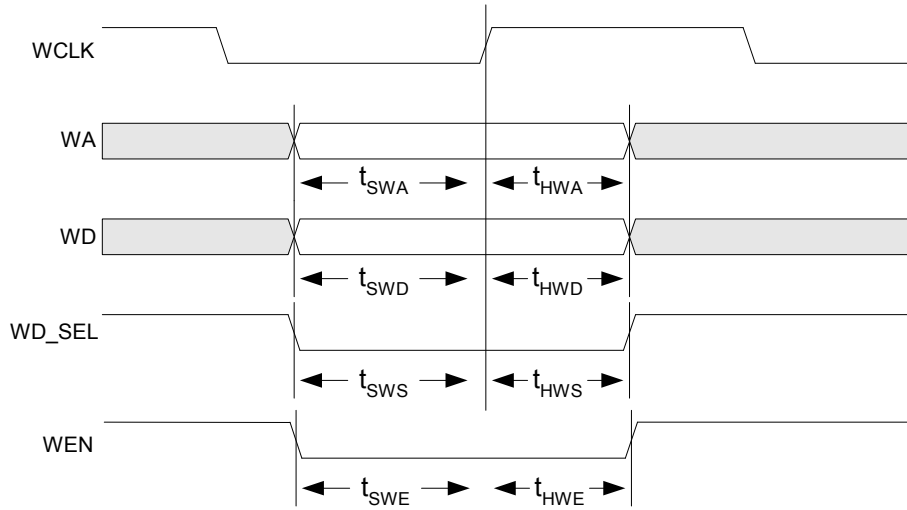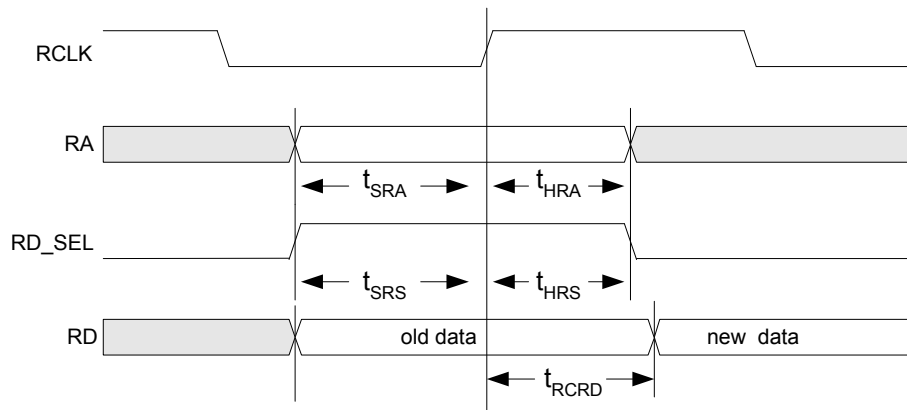| Symbol	Parameter	Commercial		Industrial	
		Min.	Max.	Min.	Max.
t_{SWA}	WA setup time to WCLK: time the WRITE ADDRESS must be stable before the active edge of the WRITE CLOCK	0.29 ns	1.10 ns	0.31 ns	1.28 ns
t_{HWA}	WA hold time to WCLK: time the WRITE ADDRESS must be stable after the active edge of the WRITE CLOCK	0 ns	0.21 ns	0 ns	0.20 ns
t_{SWD}	WD setup time to WCLK: time the WRITE DATA must be stable before the active edge of the WRITE CLOCK	0.31 ns	1.74 ns	0.40 ns	2.21 ns
t_{HWD}	WD hold time to WCLK: time the WRITE DATA must be stable after the active edge of the WRITE CLOCK	0 ns	0.22 ns	0 ns	0.17 ns
t_{SWS}	WD_SEL setup time to WCLK: time WRITE CHIP SELECT must be stable before the active edge of the WRITE CLOCK	0.42 ns	1.10 ns	0.49 ns	1.28 ns
t_{HWS}	WD_SEL hold time to WCLK: time WRITE CHIP SELECT must be stable after the active edge of the WRITE CLOCK	0 ns	0.04 ns	0 ns	0.04 ns
t_{SWE}	WEN setup time to WCLK: time the WRITE ENABLE must be stable before the active edge of the WRITE CLOCK	0.63 ns	1.10 ns	0.74 ns	1.28 ns
t_{HWE}	WEN hold time to WCLK: time the WRITE ENABLE must be stable after the active edge of the WRITE CLOCK	0 ns	0 ns	0 ns	0 ns

Figure 22: RAM Cell Write Timing
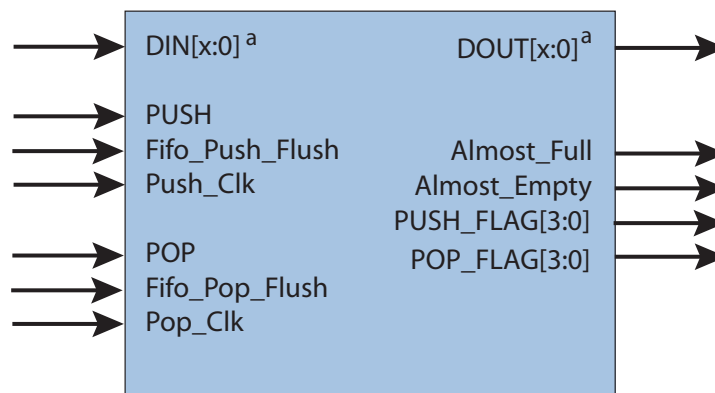

Table 28: RAM Cell Synchronous Read Timing

Symbol	Parameter	Commercial		Industrial	
		Min.	Max.	Min.	Max.
t_{SRA}	RA setup time to RCLK: time the READ ADDRESS must be stable before the active edge of the READ CLOCK	0.29 ns	1.10 ns	0.31 ns	1.28 ns
t_{HRA}	RA hold time to RCLK: time the READ ADDRESS must be stable after the active edge of the READ CLOCK	0 ns	0.21 ns	0 ns	0.20 ns
t_{SRS}	RD_SEL setup time to RCLK: time the READ CHIP SELECT must be stable before the active edge of the READ CLOCK	0.42 ns	1.10 ns	0.49 ns	1.28 ns
t_{HRS}	RD_SEL hold time to RCLK: time the READ CHIP SELECT must be stable after the active edge of the READ CLOCK	0 ns	0.04 ns	0 ns	0.04 ns
t_{RCRD}	RCLK to RD: time between the active READ CLOCK edge and the time when the data is available at RD	2.62 ns	5.67 ns	2.69 ns	5.88 ns

Figure 23: RAM Cell Read Timing

FIFO Timing

Figure 24: FIFO Module

a. $x = \{1,2,3,....35\}$.

Table 29: FIFO PUSH Timing

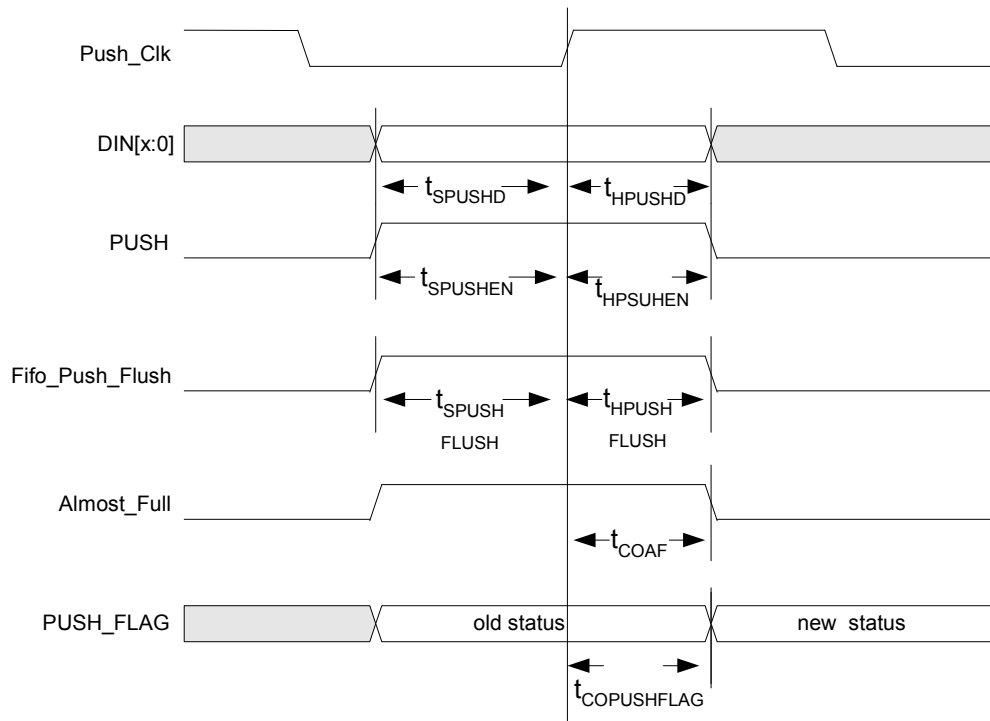| Symbol	Parameter	Commercial		Industrial	
		Min.	Max.	Min.	Max.
t_{SPUSHD}	DIN setup time to Push_Clk: time DIN must be stable before the active edge of the FIFO Push clock	0.31 ns	1.74 ns	0.40 ns	2.21 ns
t_{HPUSHD}	DIN hold time to Push_Clk: time DIN must be stable after the active edge of the FIFO Push clock	0 ns	0.22 ns	0 ns	0.17 ns
$t_{SPUSHEN}$	PUSH setup time to Push_Clk: time PUSH must be stable before the active edge of the FIFO Push clock	1.07 ns	1.57 ns	1.38 ns	2.0 ns
$t_{HPUSHEN}$	PUSH hold time to Push_Clk: time PUSH must be stable after the active edge of the FIFO Push clock	0 ns	0 ns	0 ns	0 ns
$t_{SPUSHFLUSH}$	FLUSH setup time to Push_Clk: time Fifo_Push_Flush must be stable before the active edge of the FIFO Push clock	1.11 ns	1.74 ns	1.43 ns	2.21 ns
$t_{HPUSHFLUSH}$	FLUSH hold time to Push_Clk: time Fifo_Push_Flush must be stable after the active edge of the FIFO Push clock	0 ns	0 ns	0 ns	0 ns
t_{COAF}	Clock-to-out of Almost Full	2.66 ns	3.34 ns	2.72 ns	3.42 ns
$t_{COPUSHFLAG}$	Clock-to-out of FIFO Push level indicator	2.36 ns	4.20 ns	2.41 ns	4.32 ns

Figure 25: FIFO PUSH Timing

Table 30: FIFO POP Timing

Symbol	Parameter	Commercial		Industrial	
		Min.	Max.	Min.	Max.
t$_{SPOPEN}$	POP setup time to Pop_Clk: time POP must be stable before the active edge of the FIFO Pop clock	1.01 ns	1.13 ns	1.19 ns	1.32 ns
t$_{HPOPEN}$	POP hold time to Pop_Clk: time POP must be stable after the active edge of the FIFO Pop clock	0 ns	0 ns	0 ns	0 ns
t$_{SPOPFLUSH}$	FLUSH setup time to Pop_Clk: time Fifo_Pop_Flush must be stable before the active edge of the FIFO Pop clock	1.11 ns	1.74 ns	1.43 ns	2.21 ns
t$_{HPOPFLUSH}$	FLUSH hold time to Pop_Clk: time Fifo_Pop_Flush must be stable after the active edge of the FIFO Pop clock	0 ns	0 ns	0 ns	0 ns
t$_{FPOP}$	Pop_Clk to Pop: Clock-to-out from the active FIFO CLOCK edge and the time when the data is popped from the FIFO at DOUT	2.32 ns	5.61 ns	2.37 ns	5.88 ns
t$_{COAE}$	Clock-to-out of Almost Empty	2.64 ns	3.58 ns	2.70 ns	3.66 ns
t$_{COPOPFLAG}$	Clock-to-out of FIFO Pop level indicator	2.32 ns	3.93 ns	2.38 ns	4.03 ns

Figure 26: FIFO POP Timing
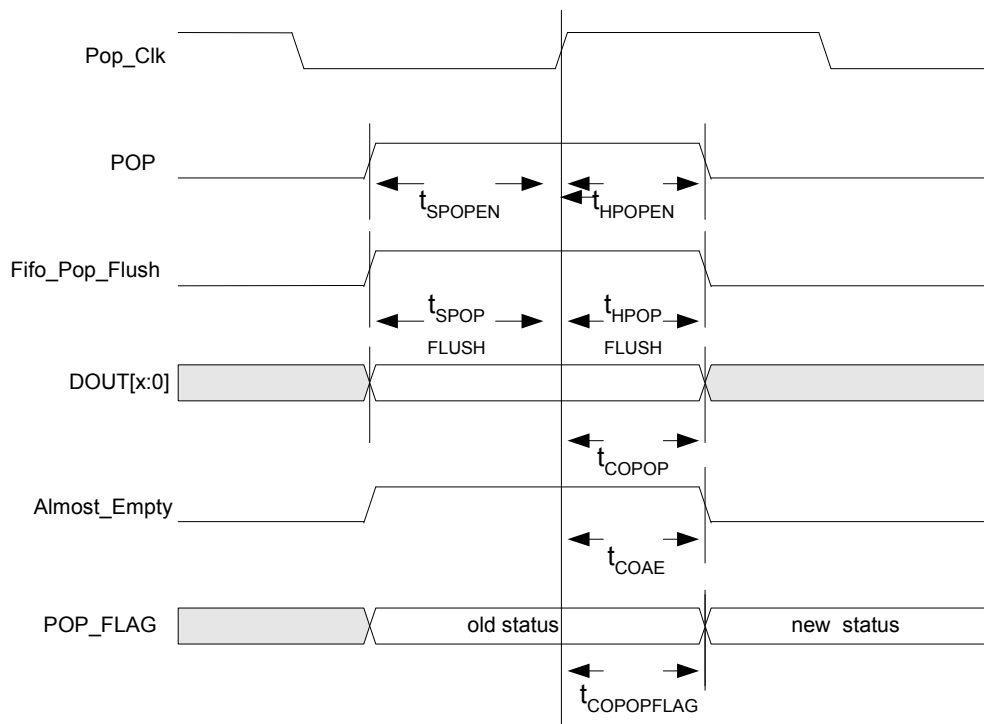
GPIO Cell Timing

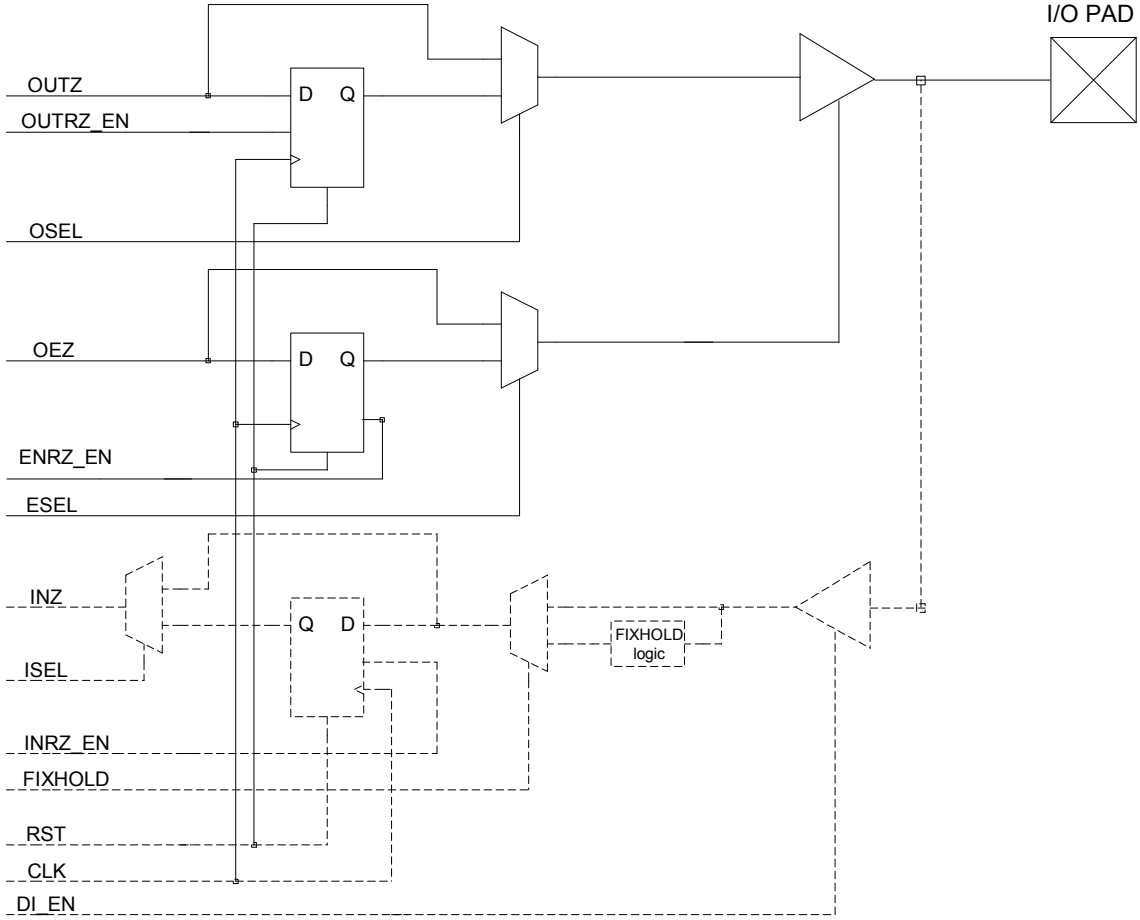Figure 27: PolarPro I/O Cell Output Path
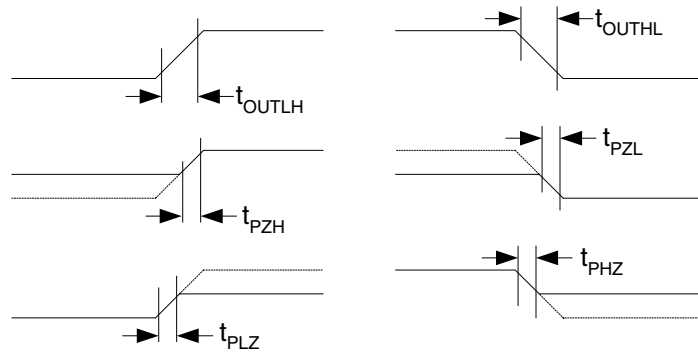

Figure 28: PolarPro I/O Cell Output Enable Timing

Table 31: Output Timing Characteristics @ VCCIO = 3.3 V, T = 25° C

Symbol	Parameter	Value (ns)	
		Slowest Slew Max.	Fastest Slew Max.
t_{OUTLH}	Output Delay low to high (90% of H)	8.10	1.00
t_{OUTHL}	Output Delay high to low (10% of L)	9.60	0.90
t_{PZH}	Output Delay tri-state to high (90% of H)	3.40	0.30
t_{PZL}	Output Delay tri-state to low (10% of L)	3.90	0.30
t_{PHZ}	Output Delay high to tri-state	3.60	0.36
t_{PLZ}	Output Delay low to tri-state	4.1	0.41

Table 32: Output Timing Characteristics @ VCCIO = 2.5 V, T = 25° C

Symbol	Parameter	Value (ns)	
		Slowest Slew Max.	Fastest Slew Max.
t_{OUTLH}	Output Delay low to high (90% of H)	12.20	1.10
t_{OUTHL}	Output Delay high to low (10% of L)	18.80	1.00
t_{PZH}	Output Delay tri-state to high (90% of H)	4.50	0.45
t_{PZL}	Output Delay tri-state to low (10% of L)	8.40	0.52
t_{PHZ}	Output Delay high to tri-state	8.10	0.52
t_{PLZ}	Output Delay low to tri-state	5.30	0.53

Table 33: Output Timing Characteristics @ VCCIO = 1.8 V, T = 25° C

Symbol	Parameter	Value (ns)	
		Slowest Slew Max.	Fastest Slew Max.
t_{OUTLH}	Output Delay low to high (90% of H)	2.50	2.20
t_{OUTHL}	Output Delay high to low (10% of L)	1.70	1.40
t_{PZH}	Output Delay tri-state to high (90% of H)	8.30	0.70
t_{PZL}	Output Delay tri-state to low (10% of L)	24.70	1.05
t_{PHZ}	Output Delay high to tri-state	23.50	1.25
t_{PLZ}	Output Delay low to tri-state	10.80	0.78

Table 34 lists the typical output slew rates (in V/ns) across three levels of output voltages, with a drive strength of 4, and a load capacitor of 10 pF.

Table 34: GPIO Output Slew Rate

Slew	Output Slew Rate (V/ns) at VCCIO =		
	1.8 V	2.5 V	3.3 V
slow	n/a	0.20	0.36
fast	n/a	0.31	0.66
vfast	0.17	0.61	1.32
wow	0.25	1.18	2.03

Table 35: I/O Output Register Cell Timing

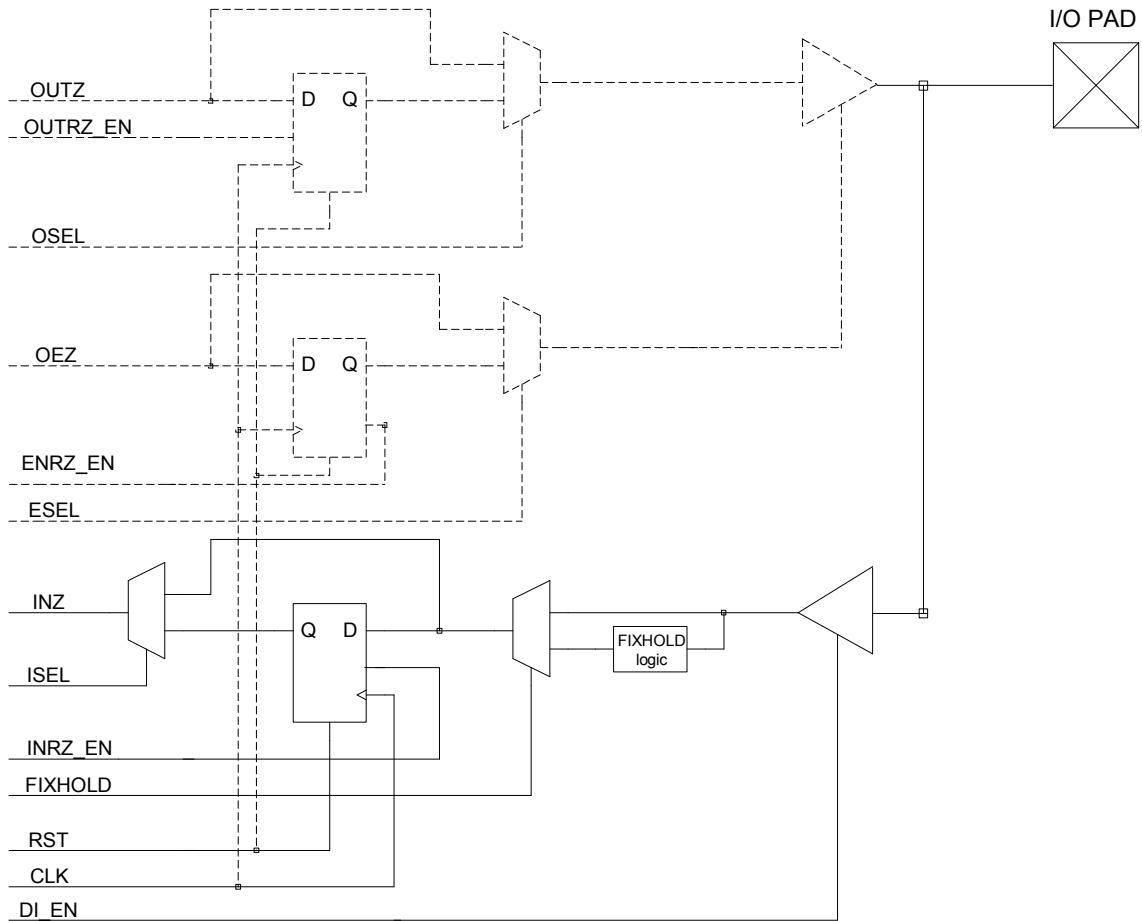| Symbol	Parameter	Commercial		Industrial	
		Min.	Max.	Min.	Max.
t_{OSU}	Output register setup time: time the synchronous OUTZ input of the flip-flop must be stable before the active clock edge	0.33 ns	0.38 ns	0.34 ns	0.36 ns
t_{OHL}	Output register hold time: time the synchronous OUTZ input of the flip-flop must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{OCO}	Output register clock-to-out: time taken by the flip-flop to output after the active clock edge	5.25 ns	5.99 ns	5.46 ns	6.29 ns
t_{ORST}	Output register reset delay: time between when the flip-flop is "reset" (low) and when the output is consequently "reset" (low)	5.85 ns	5.85 ns	6.03 ns	6.03 ns
t_{OESU}	Output register clock enable setup time: time OUTRZ_EN must be stable before the active clock edge	0.33 ns	0.51 ns	0.30 ns	0.54 ns
t_{OEH}	Output register clock enable hold time: time OUTRZ_EN must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{OEZSU}	Output register clock enable setup time: time OEZ must be stable before the active clock edge	0.14 ns	0.20 ns	0.15 ns	0.18 ns
t_{OEZH}	Output register clock enable hold time: time OEZ must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{OPD}	Output signal propagation delay: propagation delay of OUTZ to the output pad	4.82 ns	5.44 ns	5.03 ns	5.72 ns

Figure 29: PolarPro I/O Cell Input Path
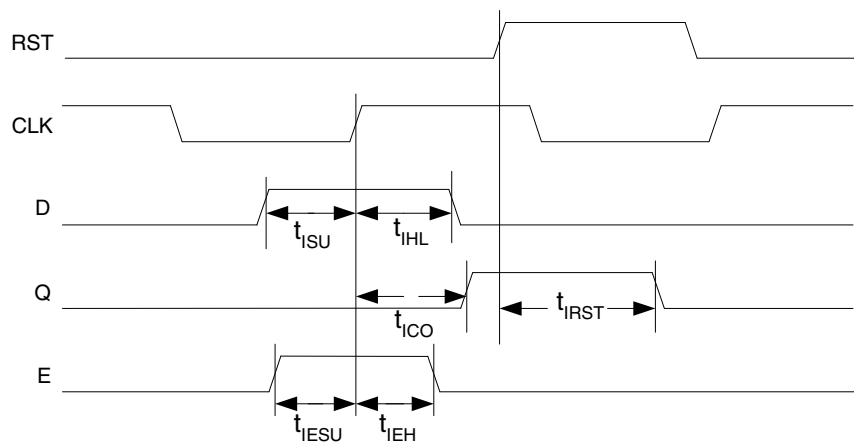
Figure 30: PolarPro Input Register Cell Timing

Table 36: I/O Input Register Cell Timing

Symbol	Parameter	Commercial		Industrial	
		Min.	Max.	Min.	Max.
t_{ISU}	Input register setup time: time the synchronous input of the flip-flop must be stable before the active clock edge	2.51 ns	2.85 ns	2.80 ns	2.82 ns
t_{IHL}	Input register hold time: time the synchronous input of the flip-flop must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{ICO}	Input register clock-to-out: time taken by the flip-flop to output after the active clock edge	1.68 ns	2.66 ns	1.58 ns	2.70 ns
t_{IRST}	Input register reset delay: time between when the flip-flop is "reset" (low) and when the output is consequently "reset" (low)	1.59 ns	1.59 ns	1.53 ns	1.53 ns
t_{IESU}	Input register clock enable setup time: time INRZ_EN must be stable before the active clock edge	0.25 ns	0.40 ns	0.23 ns	0.43 ns
t_{IEH}	Input register clock enable hold time: time INRZ_EN must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
$t_{IDIENSU}$	Input data enable setup time: time DI_EN must be stable before the active clock edge	2.39 ns	5.38 ns	2.28 ns	5.63 ns
t_{IDIENH}	Input data enable hold time: time DI_EN must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{IFHSU}	Input fixhold setup time: time FIXHOLD must be stable before the active clock edge	2.39 ns	5.38 ns	2.28 ns	5.63 ns
t_{IFHH}	Input fixhold hold time: time FIXHOLD must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns

Table 37: I/O Input Buffer Delays

Symbol	Parameter	Value	
	To get the total input delay add this delay to t_{ISU}	Min.	Max.
t_{SID} (LVTTL)	LVTTL input delay: Low Voltage TTL for 3.3 V applications	TBD	TBD
t_{SID} (LVCMOS2)	LVCMOS2 input delay: Low Voltage CMOS for 2.5 V and lower applications	TBD	TBD
t_{SID} (LVCMOS18)	LVCMOS18 input delay: Low Voltage CMOS for 1.8 V applications	TBD	TBD
t_{SID} (GTL+)	GTL+ input delay: Gunning Transceiver Logic	TBD	TBD
t_{SID} (SSTL3)	SSTL3 input delay: Stub Series Terminated Logic for 3.3 V	TBD	TBD
t_{SID} (SSTL2)	SSTL2 input delay: Stub Series Terminated Logic for 2.5 V	TBD	TBD
t_{SID} (PCI)	PCI input delay: Peripheral Component Interconnect for 3.3 V	TBD	TBD

Package Thermal Characteristics

The PolarPro device is available for Commercial (0°C to 85°C Junction), Industrial (-40°C to 100°C Junction), and Military (-55°C to 125°C Junction) temperature ranges.

Thermal Resistance Equations:

$$\theta_{JA} = (TJ - TA)/P$$
$$P_{MAX} = (T_{JMAX} - T_{AMAX})/\theta_{JA}$$

Parameter Description:

θ_{JA}: Junction-to-ambient thermal resistance

T_J: Junction temperature

T_A: Ambient temperature

P: Power dissipated by the device while operating

P_{MAX}: The maximum power dissipation for the device

T_{JMAX}: Maximum junction temperature

T_{AMAX}: Maximum ambient temperature

NOTE: Maximum junction temperature (T_{JMAX}) is 125°C. To calculate the maximum power dissipation for a device package look up θ_{JA} from **Table 38**, pick an appropriate T_{AMAX} and use: $P_{MAX} = (125°C - T_{AMAX})/\theta_{JA}$

Table 38: Package Thermal Characteristics

Package Description				Theta-JA (° C/W)		
Device	Package Code	Package Type	Pin Count	0 LFM	200 LFM	400 LFM
QL1P100	PU	TFBGA[a]	86	58	50	48

a. Thin Profile Fine Pitch Ball Grid Array

Moisture Sensitivity Level

All PolarPro devices are Moisture Sensitivity Level 3.

Table 39: Solder and Lead Finish Composition

	Lead Included	Lead-Free
BGA Solder	63% Pb, 37% Sn	Sn3AgCu:Sn4AgCu[a]

a. Sn3AgCu:Sn4AgCu means that Ag can range from 3% to 4%. Cu is always 0.5%.

Power-Up Sequencing
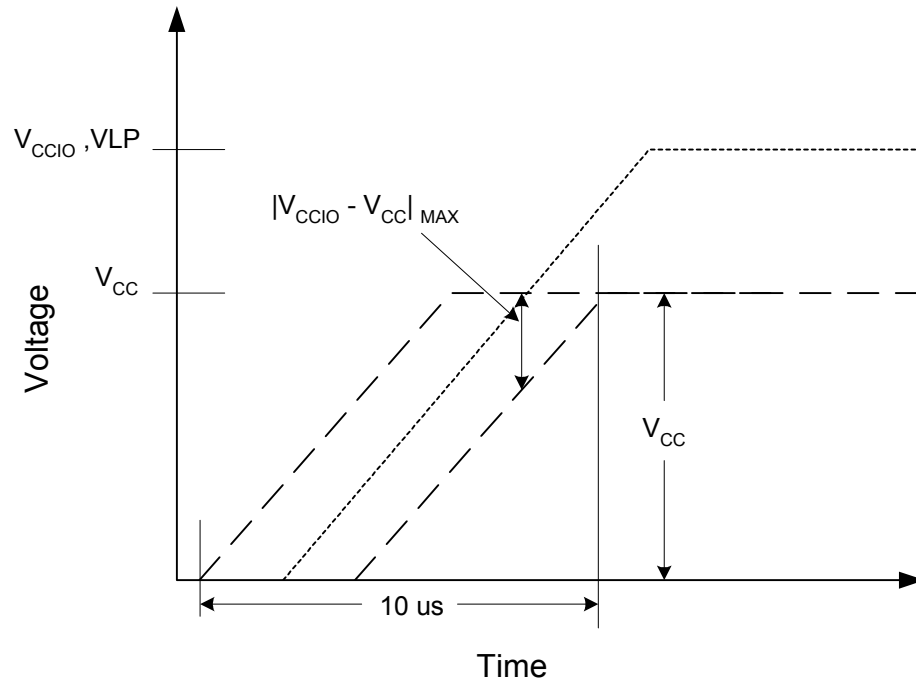
Figure 31: Power-Up Sequencing

Figure 31 shows an example where all VCCIO = 3.3 V. When powering up a PolarPro device, VCC, VCCIO rails must take 10 µs or longer to reach the maximum value (refer to **Figure 31**). Ramping VCC and VCCIO faster than 10 µs can cause the device to behave improperly.

It is also important to ensure VCCIO and VLP are within 500 mV of VCC when ramping up the power supplies. In the case where VCCIO or VLP are greater than VCC by more than 500 mV an additional current draw can occur as VCC passes its threshold voltage. In a case where VCC is greater than VCCIO by more than 500 mV the protection diodes between the power supplies become forward biased. If this occurs then there will be an additional current load on the power supply. Having the diodes on can cause a reliability problem, since it can wear out the diodes and subsequently damage the internal transistors. As noted in the VLP section, during the transition from VLP mode to normal operation, the VLP pin can draw up to 1.5 mA. Consequently, if using a pull-up resistor, use a pull-up resistor with a value that is less than $2 \text{ K}\Omega$.

Programming Stipulation

For PolarPro devices to correctly program, there must not be any race conditions or internally generated free-running oscillators in the design. This will cause an ICC programming failure during the programming process. QuickLogic cannot guarantee the operation of any device that fails programming. Therefore, race conditions and free-running oscillators must be removed from designs so that PolarPro devices can correctly pass programming.

Pin Descriptions

Table 40: Pin Descriptions

Pin	Direction	Function	Description
Dedicated Pin Descriptions			
GPIO(C:A)	I/O	General purpose input/output pin	The I/O pin is a bi-directional pin, configurable to either an input-only, output-only, or bi-directional pin. The letter inside the parenthesis means that the I/O is located in the bank with that letter. If an I/O is not used, the development software provides the option of tying that pin to GND, VCCIO, or Hi-Z.
CLK(C:A)	I	Global clock network pin low skew global clock	This pin provides access to a distributed network capable of driving the CLOCK, SET, RESET, all inputs to the Logic Cell, READ and WRITE CLOCKS, Read and Write Enables of the Embedded RAM Blocks, and I/O inputs. The voltage tolerance of this pin is specified by VCCIO(C:A).
DEDCLK(D)	I	Dedicated clock network pin low skew clock	This pin provides access to a distributed network capable of driving the CLOCK, SET, RESET, all inputs to the Logic Cell, READ and WRITE CLOCKS, Read and Write Enables of the Embedded RAM Blocks, and I/O inputs. The voltage tolerance of this pin is specified by VCCIO(D).
CCMIN(1:0)	I	CCM clock input	Input clock for CCM. The voltage tolerance for this pin is specified by the VCCIO of the same bank.
CCMVCC (1:0)	I	Power supply pin for CCM	CCM input voltage level. Configurable as 1.8 V only.
CCMGND(1:0)	I	Ground pin for CCM	Connect to ground.
VLP	I	Voltage low power	Active low. Therefore, when VLP pin is low, the device will go into low power mode. Tie VLP to 3.3 V to disable low power mode.
VCC	I	Power supply pin	Connect to 1.8 V supply.
VCCIO(D:A)	I	Input voltage tolerance pin	This pin provides the flexibility to interface the device with either a 3.3 V, 2.5 V, or 1.8 V device. The letter inside the parenthesis means that the VCCIO is located in the bank with that letter. Every I/O pin in the same bank will be tolerant of the same VCCIO input signals and will drive VCCIO level output signals. This pin must be connected to either 3.3 V, 2.5 V, or 1.8 V.
GND	I	Ground pin	Connect to ground.

Recommended Unused Pin Terminations for PolarPro Devices

All unused, general purpose I/O pins can be tied to VCCIO, GND, or Hi-Z (high impedance) internally. By default, QuickLogic QuickWorks software ties unused I/Os to GND.

Terminate the rest of the pins at the board level as recommended in **Table 41**.

Table 41: Recommended Unused Pin Terminations

Signal Name	Recommended Termination
CLK <x>[a]	Connect to GND or VCCIO(x) if unused.
VLP	Tie VLP to 3.3 V to disable low power mode.
CCMVCC(1:0)	If a CCM is not used, the corresponding CCMVCC may be tied to GND to reduce power consumption. If a CCM is used, do not try to disable the CCM by tying the CCMVCC to GND.

a. x represents A, B, C or D.

Packaging Pinout Table

## PolarPro QL1P100 – 86 TFBGA Pinout Table

Table 42: PolarPro QL1P100 – 86 TFBGA Pinout Table

| Pin	Function	Pin	Function	Pin	Function	Pin	Function
A1	VCC	C10	GPIO(A)	F9	GPIO(A)	J10	GPIO(A)
A2	GPIO(D)	D1	GPIO(C)	G1	CLK(C)	K1	GND
A3	GPIO(D)	D4	VCCIO(D)	G2	VCCIO(B)	K2	GPIO(B)
A5	GPIO(D)	D5	VCC	G3	GPIO(C)	K3	GPIO(B)
A6	DEDCLK(D)	D6	GPIO(D)	G4	VCC	K4	GPIO(B)
A8	GPIO(D)	D7	GPIO(D)	G5	VCCIO(C)	K6	GPIO(B)
A9	GPIO(D)	D9	GPIO(A)	G6	GND	K7	GPIO(B)
A11	VCC	D11	GPIO(A)	G7	GND	K8	GPIO(B)
B1	GND	E1	GPIO(C)	G8	VCC	K10	GPIO(A)
B2	GPIO(C)	E4	GPIO(C)	G10	GPIO(A)	K11	GPIO(A)
B3	GPIO(D)	E5	VCCIO(D)	G11	CLK(A)/CCMIN(1)	L1	VCC
B4	GPIO(D)	E6	GND	H1	GPIO(C)	L2	GPIO(B)
B5	GPIO(D)	E7	GND	H2	GPIO(C)	L4	GPIO(B)
B6	GPIO(D)	E8	VCCIO(A)	H5	VCCIO(C)	L5	CLK(B)
B7	GPIO(D)	E9	VCCIO(A)	H6	GND	L6	CLK(B)
B8	GPIO(D)	E11	GPIO(A)	H7	VCCIO(B)	L7	GPIO(B)
B9	GPIO(D)	F1	GPIO(C)	H8	VCCIO(B)	L8	GPIO(B)
B10	CCMGND(1)	F2	GPIO(C)	H9	VCCIO(B)	L9	VLP
B11	GND	F4	GND	H10	GPIO(A)	L10	GND
C2	GPIO(C)	F5	GND	H11	GPIO(A)	L11	VCC
C3	GPIO(C)	F7	GND	J2	GPIO(C)		
C9	CCMVCC(1)	F8	VCC	J4	GPIO(B)		

Packaging Pinout Diagram

PolarPro QL1P100 – 86 TFBGA Pinout Diagram

Top
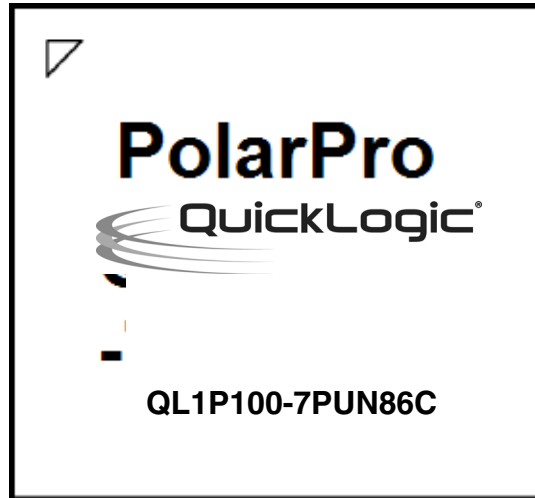
Bottom
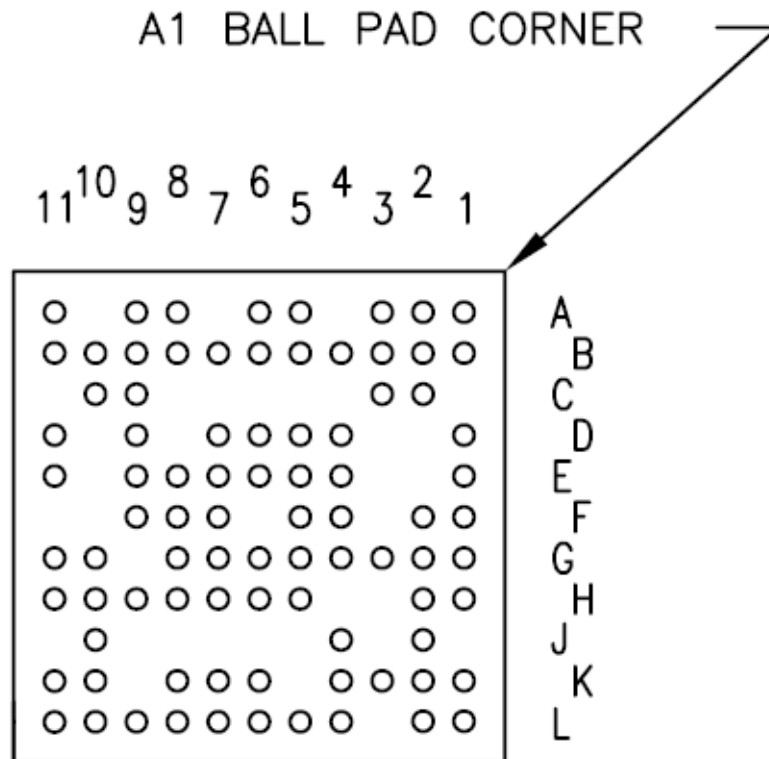
Package Mechanical Drawing
86-Pin TFBGA Packaging Drawing

Ordering Information

```
QL        1P100        -6        PU86        C
```

Operating Range:
C = Commercial
I = Industrial
M = Military

Package Lead Count:
PU86 (PUN86)* = 86-pin TFBGA (0.5mm)

Speed Grade:
-6 - fast
-7 - faster
-8 - fastest

Part Number:
1P100

QuickLogic Device
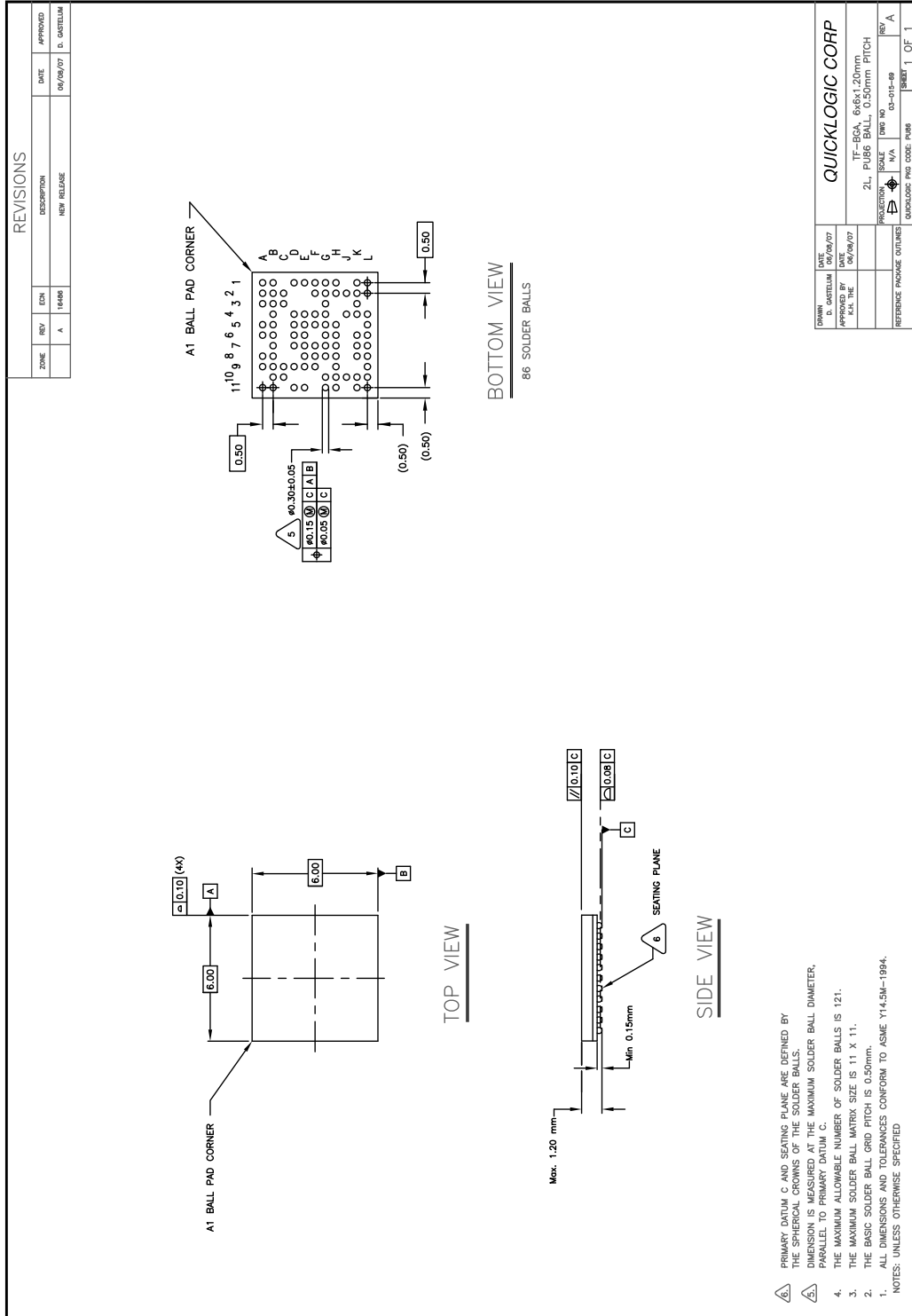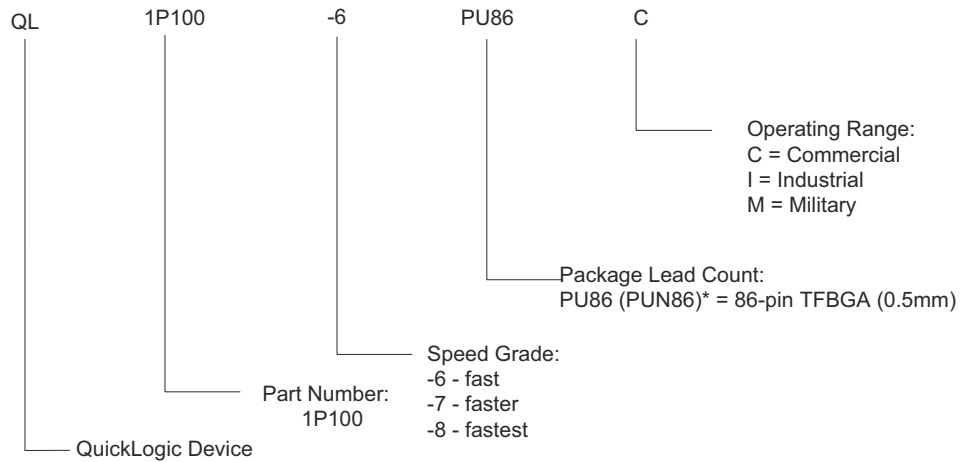
* Lead-free packaging is denoted by the character 'N' preceding the number of pins.

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Revision History

Revision	Date	Originator and Comments
A	July 2007	Jason Lew and Kathleen Murchek - First release.
B	August 2007	Jason Lew and Kathleen Murchek - Updated mechanical drawing.
C	September 2007	Jason Lew and Kathleen Murchek - Merged with other PolarPro data sheets using conditional text.
D	January 2008	Jason Lew and Kathleen Murchek - Logic Cell Delays table change t_{HL} Max. to N/A.
E	July 2008	Jason Lew and Kathleen Murchek - Updated Contact Information. - Updated Copyright and Trademark Information. - Added Notice of Disclaimer.
F	January 2010	Kathleen Murchek - Added values for Quiescent Current in DC Characteristics table.
G	September 2010	Kathleen Bylsma - Updated Contact Information.

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