SIEMENS

Preliminary

SAB 8051A/8031A Ext. Temp
8-Bit Single-Chip Microcontroller

Extended Temperature Range: −40°C to +85°C
−40°C to +110°C

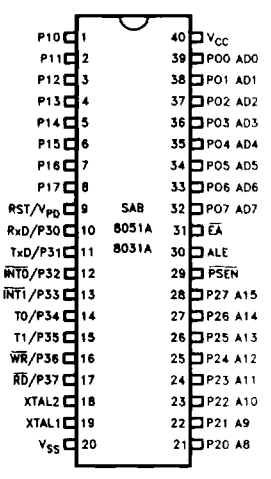
Mask-Programmable ROM
SAB 8051A-12-P-T40/85
SAB 8051A-10-P-T40/110

- Advanced Version of the SAB 8031/8051 for Extended Temperature Range
- SAB 8051A/8031A-12-T40/85: 12 MHz Operation
- SAB 8051A/8031A-10-T40/110: 10 MHz Operation
- 4K × 8 ROM
- 128 × 8 RAM
- Four 8-Bit Ports, 32 I/O Lines
- Two 16-Bit Timer/Event Counters

External ROM
SAB 8031A-12-P-T40/85
SAB 8031A-10-P-T40/110

- High-Performance Full-Duplex Serial Channel
- External Memory Expandable up to 128K
- Compatible with SAB 8080/8085 Peripherals
- Boolean Processor
- 218 User Bit-Addressable Locations
- Most Instructions Execute in 1 µs
- 4 µs Multiply and Divide

Pin Configuration



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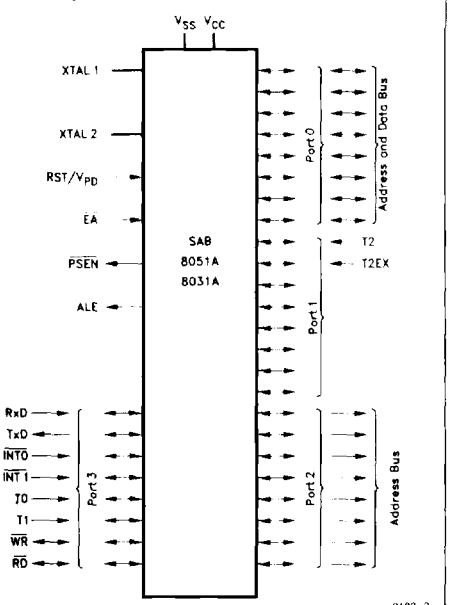
Logic Symbol



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The SAB 8051A/8031A for the two extended temperature ranges (industrial temperature range: −40°C to +85°C, automotive temperature range: −40°C to +110°C) is fully compatible with the standard SAB 8051A/8031A with respect to architecture, instruction set, and software portability.

The SAB 8051A/8031A is a stand-alone, high-performance single-chip microcontroller fabricated in +5V advanced N-channel, silicon gate Siemens MYMOS technology and packaged in a 40-pin DIP.

The SAB 8051A contains a non-volatile 4K × 8 read-only program memory; a volatile 128 × 8 read/write data memory; 32 I/O lines; two 16-bit timer/counters; a five-source two-priority-level, nested interrupt structure; a serial I/O port for either multiprocessor communications, I/O expansion, or full duplex UART; and on-chip oscillator and clock circuits. The SAB 8031A is identical with the SAB 8051A, except that it lacks the program memory.

For systems that require extra capability, the SAB 8051A can be expanded using standard TTL compatible memories and the byte-oriented SAB 8080 and SAB 8085 peripherals.

Absolute Maximum Ratings*

Ambient Temperature under Bias
T40/85 ..... −40°C to +85°C
T40/110 ..... −40°C to +110°C
Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin with
Respect to Ground (V_{SS}) ..... −0.5V to +7V
Power Dissipation 2W

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

V_{CC} = 5V ±10%; V_{SS} = 0V; T_A = −40°C to +85°C for T40/85;
T_A = −40°C to + 110°C for T40/110

Parameter	Symbol	Test Condition	Limit Values		Unit
			Min	Max	
Input Low Voltage	V_{IL}		−0.5	0.8	V
Input High Voltage Except RST/VDP and XTAL2	V_{IH}		2.0	V_{CC}+0.5	V
Input High Voltage to RST/VPD for Reset, XTAL2	V_{IH1}	XTAL 1 to V_{SS}	2.5	V_{CC}+0.5	V
Power Down Voltage to RST/VPD	V_{PD}	V_{CC} = 0V	4.5	5.5	V
Output Low Voltage Ports 1, 2, 3	V_{OL}	I_{OL} = 1.6 mA		0.45	V
Output Low Voltage Port 0, ALE, $\overline{PSEN}$	V_{OL1}	I_{OL} = 3.2 mA		0.45	V
Output High Voltage Ports 1, 2, 3	V_{OH}	I_{OH} = −80 µA	2.4		V
Output High Voltage Port 0, ALE, $\overline{PSEN}$	V_{OH1}	I_{OH} = −400 µA	2.4		V
Logical 0 Input Current Ports 1, 2, 3	I_{IL}	V_{IL} = 0.45V		−500	µA
Logical 0 Input Current XTAL2	I_{IL2}	XTAL1 = V_{SS} V_{IL} = 0.45V		−3.2	mA
Input High Current to RST/VPD for Reset	I_{IH1}	V_{IN} = V_{CC} − 1.5V		500	µA
Input Leakage Current to Port 0, $\overline{EA}$	I_{LI}	0 < V_{IN} < V_{CC}		±10	µA
Power Supply Current	I_{CC}			150	mA
Power Down Current	I_{PD}			15	mA
Capacitance of I/O Buffer	C_{IO}	f_c = 1 MHz		10	pF

AC Characteristics for T40/85: Refer to SAB 8051A/8031A Data Sheet.

AC Characteristics for T40/110

V_{CC} = 5V ±10%; V_{SS} = 0V; T_A = −40 to +110°C
(C_L for Port 0, ALE and $\overline{PSEN}$ Outputs = 100 pF; C_L for all other Outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		10 MHz Clock		Variable Clock $1/t_{CLCL}$ = 1.2 MHz to 10 MHz		
		Min	Max	Min	Max	
ALE Pulse Width	t_{LHLL}	160		$2\,t_{CLCL} - 40$		ns
Address Setup to ALE	t_{AVLL}	70		$t_{CLCL} - 30$		ns
Address Hold after ALE	t_{LLAX1}	65		$t_{CLCL} - 35$		ns
ALE to Valid Instruction In	t_{LLIV}		300		$4\,t_{CLCL} - 100$	ns
ALE to $\overline{PSEN}$	t_{LLPL}	75		$t_{CLCL} - 25$		ns
$\overline{PSEN}$ Pulse Width	t_{PLPH}	265		$3\,t_{CLCL} - 35$		ns
$\overline{PSEN}$ to Valid Instruction In	t_{PLIV}		200		$3\,t_{CLCL} - 100$	ns
Input Instruction Hold After $\overline{PSEN}$	t_{PXIX}	0		0		ns
Input Instructions Float After $\overline{PSEN}$	t_{PXIZ}*		80		$t_{CLCL} - 20$	ns
Address Valid After $\overline{PSEN}$	t_{PXAV}*	92		$t_{CLCL} - 8$		ns
Address to Valid Instruction In	t_{AVIV}		385		$5\,t_{CLCL} - 115$	ns
Address Float to $\overline{PSEN}$	t_{AZPL}	0		0		ns

NOTE:
*Interfacing the SAB 8051A to devices with float times up to 92 ns is permissible. This limited bus contention will not cause any damage to Port 0 drivers.

AC Characteristics for T40/110 (Continued)

V_{CC} = 5V ±10%; V_{SS} = 0V; T_A = −40 to +110°C
(C_L for Port 0, ALE and $\overline{PSEN}$ Outputs = 100 pF; C_L for all other Outputs = 80 pF)

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		10 MHz Clock		Variable Clock $1/t_{CLCL}$ = 1.2 MHz to 10 MHz		
		Min	Max	Min	Max	
$\overline{RD}$ Pulse Width	t_{RLRH}	500		6 t_{CLCL} − 100		ns
$\overline{WR}$ Pulse Width	t_{WLWH}	500		6 t_{CLCL} − 100		ns
Address Hold After ALE	t_{LLAX2}	165		2 t_{CLCL} − 35		ns
$\overline{RD}$ to Valid Data In	t_{RLDV}		335		5 t_{CLCL} − 165	ns
Data Hold After $\overline{RD}$	t_{RHDX}	0		0		ns
Data Float After $\overline{RD}$	t_{RHDZ}		130		2 t_{CLCL} − 70	ns
ALE to Valid Data In	t_{LLDV}		650		8 t_{CLCL} − 150	ns
Address to Valid Data In	t_{AVDV}		735		9 t_{CLCL} − 165	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	250	350	3 t_{CLCL} − 50	3 t_{CLCL} + 50	ns
Address to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	270		4 t_{CLCL} − 130		ns
$\overline{WR}$ or $\overline{RD}$ High to ALE High	t_{WHLH}	60	140	t_{CLCL} − 40	t_{CLCL} + 40	ns
Data Valid to $\overline{WR}$ Transition	t_{QVWX}	50		t_{CLCL} − 50		ns
Data Setup Before $\overline{WR}$	t_{QVWH}	550		7 t_{CLCL} − 50		ns
Data Hold After $\overline{WR}$	t_{WHQX}	50		t_{CLCL} − 50		ns
Address Float After $\overline{RD}$	t_{RLAZ}		0		0	ns

NOTE:
*Interfacing the SAB 8051A to devices with float times up to 92 ns is permissible. This limited bus contention will not cause any damage to Port 0 drivers.

External Clock Drive XTAL2

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 1.2 MHz to 12 MHz (T40/85) Freq. = 1.2 MHz to 10 MHz (T40/110)		
		Min	Max	
Oscillator Period T40/85 T40/110	t_{CLCL}	83.3 100	833.3	ns
High Time	t_{CHCX}	20	$t_{CLCL}-t_{CLCX}$	ns
Low Time	t_{CLCX}	20	$t_{CLCL}-t_{CHCX}$	ns
Rise Time	t_{CLCH}		20	ns
Fall Time	t_{CHCL}		20	ns

Waveforms: Refer to SAB 8051A/8031A Data Sheet

Ordering Information

Type	Description
SAB 8051A-12-P-T40/85	8-Bit Single-Chip-Microcomputer with Mask-Programmable ROM (Plastic)
SAB 8051A-10-P-T40/110	With Mask-Programmable ROM (Plastic)
SAB 8031A-12-P-T40/85	For External Memory (Plastic)
SAB 8031A-10-P-T40/110	For External Memory (Plastic)